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Full Chip Signal and Power Integrity with Silicon Substrate Effect

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Abstract
This paper proposes a new method for analyzing signal and power integrity issues on LSI chips. This method can model a full chip power and ground grids considering the effects of transmission line and silicon substrate. A full chip layout data is divided into sections, then each section is modeled as SPICE transmission lines. N-port parameters of the each section are extracted by newly developed super linear solver. The extracted parameters are converted into compact SPICE frequency table. Using this method, the impedance of power/ground grids and dynamic IR drop for signal traces considering full power/ground grids are analyzed.

Authors' Biography

Norio Matsui

Norio Matsui holds a Ph. D. from Waseda University, Tokyo and was a researcher in NTT Labs for over 16 years. During this period he developed noise simulators integrated with PCB-CAD for Signal and Power Integrity as well as physical designs for high speed tele-switching systems. Apart from authoring numerous papers, he also lectured at Chiba University. He is currently President of Applied Simulation Technology and is actively involved in Power Integrity, Signal Integrity, and EMI/EMC solutions.

Dileep Divekar

Dileep Divekar obtained a B.S. in Electrical Engineering from Pune University, Pune, India and M.S. and Ph.D. in Electrical Engineering from Stanford University, Stanford, CA. He has worked in the areas of circuit simulation, semiconductor device modeling, static timing analysis and signal integrity. He is currently Vice President of Applied Simulation Technology.

Neven Orhanovic

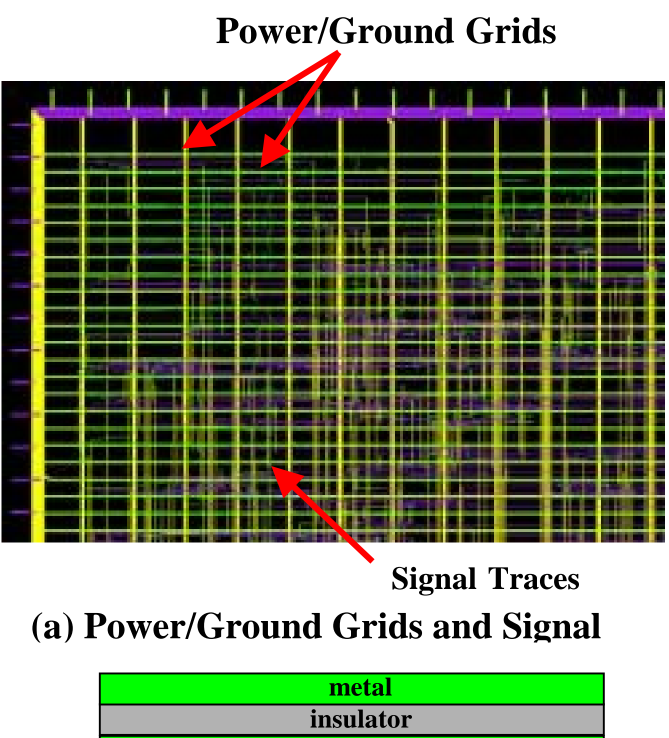
Neven Orhanovic received his B.S. degree in Electrical Engineering from the University of Zagreb, Croatia and his M.S. and Ph. D. degrees in Electrical and Computer Engineering from Oregon State University, Corvallis. From 1992 until 1999, he was with Interconnectix and Mentor Graphics Corp. developing numerical methods and simulation software in the area of interconnect analysis and interconnect synthesis. He is currently with Applied Simulation Technology working mainly on full-wave analysis methods

Hiroshi Wabuka

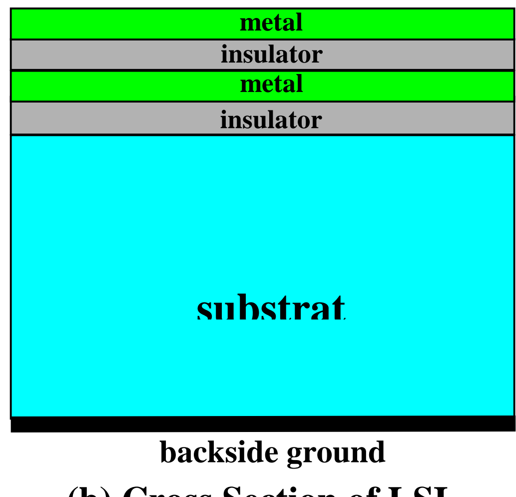
Hiroshi Wabuka received the M.S. degree in electrical engineering from Himeji Institute of Technology in 1982. He joined the semiconductor group, NEC in 1982 and was responsible for CMOS VLSI circuit design. He is a principal researcher in Jisso research laboratory, NEC and his responsibility is LSI modeling for packaging design and EMC analysis.

1. Introduction

With an increase in operating frequency and complexity of SOC, it becomes important to consider the power integrity (PI) as well as signal integrity (SI). Most SI approaches are focusing only on signal traces ignoring power and ground grids or assuming silicon substrate as a perfect conductor as shown in Figure. 1. However, the power and ground grids and a silicon substrate significantly affect the signal quality when the frequency is increased. There are two types of methods for evaluating power and ground noise as shown in Table 1. The first method is the frequency dependent impedance between power and ground grids which are modeled as transmission lines. It can be calculated by SPICE AC Analysis. Although this method does not directly treat waveforms, the noise voltage levels can be estimated by the obtained impedance multiplied by assumed currents at given frequencies. On the contrary, the second method can directly show waveforms considering the effect of nonlinear devices in time domain. The advantage of the first method is much faster than the second one. Key issues to realize the both analysis for real chips are how to handle such huge data of power and ground grids, because they are spreading a whole chip area.



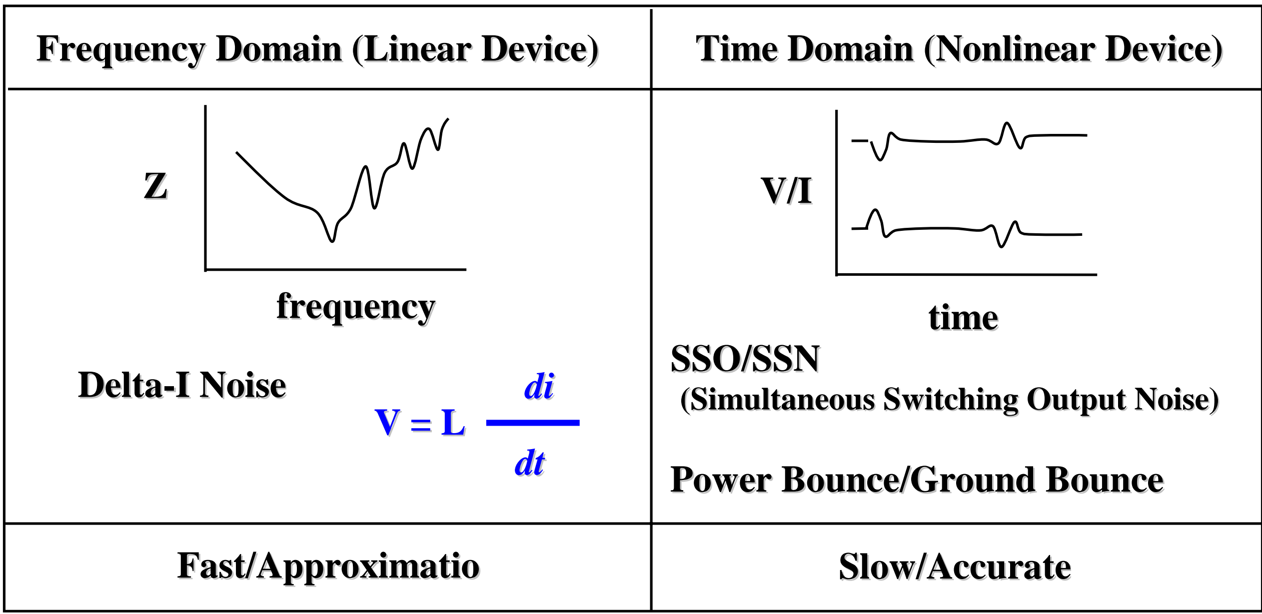
(a) Power/Ground Grids and Signal



(b) Cross Section of LSI

Figure 1. Typical structure of LSI chip.

Table 1. Two methods for evaluating power and ground noise.



Frequency Domain (Linear Device)	Time Domain (Nonlinear Device)
Z / frequency Delta-I Noise $V = L \frac{di}{dt}$	V/I / time SSO/SSN (Simultaneous Switching Output Noise) Power Bounce/Ground Bounce
Fast/Approximatio	Slow/Accurate

2. Methodology

2.1 Model Order Reduction

In order to analyze impedance and dynamic IR drop, it is necessary to make a full chip macro model for such huge power and ground grids with or without signal traces. It is well-known that a large size circuit can be compressed by converting a circuit model into N-port parameters which have less number of nodes. This is so called Model Order Reduction (MOR). However, this method has a problem when applying it to today's huge LSIs. With an increase in the number of the nodes of the final circuit model, it takes so long time to extract N-port parameters by conventional SPICE. To resolve this issue, we have developed a super linear solver (SLS). It can use memory effectively and drastically speed up. SLS consists of parser and solver. Figure 2 indicates no difference between ApsimSPICE and ApsimSLS. Table 2 compares the speed and memory between SPICE and SLS.

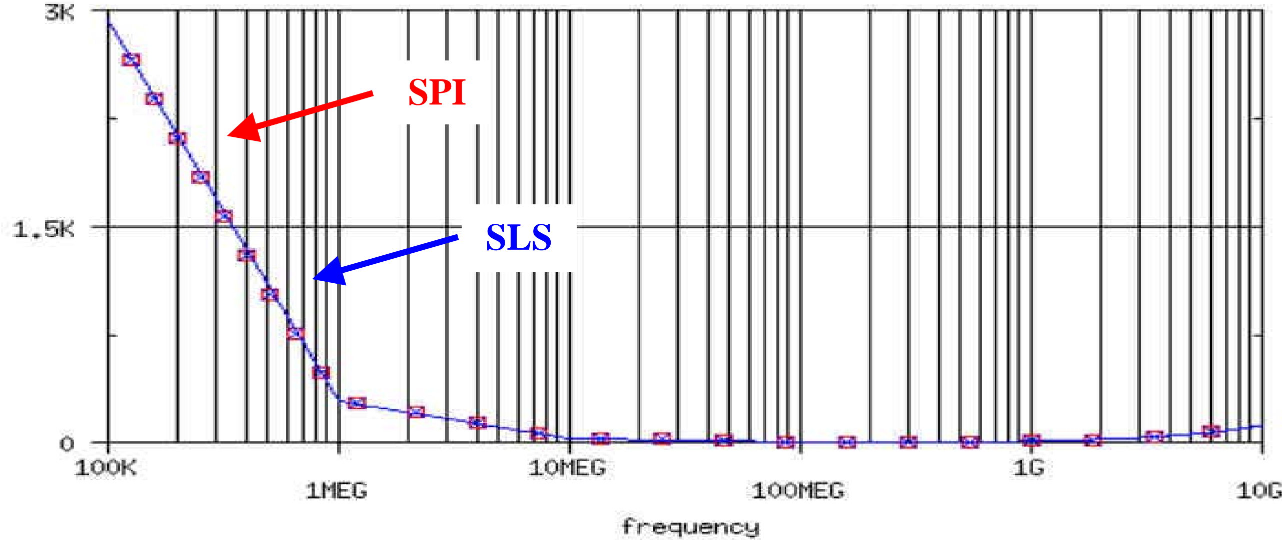


Figure 2. Comparison of accuracy between ApsimSPICE and ApsimSLS.

Table 2. Comparison of CPU Time and Memory.

- Comparison with SPICE
  - Circuit with ~ 14,000 nodes, 730,000 components
  - Matrix size 21,000 x 21,000
  - Six frequency points

Parse	CPU
SPICE	1
SLS	1/60

Solve	CPU	Memory
SPICE	1	1*
SLS	1/2	1/2.5

* Total memory including input parsing

Once we get N-port parameters, we must convert them into SPICE readable elements in frequency and time domains. This can be performed by fitting the rational function expansion (Figure 3) or frequency table model (Figure 4) [1]. Circuit simulator uses state variable approach and DFFT + Convolution for the rational function expansions and frequency table model, respectively.

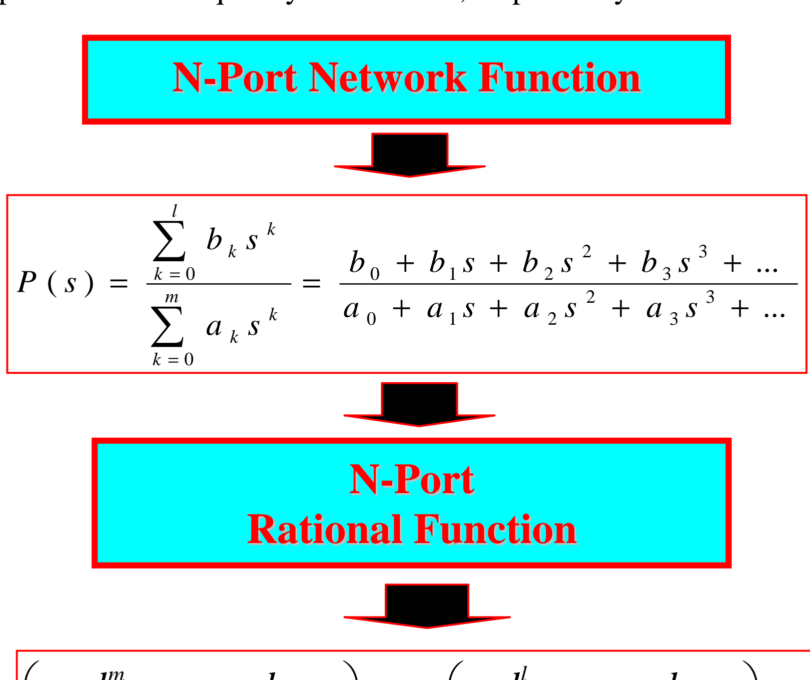


Figure 3. Fitting of Rational function in N-port conversion.

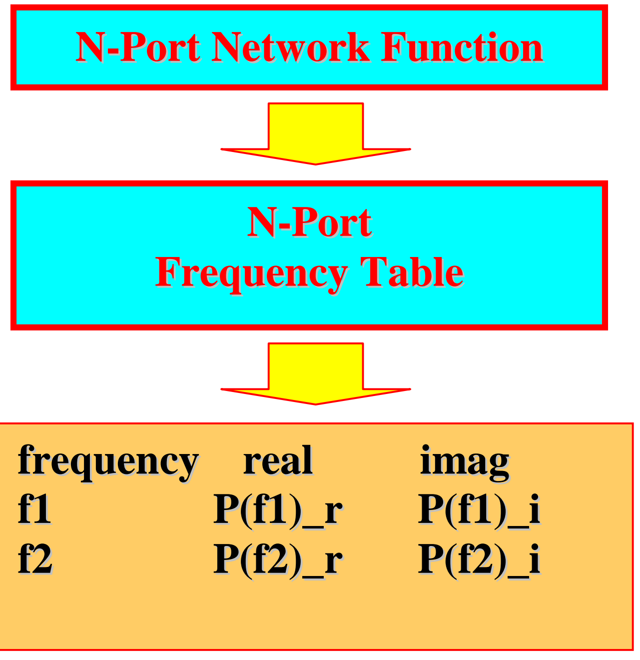


Figure 4. Frequency tables in N-port conversion.

Electrically short structures should use rational function approximation. This enables us fast transient simulation. On the other hand, electrically long structures should use frequency tables. This is slower than rational function, but no need for frequency fitting. Figure 5 shows an example of the rational function for electrically short structure. Figure 6 compares the rational function and the frequency tables for electrically long structure.

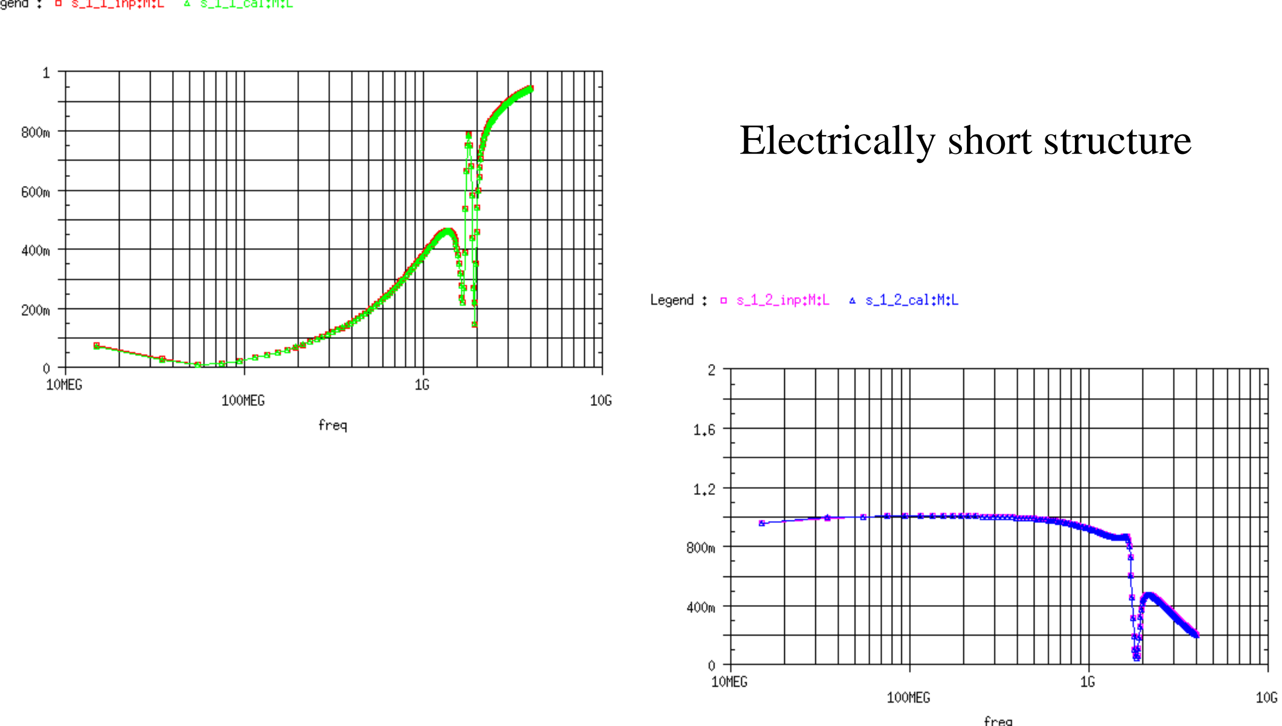


Figure 5. Fitting in the rational function for electrically short structure.

Electrically long

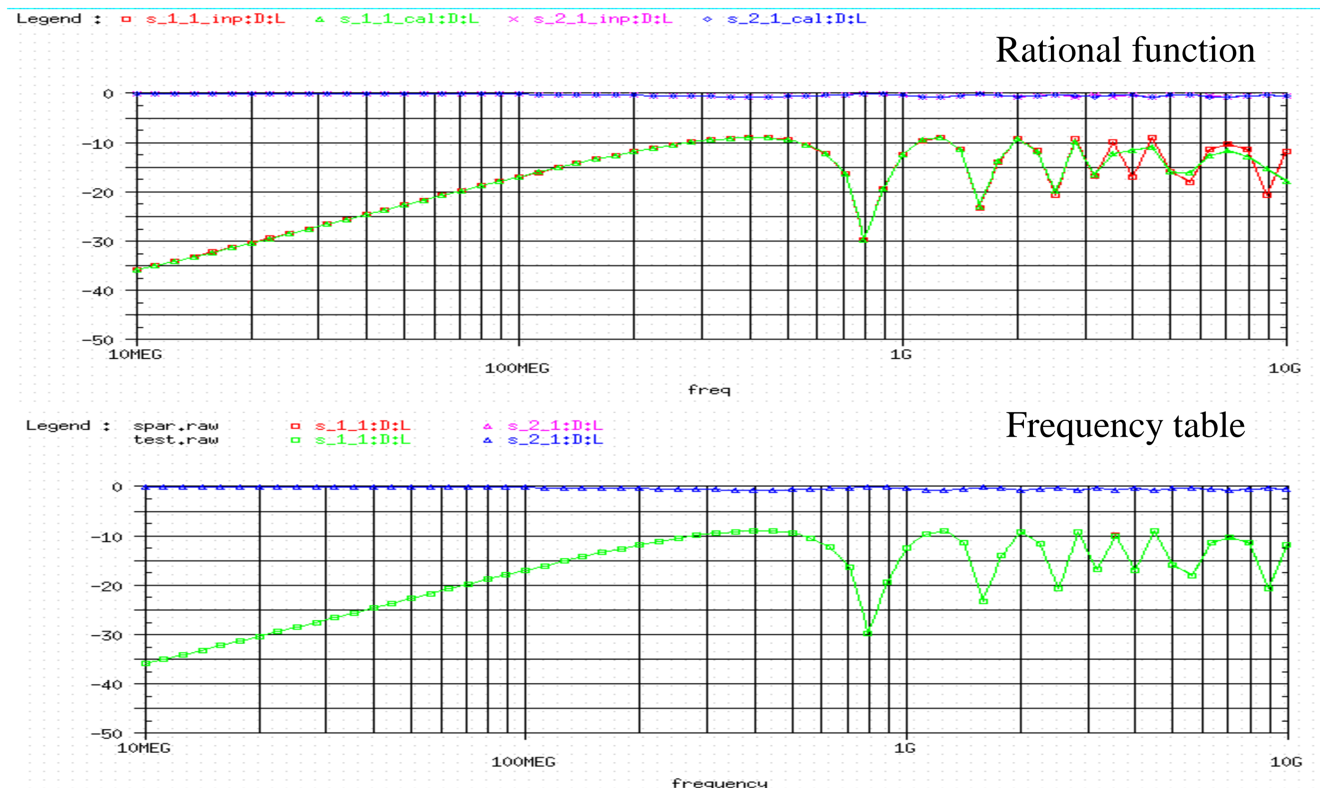


Figure 6. Comparison between rational function and frequency table for electrically long structure.

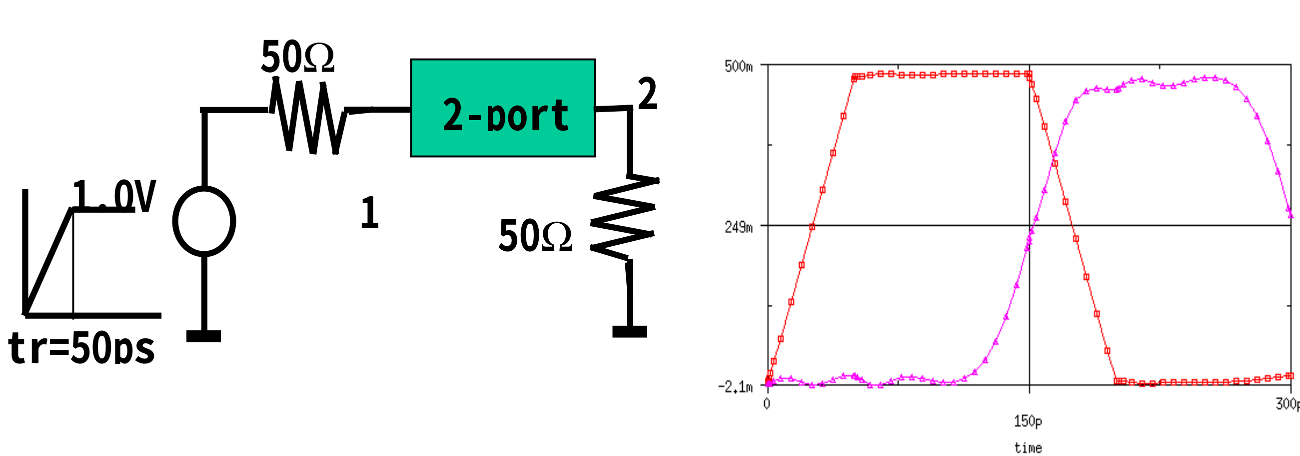


Figure 7. 2-port sub-circuit modeled by N-port fitting of rational function for transient analysis.

The compression by the N-port parameter extraction by SLS and the conversion of N-port parameters into SPICE readable element may not be good enough for today's much bigger chips. In fact there is a practical limitation of hardware or its cost. Therefore, we have added a sectioning method which was developed for return path analysis for printed circuit boards [2]. The physical data of a chip is divided into number of sections. Each section is modeled by the combination of N-port extraction and conversion to SPICE readable element. This method enables us to use the multi processing for modeling all sections in parallel. This can be also repeated for the obtained some grouped sections. This expands our method to much larger chips.

2.2 Silicon Substrate Effect

The effect of a silicon substrate on transmission properties was first analyzed in 1960's [3], [4]. There are three dominant propagation modes which are determined by silicon resistivity, dielectric constant and frequency as shown in Figure 8 (a). For the slow wave mode, the silicon substrate approximately behaves as a conductor for electric field, but it behaves as an insulator for magnetic field shown in Figure 8 (b). We have implemented these three modes into 2D field solver RLGC[5], SPICE[6], [7] and special linear solver SLS as a new transmission line model. Figure 8 (c) shows per unit length model of the transmission lines. The models become matrix for multi-conductors. The power/ground grids and signal traces described in the section 2.1 are described in this model.

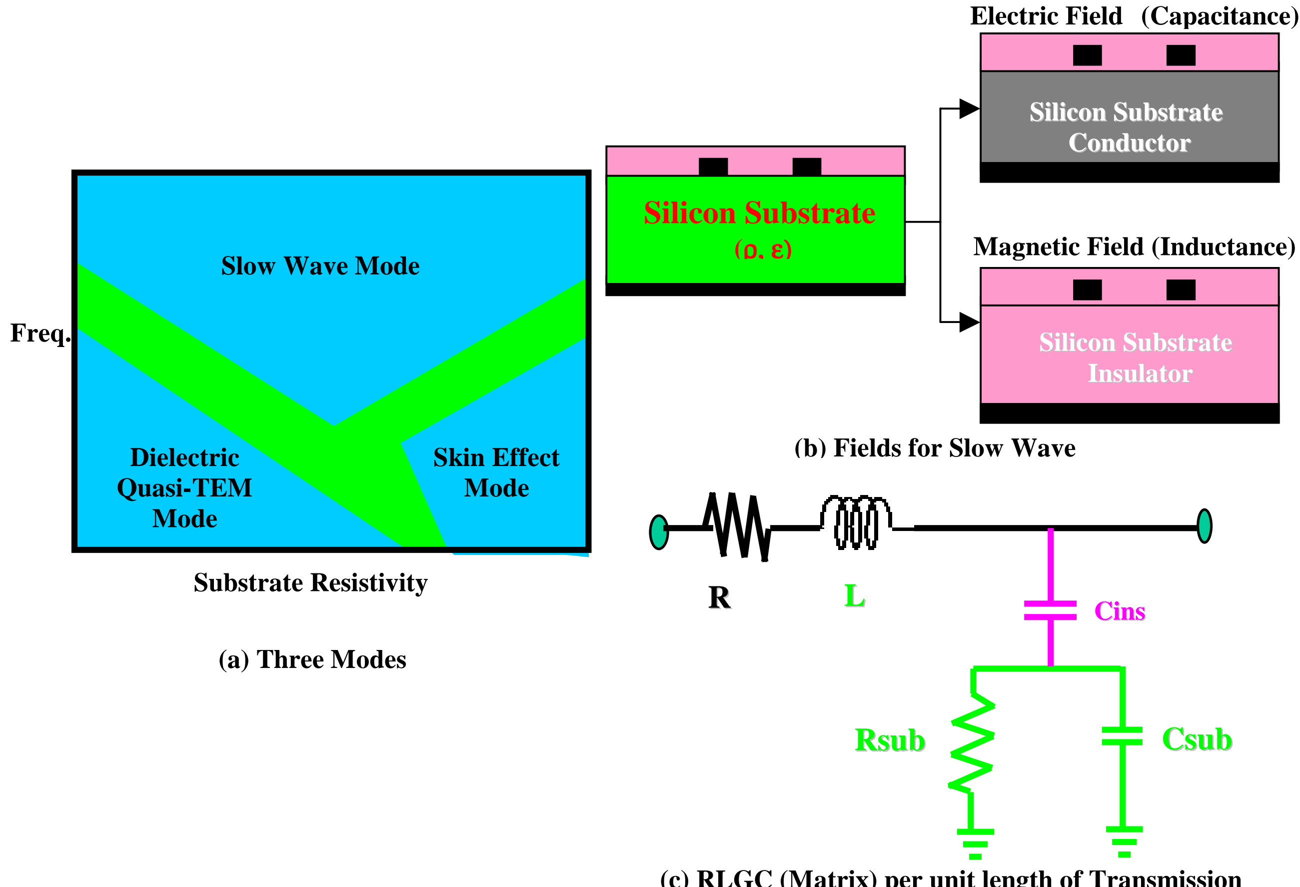


Figure 8. Three propagation modes of transmission lines over a silicon substrate.

2.3 Simulation Flow

There are two targets in our simulation. The first one is to calculate frequency dependent input impedance between power and ground grids. The second one is to simulate dynamic IR drop in time domain for connecting nonlinear devices to the model.

Figure 9 shows a fundamental simulation flow. The simulations starts with LSI-CAD data such as LEF (Library Exchange Format) and DEF (Design Exchange Format). LFE/DEF are converted into an intermediate proprietary format AAIF/AIF. Since the physical data AAIF/AIF is common to the printed circuit boards or IC packages, it is possible to simulate the mixing of LSI, IC package, and PCB layout data with common simulators. The AAIF/AIF data is converted into SPICE model by the 2D field solver with R, L, G, and C considering the effect of silicon substrate. Coupling levels can be defined for the horizontal and vertical distances in this conversion. If look up tables for such RLGC matrix are prepared, the SPICE model can be directly made from LEF/DEF files. There are two methods to make SPICE

model of the interconnections. One is to separate power/ground grids and signal traces. Although this model has no coupling between power/ground grids and signal traces, major interactions between power/ground and signals are considered at power feeding points of device models. The advantage of this method is to perform fast and stable simulation. The second method is that power/ground grids and signal traces are modeled considering coupling. This method is more accurate than the first one but slow. Once the interconnection model is made, an input impedance between power and ground at any give points can be calculated by SLS. For the dynamic IR drop analysis, N-port parameters at I/O pins and device connection points are also calculated by SLS. After getting the interconnection model, the signal waveforms and power/ground bounce in time domain can be simulated by SPICE. Since the model of the power and ground grids is compressed, the simulation time becomes very fast ever for connecting nonlinear device models to the N-port frequency table model.

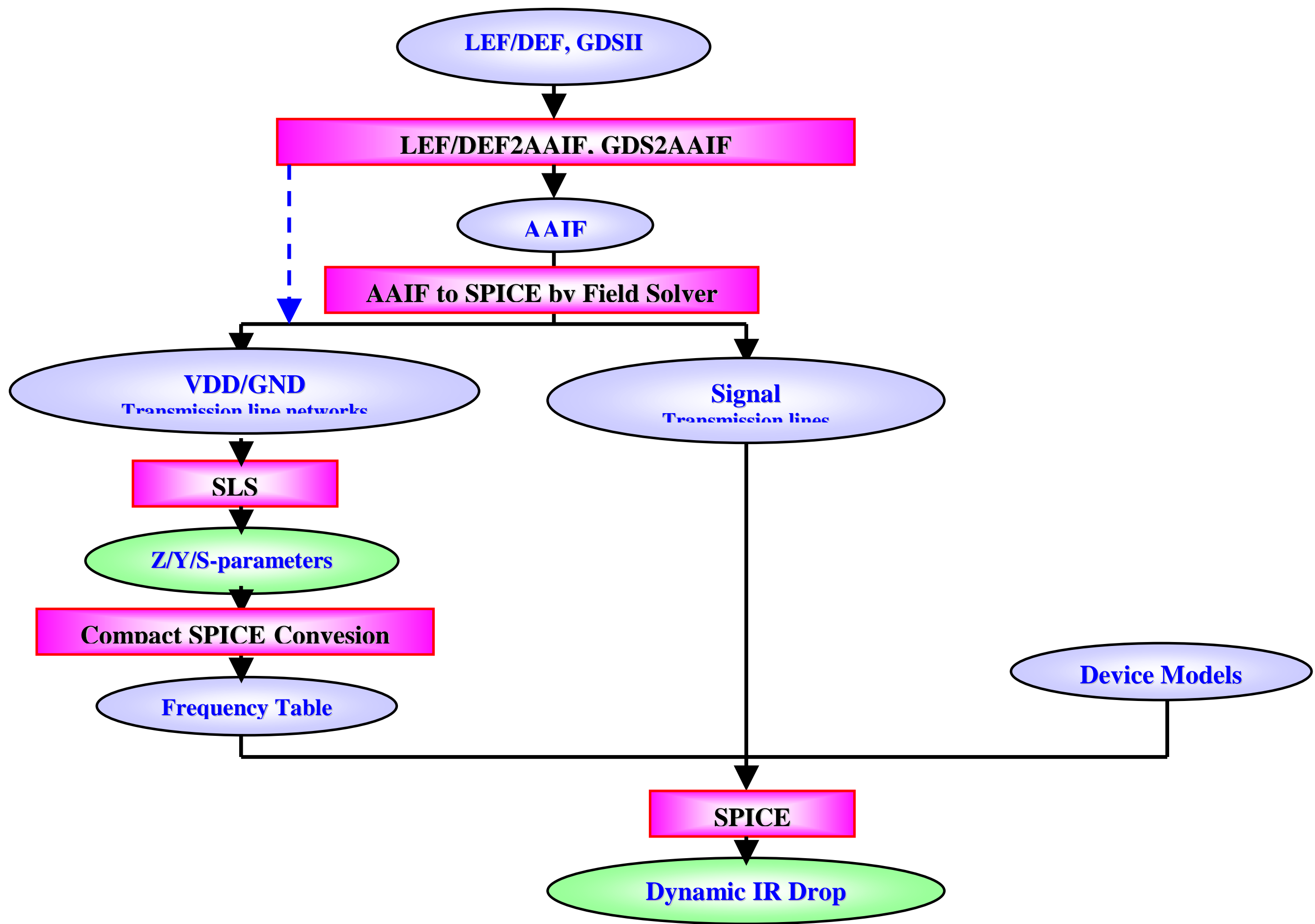


Figure 9. Simulation Flow of Input Impedance and Dynamic IR Drop.

Figure 10 shows a more complex simulation flow for much larger chips. A full chip structure is divided into sections. Each section of interconnection model can be modeled by using the procedures shown in figure 9. Each section can be simultaneously modeled by multi processor. The parallel processing makes speed up and treat larger chips. The obtained all the section models can be compressed again by using the same method of the N-port extraction and frequency table conversion. If the resultant model is still large, the same procedures can be repeated for groups which consist of number of section models. The input impedance between power and ground grids and the dynamic IR drop are also calculated by the similar procedures.

LEF/DEF, GDSII
LEF/DEF2AAIF, GDS2AAIF
AAIF
Sectioning
Substrate Effect
Inductance Effect
1 1 AAIF
m m AAIF
m n AAIF
AAIF to SPICE
AAIF to SPICE
AAIF to SPICE
VDD/GND Transmission line
Signal Transmission
SLS
Z/Y/S-parameters
N-port to SPICE
1 1 FreqTabl
m_m_Freq
m_n_Freq
Device Models
SLS
N-port to SPICE
SPICE
Impedance
Dynamic IR Drop

Figure 10. Simulation Flow for Input Impedance and Dynamic IR Drop for large Chips.

3. Example

We applied the proposed method to a real LSI chip shown in Figure 11. It has three metal layers.

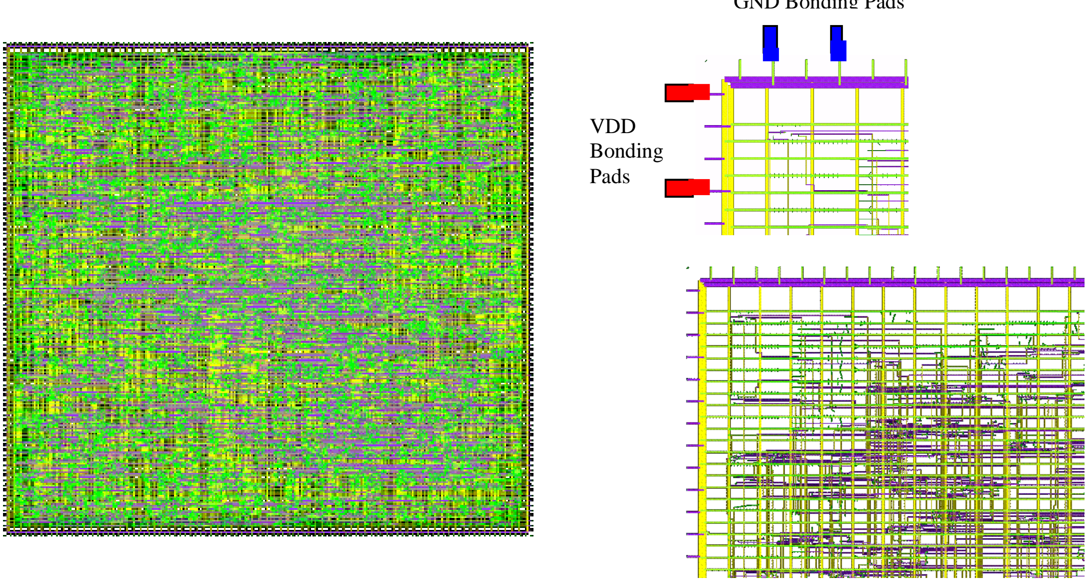


Figure 11. An example of LSI Chip.

3.1 Input Impedance between Power and Ground Grids

Figure 12 shows an example of a short circuit impedance between power and ground girds. The red and purple curves indicate RLGC calculation by look up table and by field solver, respectively. Both curves are close.

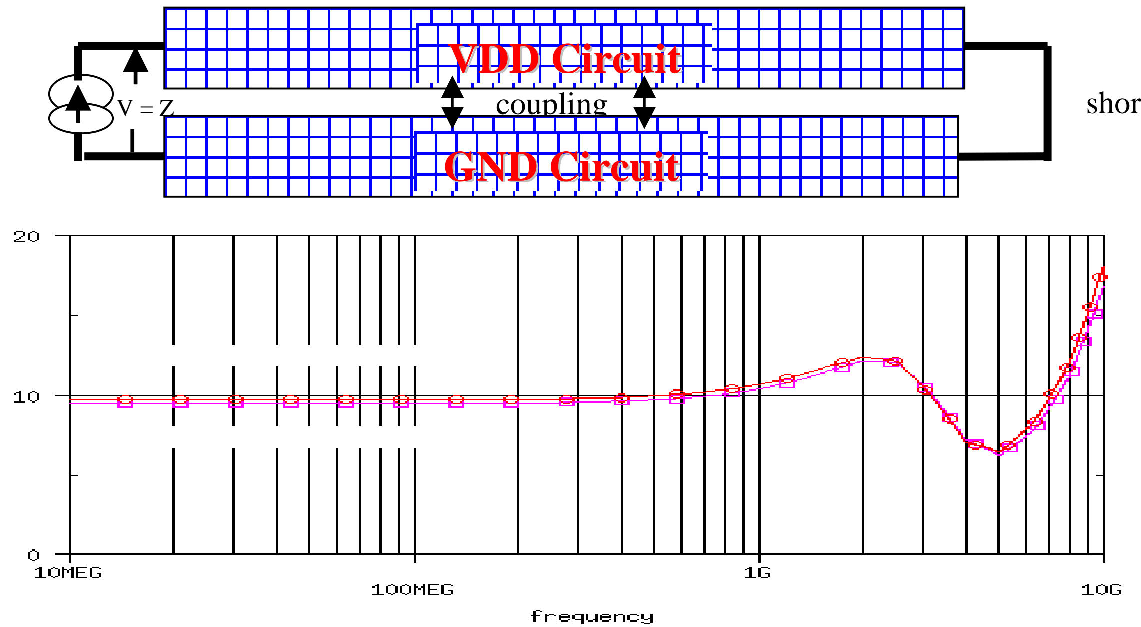


Figure 12. Short circuit impedance between power and ground grids.

Figure 13 compares a conventional quasi TEM model assuming silicon substrate as a perfect ground metal with the slow wave mode of silicon substrate. At low frequency, the impedance of the conventional model is lower than that of the slow wave mode. This is because a signal trace is closer to the ground and the capacitance value is larger. The inductance effect also can be seen beyond 10GHz.

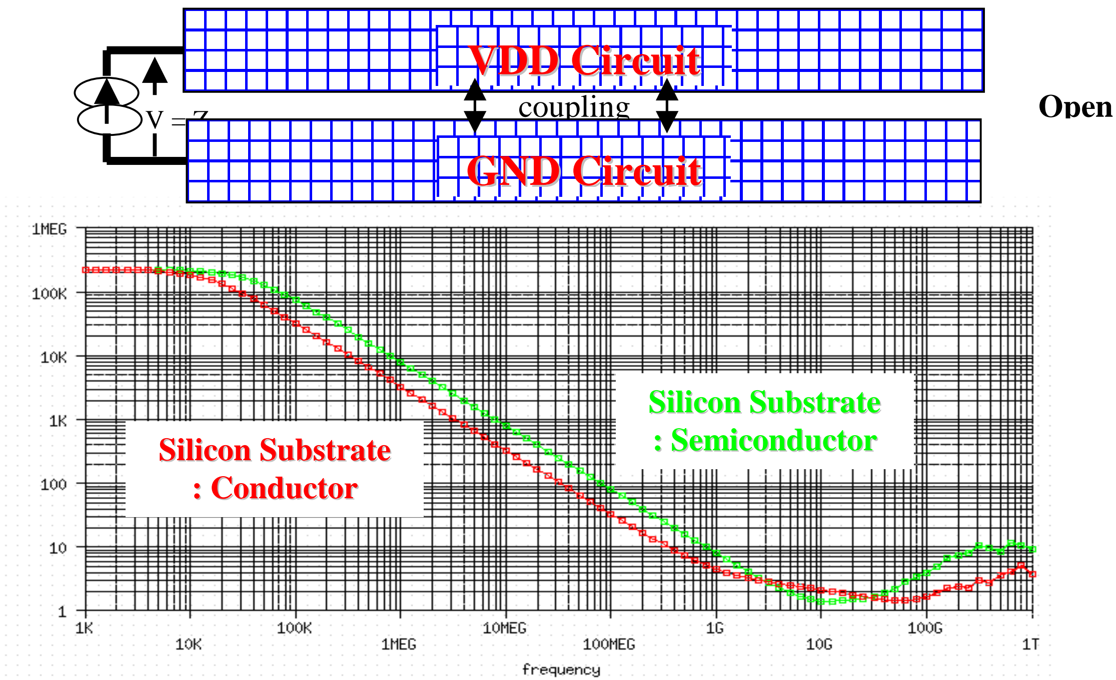


Figure 13. Open circuit impedance between power and ground grids.

The input impedance shown in Figure 14 can be used for optimizing on chip capacitors to reduce simultaneous switching output noise (SSO) and common mode EMI. There are two types of implementation of on chip capacitors. One is within a cell, and the other is using special capacitor cells. With an increase in the on chip capacitors, the impedance at the low frequency will be decreased. With an increase in the number of parallel path of power/ground grids, the impedance at the high frequency will be reduced. However, it should be noted that these two increases cost and chip size. There are trade offs between the noise reduction and the cost.

Figure 15 summarizes typical on chip capacitor strategies. There are two ways to place on chip capacitors. One is within a cell, and the other is using special capacitor cells. Usually capacitors are obtained by gate oxide layer of MOS transistors, because the value of MIM capacitors is much smaller. These strategies can be evaluated by analyzing the impedance between power/ground grids.

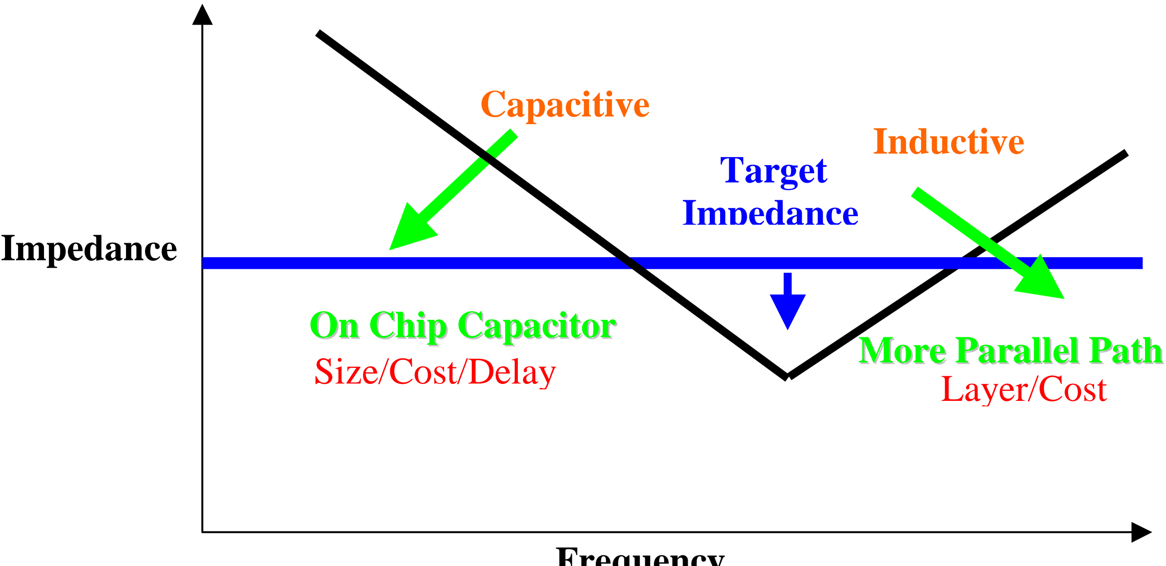


Figure 14. How to reduce impedance between power and ground grids.

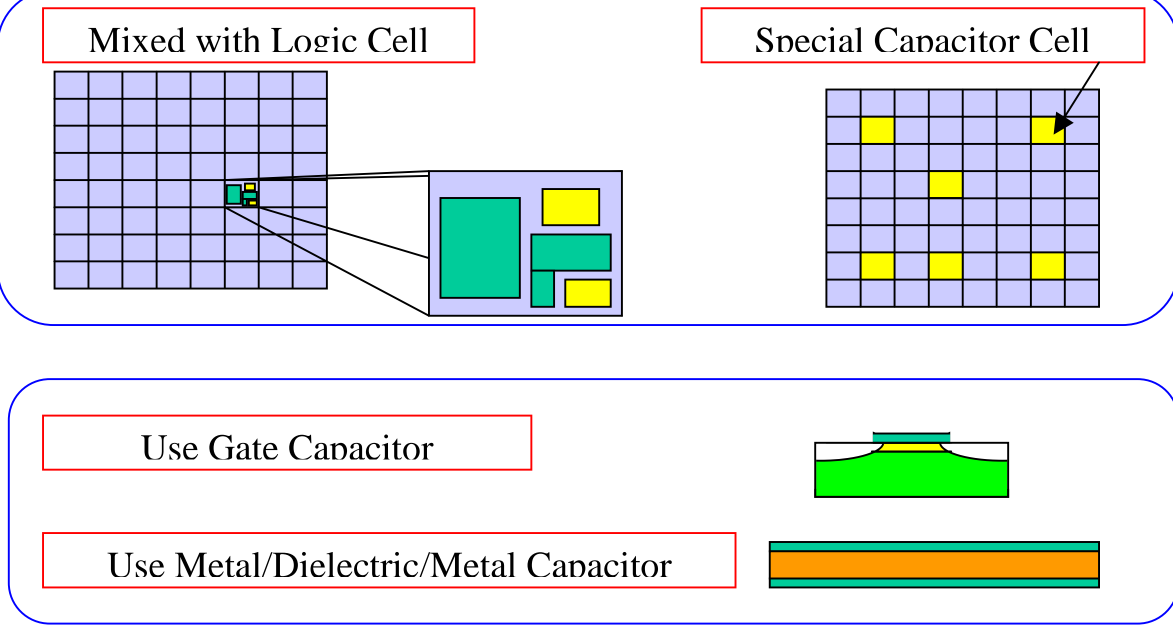


Figure 15. On chip capacitor strategy.

3.2 Dynamic IR Drop

To analyze waveforms along signal traces taking care of power/ground grids and silicon substrate in time domain, the N-port parameters were extracted by SLS. Then the parameters in frequency domain are converted into rational function or frequency table model in time domain analysis. Signal trace models and nonlinear transistor models are connected to the power/ground grid model, then signal waveforms and power/ground bounce are simulated as shown in Figure 16.

Figure 17 shows dynamic IR drop along a clock net of chip layout shown in Figure 18.

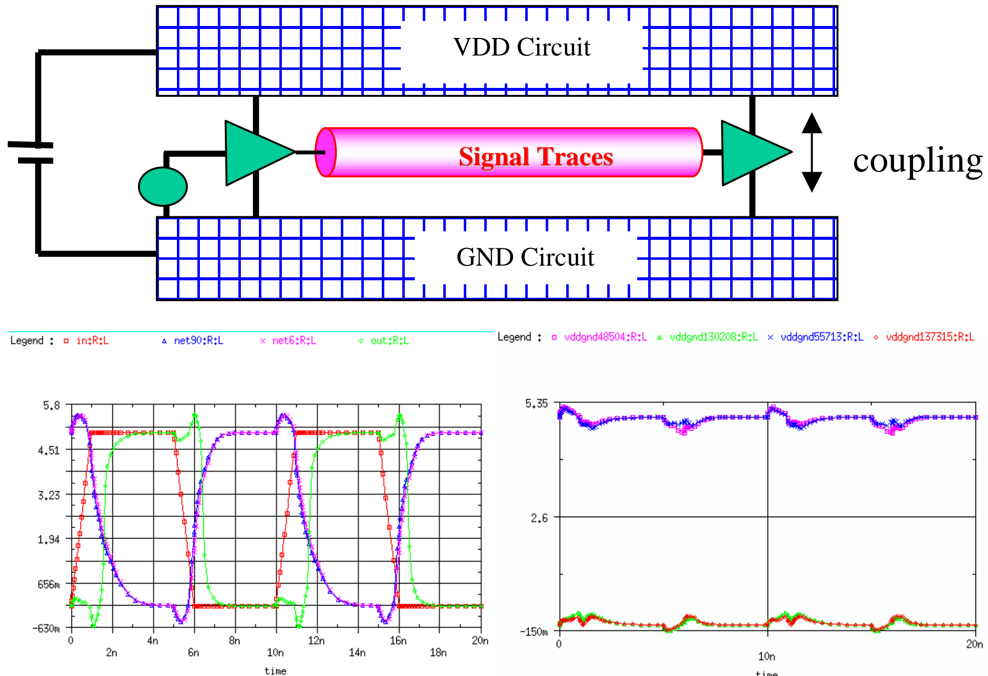


Figure 16. Signal and power and ground net simulation.

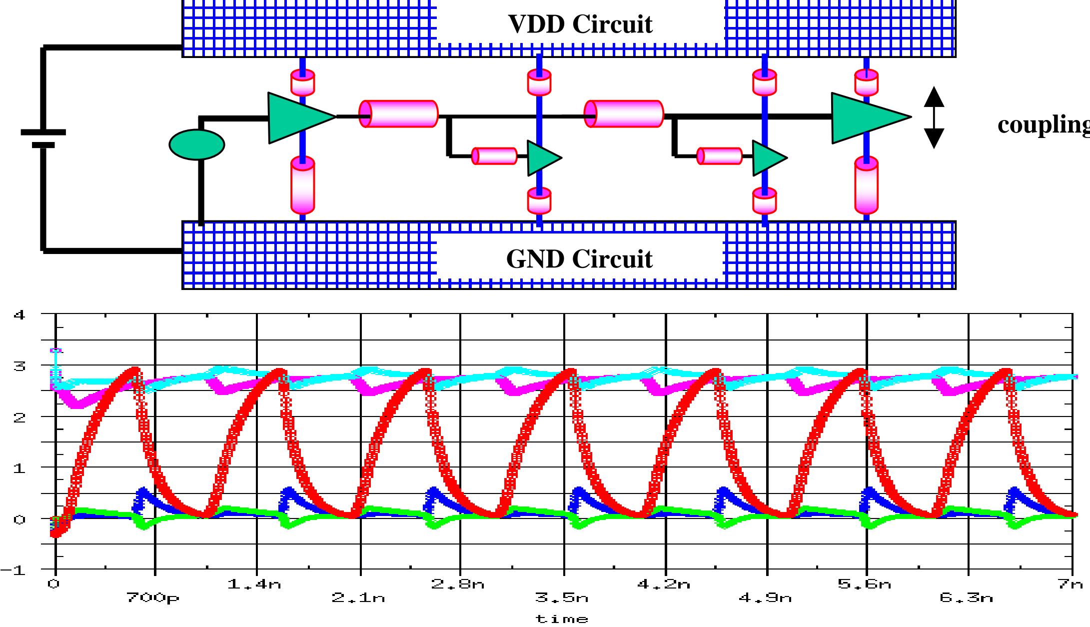


Figure 17. Dynamic IR Drops for a clock net and a compressed full chip power/ground grid.

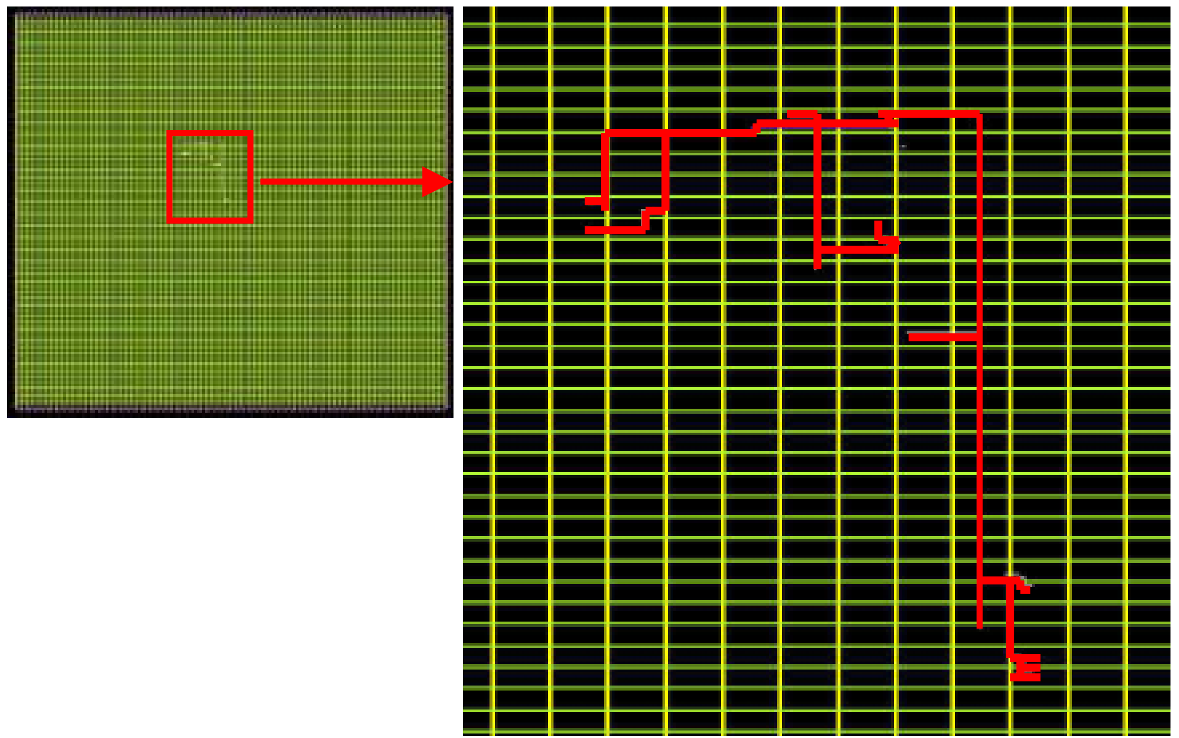


Figure 18. An example of clock nets and full chip power/ground grids.

4. Conclusion

We have developed a new simulation method for the full chip level Signal and Power Integrity. The physical CAD layout data is converted into SPICE transmission line models taking care of substrate Effects. To compress the model size, the N-port parameters extraction by super linear solver, the frequency table conversion, and repeatable sectioning method have been introduced. Using this method, input impedance between power and ground grids and dynamic IR drop (power and ground bounce) are simulated. This method can be interfaced with LSI CAD data LEFDEF. The common intermediate format of the physical data enables us to use the same simulation tools from LSI, Package through PCB. We have also developed another CAD interface GDSII for arbitrary polygon shapes. This uses PEEC model instead of transmission line models.

References

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