Full-Chip Verification of UDSM Designs

R. Saleh
Simplex Solutions
521 Almanor Avenue
Sunnyvale, CA 94086
(408) 617-6100
res@simplex.com

D. Overhauser
Simplex Solutions
521 Almanor Avenue
Sunnyvale, CA 94086
(408) 617-6100
ovee@simplex.com

S. Taylor
CMOS Solutions
HC1, Box 238
Olga, WA 98245
(360) 326-6691
ina@rockisland.com

1. ABSTRACT

This tutorial describes the problems encountered in typical ultra-deep submicron (UDSM) designs, and the full-chip interconnect verification methodologies needed to successfully identify these problems before tape-out. We first illustrate that UDSM verification must go well beyond simple geometric and circuit comparison checks to address increasingly important issues such as timing, power integrity, signal integrity, and reliability. The key issues of IR drops in the power grid, electromigration in power and signal lines, clock skew, signal coupling and its effect on timing and noise are described. We present real-world examples of such problems and how to find these problems using full-chip verification.

2. INTRODUCTION

Steadily shrinking process technologies and ever-increasing design sizes require new interconnect-centric verification tools to address the complexities of ultra-deep submicron (UDSM) design. In processes > 0.5µm, gate and transistor delays dominated interconnect delays. The advent of deep submicron processes is invalidating the assumptions and approximations that form the basis for device-centric verification methodologies such as DRC and LVS. In UDSM design (i.e., 0.25µm and below) parasitic capacitance and resistance effects begin to dominate [14].

For example, in a typical 0.25µm process, approximately 70 percent of the signal delay is due to interconnect and only 30 percent due to the gate driving the interconnect. The parasitics also effect the integrity of the signals traveling from the drivers to the receivers, and the voltage levels of power and ground seen by the gates.

Front-end CAD tools and design methodologies that have enabled million-gate ICs in UDSM have also placed an increasing burden on back-end verification tools. Fixing problems due to physical technology characteristics requires multiple iterations through expensive fabrication processes, resulting in higher costs and significant increases in time-to-market.

In this tutorial, the key issues of UDSM design verification – timing, IR drop, signal integrity, clock skew and electromigration – are described, along with the related analysis issues. Methodologies used to identify potential violations in the design are also described. Designing with these issues in mind and performing full-chip interconnect verification enables designers to address what would otherwise be an intractable problem.

3. FULL-CHIP VERIFICATION METHODOLOGY

3.1 A Brief History of Timing

The timing picture has been evolving over the last decade due to advances in IC technology, and it is interesting to step back and look at this evolution before getting into the full-chip verification issues. When process geometries were greater than one micron, the performance of a design could be accurately predicted by analyzing gate delays and approximating (or in some cases, ignoring) the interconnect delays and slew rates. Device loads were typically treated as a **lumped capacitance**, an approximation enabled by the fact that device delays dominated the equation. Slew rates were also typically ignored for the same reason. No interconnect resistance modeling was required:

$$T_d = T_g(C_L), \text{ and } T_{path} = \Sigma T_d. \quad (1)$$

As processes were scaled below one micron, these approximations became more and more inaccurate. With the total delay decreasing, slew could no longer be ignored, since it affected a more significant percentage of the total

delay. For the same reason, device loads could no longer be accurately represented by a simple capacitance, so the **lumped RC** model (single R and C) was used. Despite these relatively minor changes, device delays still dominated the total delay equation. The timing equation was updated to add the slew rate effects and the increasing impact of interconnect resistance:

$$T_d = T_g(C_L, \text{input slew}, \text{lumpedRC}), \text{ and } T_{path} = \Sigma T_d. \quad (2)$$

An interesting phenomenon occurred as the process geometries shrank below 0.5•m. Somewhere in the 0.5–0.25µm process size, the interconnect delay caused by device loading became equal to the device delay for long nets. This event, while not perceived to be a dramatic change, emphasized the effects of deep submicron by changing the basic paradigm of design: gate delay no longer dominated interconnect delay. Original approximations based on this paradigm failed, and interconnect delays could no longer be treated as second-order effects. Since interconnect delays began to play a major role in determining total delay, the **distributed RC** model (multiple R's and C's) was introduced to improve the accuracy of interconnect modeling. Delay calculators now rely on the parasitic data in order to compute path delays accurately:

$$T_d = T_g(C_L, \text{input slew}, RC) + T_I(\text{distRC}) \quad (3)$$

And $T_{path} = \Sigma T_d$.

However, even this model does not take all the UDSM effects into account. The increased coupling capacitance between adjacent interconnect wires increases delay times and may cause failures due to noise injection. The narrow line widths used in power and ground lines increases their resistances. As a result, voltage drop and ground bounce in poorly designed power rails further impact delay due to weakened driver strengths. To summarize, the timing picture is getting increasingly more complicated. In order to take all the important effects into account, one must first analyze the design in a full-chip context and combine the results of the analysis back into the timing equation.

3.2 Full-Chip Interconnect Verification

In the absence of front-end design tools to handle the UDSM issues, designers are employing full-chip verification in the back-end to identify potential problems before tape-out. Before deep submicron, it was sufficient to use geometric checks such as DRC and schematic comparisons such as LVS to ensure that the design would work. However, the parasitic effects of UDSM are causing problems that are now electrical in nature. Certainly LVS does not address deep submicron issues, but the geometric checks of DRC cannot even begin to address the complex issues of UDSM design.

The first step in full-chip verification is to extract all the parasitic information from the design. With multi-layer metal processes, 3D extraction methods are required to obtain the needed accuracy. After the extraction of signal and power nets is complete, the entire chip, including all the transistors, must be analyzed for potential problems. This two-step process can be expressed simply as:

Interconnect Verification = Extraction + Analysis

The amount of interconnect verification performed on a design is dependent on the target process technology, frequency, and the design itself. Designs targeted to a non-deep submicron process technology will not experience the same severity of interconnect-related problems as a design targeted to a UDSM technology. Similarly, high-performance designs such as today's microprocessors and microcontrollers will typically require significantly more interconnect verification than more conservative designs running at much slower clock frequencies.

3.3 Full-chip vs. critical net extraction

Before deep submicron, resistances and capacitances were extracted essentially in a 2D context. However, in UDSM design, capacitances can no longer be extracted in a 2D or 2.5D context. With dense multi-level metal exceeding 6 layers in advanced processes, these components must be accurately extracted in a 3D context [1] in order to perform accurate verification. As shown in Figure 1, there are three basic components. The area (overlap) component is the capacitance between the metal and substrate, the lateral component is between two metal lines on the same layer, and the fringing component is the capacitance between metal lines on different layers. Note that there is another area component between two metal lines on different layers where they overlap.

Two approaches are used for parasitic 3D extraction. The first assumes the full-chip netlist can be divided into two groups: critical nets and non-critical nets. Once divided, each group is treated differently such that the critical nets are extracted with high accuracy and the non-critical nets are extracted with lower accuracy. The reasoning behind this approach is that not all nets require accurate extraction, and so there is a runtime vs. accuracy tradeoff made for the non-critical nets.

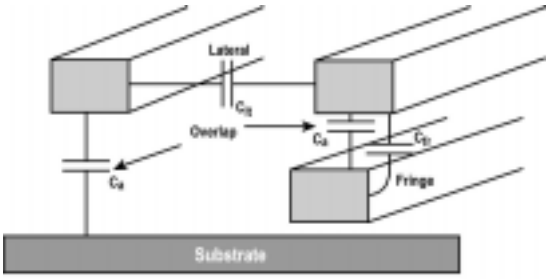

Figure 1: 3D capacitances in multi-layer metal

The alternative approach assumes that the capacitance extracted from any net could be associated with a critical net, and therefore, all capacitance should be extracted with high accuracy. This is the most predictable approach for UDSM technology. The lateral and fringe components of capacitance are clearly dominant below 0.25μm, and coupling capacitance is dominated by these components. The ratio of coupled to non-coupled capacitance continues to increase as the process technology shrinks.

The danger with the first approach is that there is no guarantee that *all* critical nets are identified. The filtering mechanism used to divide the full-chip netlist must account for all factors that could determine criticality, including driver size, distributed RC load, coupling between nets, and signal timing. While it may be possible to identify critical nets based on the first two criteria, it is extremely difficult, if not impossible, to pre-determine criticality based on the last two.

Consider the example in Figure 2: three nets, pre-determined to be non-critical (based on driver size/loading criteria), are tightly coupled to each other because their routes are adjacent. The central net has a large driver and large capacitive load, which causes the adjacent nets to become critical due to high coupling capacitance.

Since all of these nets were pre-determined to be non-critical, all of the associated capacitances are extracted with gross accuracy, despite the fact that high coupling capacitances C_{12} and C_{23} have caused two of the nets to become critical.

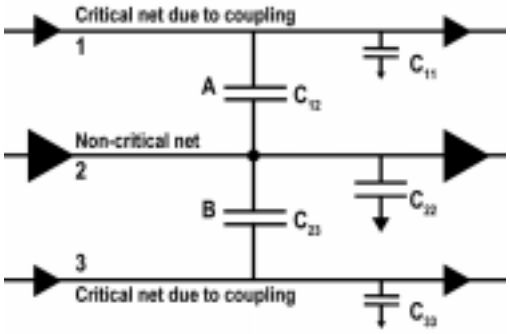

Figure 2: All capacitance is extracted with gross accuracy, even for critically coupled nets

4. FULL-CHIP VERIFICATION TECHNIQUES

4.1 Timing Verification

Chip timing is the cornerstone around which the majority of design methodologies are based today. Design flows and methodologies have been modified over the years to better support the meeting of chip timing goals in the minimal turnaround time. Power and reliability are usually considered as secondary issues. Unfortunately, in UDSM these secondary issues are growing in impact to the extent that they impact timing. As a result there will be changes occurring in the coming years to support this impact.

With each evolution of technology, changes have been made in the design methodology to account for the increasing complexity of computing timing and meeting chip timing goals. Floorplanning is now used to provide some wireload models to synthesis tools. Place and route tools are now timing based and include ECO capabilities to address convergence in meeting timing goals. Timing verification tools use more sophisticated timing equations. This trend to modifying the design and verification methodologies will continue into UDSM technologies. These changes will be driven by design failures resulting from methodologies not accounting for issues of importance. This trend is already being observed.

Today's timing verification relies on 2D or 2.5D parasitic extraction feeding into a combination of static and dynamic timing analysis, as shown in Figure 3. Static and dynamic timing analysis are used in conjunction to find critical paths. Dynamic timing analysis uses vectors to simulate paths in the design to find path delays. Static timing analysis uses different techniques to find path delays independent of vectors. The results of each analysis are compared to identify critical paths.

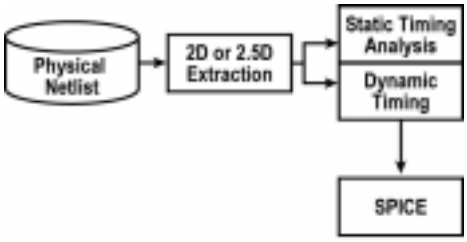

Figure 3. Traditional Timing Verification Flow

Discrepancies between the analyses are the focus. Critical paths identified in static analysis but not found in dynamic analysis are either false paths or unsensitized paths in dynamic analysis. Critical paths identified in dynamic analysis but not in static analysis may indicate shortcomings in the static analysis tool. Once a set of critical paths is identified, some subset of those paths may be forwarded to SPICE simulation to obtain very accurate measurements of the path delays. When timing violations are verified, some action is required to change the design. The action can be a change in the RTL description of the design, a change in the design constraints for any tool in the design loop, or a change in the floorplan of the chip. In any case the loop back through the design tools is required.

In examining today's verification methodology, a variety of failure mechanisms in UDSM design are not accounted for:

- Power grid IR drop impacting timing due to increased gate delay (a 5% IR drop increases delay by up to 15%)
- Interconnect delay due to signal coupling

- Power grid ringing due to inductance
- Clock skew impacting timing and functionality
- Noise injection due to signal coupling
- Noise injection due to inductance
- Power grid electromigration impacting timing and functionality (EM failures can increase IR drop or result in no power to some gates)
- Signal line electromigration impacting delay and functionality

As a result of these issues, design and verification methodologies will change in the 0.25μm and below design era. The scope of the methodology changes required depends on the process technology and the design frequency. We now address a number of these issues.

4.2 Signal Verification

Signal verification involves three types of analysis: timing, noise, and reliability. The reliability issue, in terms of signal-EM, is described in a later section. This section is concerned with coupling capacitance and its affect on timing and noise. This is commonly referred to as signal integrity (SI).

In today's timing verification methodology, there is no accounting for delay as affected by coupling capacitance. Consider Figure 2 again where the delay of interest is associated with net 2. It is capacitively coupled to nets 1 and 3. The actual delay associated with this net when switching from high-to-low depends on what is going on at nets 1 and 3.

For example, if both neighboring nets are stationary, then $C_2 = C_{22} + C_{21} + C_{31}$. However, if both are switching in the opposite direction to net 2, then $C_2 = C_{22} + 2C_{21} + 2C_{31}$. There are many other possible combinations of switching that results in different values of C_2. Furthermore, more combinations are possible if there are more neighboring nets. In general,

$$C_2 = C_{22} + K_{12}C_{12} + K_{32}C_{23} + \ldots + K_{n2}C_{2n} \qquad (4)$$

where the K-factors are determined by the switching conditions. Typically, $0 \le K \le 2$, but there are situations where K>2 [4]. Note also that, in general, $K_{12} \neq K_{21}$. That is, the K-factor for net 1 to net 2 may be different from the K-factor for net 2 to net 1.

Since timing verifiers rely on delay calculators, which in turn rely on RC netlists with grounded capacitances representing the parasitic interconnect effects, one approach to handling coupling effects is to ground all coupling capacitances after taking the K-factors into account. While this is a simplistic solution, it is one of the more practical approaches to the problem.

The issue that remains is the proper calculation of the K-factors, since the accuracy of the approach depends on the accuracy of the K-factors. Note that the delay computed using this approach can be worst-case or best-case depending on the selection of the K's. If $K_{ij} = 2$, for all i, j, then a worst-case delay is computed. This may be too pessimistic since the actual worst-case does not usually involve a factor of 2 for all K's.

To compute the K-factors, usually a static timing verification is performed at the gate level or higher with an initial assumption of $K_{ij}=1$ for all i, j. This is a relatively good assumption since it implies that most neighboring signals are stationary while a given signal is switching. Then the results from timing verification are scanned for each net to determine the proper value of K using the switching data in the associated timing windows for each net. Again, the worst-case K-factors can be determined by always assuming the highest values of K whenever necessary. These factors are then fed into equation (4), above, for each parasitic network and the resulting RC netlists are fed into the delay calculator and timing verifier. The K-factors can be updated with a second pass through timing verification, if desired. More accurate values of K require some form of logic satisfiability to be used [11].

Coupling noise is the other area of signal verification that is beginning to gain importance [15] [18], primarily at 0.25μm and below, although a number of chips have encountered problems at 0.35μm. The effect of coupling noise is to upset the functionality of a design – that is, a "soft" error occurs. Tracking down these types of problems in a multi-million-transistor chip has consumed many engineers for months, often without success.

Coupling noise can be catastrophic at latch inputs and in dynamic logic circuits. Specifically, incorrect values can be latched or dynamic values at capacitive nodes may be upset due to noise injection. Noise may also propagate through logic gates, assuming the levels of noise injection are high enough.

To verify the noise immunity of a design, a number of factors must be taken into account: coupling capacitance values, driver strengths, resistive shielding, timing information, and logic satisfiability. Since it is virtually impossible (NP-hard, if you like) to solve this problem in finite time, a practical alternative is to filter the signals through a series of operations, each one of increasing complexity but carried out on fewer and fewer nets. Eventually, only a few nets remain and they may require detailed SPICE-like analysis to determine noise susceptibility. This static approach to noise analysis is the subject of ongoing research and development [15].

4.3 Power – IR

Power distribution verification is rapidly becoming a necessary step in UDSM design of integrated circuits. With the increased load and reduced tolerances of deep submicron circuits, more failures are being seen due to

poorly designed power distribution systems. Failures were initially observed in microprocessor designs, but are becoming more common in ASSP and ASIC design as well.

With the narrow noise margins of a UDSM design, severe IR drop due to missing vias or an inadequate power grid causes functional failures. Less severe IR drop may cause timing problems. Again, a 5% drop in the supply voltage of a gate can cause a 15% increase in the gate delay.

It is reasonable to start looking for IR drop problems early in the design cycle. As soon as the layout of a functional block is completed, power distribution analysis of the block may be performed. This is referred to as block-level analysis. Many common design mistakes may be found by performing block-level analysis. However, due to the tight and complex interactions between different blocks of the design, an analysis at the full-chip level must eventually be performed to ensure that no IR-drop-related problems will occur in the assembled design.

Full-chip analysis often reveals problems with the power grid that were not evident from the block-level analysis. The power supply for blocks near the center of the chip may be routed through neighboring blocks that are not prepared to handle the additional current load. These blocks, which appeared fine during block-level analysis, could show excess voltage drop due to the current drain of their neighbors.

A static approach to calculate the currents is useful as a first step in power-grid analysis. Practical experience has shown that most major power-grid design problems will show up during analysis based on static current data.

Very simple and fast current estimates can be generated by calculating the Id-sat of the devices connected to the power grid. A much more accurate static calculation can be performed by considering the amount of charge drawn from the power grid during each clock cycle based on the switching activity at the gate level. Switching data can be derived from probabilistic analysis as well as vector-based simulation at the behavioral, gate or transistor level [17], [6], [9]. The average power dissipation for each gate can be expressed by the relatively accurate approximation:

$$P_{avg} = C_L * V_{dd}^2 * P_s * f \quad (5)$$

whereby C_L is the effective loading capacitance seen by the gate, V_{dd} the supply voltage, P_s the switching probability and f the clock frequency.

Dynamic analysis has to be performed to verify instantaneous voltage drops in the power grid due to simultaneously switching gates. Just after a clock transition, many of the gates in a design begin to switch simultaneously, causing peak current consumption and peak IR drop on a power grid. The dynamic peak IR drop will cause additional delays until the signals settle and may cause timing conflicts in aggressive designs, especially if cycle-stealing techniques are used. Different techniques have been proposed to either reduce the number of vectors to be considered for a dynamic analysis [17] or to find a subset from all possible input stimuli representing a similar power distribution [7]. In practice, only a few tens of vectors are necessary to identify IR drop problems.

Dynamic power-grid analysis presents some unique challenges due to the size of the problem as well as the time required to perform dynamic simulation at the transistor level. To reduce the time required for performing dynamic simulation at transistor level, macro modeling techniques based on gate-level simulation have been proposed [5], [3] and are utilized during synthesis and optimization.

A modified design of a multi-media chip with 1.6M transistors has been used to demonstrate the capabilities of the proposed methodology. Figure 4 shows the result of a static IR-drop analysis. The highest voltage drop is represented in the darkest color, giving immediate feedback to the designer on which blocks are the most critical as well the location of the critical spots inside the blocks.

It is clearly visible that the large block in the middle draws current from its neighbors, causing remarkable voltage drops in the surrounding blocks.

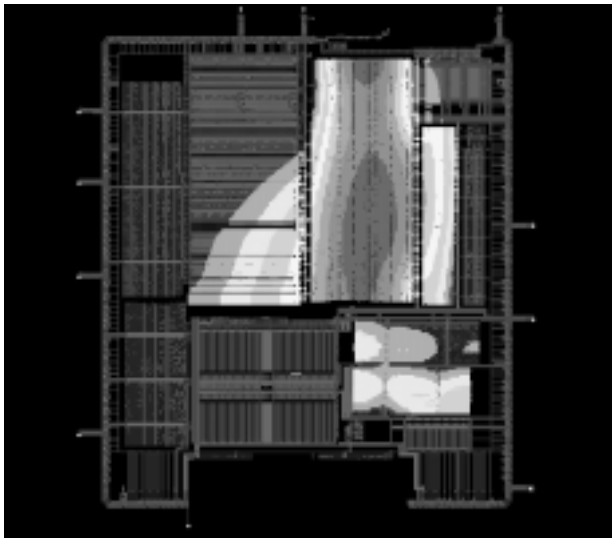

Figure 4. Static IR drop

4.4 Power – EM

Much research has been performed in order to understand the physics of device and interconnect reliability. Models and methodologies, such as those in BERT [8], have been developed to estimate the performance and reliability of small test circuits. Full-chip reliability analysis looks at reliability in the complete physical layout context and requires techniques to extract, manage, and process full-chip data.

Traditionally, designers are given simple wire current density limits to which they must adhere. These limits are based on "worst-case" estimates of the current density that is expected under use conditions, usually maximum temperature. Clearly this is overly restrictive.

The primary reason that full-chip electromigration analysis is necessary is that with growing chip complexities, designers no longer understand exactly how their chip operates. Due to complex power grids and distributed blocks in a design, current flow from a pin to the transistors cannot be determined without full-chip analysis. Adjacent blocks and their internal power routing have a significant impact on current distribution. In addition, since design tools do not consider electromigration limits, signal lines can experience excessive currents due to logic hazards and higher chip frequencies. Higher currents also increase the likelihood for signal line Joule heating failures.

Both power grid and signal electromigration analyses require the use of failure models. The choice of failure model must be made for each particular manufacturing process and set of design rules. The median time to failure at use conditions calculated from the test structure data is obtained at accelerated test conditions according to the generalized Black's equation [2], [13].

The power grid of a chip is operated primarily in a pulsed DC sense with respect to electromigration analysis. It has been shown that at operating frequencies and temperatures, electromigration driving force is determined by the average current density [16]. Thus, average current throughout the circuit is used to perform electromigration analysis on the grid. One at a time, each power grid is modeled by voltage sources at the pins providing power to the chip and the transistor tap currents at the device connection points. The large linear system is then solved to determine the precise current flowing through every wire segment and via in the chip. Once current density for each wire segment has been determined, simple checks are applied to identify those wires in the design which exceed a predetermined.

Figure 5 shows the result of applying electromigration analysis to a chip and generating a graphical report. This figure shows the Vdd grid for the chip in a variety of levels of gray. Different gray levels indicate different metal routing layers (graphical reports are normally colored, but are gray here due to limitations in printing). Errors are superimposed on the grid as bright white spots in this case. A variety of errors are flagged. Two sets will be discussed.

The first set of errors is along the top-left portion of the chip. The second set of errors occurs on the right side of the chip. The source of these errors demonstrates why reliability analysis of power grids must be performed at the full-chip level.

These two sets of errors are due to the currents resulting from the assembly of the chip blocks. The large block in

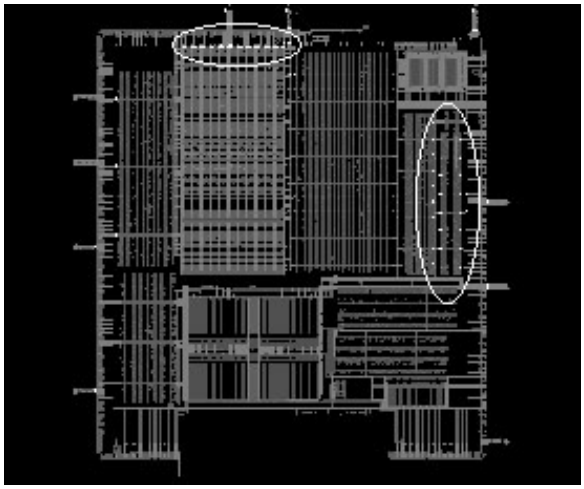

Figure 5. Electromigration violations in chip.

the right center of the chip is not connected to the power rail directly, but is supplied by power through adjacent blocks. Since the adjacent blocks are not designed to route power, their power grids conduct much more current than expected, yielding electromigration violations. The violations at the top are in the vias connected to metal 3. Additional current flows through these vias into the vertical metal 3 lines and eventually diverts horizontally to the right.

The errors on the right also occur in vias and are due to excessive current routed through the block. There is a power rail routing power around the rightmost blocks, but due to the power routing in these blocks, the path through the blocks is less resistive than the path around them. This is a case of block power routing drastically altering expected full-chip currents.

4.5 Clock Verification

Clock is the most critical net in a synchronous design. Because it has the highest frequency and power, it essentially defines time for logic throughout the chip, and it spans the entire chip. Not only is its delay throughout the chip strongly controlled, but its skew and waveform shape are critical for correct functional operation of the chip. Clock design is a problem of over-constraint. Clock designers generally must minimize clock skew, minimize clock delay, minimize clock layout area and power, maximize clock reliability, minimize clock noise, and design for an unbalanced load that will not be known until the chip is nearly done. The many constraints easily lead to over-designed clocks.

Cycle time available for critical-path delays is directly impacted by clock skew. Excessive clock skew can also lead to hold-time violations in paths with little delay. Clock verification is important because both under-design and over-design of the clock can result in chip failure. An under-designed clock will not attain the desired frequency, functionality, or reliability or have excessive skew that

results in functional failures. An over-designed clock will introduce functionality, timing, or reliability failures.

Physical issues impacting clock skew are not extensively verified today. Clock synthesis tools apply crude parasitic estimations and simple delay calculations when estimating net delays, and thus provide low confidence in their final performance. Few additional methodologies beyond SPICE simulation are applied to clock verification today. Proper verification relies on accurate parasitic extraction, accurate simulation at the full-chip capacity, consideration of coupling capacitances, and additional analyses. Additional analyses include power-grid IR-drop analysis due to clock switching, clock skew resulting from IR-drop variations across the clock distribution network, and process variations across the chip.

As an experiment, a 2M transistor ASIC was analyzed for clock skew before and after IR-drop analysis. After the effect of IR drop is accounted for, the skew of the clock increased by 15%. The skew increase results from those select regions of the chip that suffer from delay increases from IR drop, while other regions retain their speed because they retain full power during switching.

4.6 Signal – EM

Signal-electromigration analysis is more complex than power-grid analysis [13], [12]. In addition to the electromigration lifetime based on the average current, the RMS current is also calculated. Joule heating depends on RMS current and it must be realized that RMS current always exceeds average current for any duty cycle less than one.

Joule heating produces temperature gradients that can cause failure due to temperature-gradient-induced flux divergences.

Due to the AC current behavior of signal nets in digital designs, signal wires must be checked for average, RMS, and peak current density violations[10]. Average checks find those wire segments with high levels of unidirectional current density impacting electromigration while RMS checks find those wire segments that suffer from Joule-heating-induced failure mechanisms. Nearly all signal lines include metal segments that exhibit DC current behavior while most metal segments exhibit AC current behavior. Signal electromigration analysis is performed on a net by net basis and requires the simulation of the charging and discharging of the signal net for all possible current paths in order to determine the worst-case peak, average, and RMS current for each wire segment in the net. Computing all current parameters permits a wide range of electromigration checks and MTTF models to be applied.

In addition to power-grid analysis, signal reliability analysis is applied to the design of Figure 4. We selected the clock signal distribution tree (network) to illustrate the analysis. The clock tree is composed of 6700 nets and spans the chip. The source of the clock is a driver at the bottom of the chip.

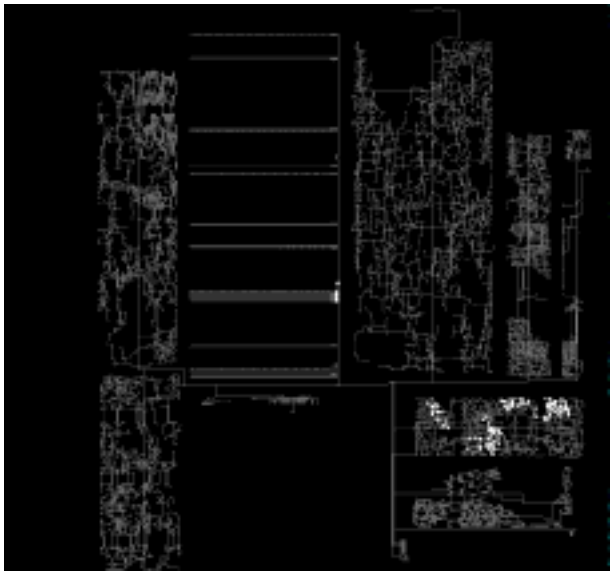

Figure 6. Signal electromigration simulation result.

The results of the simulation step for RMS analysis are shown in Figure 6. In this case, six nets are identified as being close to RMS current limits when this chip is operated at 200 MHz. Examination of these errors proves informative. One error occurs in the middle of the chip. A clock driver driving six additional large clock drivers nearby caused this error, but several jumper wires in the routing are too narrow for the high currents through the wires.

Another set of errors occurs in the lower right of the chip. These violations also occur due to a large driver and larger loading. These errors seem to occur because the clock routing in this area is designed differently than the rest of the chip in that they have a higher loading per driver than other blocks. The signal line reliability analysis is therefore critical in ensuring the long-term reliability of clock circuits.

5. SUMMARY

Given the various contributors to chip performance, functionality, and reliability in UDSM, it is clear that the methodologies used in design verification will change. Extractors with 3D extraction accuracy are required. Power and clock analyses are required to examine power-grid integrity and its impact on clock delay and skew. Coupling analysis and noise analysis must contribute to static and dynamic timing analysis. As a result, you may see design verification flows in the future resembling that shown in Figure 7. The timing delay equation will gain additional factors for IR, SI and clock skew:

$$T_d = T_g(C_L, \text{input slew}, RC, IR) + T_I(RC, SI) \quad (6)$$

where $T_{path} = T_{clockskew} + \Sigma T_d$

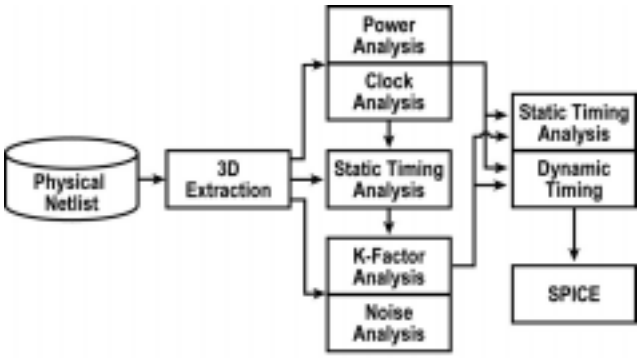

Figure 7. Timing verification flow with coupling analysis and noise analysis

will explicitly include clock skew factors to account for the increasing impact of IR drops and signal integrity, and path delay equations. In the future, low-k dielectrics will be introduced to reduce coupling [14], but interconnect lines will be spaced closer together as technology scales so the coupling issues will remain. For high-performance designs, inductance will start to play a role in interconnect delays, and the delay model will transition from a distributed RC model to a **distributed RLC** model. The introduction of copper interconnect to mitigate EM effects [14] will actually accelerate the inductive effects, since $R < j\omega L$. It will be interesting to see what new challenges lie ahead in full-chip verification below 0.1μm.

6. ACKNOWLEDGEMENTS

The authors would like to thank Pete McCrorie, Michael Benoit, Steffen Rochel, Zakir Hussain, Greg Steele and Janet Greene for their contributions in putting this tutorial together.

7. REFERENCES

[1] Arora, N., Raol, K., Schumann, R., and Richardson, L. Modeling and Extraction of Interconnect Capacitances for Multilayer VLSI Circuits, IEEE Transactions on Computer-Aided Design of IC's and Systems, pp. 58-67, Jan. 1996.

[2] Black, J.R. Electromigration Failure Modes in Aluminum Metalization for Semiconductor Devices. Proceedings of IEEE, 57, p. 1587, 1969.

[3] Bogliolo, A., Benini, L., De Micheli, G. and Ricco, B. Gate-Level Power and Current Simulation of CMOS Integrated Circuits. IEEE Trans. VLSI Syst., 5(4):473-487, December1997.

[4] Dartu, F., and Pilleggi, L. Calculating worst-case gate delays due to dominant capacitance coupling. Proc. Of Design Automation Conference, pp. 46-51, June 1997.

[5] Gupta, S. and Najm, F.N. Power Macromodeling for High Level Power Estimation. In Design Automation Conf., pages 365-370, June 1997.

[6] Kozhaya, J.N. and Najm, F.N. Accurate Power Estimation for Large Sequential Circuits. In Int'l Conf. On C omputer Aided Design, pages 488-493, November 1997.

[7] Krstic, A. and Cheng, K.T. Vector Generation for Maximum Instantaneous Current Through Supply Lines for CMOS Circuits. In Design Automation Conf., pages 383-388, June 1997.

[8] Liew, B.-K., Feng, P., Cheung, N.W., and Hu, C. Circuit reliability simulator for interconnect, via, and contact electromigration, IEEE Tr. Electron Devices, vol. 39, no. 11, pp. 2472, 1992.

[9] Lim, Y. J., Son, K.I., Park, H.J., and Soma, M. A Statistical Approach to the Estimation of Delay-Dependent Switching Activities in CMOS Combinational Circuits. In Design Automation Conf., pages 445-450, June 1996.

[10] Maiz, J.A. Characterization of Electromigration under Bidirectional (BX) and Pulsed Unidirectional (PDC) Currents. In Proceedings of 27th Annual International Reliability Physics Symposium, IEEE, 1989, pp.220-228.

[11] McGeer, R., and Brayton, R. Integrating Functional and Temporal Domains in Logic Design, Kluwer Academic Publishers, 1991.

[12] Nagaraj, N.S., Cano, F., Haznedar, H. and Young, D. A Practical Approach to Static Signal Electromigration Analysis. In Design Automation Conf., pages 572-577, June 1998.

[13] Overhauser, D., Lloyd, J.R., Rochel, S., Steele, G., and Hussain, S.Z. Full-Chip Reliability Analysis. In European Symposium on Reliability of Electron Devices Failure Physics and Analysis. October 1998.

[14] Semiconductor Industry Association (SIA), The National Technology Roadmap for Semiconductors, 1997.

[15] Shepard, K. L. and Narayan, V. Conquering noise in Deep Submicron Digital Design. IEEE Design and Test of Computers, pp. 51-62, Jan/Mar. Issue.

[16] Towner, J.M. and van de Ven, E. Aluminum Electromigration Under Pulsed DC Conditions. In Proc. 21st Annual IRPS, pp. 36, 1983.

[17] Tsui, C.Y., Marculescu, R., Marculescu, D. and Pedram, M. Improving the efficiency of power simulators by input vector compaction. In Design Automation Conf., pages 165-168, June 1997.

[18] Zhang, X. Coupling effects on Wire Delay, Circuit and Devices Magazine, pp. 12-18, Nov. 1996.