Full-Circuit Design Optimization of an RF Silicon Integrated Passive Device

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Abstract: A schematic-electromagnetic (EM) hybrid optimization scheme was used to design an integrated passive device (IPD)-diplexer. The method uses component values derived from circuit simulation and optimization to determine physical design changes. The diplexer was fabricated in a silicon wafer process. The small form factor (2.6x1.3x0.25 mm) of this device makes it very attractive for System in Package (SiP) applications. Simulated and measured results show good agreement.

1.Introduction

The trend in electronic packaging for wireless systems is toward integration of components by System in Package (SiP) methods. In particular, passive elements such as filters, diplexers, baluns and matching networks are often placed in packages alongside active semiconductor ICs. Traditionally, these components have been made by ceramic and SAW technologies. However, demands for more integration and smaller form-factor have made silicon-based integrated passive device (IPD) technology more favorable [1, 2, 3].

The traditional method of circuit design for devices like this is typically based on an approach in which elements of the design – components, interconnections, pads etc. – are individually modeled and then co-simulated in the circuit simulator. Such methods usually do not account for coupling between these elements, and fall short of the accuracy needed in RF filter design. Accurate behavioral modeling of the circuit requires electromagnetic simulation. Because this is time-consuming, it is usually done near the end of the design process, mainly for validation. A problem with this approach, however, is that when EM simulation shows that the design does not meet specification (which may frequently occur) it is not always straightforward to know how to correct the design.

Recent development of fast, iterative EM solvers [4] enables the adoption of an alternative hybrid design approach that uses EM simulation in conjunction with circuit optimization. We have developed an efficient methodology using this approach. The design cycle time is very short compared to other design processes, and final EM-simulation-based validation is the end-product of the methodology. This process is suitable for tuning large numbers of circuit variables, which is often difficult to achieve through 'blind' EM simulation. The design flow-chart can be found in Figure 1. It starts with a conventional schematic-level design, and the layout and first EM simulation follow the usual methodology. The key difference is the subsequent optimization loop, which uses a combination of circuit and EM simulation and optimization to fine-tune the physical design.
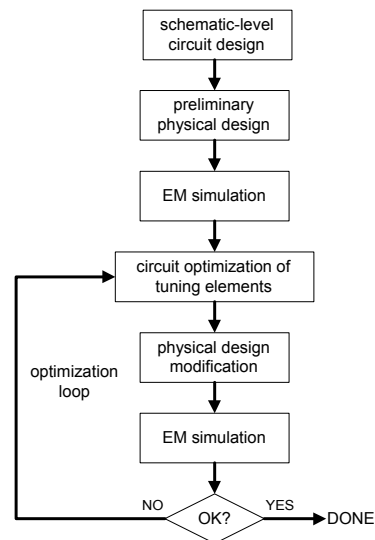

Figure 1. IPD design flow-chart.

2.Design Example

As an example, a GSM/DCS diplexer design is described below. Diplexers are basically two filters that are coupled to a common output using a low-pass/high-pass stage. They can be especially difficult to tune because of this coupling. Changes to the circuit that improve the characteristics of one band may degrade the other. The schematic for this example diplexer is shown in Figure 2. In this circuit, port-1 is the combined port, and ports-2 and 3 are the low (GSM) and high (DCS) band ports, respectively. L1-C3 forms a low-pass stage and L4-C5 is high-pass.

In most cases, circuits like the one shown in Figure 2 are designed using optimization methods. Many simulators used for RF circuit design include optimizers that adjust the values of the components, minimizing the difference between the circuit's performance and a user defined set of specifications. These optimization techniques are useful not only in initial circuit design, but can be used subsequently to find adjustments to the physical design.

Figure 2. Circuit schematic of a GSM/DCS diplexer.

Circuits usually require significant modification when they are translated from schematic to physical design. Interconnections between the components add parasitic elements that substantially affect the circuit performance. More importantly, the components themselves, especially the inductors, have complex characteristics that are poorly modeled by the simple inductance represented in the schematic-level simulation. More subtle differences, particularly in cases where high levels of isolation are required, happen as a result of low levels of electromagnetic coupling between the components themselves.
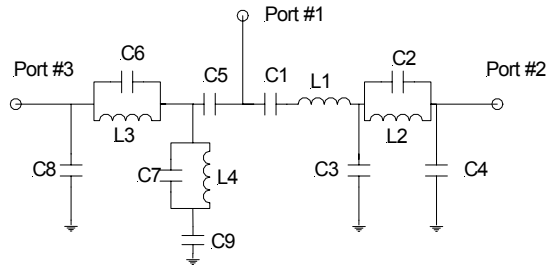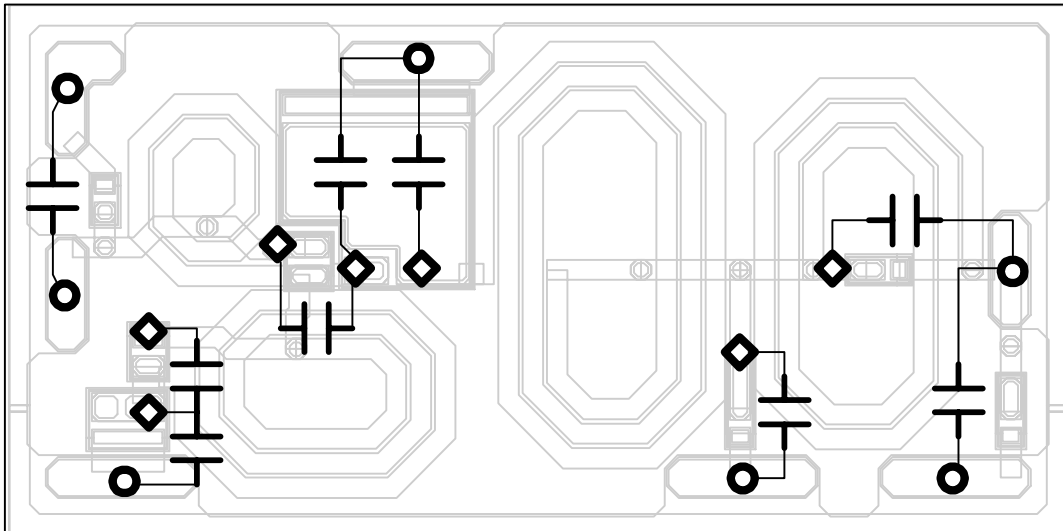
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Figure 3. Initial layout for the GSM/DCS diplexer, showing port designations and tuning capacitor connections.

Figure 3 shows the preliminary layout of the silicon IPD. For EM simulation, ports are located at the wire-bond terminals (indicated by ○) and at internal points in the circuit (◊). The internal port locations are chosen so that in subsequent circuit simulation, ideal capacitors (also indicated in the Figure) can be connected between the ports, in parallel with the physical capacitors in the layout. In this particular example, there are a total of 14 ports in the initial EM simulation model.

Figure 4 shows the circuit simulation setup. In this setup, the S-parameter model generated by EM simulation is used in circuit simulation, along with the added tuning capacitors and any external package model (typically wire-bond inductance) to be taken into account in the IPD characteristics. The circuit simulator's optimizer is then used to tune the capacitors to meet the objectives set by the circuit specifications. The optimization is configured so that the tuning capacitors can assume either positive or negative values. The post-optimization values of the tuning capacitors indicate changes to make in the layout of the physical capacitors. This process of EM simulation, re-optimization of the tuning capacitors and adjustment to the layout constitutes the optimization loop shown in Figure 1.

After each round of optimization, closer response to the specifications is achieved, and the optimum value of the tuning capacitors approaches zero. It usually takes 2-3 iterations to obtain a satisfactory result for this kind of IPD. The capacitor values after each round of optimization for this particular example are listed in Table 1, and the simulated response for the low band after each tuning is plotted in Figure 5. As initially designed, the isolation (attenuation of this signal above its pass-band) was inadequate. As the figure shows, this improved with each subsequent optimization, resulting in more than 10dB improvement.

Table 1. Capacitor values (pF) for the diplexer circuit in Figure 2.

	C1	C2	C3	C4	C5	C6	C7	C8	C9
Initial Design	5.88	0.73	3.02	2.45	2.35	2.1	0.33	0.4	2.98
Tuning #1	5.88	1.05	2.72	2.05	2.35	1.79	1.05	0.7	3.89
Tuning #2	5.88	1.38	2.42	1.65	2.35	1.62	1.29	0.825	4.08

Figure 5. Low-band simulation (dashed) versus measurement. The simulation result converges after three iterations.
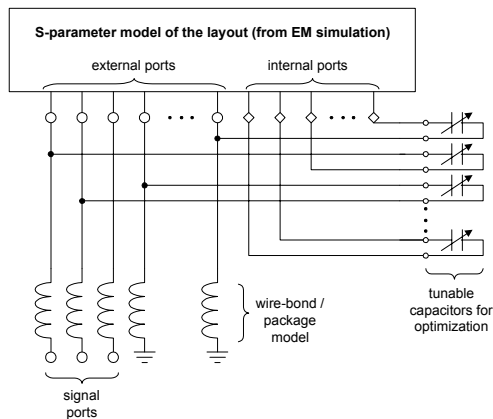

Figure 4. Circuit simulation set-up. Tuning capacitors are added between ports in parallel with the physical capacitors. Tuning capacitors can have either positive or negative value.
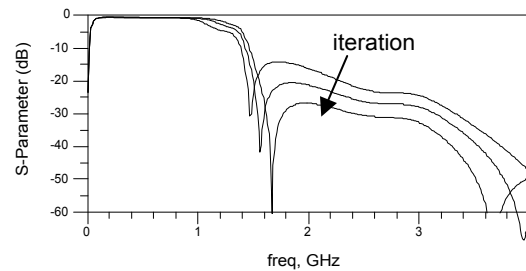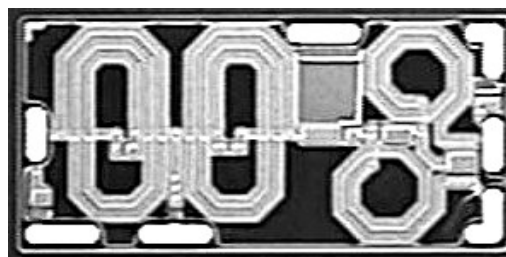

Figure 6: IPD Micrograph

3. Measurement and Simulation

The silicon IPD diplexer was fabricated at STATS ChipPAC. The size of the device, shown in Figure 6, is 2.6x1.3x0.25 mm. The small thickness of the device makes it especially well-suited for SiP assemblies, in which overall package thickness is often at a premium. In the measurement, the device was wire bonded to a laminate test substrate and measured. The measured result including the contribution of
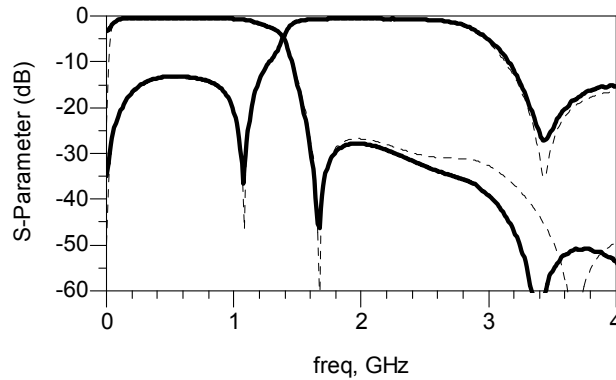
Figure 7. Simulation (dot) versus measurement (bold).

the bond wires is plotted in Figure 7. The simulated result, using the method described above, is shown for comparison. The results show very good agreement between measured and simulated characteristics.

4. Discussion and Conclusion

In the smaller form-factors demanded by SiP applications, RF components are necessarily pushed closer together. In such cases they are not well isolated from each other. It is important to adopt design methodologies that incorporate full-circuit EM simulation to accurately account for the interactions between the components in the circuit.

In the example presented above, the optimization and layout modification procedure was done only on capacitors. In most RF circuit designs, made up of L-C networks, adequate performance can be obtained by this procedure. It is especially suited to capacitors because it is straightforward to determine the layout changes that are required to increase or decrease a physical capacitor's value after each round of optimization. Similar tuning could be done for the inductors, but because we lack good scalable inductor models the correspondence between inductor changes and layout changes are less obvious. In circuits that require tuning of resistors, we have also used this procedure with good results.

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