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Fully-depleted Ge interband tunnel transistor: Modeling and junction formation

Qin Zhang, Surajit Sutar, Thomas Kosel, Alan Seabaugh *

Department of Electrical Engineering, University of Notre Dame, 275 Fitzpatrick Hall, Notre Dame, IN 46556-5637, USA

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ABSTRACT

Complementary fully-depleted Ge interband-tunneling field-effect transistors (TFETs) and static inverters are modeled to quantify TFET performance relative to Si MOSFETs. SYNOPSYS TCAD is used to compute the two-dimensional electrostatics and determine the tunnel junction electric field. This electric field is used in an analytic expression to compute the tunnel current. The speed and power performance of TFETs are compared with the nMOSFET at the same supply voltage, 0.5 V. For a gate length of 20 nm, Ge tunnel transistors can provide similar speed in comparison to 45-nm-node nMOSFETs (18 nm gate length), but saves more than 2× in power and lowers energy by over 7×. Toward demonstrating these transistors, a process for forming submicron p^+n^+ Ge tunnel junctions has been utilized in which Al-doped p^+ Ge is regrown on n^+ Ge, following melt-back of a patterned Al deposition. Transmission electron microscopy (TEM) reveals the regrown film and a contact microstructure consistent with the Al–Ge phase diagram. The low peak-to-valley current ratio (PVR) of devices produced by this growth method is likely a result of point defects or junction doping non-uniformity as TEM suggest no dislocations at the regrown junction. The PVR of these junctions does not improve as the device area is reduced from 100 to 0.1 μm^2, a size smaller than the formation scale for grains in the Al–Ge system.

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1. Introduction

Interband tunnel transistors can achieve a room temperature subthreshold swing below the metal–oxide–semiconductor field-effect transistor (MOSFET) limit of 60 mV/decade [1]. Lowering subthreshold swing is the single most effective way to decrease power dissipation in devices, because it enables use of a lower supply voltage. Sub-60-mV/decade subthreshold swing was first realized in a carbon nanotube tunnel FET (TFET) [2] and recently a subthreshold swing of 52.8 mV/decade has been demonstrated in a planar Si TFET [3]. In addition to lowering subthreshold swing, TFETs offer lower off-state current than MOSFETs, as a higher off-state thermal barrier exists between source and drain [4]. However, the Si TFET [3] achieves an on-state current density of 12.1 μA/μm at 1 V supply voltage, over two orders of magnitude lower than a high-performance MOSFET.

The method for deriving the dependence of tunnel current density on semiconductor properties is given by Moll [5]. Using the triangular barrier WKB approximation of Sze and Ng [6], the following relation is obtained:

$$J = \frac{q^3 \xi V_R}{4\pi^2 \hbar^2} \sqrt{\frac{m^*}{2E_G}} \exp\left(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\xi\hbar}\right), \quad (1)$$

where in good agreement with experiment [7], ξ is the maximum electric field at the junction, V_R is the reverse bias, m^* is the tunneling reduced effective mass, E_G is the bandgap, and the constants q and $\hbar$ are electron charge and Planck's constant, respectively. Using Eq. (1), the dependence of tunnel current density is computed versus junction internal field for Si and Ge. For the case of Si, measurements (open and closed circles) from eight different p^+n^+ tunnel junctions [8,9], spanning over eight orders of magnitude in current density, are shown in Fig. 1. Eq. (1) (dashed line) is in excellent agreement with the calculations using only the tunneling reduced effective mass as a fitting parameter. The calculations in Fig. 1 are also in reasonable agreement with the recent Si TFET demonstration [3] if a 10 nm channel thickness and a 4 MV/cm maximum electric field are assumed. For the Ge case, the current density is slightly higher than measurements [10–12], which might be caused by the junction non-abruptness. Fig. 1b shows that Ge tunnel junctions can have about two orders of magnitude higher current density than Si at the same electric field.

In this paper, Section 2, Ge-based fully-depleted TFETs are designed and modeled using Synopsys. The simulation results of Ge TFETs are compared with Si TFETs and high-performance Si MOSFETs in Section 3. To achieve high tunneling current density designed for Ge TFETs, submicron abrupt heavily-doped Ge tunnel junctions are explored using rapid melt regrowth (Section 4).

2. Ge interband tunnel transistor modeling

The two-dimensional (2D) electrostatics of Ge interband tunnel transistors and inverters are simulated with the SYNOPSYS TCAD 2005 tool, used in conjunction with Eq. (1), to determine the tunnel

* Corresponding author. Tel.: +1 574 631 4473; fax: +1 574 631 4393.
E-mail address: seabaugh.1@nd.edu (A. Seabaugh).

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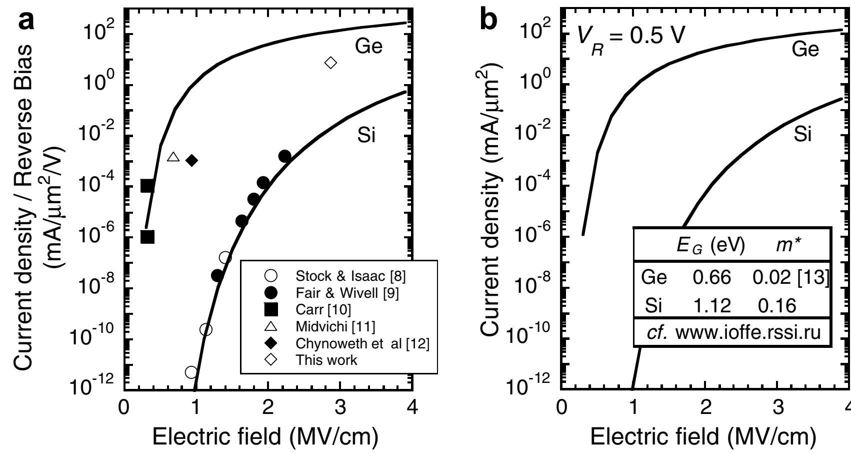

Fig. 1. (a) Tunnel current density per reverse bias vs. electric field for Si and Ge tunnel diodes. Close agreement is obtained between Eq. (1) and measurements with a fitted effective mass of $0.16m_0$, for Si while for Ge, a theoretical mass, $0.02m_0$ [13] is used. (b) Tunnel current density vs. electric field for a reverse junction bias of 0.5 V, showing Ge can provide two orders of magnitude higher current than Si at the same electric field.

transistor current–voltage relations. Scaled cross-sections of the complementary Ge tunnel-transistor pair are shown in Fig. 2a, for an n-TFET, and Fig. 2b, for a p-TFET. The transistors utilize a germanium-on-insulator (GOI) structure, in which a lateral abrupt p^+n^+ tunnel junction is formed in a 2 nm Ge body. A 20 nm long gate is oriented adjacent to the junction to fully-deplete the underlying semiconductor. In the simulations, a 1 nm thick Al_2O_3 dielectric is used as the gate oxide ($\varepsilon_R = 9$, $E_G = 8.7$ eV). Gold with a work function of 4.8 eV is used for the n-TFET gate metal, and Al with a work function of 4.25 eV is used for the p-TFET gate.

The device operation can be understood from the simulated band diagrams shown in Fig. 2a and b. At zero gate bias, the n^+ (n-TFET) or p^+ (p-TFET) body is fully depleted and the transistor is normally off (solid lines) with no direct interband tunneling path. With a 0.5 V gate bias, interband tunneling is turned on (dashed lines) in the Zener tunneling direction. In this geometry, the gate screens the drain field and the current injection is set by the gate-source bias.

SYNOPSYS is used to compute the 2D electrostatics for the transistors of Fig. 2a and b. The channel is divided into 16 layers (with unit thickness of 2 nm/16 = 1.25 Å). For each layer, the band diagram is calculated, from which the reverse voltage and the maximum electric field at the junctions are read and entered into the tunneling current relation of Eq. (1) to determine the current density in mA/μm^2 in each incremental layer; the current is then summed over all 16 layers. The tunneling path may not be restricted to each divided layer, but since the electric field does not change much across the junction (see Fig. 4), this integral method is a good approximation. Shown in Fig. 3 is the dependence of the channel current on gate-to-source bias for drain-to-source biases of 0.5 and 0.1 V, respectively. For both the n- and p-TFET, an on-state current density of nearly 450 μA/μm is achieved at $V_{DS} = |V_{GS}| = 0.5$ V, and the off-state current density, determined from Synopsys, is 3.6 nA/μm. The threshold voltage is 0.05 V using a constant current method with a current of 100 nA, a typical number for MOSFETs [14]. A swing of 50 mV changes the current by more than 3 orders of magnitude, giving an effective subthreshold swing less than 17 mV/decade.

Fig. 4 calculates the influence of the junction abruptness. At on-state, as the abruptness degrades from 0 to 4 nm/decade, the maximum electric field at the junction decreases from ~4 MV/cm to 2.2 MV/cm and the on-state current density degrades almost one order of magnitude. Quantization on the ultra thin Ge body should also influence the current density: the tunneling probability will

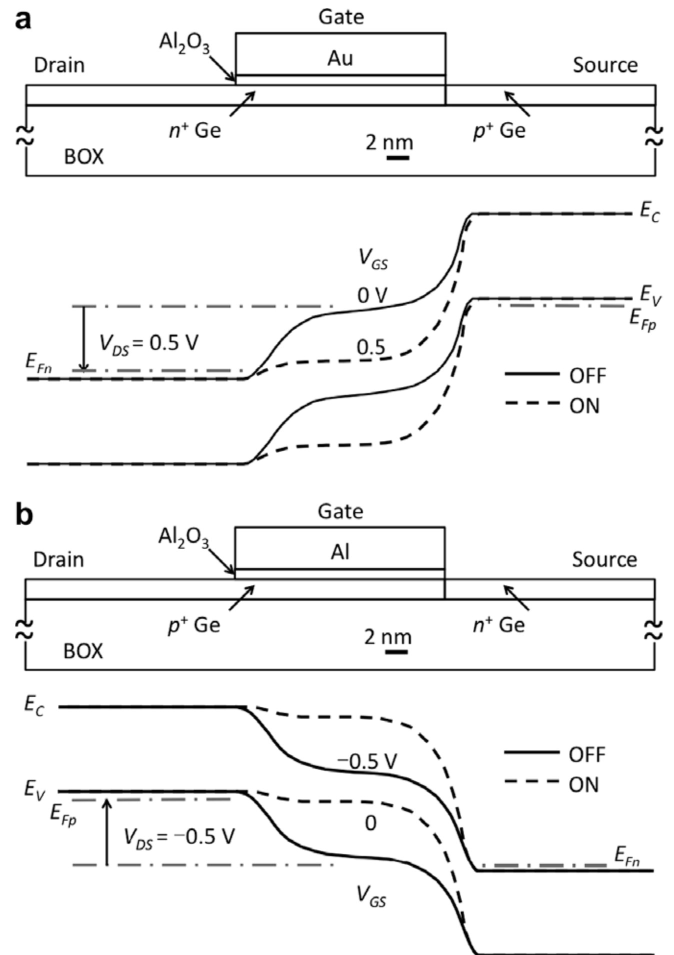

Fig. 2. Cross-section of complementary Ge TFETs, (a) n-TFET and (b) p-TFET, where the ultrathin body is heavily-doped to form a p^+n^+ tunnel junction and the gate is fully-depletes the channel. The computed energy-band diagrams along the center of the channel are shown for both off-state (solid line, $|V_{DS}| = 0.5$ V, $V_{GS} = 0$) and on-state (dashed line, $|V_{DS}| = 0.5$ V, $V_{GS} = 0.5$ V). For the n-TFET, the n^+ doping is 1.8×10^{20} cm^{-3}, and the p^+ doping is 3.2×10^{20} cm^{-3}; for the p-TFET, the n^+ doping is 3.4×10^{20} cm^{-3}, and the p^+ doping is 1.1×10^{20} cm^{-3}.

decrease due to the increase of band gap, while the tunneling density of states will increase from 3D to 2D. The quantization can

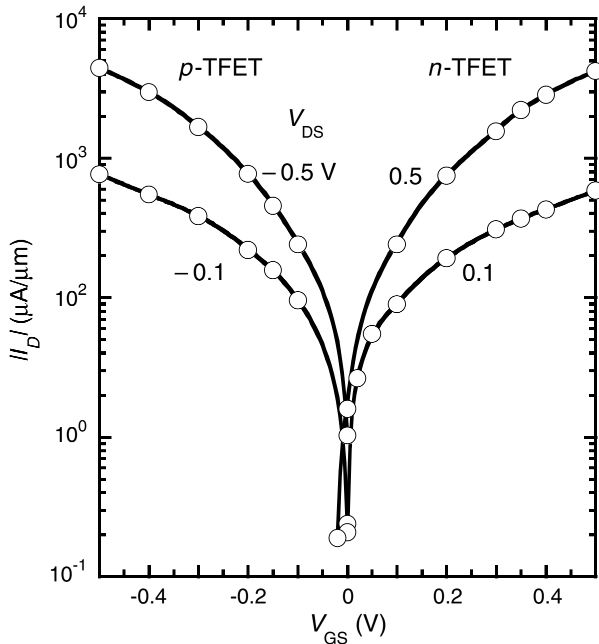

Fig. 3. Simulated transfer characteristics of complementary Ge interband tunnel transistors, using the parameters of Fig. 2 and a gate width of 200 nm.

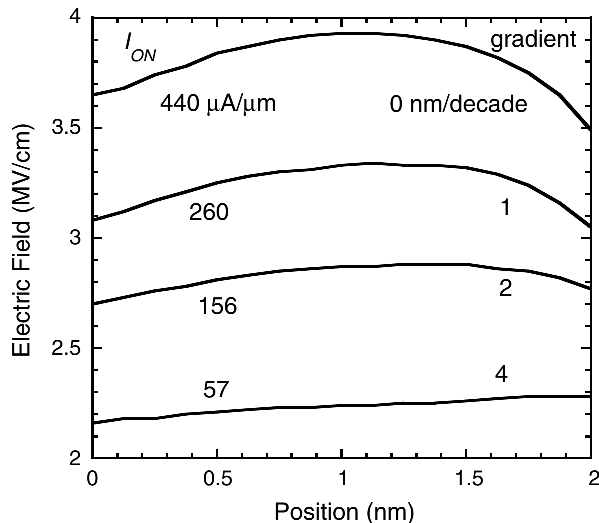

Fig. 4. Junction maximum electric field vs. position to the Ge/Al_2O_3 interface in the channel and as a function of abruptness in the on-state. The on-state current density degrades approximately one order of magnitude as the abruptness degrades from 0 to 4 nm/decade.

cause current to increase or decrease depending on the energetic position of the quantized state.

Fig. 5a shows the simulated load curves of the static Ge tunnel transistor inverter at a supply voltage of 0.5 V. For channel currents under 170 μA/μm, in both the n- and p-TFET, the current saturates with high output resistance. The voltage transfer characteristic is extracted from the load curves and is shown in Fig. 5b. The noise margin is around 100 mV, better than CMOS noise margin requirements of approximately 10% of the supply voltage [15]. The output characteristics and noise margin can be improved by lowering both the n^+ and p^+ doping to 10^{20} cm^{-3} and on-state current density, as shown in Fig. 6. The improved gate control with lower tunnel junction doping results both in better turn-on, saturation characteristics, and higher noise margin, but at the expense of lowering the on-state current density.

3. Interband tunnel transistor performance estimates

Table 1 compares n-TFET performance with scaled nMOSFET targets (highlighted in italic) from the International Technology roadmap for Semiconductors (ITRS) [16]. The on-state MOSFET currents are computed from Frank's model [17] at a supply voltage of 0.5 V, and the off-state MOSFET currents are computed from Hanson's model [18] with $V_{GS} = 0$ and $V_{DS} = 0.5$. From Hanson's model, the off-state current at the 65 nm node (2007) is 0.29 μA/μm, within the ITRS requirement which is 0.34 μA/μm; but the 45 nm (2010) and 32 nm (2013) nodes are $\sim 3\times$ of the ITRS requirements. As the development of high-*k*/metal gate stack technology, the gate leakage could be much lower than the off-state leakage at this stage; Chui has claimed a gate leakage less than 10^{-3} A/cm^2 for HfO_2/Ge structure at 1 V bias, where the equivalent thickness of the oxide is less than 1 nm [19]. This gate leakage level is equal to 2×10^{-7} μA/μm at 20 nm gate length. So the gate leakage is neglected here for the total leakage calculation. For the TFET, the transistor properties are evaluated for Si and Ge with a maximum internal junction field of 4 MV/cm. The off-state current is simulated by SYNOPSYS' generation–recombination model which is in agreement with measurements for the case of Si [4]. Quantization effects are not included in these calculations; quantization would raise the effective band gap and lower the off-currents relative to these predictions. The speed is calculated by *CV*/*I*, and in the last six rows, power and energy consumptions (dynamic and leakage) are calculated for an *n* stage inverter chain ($n = 50$) with an activity factor α ($\alpha = 2\%$), after Hanson et al. [18]. The activity factor of 2% accounts for an average switching of 1 in 50 MOSFETs per cycle.

Since the MOSFET and the TFET are compared at the same supply voltage and similar capacitance, the speeds are determined by the on-state current. Silicon is not attractive for the TFET channel because of its low on-state tunnel current, only 1.2 μA/μm. With this low current the speed is more than $400\times$ lower than the MOSFET. In contrast, the Ge tunnel transistor shows an on-state current density as high as 440 μA/μm at 0.5 V supply voltage, and comparable speed to the 2010 nMOSFET with 18 nm gate length. The off-state current density for the Ge tunnel transistor is 0.0036 μA/μm, much lower than the MOSFET. The low off-state current of the Ge TFET dissipates $2\times$ less power with energy dissipation more than $20\times$ lower than the 2010 MOSFET for a 50-stage inverter chain with an activity factor of 2%.

4. Ge tunnel junctions

4.1. Device fabrication

To realize the proposed Ge interband tunnel transistor requires the development of an abrupt, heavily-doped lateral tunnel junction. Toward this end, a rapid melt growth process for forming Ge interband tunnel junctions has been developed in which evaporated Al contacts on n^+ Ge are liquified in a rapid thermal processor to dissolve back and regrow p^+ Ge and form the tunnel junction [20]. Prior work [20] has shown high current density exceeding 1 mA/μm^2 for micron-scale diodes, but with low peak-to-valley ratio (PVR), under 1.5 at room temperature. In this work, Ge p^+n^+ junctions with sizes ranging from 30×30 μm to 300×300 nm were prepared to explore the tunnel junction dependence on junction size.

The process uses a phosphorus 1×10^{21} cm^{-3} spin-on diffusant followed by rapid thermal annealing to form the n^+ side of the junction [20]. Secondary ion mass spectroscopy (SIMS)

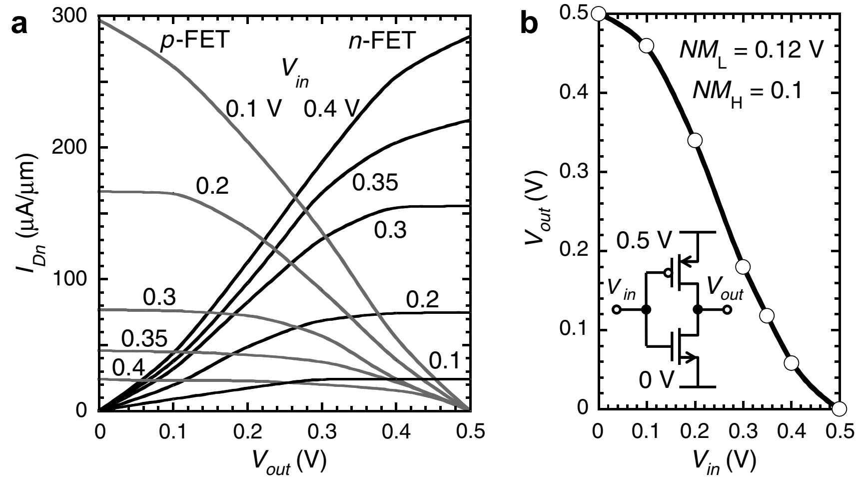

Fig. 5. (a) Simulated load curves for a complementary pair of Ge tunnel transistors in a static CMOS TFET inverter using the geometry of Fig. 2a, n-TFET, n⁺ doping of 1.8×10^{20} cm^{-3}, and p⁺ doping of 3.2×10^{20} cm^{-3}, while for the p-TFET, the n⁺ doping is 3.4×10^{20} cm^{-3} with p⁺ doping of 1.1×10^{20} cm^{-3}: (a) common-source load characteristics and (b) voltage transfer characteristics.

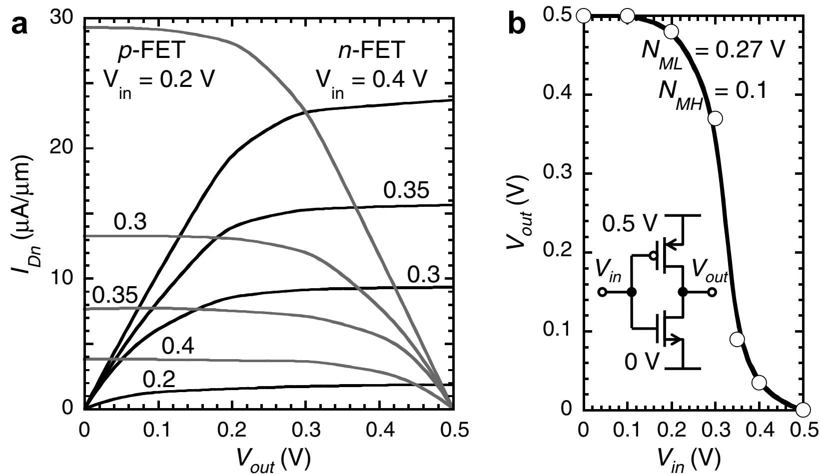

Fig. 6. (a) Simulated load curves for a complementary pair of Ge tunnel transistors in a static CMOS TFET inverter using the geometry of Fig. 2 with identical n- and p-TFET junction dopings, n⁺ = p⁺ = 1×10^{20} cm^{-3}: (a) common–source load characteristics and (b) voltage transfer characteristics.

Table 1

Speed and power estimates comparing nMOSFETs with TFETs. The MOSFET projections are based on the 2007 Edition ITRS Roadmap [16] targets. The TFETs use the geometry of Fig. 2 and are projected as a function of channel material using Synopsys TCAD to compute the leakage currents. For the tunnel currents, Eq. (1) is used with the electric field computed from Synopsys.

Parameter	MOSFET[a]			Tunnel transistor		Unit
	2007	2010	2013[b]	Si	Ge	
Gate length L_G	*25*	*18*	*13*	20	20 nm	
Gate width $W \sim 10L_G$	250	180	130	200	200	nm
Equivalent oxide thickness EOT	*1.1*	*0.65*	*0.5*	1	1	nm
Supply voltage V_{DD}	0.5	0.5	0.5	0.5	0.5	V
On current I_{ON}	428	701	1053	1.2	440	μA/μm
Off current I_{OFF}	0.29	2.02	1.88	2.7E-06	0.0036	μA/μm
Oxide capacitance density $C_{OX} \sim \varepsilon / t_{OX}$	31.4	53.1	69.1	34.5	34.5	fF/μm^2
Gate capacitance $C_G \sim C_{OX}L_G$	0.78	0.96	0.90	0.69	0.69	fF/μm
Intrinsic speed $\tau \sim C_G V_{DD}/I_{ON}$	0.92	0.68	0.43	288	0.78	ps
Leakeage $P_{leak} \sim n\ I_{leak}\ V_{DD}$	7.25	50.50	47.00	6.8E-05	0.09	μW/μm
Dynamic $P_{dyn} \sim 1/2 n I_{ON} V_{DD}\ \alpha$	107	175	263	0.300	110	μW/μm
Total $P \sim P_{leak} + P_{dyn}$	114	226	310	0.300	110	μW/μm
Leakeage $E_{leak} \sim (n I_{leak})\ V_{DD}\ (n\tau)$	332	1722	1002	1	4	aJ/μm
Dynamic $E_{dyn} \sim 1/2\ (nC_G)V_{DD}^2\alpha$	98	120	112	86	86	aJ/μm
Total $E \sim E_{leak} + E_{dyn}$	430	1842	1114	87	90	aJ/μm

Logic depth $n = 50$, activity factor $\alpha = 2\%$.

[a] *ITRS 2007 Edition.*

[b] UTB FD ultra thin body fully depleted.

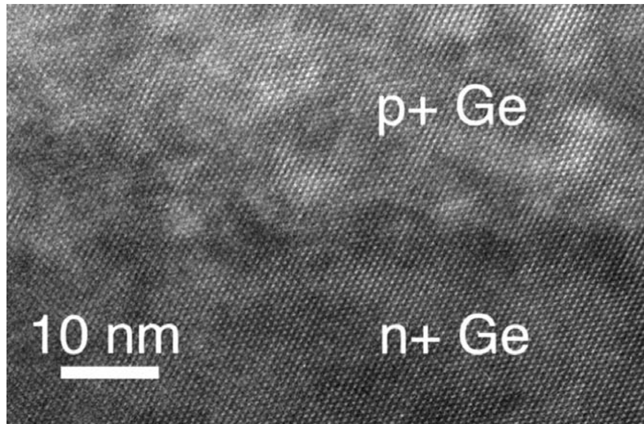

Fig. 7. High resolution TEM image of the Ge p^+n^+ junction. No dislocations are observed.

measurements show that a density of 6×10^{19} cm^{-3} is achieved for the n^+ doping. A 50 nm thick Al film is then patterned by electron beam lithography and lift-off, serving as the acceptor dopant source. A 50 nm plasma Si_3N_4 cap is applied to act as a microcrucible after Liu et al. [21] and hold the Al–Ge melt during the annealing. The rapid thermal annealing of Al in contact with Ge above the eutectic temperature [22] causes Ge to be dissolved into the liquefied Al. On cooling the Ge regrows epitaxially until the eutectic temperature is reached, forming an abrupt, heavily-doped p^+ layer. As the temperature further decreases, Al-rich and Ge-rich phases are nucleated, leaving a eutectic mixture above the Ge p^+n^+ junction. To measure the submicron devices, 100×100 nm vias were written by electron beam lithography and etch, and Ti/Au bondpads were patterned by lift-off.

Fig. 7 shows a transmission electron microscopy (TEM) image of an AlGe-p^+n^+ tunnel junction after 600 °C, 1 s rapid thermal annealing with a cooling rate of 30 °C/s. Energy-dispersive X-ray spectroscopy (EDXS) is used to confirm the presence of Al and locate the junction. Close examination of the p^+n^+ junction in this location and elsewhere shows no evidence of dislocations. Fig. 8 shows the overall non-uniformity of the junction, a cross section through a 10×10 μm^2 device. EDXS analysis of the eutectic mixture above the regrown Ge layer shows that the darker regions are the Al-doped Ge-rich phase, and the lighter regions are the Al-rich phases as expected from the phase diagram [22]. Electron diffraction patterns show that the Ge-rich regions of the eutectic mixture are within a few degrees of the same crystallographic orientation as the Ge substrate, indicating that these regions are nucleated epitaxially off the regrown layer.

4.2. Current–voltage characteristics

Fig. 9 shows the current–voltage (*I–V*) characteristics of Ge tunnel junctions with sizes ranging from 10×10 μm^2 to 300×300 nm^2. Negative differential resistances are observed, a signature of abrupt heavily-doped junctions. Series resistance shifts are responsible for the voltages differences between small and large area devices. For the 300×300 nm^2 diode, a peak current density of 0.15 mA/μm^2 is achieved, corresponding to an effective doping of $\sim 3.5 \times 10^{19}$ cm^{-3} [23]; and 1 mA/μm^2 zener tunneling current is achieved at the reverse bias of 0.13 V, where the maximum electric field of 2.87 MV/cm is calculated assuming an ideal abrupt junction. Compared with the calculated current density of Ge tunnel diodes shown in Fig. 1, the measured current density is lower, which might be caused by the non-ideal junction abruptness. If a 4 nm/decade abruptness is assumed, the electric field will decrease to 1.6 MV/cm, in agreement with the current density calculation. The PVR is low and does not increase significantly as junction area is reduced. The low PVR appears to be a result of point defects or the junction doping non-uniformity. Doping non-uniformity results in a peak current and peak voltage which depends on position. Measurements on a non-uniform junction is the superposition of *I–V* behavior over each incremental area; these sum to lower the overall PVR.

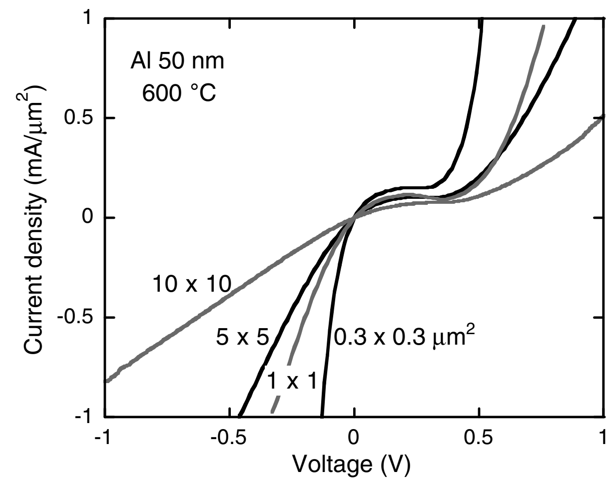

Fig. 9. Current–voltage characteristics of Ge tunnel junctions formed by 600 °C rapid melt regrowth of 50 nm Al on n^+ Ge.

5. Conclusions

Complementary fully-depleted Ge interband tunnel transistors are designed and simulated, showing low subthreshold swing, low off-state current and on-state current density as high as 440 μA/μm. Compared with a 2010 nMOSFET at 0.5 V supply voltage, Ge interband tunnel transistors can save 2× in power and 20× in energy for a 50-stage inverter chain with an activity factor of 2% while not sacrificing speed. Submicron Ge tunnel junctions were

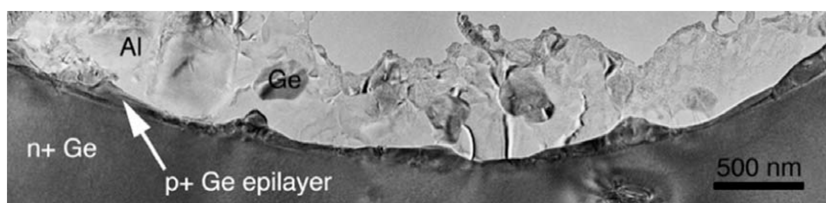

Fig. 8. Transmission electron micrograph of a 10×10 μm AlGe-p^+n^+ tunnel junction after 600 °C rapid thermal annealing. The interface is flat is some areas and curved in other areas, like the one shown.

fabricated by a rapid melt growth technique, and show a clean doping interface without observable dislocations. The low PVR is explained by point defects or junction non-uniformity.

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