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Fully Differential Current-Mode Configuration for the Realization of First-Order Filters with Ease of Cascadability

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Abstract: It is well known that fully differential signal processing is more advantageous than single-ended signal processing in a noisy environment, and is widely used in audio, video and other signal processing applications. This paper introduces a new fully differential configuration that contains a first-order low-pass (LP) filter, high-pass (HP) filter, and all-pass (AP) filter, all present within the same circuit design. The proposed fully differential configuration is simple and employs only one multiple-output current differencing transconductance amplifier and one grounded capacitor. The circuit has a wide operating frequency range (up to 73 MHz). The additional features offered by the proposed circuit include use of the lowest number of active and passive components, suitability of the integrated circuit chip, support of cascadability, electronic tunability, no passive component-matching restrictions, availability of all first-order responses, i.e., LP, HP, and AP, and low-level operating supply voltages. Non-ideal and parasitic analyses are investigated for the proposed circuit, and PSPICE simulation results are presented to verify the proposed theory. Additionally, the proposed fully differential LP filter circuit is experimentally verified using off-the-shelf ICs. Moreover, the cascading feasibility is demonstrated by realizing a fully differential *n*th-order LP filter.

Keywords: analog circuit; current-mode; fully differential filters; low-pass filter; high-pass filter; all-pass filter

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1. Introduction

The design of continuous-time analog filters remains a highly vital and demanding area of research. The main reason that analog filters are popular is their application in audio, video and communication systems; for example, all-pass (AP) filters are used as phase equalizers and are applied as a sub-component of quadrature oscillators [1–3]. A first-order universal filter realizes high-pass (HP), low-pass (LP), and AP configurations in the same circuit. A large part of technical documentation [4–11] is focused on single-ended first-order filters, due to their design simplicity and implementation. However, single-ended circuits have several drawbacks in a few specific ambient conditions. For example, the single-ended circuits' performance in a noisy environment deteriorates, whereas a fully differential (FD) circuit performs better in noisy conditions. FD filter designs have many advantageous features over single-ended filters, such as better rejection of noise associated with power supply, a wider output linearity range, and less even-order harmonics. Subsequently, several FD first-order filters, voltage-mode (voltage input and voltage output)-type and current-mode (current input and current output)-type, have been reported in the literature [12–20]. The FD configurations of [12–14,16,18–20] only realize AP filters. The circuit

presented in [17] realizes LP and HP filters in one circuit, and AP filters in another. The circuit of [15] can realize either LP and AP, or HP and AP, within the same circuit. Thus, none of the earlier reported FD circuits realize all first-order filters within the same circuit topology. Additionally, the study of these FD circuits reveals that all the earlier reported FD circuits use either one or more floating passive component(s), which is not desirable from an integration point of view. There are also several other limitations in the earlier reported circuits, which are as follows:

- Excessive count of passive components [12–17,19,20];
- Passive component matching restriction [12–17,19,20];
- Not cascadable [12–16,19,20];
- Use of high-power supplies [13,15–18,20];
- Low operating frequency [12–20].

This work aims to present an FD configuration that can realize all the responses of a first-order filter (LP, HP and AP) within the same circuit, and overcome the limitations of earlier reported FD circuits. Using a single multiple-output current differencing transconductance amplifier (MOCDTA) and one grounded capacitor makes the circuit structure simple and suitable for integrated circuit fabrication. Ease of cascadability, electronic adjustment of pole frequency, no passive component-matching restrictions, fewer sensitivity figures and low operating supply voltages are additional attributes of the proposed circuit. In the paper, the non-idealities and parasitic analyses are also included. An FD nth-order LP filter is also realized to demonstrate the cascading feature.

2. First-Order Fully Differential Configuration

The proposed first-order FD configuration is based on active element CDTA. The active element used, CDTA [21], is a versatile active element and has a wide operation frequency range. Numerous linear and non-linear circuits operating in voltage and/or current-mode, using CDTA, are presented in the literature [22–25]. A symbol of MOCDTA is depicted in Figure 1. The terminal relationships of MOCDTA are specified below.

$$\begin{bmatrix} I_{Z1} \\ I_{Z2} \\ I_{Z3} \\ I_{O1+} \\ I_{O2-} \\ I_{O3-} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & g_m & 0 & 0 \\ 0 & 0 & -g_m & 0 & 0 \\ 0 & 0 & -g_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_P \\ I_N \\ V_{Z1} \\ V_{Z2} \\ V_{Z3} \end{bmatrix} \quad (1)$$

where g_m is transconductance gain of MOCDTA.

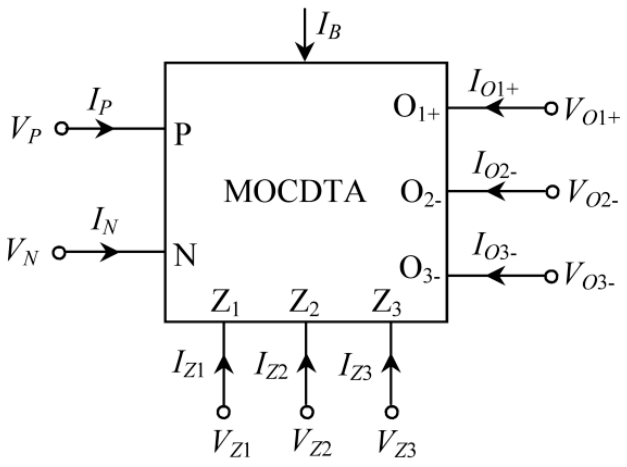


Figure 1. Symbol of MOCDTA.

The proposed first-order FD configuration using single MOCDTA and one capacitor, which realizes LP, HP and AP filters within the same circuit structure, is shown in Figure 2. The input differential current ($I_{in} = I_{in1} - I_{in2}$) signal is connected between low impedance terminals, whereas output differential current signals are accessible between high impedance terminals. Thus, the circuit offers rich cascadability without requiring any additional current buffer(s). By using the terminal relationships of Equation (1) and solving the nodal equations of the circuit, the following expressions of currents I_1, I_2, I_3 and I_4 are obtained.

$$I_1 = \frac{g_m I_{in}}{sC + g_m},\ I_2 = \frac{-sCI_{in}}{sC + g_m},\ I_3 = \frac{-g_m I_{in}}{sC + g_m},\ I_4 = -I_{in} \tag{2}$$

where $I_{in} = I_{in1} - I_{in2}$.

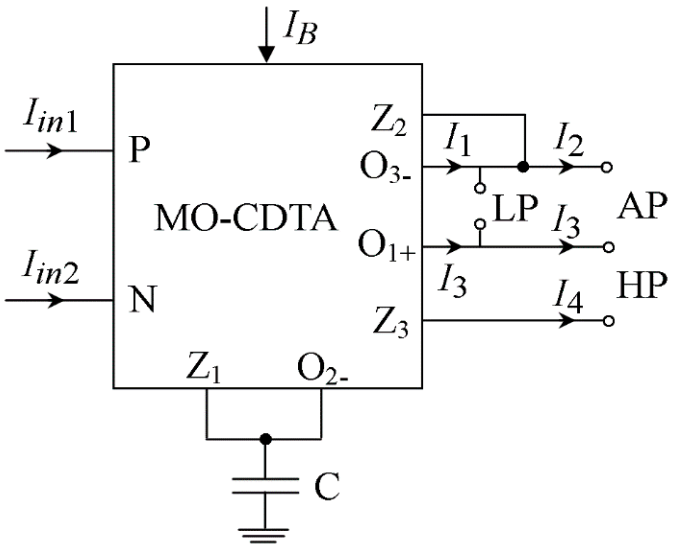


Figure 2. The proposed fully differential configuration realizing first-order filters.

The transfer functions of the proposed FD LP, HP and AP filters are given as follows:

$$\frac{I_{LP}}{I_{in}} = \frac{I_1 - I_3}{I_{in1} - I_{in2}} = \frac{2g_m}{sC + g_m} \tag{3}$$

$$\frac{I_{HP}}{I_{in}} = \frac{I_3 - I_4}{I_{in1} - I_{in2}} = \frac{sC}{sC + g_m} \tag{4}$$

$$\frac{I_{AP}}{I_{in}} = \frac{I_2 - I_3}{I_{in1} - I_{in2}} = -\frac{sC - g_m}{sC + g_m} \tag{5}$$

The pole frequency f_P obtained from Equations (3)–(5) is given as follows:

$$f_P = \frac{g_m}{2\pi C} \tag{6}$$

The pole frequency can be varied electronically by controlling the value of g_m via the bias current of MOCDTA.

3. Non-Ideal and Parasitic Aspects

The non-ideal model of MOCDTA is specified below:

$$\begin{gathered} I_{Z1} = \alpha_1(I_P - I_N), I_{Z2} = \alpha_2(I_P - I_N), \\ I_{Z3} = \alpha_3(I_P - I_N), I_{O1+} = \gamma_1 g_m V_{Z1}, \\ I_{O2-} = -\gamma_2 g_m V_{Z1}\ and\ I_{O3-} = -\gamma_3 g_m V_{Z1} \end{gathered} \tag{7}$$

In Equation (7), α_1, α_2 and α_3 are the non-ideal current transfer gains and γ_1, γ_2 and γ_3 are the non-ideal transconductance gains. By considering the non-ideal model of Equation (7) and solving the nodal equations of the circuit, the following expressions of LP, HP and AP filter functions are obtained.

$$\frac{I_{LP}}{I_{in}} = \frac{\alpha_1(\gamma_1+\gamma_3)g_m}{sC+\gamma_2 g_m} \tag{8}$$

$$\frac{I_{HP}}{I_{in}} = \frac{\alpha_3 sC + g_m(\alpha_3\gamma_2 - \alpha_1\gamma_1)}{sC+\gamma_2 g_m} \tag{9}$$

$$\frac{I_{AP}}{I_{in}} = \frac{-\alpha_2 sC + \alpha_1\gamma_1 g_m + g_m(\alpha_1\gamma_3 - \alpha_2\gamma_2)}{sC+\gamma_2 g_m} \tag{10}$$

Equations (8)–(10) show that the filter's gain and pole frequency now depend upon the non-ideal gains. The new pole frequency obtained from Equations (8)–(10) is given as follows:

$$f_P = \frac{\gamma_2 g_m}{2\pi C} \tag{11}$$

It is to be noted from Equation (11) that the pole frequency f_P is not adversely affected and depends only on γ_2, while it is independent of other non-idealities. It is to be mentioned that the -3 dB bandwidth of non-ideal gains is quite high, and at lower frequencies, their magnitude is almost the same. Therefore, the effects of these non-ideal gains at lower frequencies may be neglected. The sensitivities of f_P relating to g_m, capacitor and non-ideal gains are given in Equation (12), which conforms low-sensitivity figures.

$$\begin{gathered} S_{f_P}^{g_m} = -S_{f_P}^{C} = S_{f_P}^{\gamma_2} = 1, \\ S_{f_P}^{\alpha_1} = S_{f_P}^{\alpha_2} = S_{f_P}^{\alpha_3} = S_{f_P}^{\gamma_1} = S_{f_P}^{\gamma_3} = 0 \end{gathered} \tag{12}$$

The following parasitic effects are included in MOCDTA: small resistances R_P and R_N in series at P and N terminals, respectively, and parallel combinations of $R_{Z1}//(1/sC_{Z1})$, $R_{Z2}//(1/sC_{Z2})$, $R_{Z3}//(1/sC_{Z3})$, $R_{O1+}//(1/sC_{O1+})$, $R_{O2-}//(1/sC_{O2-})$ and $R_{O3-}//(1/sC_{O3-})$ at Z_1, Z_2, Z_3, O_{1+}, O_{2-}, and O_{3-}, respectively. The inclusion of these parasitic effects may affect the proposed circuit, and reanalysis of the circuit gives the following expressions of transfer functions of the LP, HP and AP filters:

$$\frac{I_{LP}}{I_{in}} = \frac{2g_m}{sC_P+g_{mP}} \tag{13}$$

$$\frac{I_{HP}}{I_{in}} = \frac{sC_P+1/R_P}{sC_P+g_{mP}} \tag{14}$$

$$\frac{I_{AP}}{I_{in}} = -\frac{sC_P-g_{mP}}{sC_P+g_{mP}} \tag{15}$$

where $g_{mP} = g_m + \frac{1}{R_P}$, $R_P = R_{Z1} + R_{O2-}$ and $C_P = C + C_{Z1} + C_{O2-}$.

The grounded capacitor C can easily absorb the parasitic capacitances C_{Z1} and C_{O2-}. Equations (13)–(15) show that the proposed fully differential circuit is less affected by the parasitic effects of MOCDTA.

The pole frequency f_P is now changed, as expressed below:

$$f_P = \frac{g_{mP}}{2\pi C_P} \tag{16}$$

The parasitic resistances R_{Z1} and R_{O2-} are quite large in magnitude; therefore, $g_{mP} \approx g_m$. Thus, the parasitic effects on pole frequency are negligible. The filter order is also not changed by the parasitic effects.

4. Simulation Results

The proposed FD first-order filters are simulated through PSPICE with 0.13 µm TSMC CMOS technology. The CMOS structure of MOCDTA is shown in Figure 3 [22] and the transistor's W/L ratios are listed in Table 1. The supply voltage and bias voltage are set to ±1 V and −0.56 V, respectively. The bias current is I_B = 150 µA (for which g_m = 1 mS). The simulated values of non-idealities and parasitic effects of MOCDTA are given in Table 2. The designed pole frequency is 1.59 MHz, for which the capacitor is selected as 100 pF. The AC responses of the proposed circuit for gain and phase are shown in Figure 4. The simulated value of pole frequency is observed to be 1.587 MHz. The transient response for an AP filter at pole frequency, when a differential current of 50 µA in amplitude is applied at the input, is depicted in Figure 5. In Figure 5, the differential input and output current signals are in a quadrature relationship at pole frequency. The total harmonic distortion of AP output current is found to be less than 2%. The gain and phase plots of the AP filter for the bias current values of I_B = 50, 100, 150 and 200 µA are depicted in Figure 6. The gain plots at different bias currents are overlapped with each other and phase plots at different values of bias current, I_B = 50, 100, 150 and 200 µA, provide pole frequency values of 0.74, 1.24, 1.587 and 1.78 MHz, respectively. The high-frequency response of the circuit at 73 MHz is also tested for C = 2 pF and I_B = 150 µA. The transient response for an AP filter at pole frequency of 73 MHz is depicted in Figure 7, which confirms the good operating frequency. Additionally, the temperature stability of the circuit is also examined. The transient responses for an AP filter for 0 °C to 75 °C temperature variations are depicted in Figure 8. It is noted that the performance of the circuit as a result of the temperature variation is not adversely deteriorated. Furthermore, Monte Carlo simulations for 1000 runs were carried out to verify the performance of the proposed circuit against capacitor variation and the MOS transistor's threshold voltage variation. Figure 9 shows the histogram of maximum amplitude and pole frequency for an AP filter with 10% Gaussian deviation in capacitor values. Figure 10 shows the histogram of maximum amplitude and pole frequency for an AP filter with 5% Gaussian deviation in threshold voltages. For the capacitor deviation, the mean values of amplitude and pole frequency are 51.22 µA (2.44% error) and 1.58 MHz (0.62% error), respectively. For threshold voltage deviation, the mean values of amplitude and pole frequency are 51.37 µA (2.74% error) and 1.58 MHz (0.62% error), respectively. Figures 9 and 10 confirm that the proposed FD circuit is less affected by the capacitor and threshold voltage variations. The proposed circuit consumes a maximum power (measured in simulation) of 2.5 mW at I_B = 150 µA. Table 3 shows the key features of the proposed FD configuration, illustrating the advantages of the proposed first-order FD circuit over earlier reported first-order FD circuits.

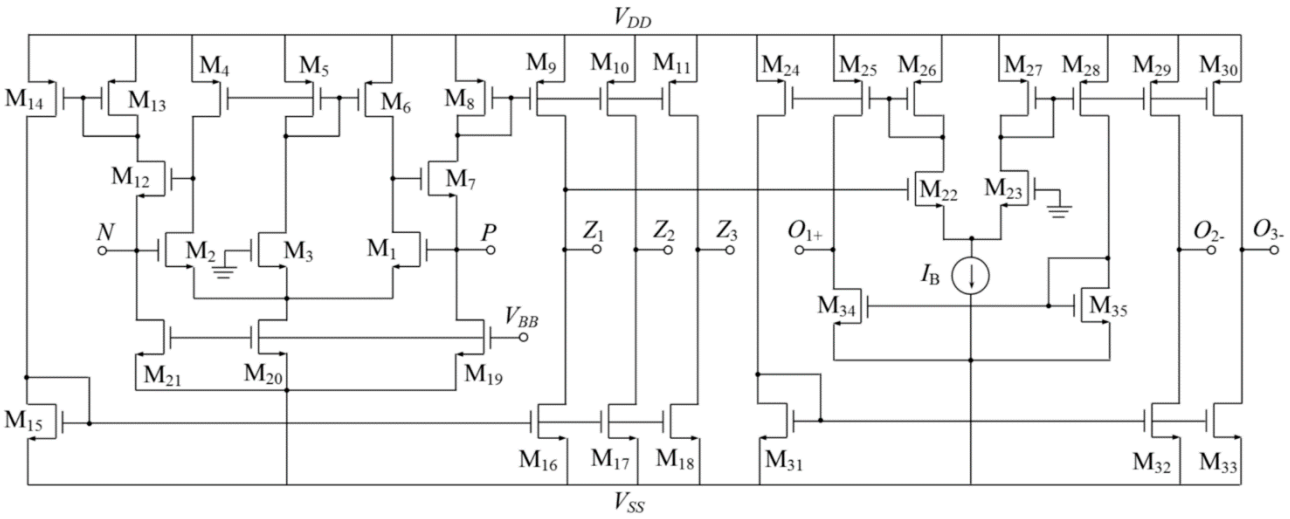


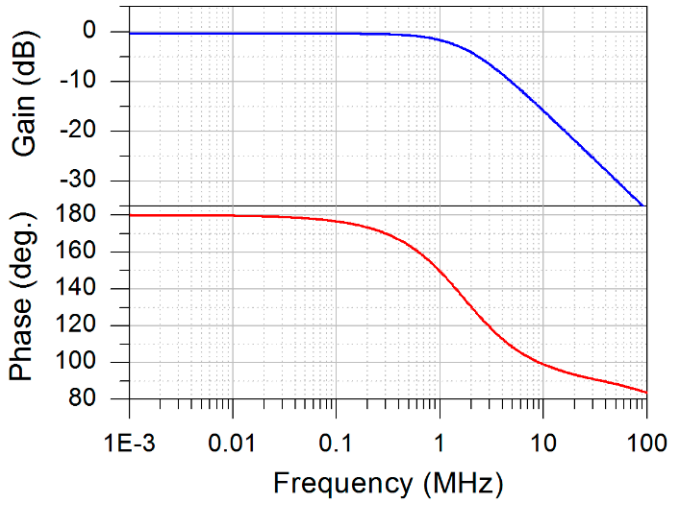
Figure 3. CMOS implementation of MOCDTA.

Table 1. W/L ratios of MOS transistors.

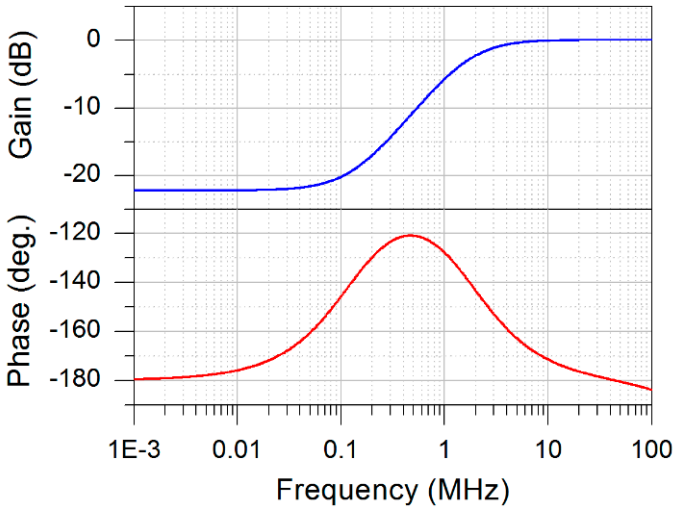
MOS Transistors	W(μm)/L(μm) Ratio
M_1–M_3	26/0.26
M_4–M_6,	10.4/0.26
M_8–M_{11}, M_{13}–M_{18}, M_{22}, M_{23}	3.9/0.26
M_7, M_{12}	15.6/0.26
M_{19}–M_{21}	13/0.26
M_{24}–M_{30}	1.5/0.26
M_{31}–M_{35}	1/0.26

Table 2. Simulated values of non-idealities and parasitic effects of MOCDTA.

Parameter	Simulated Value
α_1, α_2, α_3	0.99
−3 dB bandwidth of α_1, α_2, α_3	1 GHz
−3 dB bandwidth of γ_1, γ_2, γ_3	2 GHz
R_P, R_N	14 Ω
R_{Z1}, R_{Z2}	100 kΩ
R_{O1+}, R_{O2-}, R_{O3-}	125 kΩ

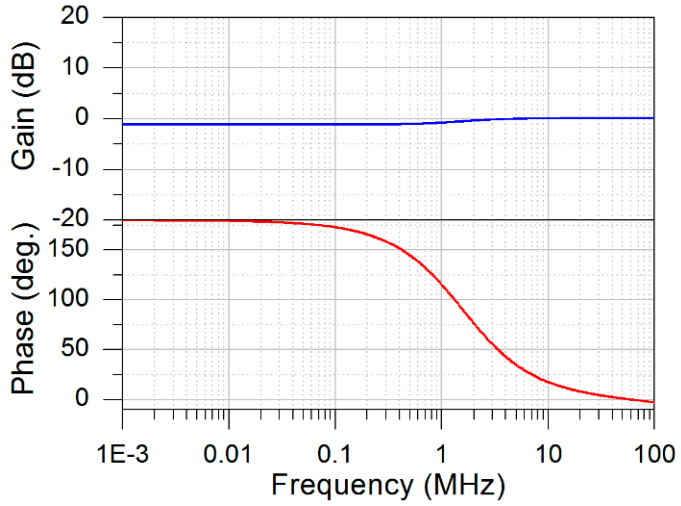


(**a**)



(**b**)

Figure 4. *Cont.*



(**c**)

Figure 4. Frequency responses of gain and phase: (**a**) LP; (**b**) HP; (**c**) AP.

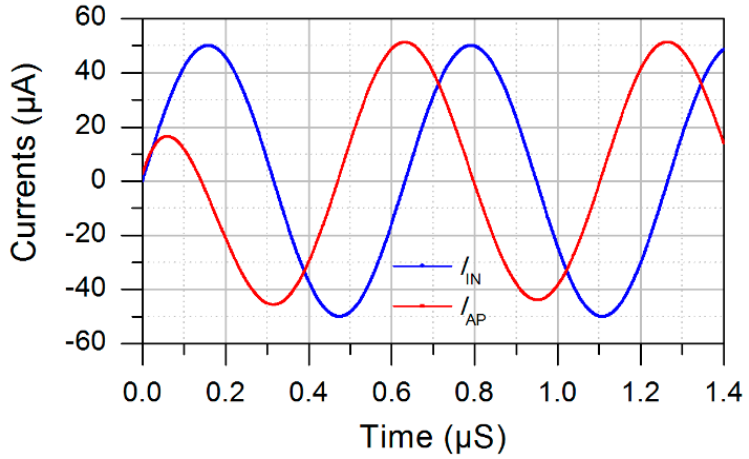
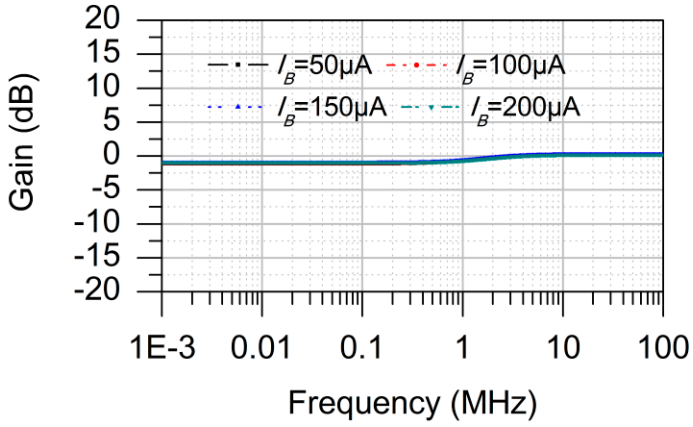
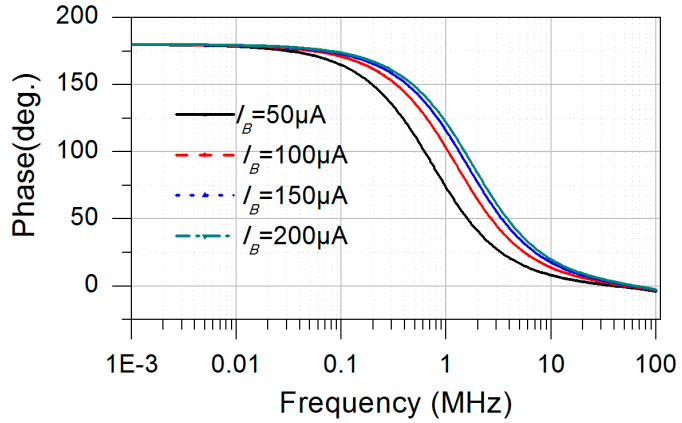


Figure 5. Differential input current and differential AP output current at 1.58 MHz.



(**a**)

Figure 6. *Cont.*



(**b**)

Figure 6. Frequency responses of AP filter at different bias current for (**a**) gain and (**b**) phase.

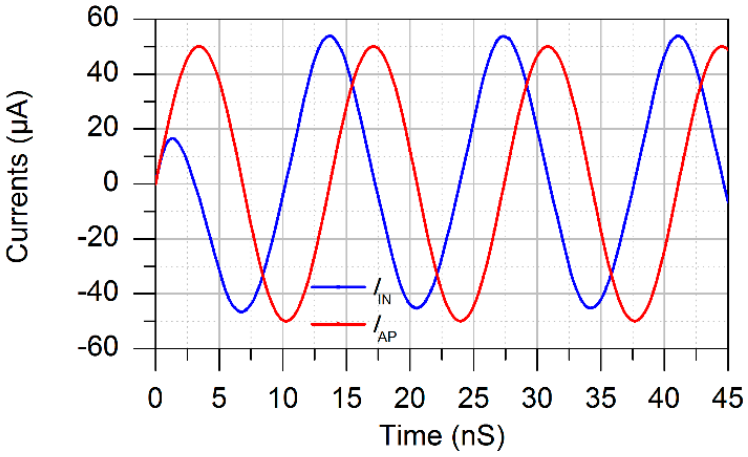


Figure 7. Differential input current and differential AP output current at 73 MHz.

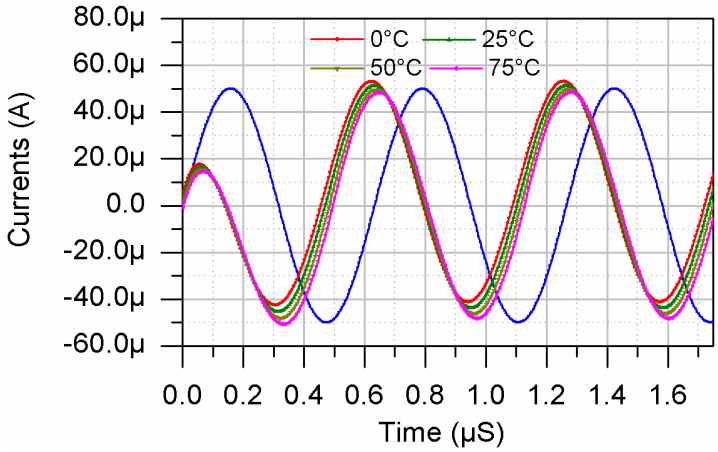


Figure 8. Transient responses of differential AP output currents at 0, 25, 50 and 75 °C.

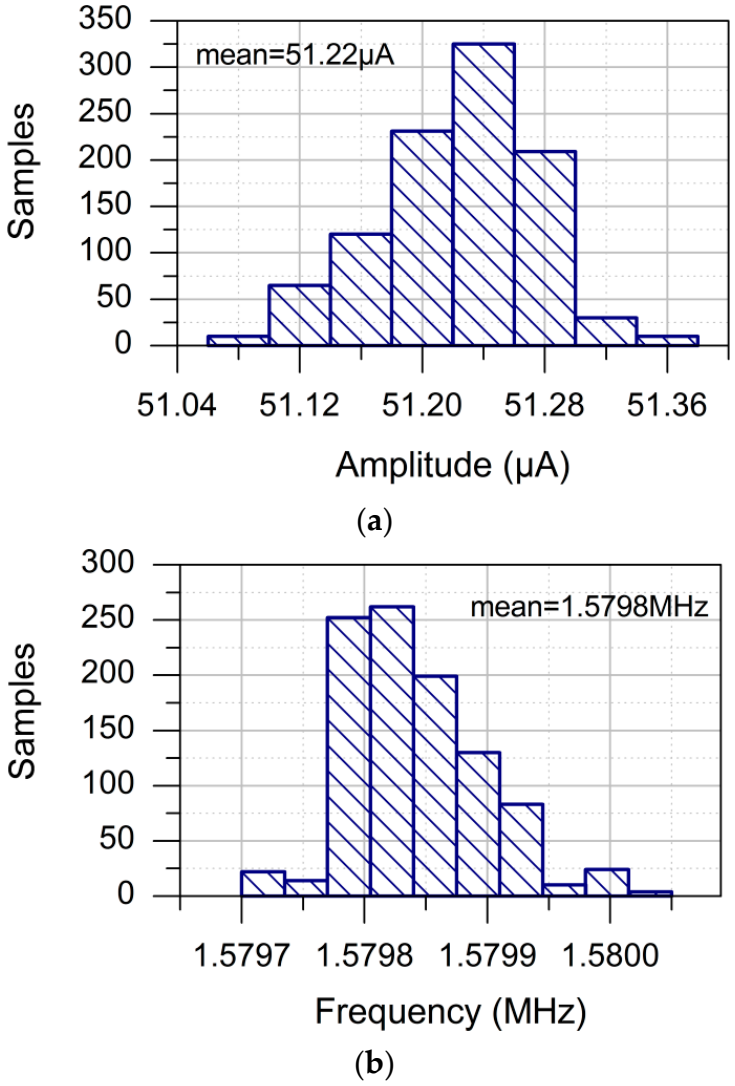


Figure 9. Monte Carlo simulation results for the variation in capacitor value: (**a**) histogram for maximum amplitude; (**b**) histogram for pole frequency.

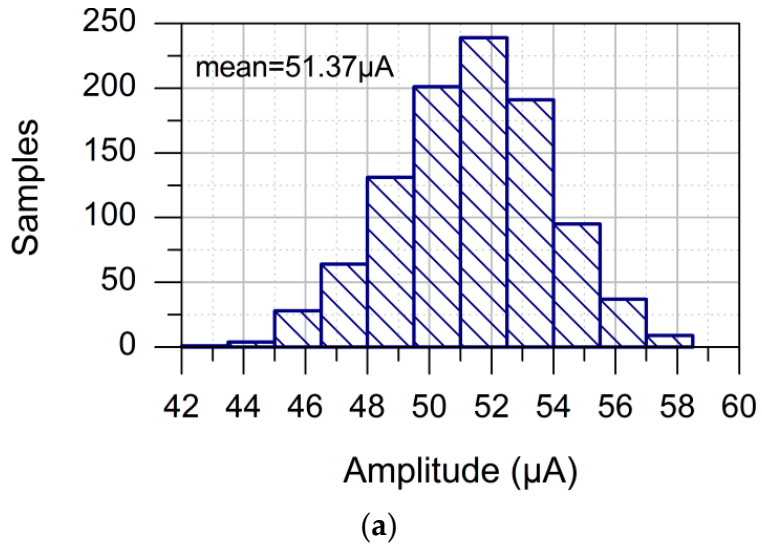
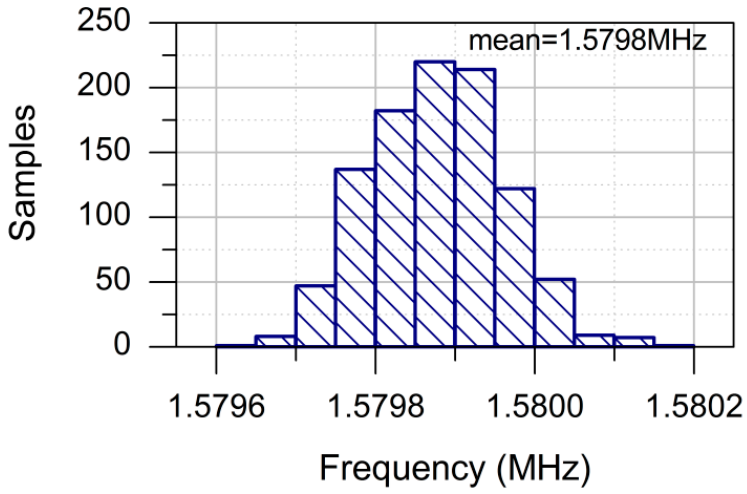


Figure 10. *Cont.*



(**b**)

Figure 10. Monte Carlo simulation results for the variation in threshold voltages: (**a**) histogram for maximum amplitude; (**b**) histogram for pole frequency.

Table 3. Comparison among the proposed fully differential first-order circuit and earlier reported fully differential first-order circuits.

Ref.	Active Element/Count	Passive Components with Count	All Grounded Passive Component	Passive Component Matching Restriction	Operating Mode	Cascadable	Availability of LP, HP and AP Responses	MOS Transistors Count	Technology (µm)	Max Operation Frequency	Supply Voltage(s) (V)
[12]	FDDTA/1	1-R, 2-C	No	Yes	VM	No	Only AP	34	0.18	0.04 MHz	0.5
[13]	DVCC/1	3-R, 1-C	No	Yes	VM	No	Only AP	18	0.5	2.27 MHz	±2.5
[14]	DDCC/1	3-R, 1-C	No	Yes	VM	No	Only AP	12	0.18	0.32 MHz	±0.9
[15]	DPDVCC/2	2-R, 2-C	No	Yes	VM	No	AP and LP or AP and HP	92	0.25	0.27 MHz	±2.5
[16]	DV-DXCCII/1	3-R, 2-C or 2-R, 3-C	No	Yes	VM	No	Only AP	30	0.25	6.13 MHz	±1.25
[17]	DC-DVCC/1	2-R, 1-C	No	Yes	CM	Yes	LP and HP	38	0.5	1.58 MHz	±2.5
	DC-DVCC/2	4-R, 2-C	No	Yes	CM	Yes	Only AP	76	0.5	1.58 MHz	±2.5
[18]	ACA/1, CF/2	1-C	No	No	CM	Yes	Only AP	50	0.18	0.94 MHz	±1.2
[19]	FBCCII/1	6-R, 2-C	No	Yes	VM	No	Only AP	34	0.18	290 Hz	0.5
[20]	DVCC/1	1-R, 3-C	No	Yes	VM	No	Only AP	18	0.5	3.18 MHz	±2.5
This work	MOCDTA/1	1-C	Yes	No	CM	Yes	All LP, HP and AP	35	0.13	73 MHz	±1

FDDTA: fully differential difference transconductance amplifier, DVCC: differential voltage current conveyor, DDCC: differential difference current conveyor, DPDVCC: digitally programmable DVCC, DV-DXCCII: differential voltage dual-X second-generation current conveyor, DC-DVCC: digitally controllable DVCC, ACA: adjustable current amplifier, CF: current follower, FBCCII: fully balanced CCII, VM: voltage mode, CM: current mode, LP: low-pass, HP: high-pass, AP: all-pass.

5. Experimental Results

The proposed fully differential LP filter configuration is experimentally verified using off-the-shelf ICs. The practical implementation of the proposed LP filter configuration is shown in Figure 11. The experimental set-up using breadboard and discrete components is depicted in Figure 12. The input currents I_{in1} and I_{in2} are applied with the help of external resistors R_1 and R_2, respectively. The output LP signal is observed across the load resistor

R_3. The power supplies used are ±10 V. The passive components are selected as follows: $R_1 = R_2 = R_3 = 1$ kΩ, $C = 10$ nF. The bias current is set to 70 µA ($g_m = 1$ mS). The input signal of 0.75 V in magnitude is applied to observe the output across resistor R_3. Figure 13 shows the input and output signals at different frequencies (1 kHz, 10 kHz, 40 kHz and 100 kHz). A phase difference of 180° is clearly seen between the input and output at low frequency (1 kHz), which is in accordance with the simulation results shown in Figure 4a. Additionally, the plot of gain response for the LP filter configuration is shown in Figure 14.

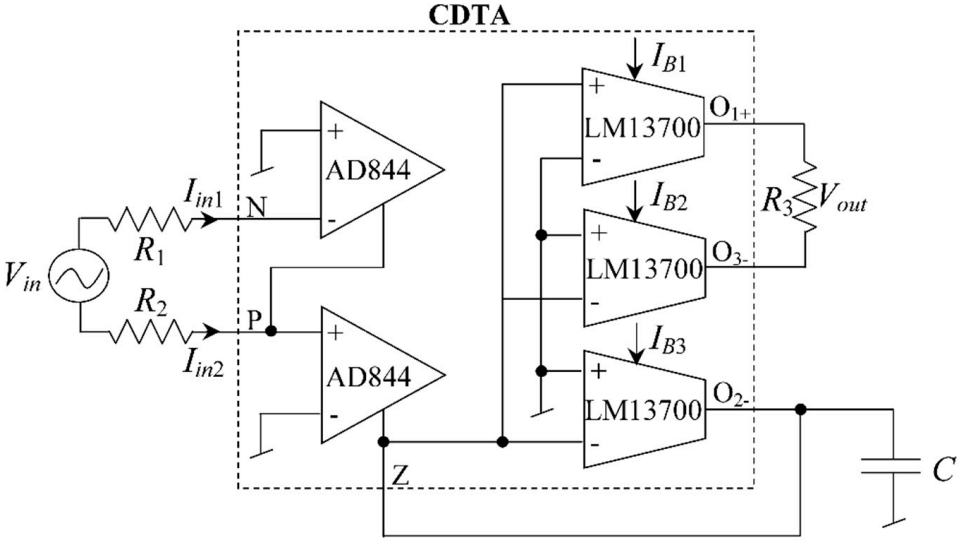


Figure 11. Practical implementation of the proposed fully differential LP filter.

Figure 12. Experimental set-up using breadboard and discrete components.

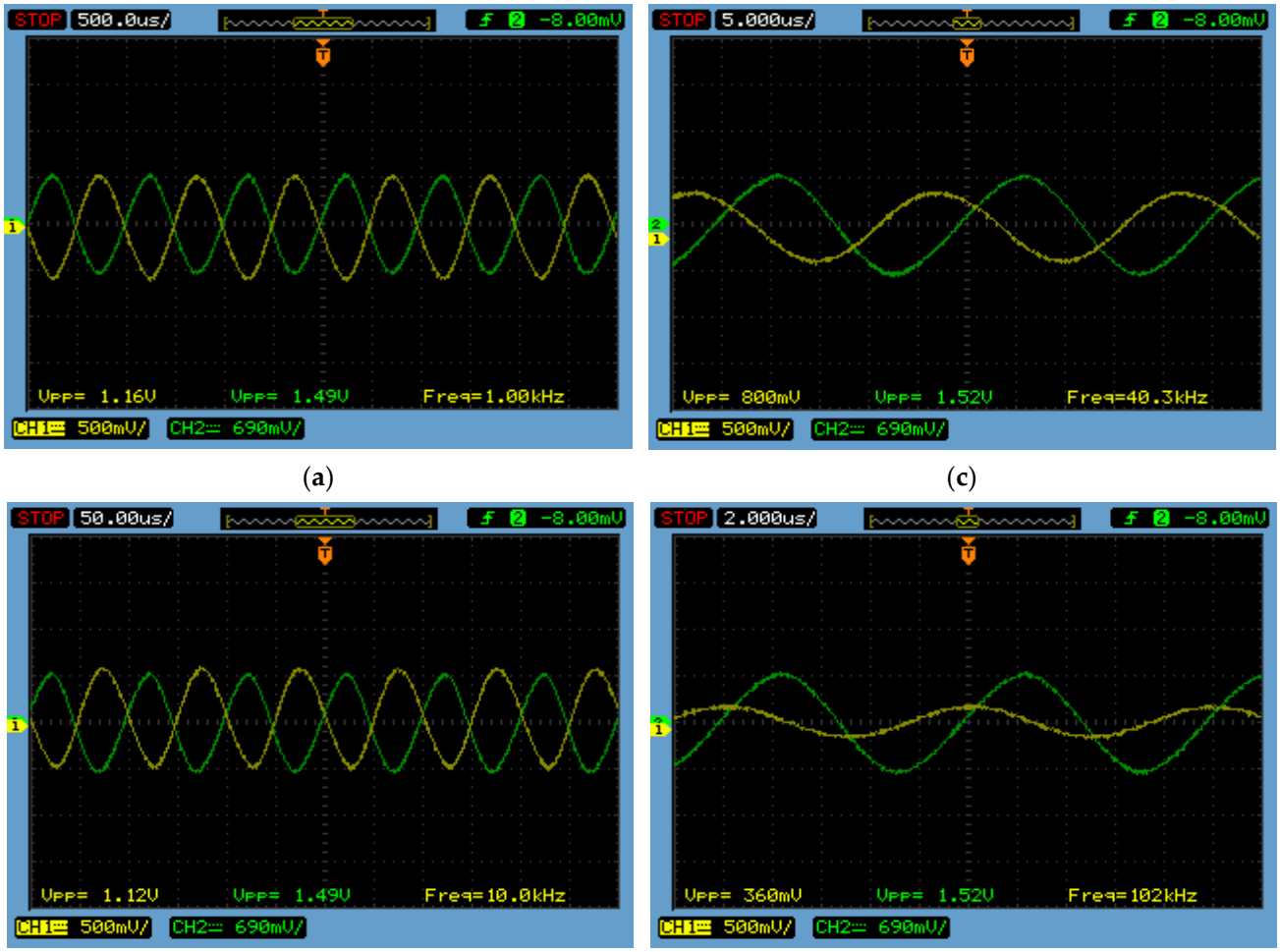


Figure 13. Experimental results of the LP filter showing input and output waveforms at (**a**) 1 kHz, (**b**) 10 kHz, (**c**) 40 kHz and (**d**) 100 kHz.

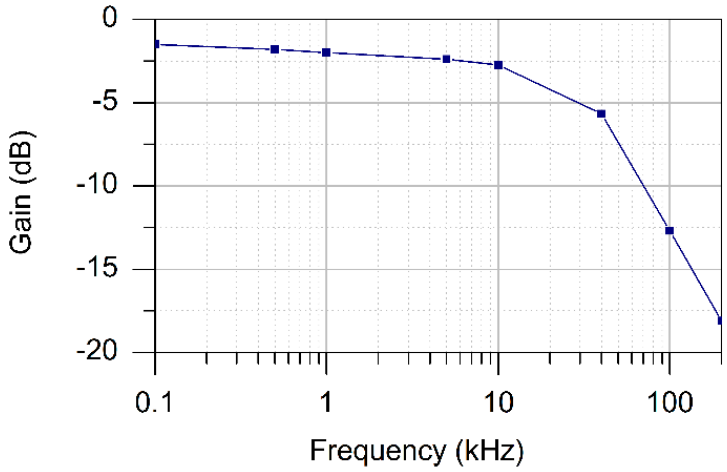


Figure 14. Plot of gain response for the LP filter for experimental results.

6. Cascading Feasibility

The cascading ability of the presented configuration is further examined by realizing an *n*th-order FD LP filter. The output currents of the proposed fully differential filters are available from the high impedance terminals, making the proposed filters easily cascadable

without requiring additional circuitry. Figure 15 shows the FD nth-order LP filter circuit, which is realized by cascading the n number of FD first-order LP filters. The transfer function of the realized FD nth-order LP filter is given as follows.

$$\frac{I_{LP}}{I_{in}} = \frac{I_1 - I_2}{I_{in1} - I_{in2}} = \left(\frac{2g_m}{sC + g_m}\right)^n \tag{17}$$

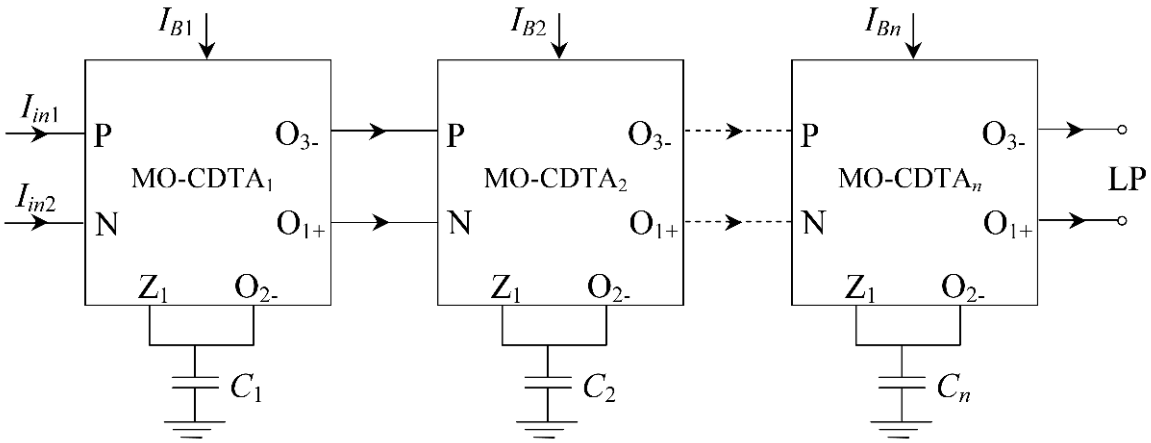


Figure 15. The proposed fully differential configuration realizing the nth-order LP filter.

The pole frequency f_P of the filter obtained from Equation (17) is given as follows:

$$f_P = \frac{g_m}{2\pi C} \tag{18}$$

The nth-order circuit is validated by simulating it for n = 3. The circuit is simulated by using I_B = 150 µA and C_1 = C_2 = C_3 = 100 pF. The simulated gain and phase of the circuit are shown in Figure 16. The variation in the phase of the third-order LP filter from 0° to −270° is confirmed in Figure 16.

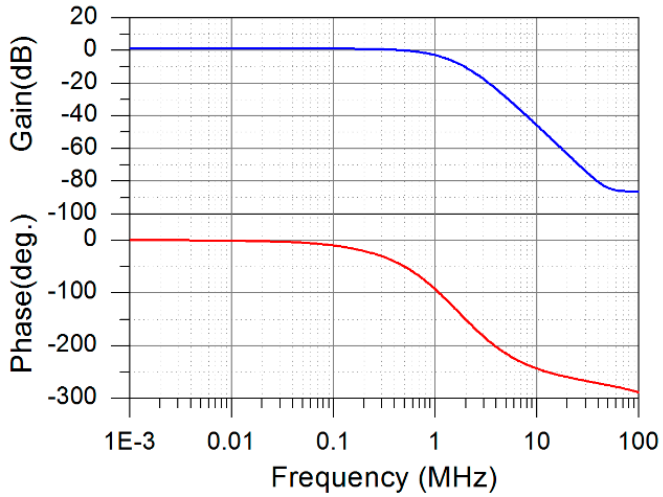


Figure 16. Frequency responses of gain and phase of the third-order LP filter.

It should be noted that a higher-order HP filter and higher-order AP filter can also be implemented by cascading first-order filters in the same way as the higher-order LP filter shown in Figure 15. Figure 17 shows the gain and phase of the third-order HP filter. The frequency and transient responses of the third-order AP filter are shown in Figure 18. Figure 18a shows a phase variation of 0° to −540° for the AP filter.

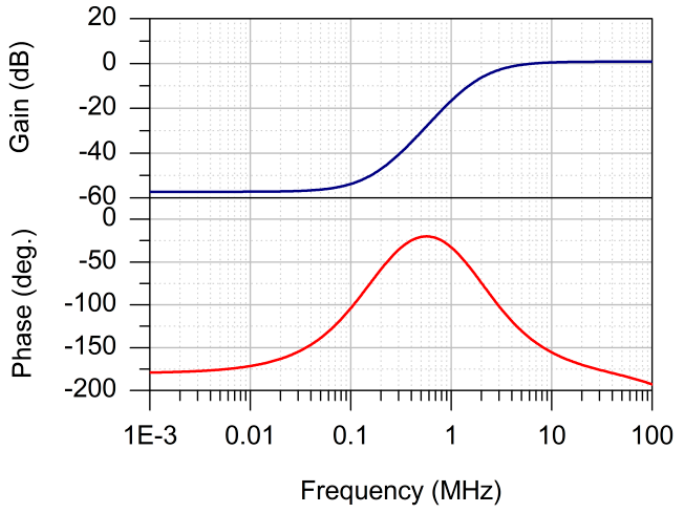
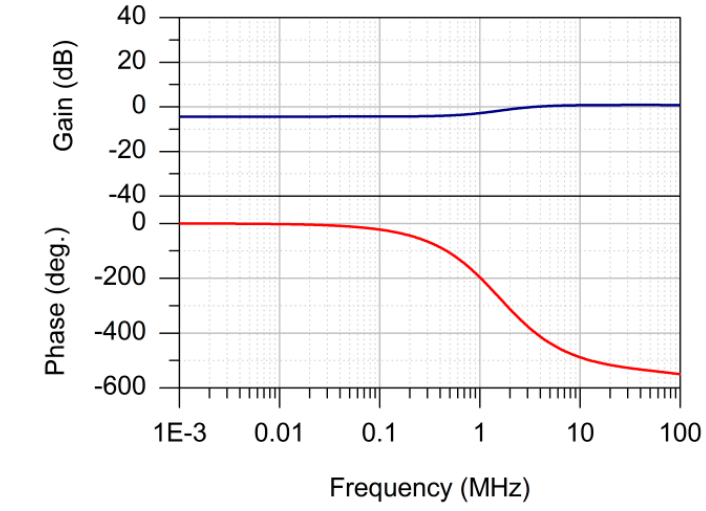
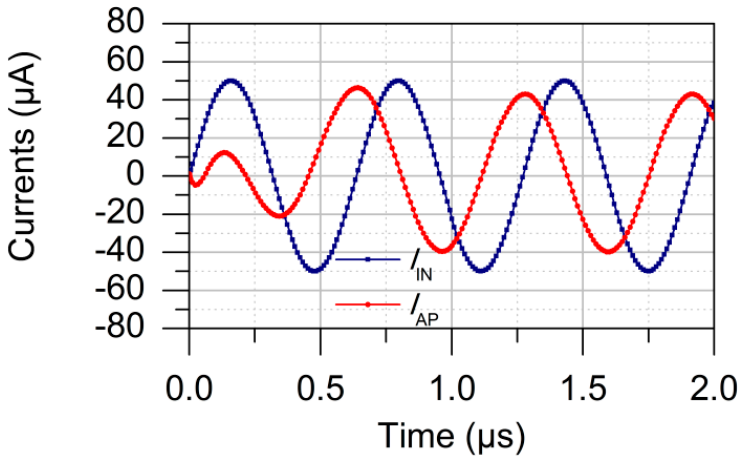


Figure 17. Frequency responses for gain and phase of the third-order HP filter.



(**a**)



(**b**)

Figure 18. Third-order AP filter's responses: (**a**) frequency responses of gain and phase; (**b**) transient response for differential input and output currents.

7. Conclusions

In this paper, a MOCDTA-based FD first-order filter circuit, has been realized, with the LP, HP, and AP responses all obtainable within the same circuit structure. Low input and high output impedances are favorable for cascadability. Some other valuable features of the circuit include resistorless realization, use of grounded capacitor only, electronic tunability, lower sensitivity figures, low operating supply voltages, wider operational frequency range and low power consumption. The proposed FD configuration is less affected by temperature variation, capacitor variation and threshold voltage variation. An *n*th-order FD LP filter has also been realized to demonstrate the cascading feasibility of the proposed FD first-order filter. The fully differential operability of the proposed circuit makes it favorable for several applications, such as audio systems, data transmission and communication systems.

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