MSc THESIS

Fully Integrated Analog Front-end for a 2-electrode ECG device

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Abstract

Cardiovascular diseases are leading cause of deaths worldwide. With increasing graying population and limited health infrastructure there is a need for portable and implantable ECG devices to diagnose these diseases early on. In general an ECG device requires three or more electrodes, which need to be applied to the body via a gel, to obtain a satisfactory reading. This puts a constraint on the portability of the device. This thesis deals with designing a fully-integrated 10 bit analog front-end i.e. an instrumentation amplifier and an ADC, specifically, for a two-electrode ECG device. Integrated ECG read-out circuits have to deal with two challenges mainly viz. obtaining a high common-mode rejection ratio (CMRR) and integrating large time-constants on the chip.

Firstly, all sources of interference which affect an ECG reading is studied. It is shown that for a portable and integrated read-out circuit, a high CMRR is obtained from the fact that the device will be floating and hence the circuit itself need not have a high CMRR.

Existing techniques for integrating large time-constants are presented and compared. It is shown that these techniques either give rise to unpredictable time-constants and are non-linear near the required cut-off frequency or consume a lot of power from a system perspective. A novel mixed-signal feedback technique using a sigma-delta ADC has been proposed wherein the digital signal is scaled, integrated and fed back to the previous analog stage. The advantages of such a method are more control over the position of the cut-off frequency and higher linearity. The power consumption needed to implement such a technique is negligible.

The circuit is designed in CMOS 0.35μm I3T25 technology. The designed instrumentation amplifier reports the best SNR and 3rd highest Noise-Efficieny Factor (NEF). The linearity at the cut-off frequency is shown to be of 10 bits which is an improvement of 3 bits over existing techniques. The total static power consumption for the system is 66μW. The implementation of the time-constant consumes only 40nW of static power.

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It's a magical world, let's go exploring - *Calvin's last words (of Calvin and Hobbes fame)*

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Introduction

Use of electricity in medical diagnosis has undergone rapid progress since the time Lugi Galvani, an Italian anatomist in the 18th century, demonstrated the existence of 'animal electricity' in frogs [8]. From then to nowadays, wherein electrical currents generated by the various parts of the body such as the heart, the brain, the muscles to name a few, are used for medical diagnosis, the understanding and usage of this discovery has advanced a great deal.

ECG(electrocardiogram) is by far the most common usage of electrical activity reading for medical diagnosis [9]. It is a recording of the electrical activity generated by the heart over a period of time. By interpreting this activity, one can diagnose the condition of the heart. The first ECG device was invented in 1902 by Willem Einthoven, a Dutch scientist [10]. Generally, the ECG is monitored by placing a number (3-12) of electrodes (also known as leads) on the human body. To obtain a satisfactory reading, the skin needs to be chafed and a special (Ag-AgCl) gel needs to be applied before connecting the electrodes [11].

Traditionally, the ECG devices have been quite bulky and costly and thus are present only in select hospitals and health centers. The increasing graying population, especially in the western world, has spawned a need for the overhaul of the present limited health infrastructure and enablement of personal, cheap and immediate health-care to people. Thus there is a great deal of interest in portable, hand-held devices and implantable solutions which would enable in the read-out of these electrical signals.

This thesis concentrates on developing an integrated analog front-end circuit for a portable 2-electrode ECG device which uses 'dry' electrodes i.e. no gel needs to be applied. By using such electrodes not only certified technicians are not needed to operate the ECG device but also ensures that the skin need not be prepared every time an ECG is to be read and thus increases patient comfort. By reducing the number of electrodes, the size of the device can be made smaller and thus more portable. A fully integrated front-end solution also helps in this respect. Currently, integrated solutions manage to achieve a maximum of 8 bits of resolution. There is a need for High-resolution ECGs (> 10 bit) which aid in diagnosing conditions such as AMI (Acute Myocardial Infarction) [12].

This thesis will examine the feasibility i.e. the advantages and challenges of using a 2-electrode device from a circuit-level perspective. This thesis will also investigate the challenges in increasing the resolution of an integrated front-end. The main objectives of the thesis can be broadly stated as:

1. Identify all the interference sources which would affect the performance of the above described device.

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2. Identify the bottleneck for resolution in an integrated design and suggest possible solutions.

3. Develop a circuit-level schematic of the system based on the study done in the above points.

4. Design the whole system for low-power operation.

This report is divided into six chapters. Chapter 1 provides pre-requisite knowledge for designing an ECG read-out device. It discusses the principle of generation of an ECG signal and ECG device characteristics. It also discusses the existing work in literature in this area and original contributions of this thesis in brief. Chapter 2 studies the interference sources that affect an ECG reading. This will be followed by discussing the system-level design in Chapter 3. Chapter 4 concentrates on circuit-level design and the challenges encountered for each of the blocks identified in Chapter 3. In Chapter 5, system simulation results are presented. Chapter 6 provides a summary of this report and concludes with possible improvements in the design.

ECG signal and device characteristics

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To understand the specifications of the read-out device, it is first necessary to understand the characterisctics of the input signal i.e. the ECG. Section 1.1 describes the working of the heart and explains how the ECG is generated. Section 1.2 and Section 1.3 present the nomenclature and the characteristics of the ECG signal. Section 1.4 describes the physical characteristics of the read-out device. This knowledge is important as it will be used in later chapters to make a few decisions regarding the design of the circuit. The chapter concludes by a brief discussion on the existing work in literature in this area, the challenges specific to the design of read-out circuit for this particular application and original contribution of this thesis.

1.1 Structure of the heart

The heart is an inverted conical shaped, hollow muscular organ, about the size of a human fist. It is divided into right and left sides by a vertical wall made of muscle called the septum. Both the sides are further divided into two with the top chambers called the atria and the bottom chambers called the ventricles. The left and right atria and their corresponding ventricles are separated from each other by one-way valves called mitral valve and tricuspid valve respectively.

The left and right sides of the heart can be imagined as self-contained pumping
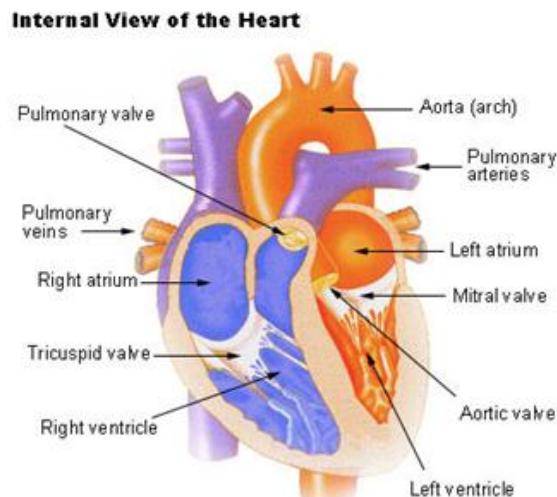
Figure 1.1: Internal view of the heart [1]

stations which are connected in series. The left side drives oxygen-rich blood, which it receives from the lungs, to all the cells of the body. The oxygen-rich blood enters into the left atrium from the lungs through a valve called the pulmonary valve. The atrium contracts and sends the blood into the left ventricle through the mitral valve which closes once this operation is over to prevent it from flowing back into the atrium. The left ventricle then contracts and sends it for circulation into the body. The working of the right atrium and the right ventricle is similar to that of its left counterparts. After circulation, the oxygen-poor blood returns to the right atrium. The right atrium then contracts and transfers it to the right ventricle through the tricuspid valve. Like the mitral valve, this also closes after the blood is transferred to prevent the blood from flowing back. The right ventricle then contracts and sends this blood to the lungs for replenishment, completing one full cycle.

The contraction of the chambers is triggered through application of electrical impulses or stimuli. These impulses are generated at regular intervals by the SA node (SinoAtrial node) present in the right atrium. Each impulse travels throughout the walls of the atrium, causing it to contract. There is a node present between the atrium and ventricles called the AV node (AtrioVentricular node) which adds a delay to the impulse traveling from the atrium to the ventricle. This ensures that the atria contract before the ventricles do. Electrical impulses travel in the heart (as a matter of fact in the whole human body) by a phenomenon called depolarization and re-polarization which will now be discussed as it is crucial in understanding how an ECG wave is generated.

All the cells maintain an electrical charge difference across their membranes, known as the resting potential of the cell. This electrical polarization is present due to complex protein structures embedded into the cell membrane. The potential difference across the cell membrane is around 70mV-80mV for atrial cells and 90mV for ventricular cells. By convention, the potential outside the cell membrane is taken as reference.

In the resting phase, i.e., when there is no electrical stimulus applied to the cell, positive Na^+ and Ca^{2+} ions are present outside the cell membrane and negative Cl^- ions within it. If a potential below a certain threshold value is applied outside the cell (stimulus given by pacemaker cells), channels within the membrane open and positive ions rush inside the cell to achieve equilibrium. The influx of positive ions increases the potential of the cell and thus opening more channels in the membrane. This continues to happen until all the channels are open. The equilibrium is reached when the cell potential reaches around +10mV w.r.t its surroundings. This causes a breakdown in the membrane of the adjacent cell and so on, leading to a wave called the depolarization wave.

After depolarization of the cell, the concentration of Ca^{2+} ion within it increases by almost an order of magnitude. This leads to hydrolysis of ATP (a type of protein) present within the cell, causing the cell membrane to close and the cell to contract. The whole cycle of depolarization and re-polarization keeps on repeating till an electrical stimulus is applied. One cycle of polarization is known as an action potential.

Fig. 1.2 depicts a cardiac action potential i.e. one cycle of depolarization and re-polarization of the cell. It has 5 phases (numbered 0-4). Phase 4 is the resting potential of the cell, when no stimulus is applied. The Phase 0 depicts the depolarization stage of the cycle. The maximum rate of depolarization can be calculated by the slope (dV/dt) in this region. In Phases 1 and 2, the influx and outflow of positive ions is balanced out and hence the potential of the cell is maintained. The re-polarization of the cell can be seen in Phase 3.

As the heart cells undergo the depolarization and re-polarization cycle, this
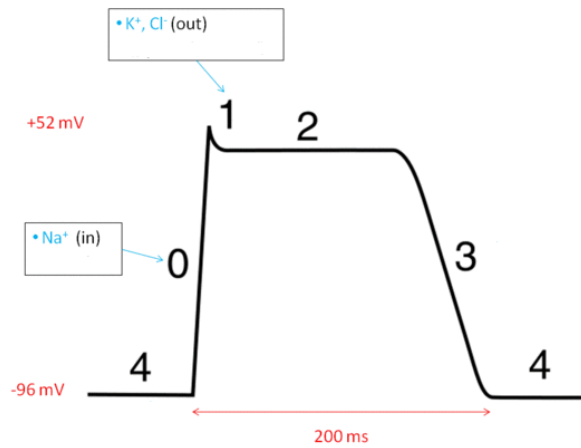
Figure 1.2: Cardiac Action Potential [2]

electrical activity is not confined not only to the heart but is also spread throughout the body through body fluids and tissues by a similar mechanism. The sum of all action potentials generated by all the cells gives a net voltage difference which is known as the ECG wave which is used for diagnosis. The next section discusses the generation of the ECG signal and its various segments vis-a-vis the mechanism described above.

1.2 ECG wave

As discussed in the previous section, the ECG wave is the net total of action potentials of all the cells. Thus the shape of the ECG wave will depend on the direction in which we view the heart and hence the position of the electrodes. In technical terms, the ECG signal is essentially a vector whose value depends on the position of the electrodes (Fig. 1.3).

Fig. 1.4 depicts the ECG wave from various electrode positions. The names of ECG waves signify the position of the electrodes. Their nomenclature standard is outside the scope of discussion for this thesis.

Although there is no fixed shape, each ECG signal can be divided into 5 main
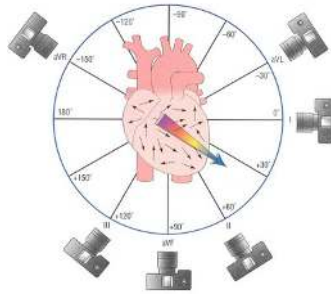
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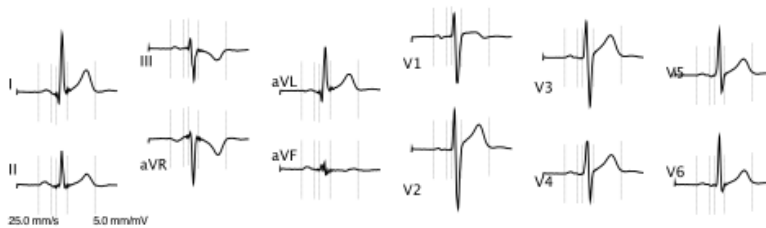
Figure 1.4: ECG signals from different leads [4]

segments viz. P, Q, R, S and T. To gain a better understanding, Fig. 1.5 shows an idealized representation of the ECG signal when the electrodes are positioned on the wrists of the person (position I in Fig. 1.4).

Each segment carries information about the functioning of a specific region of the heart. The P-wave occurs when the atria cells undergo depolarization. The electrical impulse travels from the right atrium to the left atrium. In normal working of the heart, the P-wave would be around 80ms - 100ms duration. The QRS-wave occurs when the ventricular cells undergo depolarization. It is larger in magnitude than the P-wave as the ventricular cells are thicker and larger in mass as compared to those of the atria (as can be seen from Fig. 1.1. The T-wave represents the re-polarization of ventricles. The re-polarization of atria cells coincides with the depolarization of ventricles and hence is masked by the QRS wave.

The duration of each wave and that of the connecting segments gives an insight into the working of the heart, enabling diagnosis. The amplitude and timing characteristics of the ECG signal can be seen in Fig. 1.5. The nominal amplitude of an ECG wave is 1mV, although it can be as high 5mV or as low as 0.1mV in some cases [13], [14].

In the next section, specifications for the design of the read-out system will be discussed.
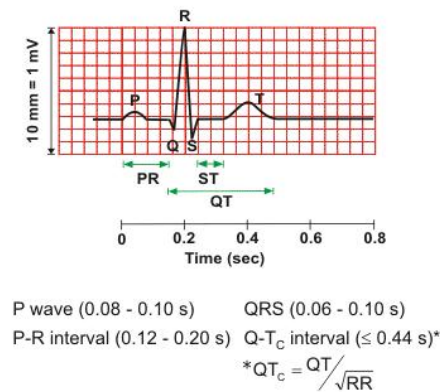
Figure 1.5: ECG signal [5]

1.3 ECG signal characteristics

Fig. 1.5, lists the nominal time durations of each of the segments of the ECG wave. Medical professionals or computer programs interpret the ECG by studying the deviations from these nominal values. Therefore it is of utmost importance that the ECG read-out system faithfully reproduces the signal. The amount of distortion that can be tolerated depends on two criterion viz. application of the ECG device and the end user of the device.

Usually all the segments of an ECG wave are not of interest. Different applications require interpretation of different segments (Table 1.1). For example, to measure the heart rate, only the R-R timing interval is required. The timing of PQ-segment and ST-segment is not of particular interest in this case. To diagnose arrhythmia, the shape and time duration of the S-wave and ST-segment is important [15]. Thus while designing the read-out system, we have to make sure that the signal content in the frequency band of interest is not affected.

The end user of the ECG readout system determines the amount of noise or distortion that the application can tolerate. For example, the human eye can distinguish distortion smaller than 1%-5% (7-bits of resolution) [16]. Thus if a human person was to interpret an ECG, a read-out system with Total Harmonic Distortion (THD) around 1% would be sufficient whereas in the case of automated signal processing, the specification would be decided by the tolerance of the DSP algorithms that would follow and in general would be much lower. Since the distortion specification is not very clear, in our system, a distortion specification which meets the resolution requirements of the ADC is considered sufficient.

Also, since the requirements of the ECG read-out are heavily application dependent there are no specific standards that an ECG reading device has to adhere to. Although there are a few standards in the IEC (*International Electrotechnical Commission*) and AHA (*American Heart Association*) which are not strictly required to be

Table 1.1: A few ECG applications along with the required frequency bandwidth

Processing	Bandwidth (Hz)
Display	0.5 - 40
QRS detection	0.5-40
Arrhythmia detection	0.05-60
ST segment monitoring	0.05-60

followed but are used as guidelines by device manufacturers.

AHA recommends that the bandwidth of an ECG device used for standard clinical applications should have a bandwidth of 0.5Hz to 100Hz. IEC 60601 standard states that the input referred noise of any ambulatory ECG device should not be greater than $30\mu V_{\mathrm{rms}}$ [17]. Assuming an input signal of $1mV_{\mathrm{rms}}$, as per the previous section, the target SNR for most applications is therefore 40dB or 8 bits of resolution.

Other design parameters that are important for any medical device are its input impedance and CMRR. These will be discussed in detail later chapters.

The next section will discuss in detail the device and the application and thus the specifications for the design of the read-out.

1.4   Description of device

Technically, an ECG device requires only two electrodes to read the electrical activity. However, three electrodes are the most common ones because a third electrode is required as a reference electrode, which provides a reference common-mode voltage for the ECG device. It is usually needed to improve the CMRR of the device or reduce the common-mode noise, which is the bottleneck in almost all front-end designs for an ECG device.

As stated in the previous section, the placement of these electrodes will decide the shape of the ECG wave. The more number of electrodes, the more the number of voltage differences, the more elaborate the information and hence better the diagnosis.

Fig. 1.6 shows one of the popular ECG electrode position. Here, the ECG signal is read out as a voltage difference between the electrodes on the left and the right arm and the electrode on the right leg providing the reference. This position is also known as the Einthoven's Triangle, named after the inventor of the first ECG reading device.

Before the electrodes are attached to the body, the skin is prepared by scraping it with sandpaper. This is done to remove the upper dry skin and hence reduce the impedance of the skin. A gel (Ag-AgCl gel) is then applied to facilitate a low impedance
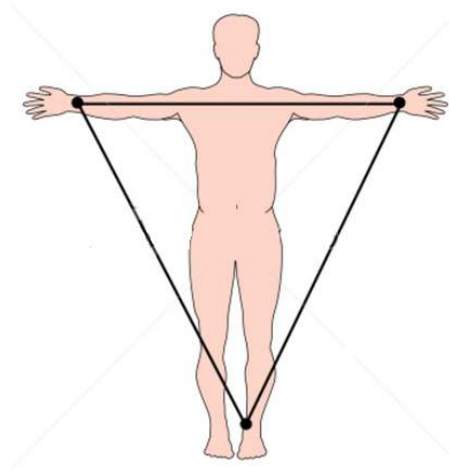
Figure 1.6: Standard 3-electrode position [6]
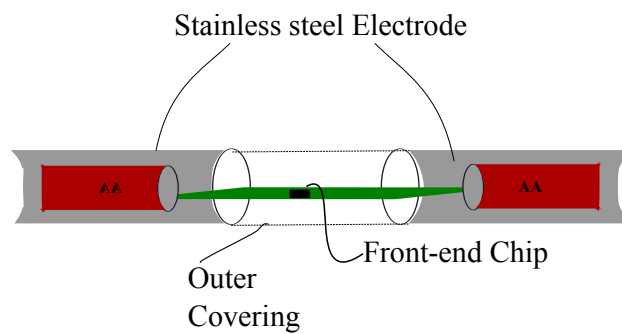
Figure 1.7: Proposed ECG device

contact with the electrode. This, although helps in obtaining a proper reading of the ECG signal, requires trained clinicians to operate it and also increases patient discomfort.

Hence, there is a need for a recording device using 'dry' electrodes which do not require any skin preparation or trained people to operate the device.

Fig. 1.7 shows a rough diagram of the proposed ECG device. The grip-style 'dry' electrodes shown are made of stainless steel. The basic idea is that the user grips the device with both the hands for the ECG signal to be measured. The device would be powered by 3V (2 AA batteries) each of which would be housed below the electrodes. The integrated front-end chip would be in the middle of the device and would be covered. There is no reference electrode in this device and thus would have different response to interference as compared to conventional ECG devices and thus would require a different front-end design.

1.5   Literature study and contribution

A lot of work in literature has been dedicated to designing front-end circuits for ECG devices. Historically, the research work mainly dealt with solving just one problem viz. increasing the CMRR of the instrumentation amplifier. [18], [19], [20] have studied the effects of all possible interferences on an ECG reading and have shown that common-mode interference is the most important of them all. Consequently many techniques and instrumentation amplifiers have been proposed to increase the CMRR of the devices [21], [22], [23], [24]. However, these designs and implementations are for ECG devices in general and no work has been done on the design of hand-held 2-electrode ECG devices specifically.

In this thesis, the effect of all possible interference sources such as power-line noise, baseline wandering, muscle artefacts for the proposed device will be studied. It will be shown that under certain conditions viz. the device is a hand-held portable one, the interference susceptibility of a 2-electrode system is comparable to or might be even superior to that of a traditional ECG device with a reference electrode.

One of the main bottlenecks in the design of an integrated bio-potential read-out front-end, apart from CMRR, is the integration of large time-constants on chip. Implementing a sub-Hz cut-off frequency, to obtain a proper high-pass characteristic, requires time-constants in the order of few seconds. Till now this has been implemented off-chip using resistors and capacitors of a few $M\Omega$s and μFs respectively.

Unfortunately, using such resistors and capacitors is not possible when designing an integrated circuit as it would take up an impractical amount of area. One of the most popular techniques for obtaining a large time-constant is by implementing an extremely high resistance by biasing transistors in sub-threshold region [25], [26]. However, their resistance is unpredictable and non-linear [27].

A new technique called mixed-signal feedback feeds back the digital signal to the previous analog stage. [28], [29], [30] use this concept to implement a sub-Hz cut-off frequency. The advantage of such architecture is that since now the cut-off frequency is implemented in the digital domain, a greater degree of control can be obtained over its value and linearity as opposed to pseudo-resistors.

Unfortunately, the mixed-signal feedback techniques presented by these authors are limited to 8 bits of resolution. In this thesis, a mixed-signal feedback technique using a sigma-delta ADC is proposed to increase the resolution to 10 bits.

This circuit will act as a prototype, since we are interested in the feasibility of using a 2-electrode ECG read-out for various applications. Hence, it would be nice if the technical specifications such as frequency and resolution are programmable. However, this thesis deals with possible solutions to the aforementioned challenges. Introducing programmability is trivial and is not presented in this thesis. Table 1.2 summarizes the

technical specifications which the read-out circuit has to meet.

Table 1.2: System specifications

Parameters	Specification
Input Amplitude	$1\text{m}V_{\text{rms}}$
Bandwidth	1Hz-200Hz
SNR	60dB
Distortion	$\sim$60dB (10 bit accuracy)
Supply Voltage	3V
Power consumption	less than 50μW
Input Impedance	$>$5MΩ
CMRR	greater than 60dB
Process Technology	0.35μm AMIS I3T25 technology

Interference sources

2

The objective of any sensing or readout system is faithful reproduction of the signal to be measured which is ECG signal in our case (henceforth mentioned only as signal). To achieve this objective, it is necessary that the signal is not modified by the read-out circuitry. Any read-out is generally affected by the following

- Source loading : Considerable signal attenuation will take place at the input of the system, if its input impedance is comparable to or smaller than the impedance of the source (body tissues and electrode). Thus it is important to properly characterize the source impedance and account for it in the design.

- Interference and noise sources: Any undesired signal can be termed as noise. The function of the read-out system is to differentiate between the signal of interest and other signals viz. noise and interference. It is important to understand the type and behaviour of all the interference sources so that they can be eliminated by proper design. Usually, in an ECG read-out, the main sources of interference and noise are coupling of the power-line source, baseline wandering, muscle artefact, instrumentation noise and electrode-skin interface offset. The behaviour of noise sources is affected by the impedance of the body and electrodes too, and hence emphasizing the need to characterize it properly.

- Distortion: Any circuit consisting of non-linear devices such as transistors will add distortion to the input signal. To meet the required resolution, it is important that the distortion components be <60dB than the main signal component.

Section 2.1 discusses the modeling of electrode and body impedances. Section 2.2 studies the effect of existing interference sources and it will be seen that power-line interference is a major concern in traditional ECG systems. It is shown in Section 2.3 that for a hand-held two electrode system, power-line interference can be completely neglected. Reduction of distortion is dependent on the design of the read-out circuit. Techniques to reduce it will be discussed in Chapter 4.

2.1   Skin-Electrode Interface

The total source impedance comprises the impedance of body tissues, electrode and the skin-electrode interface. However, the impedance of the skin-electrode interface plays the main role in deciding the total source impedance as the impedance of the metal electrode and that of the body tissues is usually much smaller relatively [31].

The linear relationship between current and voltage as stated by Ohm's law does
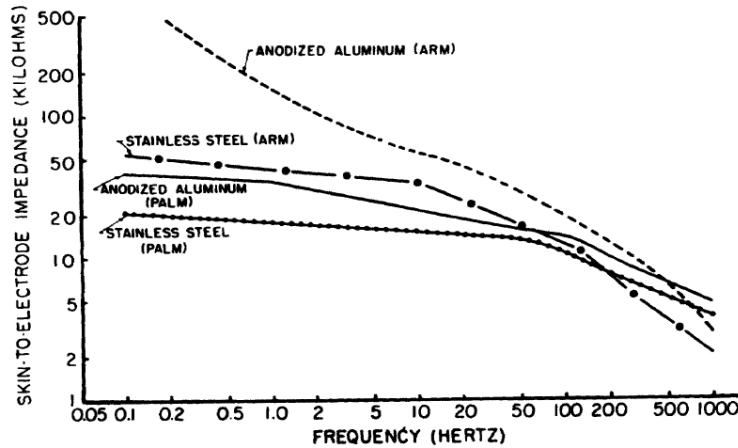
Figure 2.1: Skin-electrode impedance vs frequency for two different materials [7]

not hold true at junctions of different materials such as p-n junctions or electrode-skin interfaces. In the metal electrode, electrons are the carrier of electrical current whereas it is ions in the skin/body tissues. Complex chemical reactions decide the current-voltage relationship at the interface. Due to this, the electrode impedance not only varies with the type of metal used and frequency of the signal, but also with time. A by-product of this chemical reaction is presence of a constant DC offset potential of maximally 300mV at the interface [32].

Fig. 2.1 compares the spectral impedance of the dry electrodes made up of different materials [7]. As can be seen the impedance of the electrode can vary upto 20 times depending on the material of the electrode and frequency of operation. Passage of time also leads to change in impedance of the electrodes due to perspiration as can be seen in Fig. 2.2 [33]. The impedance of stainless steel electrodes was monitored for 20 minutes on 10 subjects. It can be seen in most cases, but cannot be generalized, that the impedance decreases as time increases. This is attributed to the fact that sweat accumulates between the electrode and skin interface which leads to increase in concentration of salts and hence increases the conductivity.

Table 2.1 [33], lists the worst-case and average initial impedances of the skin-electrode interface for stainless steel.

Numerous attempts have been made to model the skin-electrode interface. These can be broadly categorized into two categories -

- By obtaining a complex passive-element model of the interface which accurately characterizes the above impedance curves over our desired frequency range.

- Simplify the above model by using only the worst case impedance value.
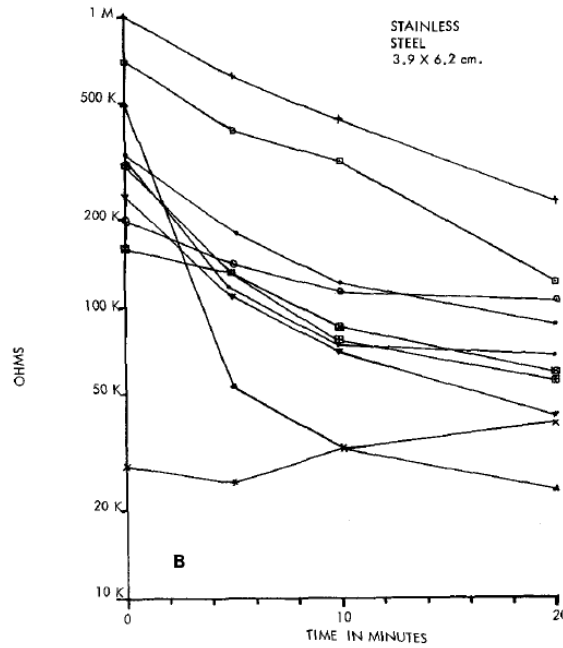
Figure 2.2: Skin-electrode impedance of stainless-steel vs time for 10 subjects

Table 2.1: Impedance values for stainless steel dry electrode

	Impedance ($k\Omega$)
Average Initial Impedance	381
Maximum	1000
Minimum	29
After 20 mins	
Average Impedance	85
Maximum	230
Minimum	27

Fig. 2.3(a) depicts a single time-constant model proposed by [34]. The drawback of this model is that it is valid over very small range of frequencies. A double time-constant model proposed by [35], as shown in Fig. 2.3(b), is more accurate. But, this model is not only quite complex but also the resistance and capacitive values will vary from person to person and thus would be inaccurate.

No single model can completely and accurately model the impedance of the interface [7] and might even be futile in our case. This is evident from Fig. 2.1 and Fig. 2.2. The impedance of stainless steel electrodes is almost an order of magnitude different in both the cases. If we consider only the worst-case impedance for our design,

(a) Single time constant model   (b) Double time constant model
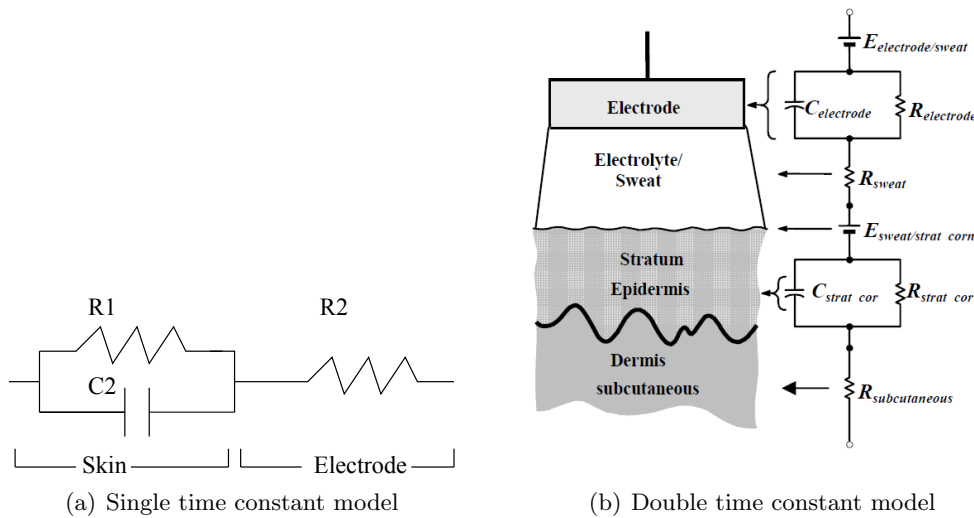
Figure 2.3: Passive models for skin-electrode interface

the only error that it would introduce is that we would be over-designing. This would be a smaller price to pay for than for developing an accurate model. If the input impedance of the system is much greater than the worst-case impedance of interface, the actual impedance value of the interface will not matter and thus can also be modeled as a simple resistor.

For our case, we will also assume that the device will be used for less than one minute and thus the impedance of the interface can be assumed to be constant over this period of time. From Table 2.1, the worst case initial impedance of a stainless-steel dry electrode is 300kΩ. Assuming an input impedance of at least 10 times than the worst-case impedance i.e. an input impedance of $\approx$5MΩ will be needed. This is also in-line with the guidelines published by AHA which requires any ECG device to have an input impedance of at least 2MΩ [36].

2.2 Interference sources

Fig. 2.4 depicts the possible sources of interference and noise that usually affect a conventional ECG read-out [37]. They are discussed below in brief

- Coupling: Power-line noise and electromagnetic interference can be coupled to the device input terminals in three ways [18] viz. capacitive coupling, magnetic coupling and resistive ground coupling.

  Resistive ground coupling refers to coupling of the noise signals in the ground leads caused by ground loops, causing a change in the ground potential. This is not applicable in our case as ours is a 2-electrode device and there is no ground lead present. The other 2 leads will be shielded by the electrodes and hence the coupling of noise signals can be neglected. Moreover, their length would be very
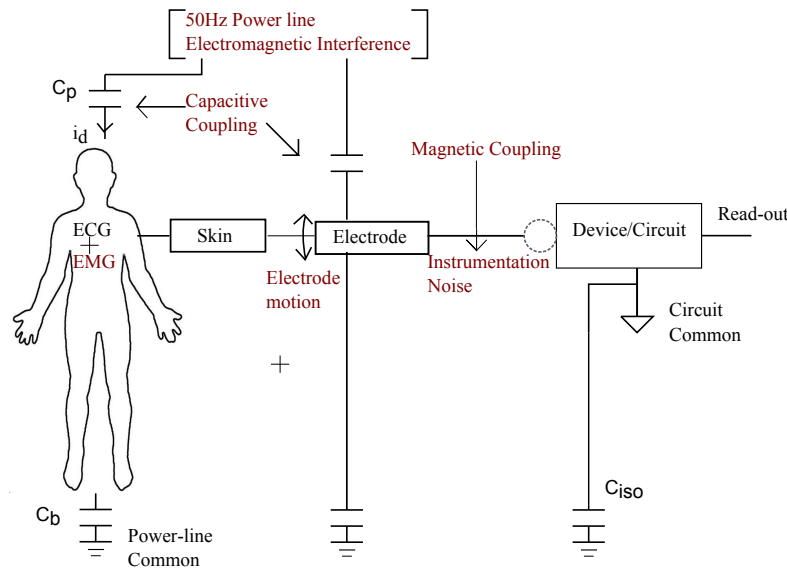
Figure 2.4: Main sources of interference in an ECG read-out

small (most probably they would be implemented as PCB traces) as opposed to long leads in traditional ECG systems. For these reasons, effect of resistive ground coupling can be neglected.

Magnetic coupling refers to mutual coupling caused by current flowing in the electrode leads. The amount of coupling depends on the area covered by this loop and shielding. This effect can also be neglected as, once again, the leads would be small and shielded.

Due to capacitive coupling, power-line noise current flowing through the body is usually around 0.2μA-0.5μA [18], [38]. Other electromagnetic interferences such as tubelight (1kHz), television video signals [18] have known to lead to incorrect signal reproducibility. Capacitive coupling of interferences from the environment into the body increases the common-mode signal amplitude at the input terminals of the device. It will be shown in the next section that for a hand-held device, common-mode current does not flow through the leads and hence does not lead to any common-mode signal. Here too, capacitive coupling of the power-line interference to the leads and the device can be neglected for the same reasons as stated as above.

- Electrode Contact noise and Motion artefact: Motion artefact stems from change in relative position of the heart from the electrodes or in other words, from movement of the electrodes. Since the device is a hand-held one, the user can be in motion. The user may also tighten or loosen his/her grip during the period of the read-out. This causes changes in the skin-electrode interface properties and thus its impedance which leads to sudden changes in the DC offset potential or known as electrode contact noise or baseline wandering. These occur at very low frequency,

usually <0.5Hz and can be filtered out.

- EMG noise: EMG noise results from generation of action potentials from muscles other than that of the heart. Tightening and loosening of muscles leads to generation of EMG. Its amplitude can usually be modeled as a Gaussian distribution curve [39] whose standard deviation is generally 10% of ECG signal amplitude. Although there can be cases where contraction of muscles would lead to transient peak voltage greater than the ECG amplitude. The bandwidth of EMG signals ranges from 30Hz-500Hz [39] which means a significant portion of the EMG energy lies in-band within the ECG signal band. Filtering will not help in this case and we will need to resort to digital techniques such as averaging. Implementation of an EMG digital filter is outside the scope of this thesis.

  Fig. 2.5(a) and Fig. 2.5(b) plot a sample 'noise-less' ECG signal and its frequency spectrum. Fig. 2.6(b) and Fig. 2.6(c) show the effect of baseline wandering and EMG noise separately on the frequency spectrum. The corresponding time-domain 'noisy' ECG signal is shown in Fig. 2.6(a). As can be seen in Fig. 2.6(b), energy of the signal has increased significantly around 0.1Hz frequency range due to baseline wandering. In Fig. 2.6(c), the energy around 30Hz-50Hz has visibly increased due to EMG noise. All the above signals were obtained from the ECG database available at [40].

- Instrumentation noise: Noise due to the read-out circuitry is termed as instrumentation noise. The device needs to be designed such that it can meet the 10-bit resolution requirement.

In summary, 3 main interference sources need to be accounted for in the design viz. common-mode interference due to capacitive coupling, baseline wandering and instrumentation noise. Baseline wandering can be filtered out by high-pass filtering. The design of the high-pass filter will be discussed in Chapter 3. Design for low instrumentation noise will be discussed in Chapter 4. Response of a 2-electrode system to common-mode noise due to capacitive coupling is discussed in more detail in the next section. Effect of rest of the interference sources can be neglected.

2.3   Capacitively-coupled common-mode interference

Fig. 2.4 shows coupling capacitances of the human body to power-line source (C_p) and power-line common (C_b). The power-line common is usually referred to as earth ground in literature. In this thesis too, it has been referred to as earth ground. i_d is the current that is capacitively coupled to the body through the power-line source. It is called the displacement current. For our analysis, only capacitive coupling due to power-line source will be considered as it lies within the band of interest. However, the analysis will hold true for any electromagnetic interference and the results derived can be applied to any capacitively coupled interference.

Evaluating the value of C_p and C_b is not trivial as it depends on a variety of
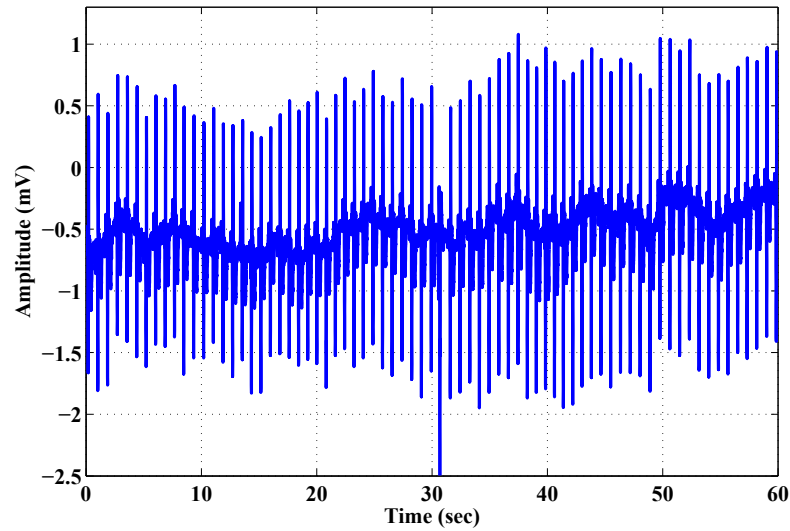
(a) Sample ECG signal without noise
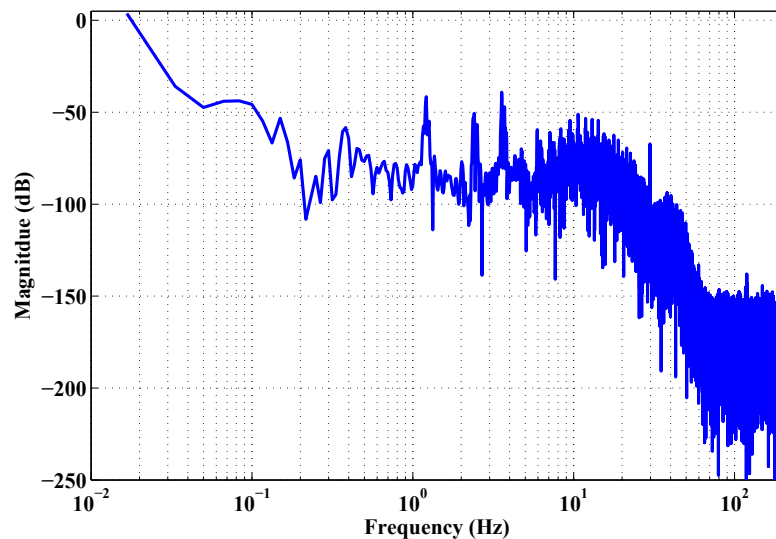
(b) Frequency spectrum

Figure 2.5: Sample ECG signal and its frequency Spectrum

factors such as environment and surroundings, skin properties, distance from power-line source or metallic objects.

Table 2.2 [38] lists the nominal and worst-case values of coupling capacitances and surroundings in which can they be encountered. The corresponding values of the displacement current have been specified in the last column. The experiments carried out by the author is by no means exhaustive. However, the results provide a good
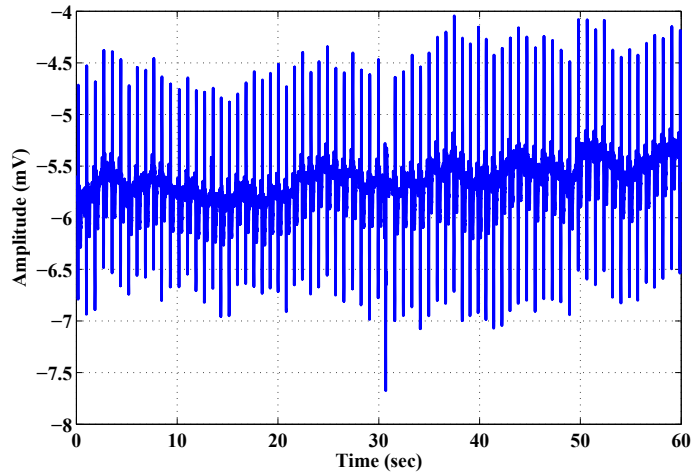
(a) ECG signal with baseline wandering and muscle arterfact
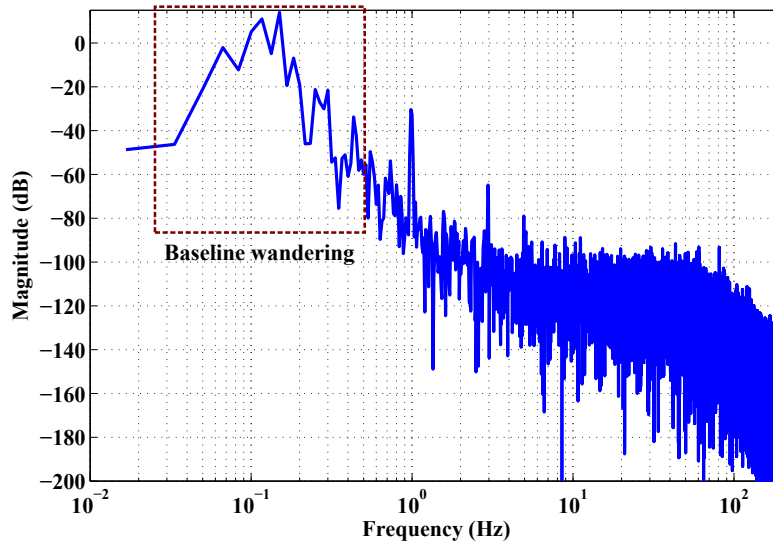
(b) Baseline wandering frequency spectrum
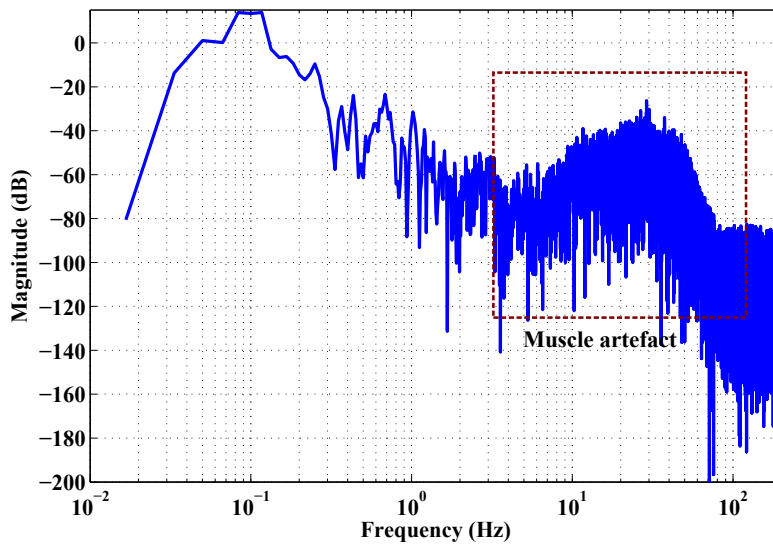
(c) Muscle arterfact frequency spectrum

Figure 2.6: Effect of Baseline wandering and muscle artefact on ECG signal

insight into the nominal coupling capacitance values that one can expect.

Fig. 2.7(a) depicts an interference model of a 2-electrode hand-held battery oper-

Table 2.2: Measured values of coupling capacitances in various locations

Location	C_{p} (pF)	C_{b} (pF)	i_{d} (nA)
Living room(near metallic lamp)	2.2	1000	424
Kitchen	1.2	735	229
Bathroom	1	3905	198
Library	0.7	111	127
Far from plugged oscilloscope	2	225	565
Touching power cord	14	260	2715
Nominal values	**2**	**500**	**200**

ated system as presented by [18], [19], [20]. Z_{d} is the differential input impedance of the device and Z_{c1} and Z_{c2} are the impedances between the input terminals of the device and the circuit common. Z_{e1} and Z_{e2} are the impedances of the skin-electrode interface.

C_{iso}, again, varies from the type of design of the device, its size and the surroundings. Coupling to the electrode leads is neglected once again.

Z_{body} in Fig. 2.7(a) can be neglected by assuming that i_{d} is equally distributed across the body and therefore the whole body is at the same potential [19], [18]. It is not possible to estimate the value of i_{d} at each point on the body as, like coupling capacitances, it too would be a function of the environment, surrounding, orientation, skin impedance and time duration. There have been no reported cases in literature wherein this assumption is proven to be false. The impact that the failure of this assumption will have on our design is discussed briefly in the last part of this section.

Fig. 2.7(b) shows the equivalent impedance diagram for calculating the common-mode voltage at the input terminals of the device. In this figure both the electrodes and common-mode impedance of both the terminals have been assumed to be equal. That is, the following assumptions have been made

$$Z_{\mathrm{e1}} = Z_{\mathrm{e2}} = Z_{\mathrm{e}}$$
$$Z_{\mathrm{c1}} = Z_{\mathrm{c2}} = Z_{\mathrm{c}}$$
$$Z_{\mathrm{eq}} = \frac{Z_{\mathrm{e}} + Z_{\mathrm{c}}}{2}$$
$$Z_{\mathrm{iso}} = \frac{1}{s \cdot C_{\mathrm{iso}}}$$
$$Z_{\mathrm{b}} = \frac{1}{s \cdot C_{\mathrm{b}}}$$
$$Z_{\mathrm{p}} = \frac{1}{s \cdot C_{\mathrm{p}}}$$
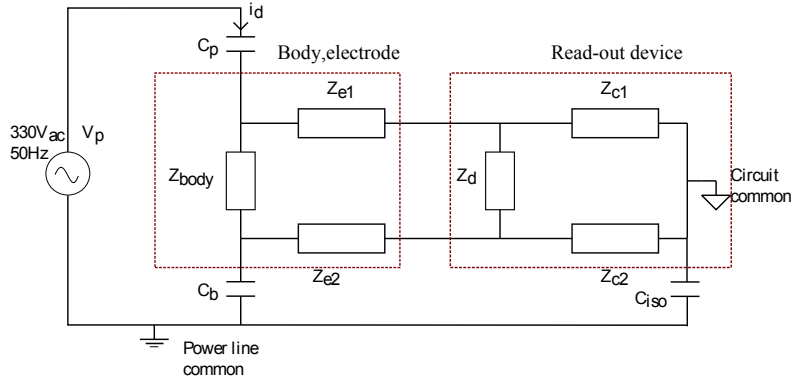
(a) 2-electrode power line interference model
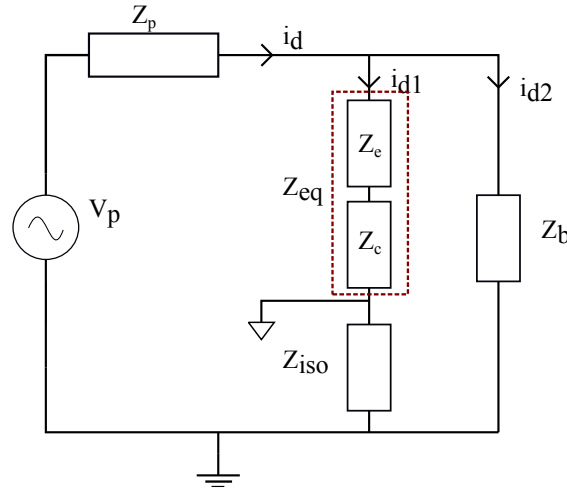
(b) Equivalent impedance for calculating common-mode voltage

Figure 2.7: 2-electrode power-line interference model and its equivalent circuit

Refering to Fig. 2.7(a), the differential input impedance of the device, Z_{idiff}, and the common-mode input impedance of the device, Z_{icm} are given by

$$Z_{\mathrm{idiff}} = Z_{\mathrm{d}} // 2Z_{\mathrm{c}} \tag{2.1}$$

$$Z_{\mathrm{icm}} = Z_{\mathrm{iso}} + \frac{Z_{\mathrm{c}}}{2} \tag{2.2}$$

To avoid source-loading,

$$Z_{\mathrm{idiff}} >> Z_{\mathrm{e}} \tag{2.3}$$

$$Z_{\mathrm{d}}, Z_{\mathrm{c}} >= 5\mathrm{M}\Omega \tag{2.4}$$

Z_{idiff} is taken to be at least 10 times greater than the worst-case electrode impedance that can be expected. From Fig. 2.7(b), the common-mode voltage due to power-line interference, V_{cm}, is

$$V_{\mathrm{cm}} \approx \frac{1}{2} \cdot \frac{Z_{\mathrm{c}}}{Z_{\mathrm{eq}}} \cdot \frac{Z_{\mathrm{eq}}}{Z_{\mathrm{eq}} + Z_{\mathrm{iso}}} \cdot \frac{Z_{\mathrm{b}}}{Z_{\mathrm{p}} + Z_{\mathrm{b}}} \cdot V_{\mathrm{p}}$$

$$V_{\text{cm}} \approx \frac{1}{500} \frac{Z_{\text{c}}}{Z_{\text{eq}} + Z_{\text{iso}}} \qquad (2.5)$$

The term $\frac{1}{500}$ is obtained by substituting nominal values of Z_{p} and Z_{b} from Table 2.2. In the case of a hand-held device and especially in the case wherein the circuit would be an integrated chip (as opposed to a PCB implementation), the coupling of the circuit common to the earth ground will be much smaller than that of the human body and it can be assumed $C_{\text{iso}} \approx 0$ and therefore $V_{\text{cm}} = 0$.

This can also be understood from (2.2) wherein infinite Z_{iso} will lead to infinite common-mode impedance and thus no common-mode signal transfer will take place. This result can be compared to the tail current impedance required for a differential amplifier stage. Infinite impedance of the tail current source would lead to infinite CMRR.

(2.5) shows that irrespective of the value of coupling capacitances, C_{p} and C_{b}, V_{cm} will always be 0 as long as $Z_{\text{iso}} >> Z_{\text{eq}}$. Mismatch between electrode impedances, common-mode impedances of the input terminals of the device will also not matter as long as C_{iso} is 0.

A brief quantitative calculation is carried out to determine the value of C_{iso} that can be tolerated for a 10-bit resolution. To obtain the specified resolution, V_{cm} should be <60dB than the differential signal. For a $1mV_{\text{rms}}$ input signal, $V_{\text{cm}} < 1\mu V_{\text{rms}}$. By substituting these values in (2.5), we get that $C_{\text{iso}} <\approx 1$fF. Given that the nominal coupling capacitance of the human body is 500pF (Table 2.2), we can safely assume that the coupling capacitance of a shielded IC would easily meet this criterion.

To understand why CMRR of the instrumentation amplifier needs to be high for traditional ECG systems, the CMRR of the system can be written as

$$\text{CMRR} = \frac{Z_{\text{eq}} + Z_{\text{iso}}}{500 \cdot Z_{\text{c}}} \qquad (2.6)$$

It is assumed here that Z_{idiff} is much greater than the source impedance. To increase the CMRR, one has to either increase Z_{iso} or decrease Z_{c}. Decreasing Z_{c} will also decrease Z_{idiff}, which is undesirable and increasing Z_{iso} is also a challenge as ECG equipments have been quite large. Hence a third electrode is used as a reference electrode to increase the CMRR. By using the third electrode, CMRR and Z_{idiff} both do not depend on Z_{c} and the two parameters are essentially decoupled. The CMRR of such systems is then limited by the mismatch between the electrodes.

The only way the common-mode noise will be able to affect our device considerably is if the assumption that the displacement current, i_{d}, is symmetric in nature is not valid i.e. different parts of the body have different coupling capacitances. In this case, the common-mode current would flow through the body impedance and manifest itself as a differential voltage. Since this current is at 50Hz frequency, it will be indistinguishable from the signal of interest. A notch filter at 50Hz would be needed

to reject it completely, which is better implemented in the digital domain. Thus for designing, we will assume that the coupling capacitances are symmetric and therefore the displacement current in the body too, which will be the case in the majority of scenarios. If it fails for certain cases, a digital notch filter can later be added.

System-Level Design

<div style="text-align: right; font-size: 3em;">**3**</div>

Two possible scenarios for the design of the front-end architecture are depicted in Fig. 3.1 and Fig. 3.2. In Fig. 3.1 the signal conditioning is carried out fully in the analog domain whereas in Fig. 3.2 it is carried out completely in the digital domain. The instrumentation
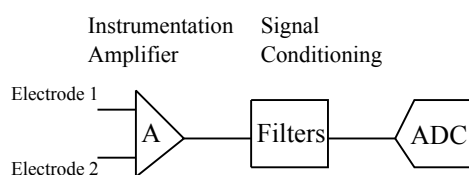
Figure 3.1: Analog Implementation of front-end of readout
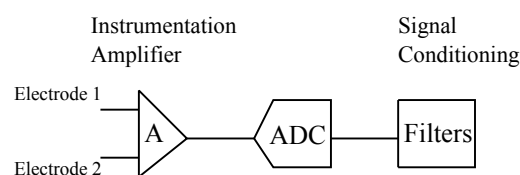
Figure 3.2: Digital Implementation of front-end of readout

amplifier is the first block in both the cases as it performs two important functions viz

- Provide a sufficiently high input impedance

- Provide a sufficiently high CMRR

To compare both approaches, Table 3.1 compares the ADCs required in each of the cases in terms of resolution, power, area and cost as ADCs are generally the most power-consuming block in a signal chain.

As only one set of input is needed, as opposed to an array of inputs, area is not a concern for this application. Hence an analog implementation is chosen. Fig 3.3 depicts a standard signal chain of a full analog implementation of a read-out circuit. The main challenge in such an implementation is obtaining the required frequency transfer.

Time-constant, τ of a cut-off frequency in general, is given by

$$\tau = \frac{2 \cdot \pi}{f_{\mathrm{c}}} = R \cdot C \tag{3.1}$$

where f_{c} = cut-off frequency and R, C are the resistance and capacitance respectively. The high-pass cut-off frequency is much lower than the low-pass one and therefore much more challenging to design for. In this chapter, implementation of the high-pass cut-off frequency will be considered. Implementation of the low-pass cut-off frequency will be discussed in the next chapter.

On-chip capacitors are generally less than few tens of pFs due to area consider- ations. To obtain the required time-constant of 6.28s (Table 1.2) corresponding

Table 3.1: Fully Analog Implementation vs Fully Digital Implementation

	Full-analog implementation	**Full-digital Implementation**
Resolution Required	Assuming that to achieve a 60dB SNR, dynamic range of 10-bits would be required and thus a 12-bit ADC is required taking into account practical implementation issues	Since the input signal to the ADC comes directly from the instrumentation amplifier, the 300mV DC offset would also be present. Thus a resolution $\approx$22-bits will be required to achieve a target SNR of 60dB.
Power consumed	Few tens of microwatts	Much greater than its analog counterpart
Area	Large because huge capacitors and resistors would be required to obtain the required bandwidth at such low frequencies	Much smaller as compared to a full-analog implementation
Advantages	Lower power	Lower area as less number of components and thus may lead to lower costs if used for array read-out applications
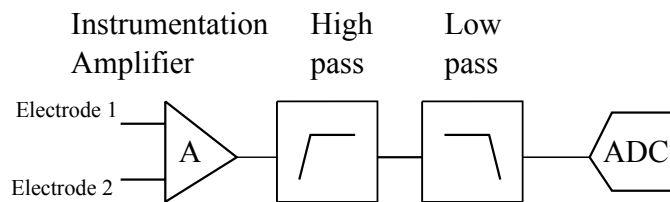
Figure 3.3: Conventional analog front-end signal flow

resistances will have to be of the order of TΩs. Analog techniques for obtaining such high-valued resistances on-chip are discussed in Section 3.1. It is shown that it is not possible to obtain 10-bit linear frequency transfer within the targeted power budget with these techniques. Section 3.2 proposes a novel mixed-signal feedback technique for achieving the required frequency transfer.

3.1 Analog techniques for implementing high-valued resistances

Table 3.2 lists a few methods of fabricating high resistances available in I3T25 technology [41]. Even with high polysilicon resistor, a resistance of 30TΩ will take up an area of 0.12m^2 (minimum width of resistor allowed is $2\mu\text{m}$). Thus, there is a need to look into other methods possible to obtain the same.

Table 3.2: Sheet resistance of a few polysilicon resistors in I3T25 technology

Resistor Model Name	Sheet resistance (Ω/sq)
HIPOR	975
LOPOR	2.4
NPOR	292
PPOR	240

Fig. 3.4 shows a T-network of resistors to implement a low transconductance, Z_{eq}^{-1} using small resistors, Z_1 and Z_{x}. The equivalent resistance across V_1 and V_2 is given by

$$Z_{\text{eq}} = 2 \cdot Z_1 + \frac{Z_1^2}{Z_{\text{x}}} \tag{3.2}$$

$$f_{\text{hpf,tnetwork}} = \frac{1}{2 \cdot \pi \cdot Z_{\text{eq}} \cdot C_1} \tag{3.3}$$

To obtain $Z_{\text{eq}} = 30\text{T}\Omega$, choosing $Z_1 = 10\text{M}\Omega$ and $Z_{\text{x}} = 3\Omega$. It can be shown mathematically that the open-loop gain of the amplifier, A, would have to be $> \frac{Z_1}{Z_{\text{x}}}$. Although this is obtainable through use of techniques such as cascoding and gain-boosting, it will consume a lot of power. Moreover, the more the number of resistors in feedback, the greater would be the input-referred noise.

The switched capacitor technique is also often used for obtaining large on-chip resistances [42]. The cut-off frequency of switched-capacitor implementation is given by

$$f_{\text{hpf,sc}} = \frac{C_2}{2 \cdot \pi \cdot C_1 \cdot f_{\text{clk}}} \tag{3.4}$$

where f_{clk} is the frequency at which C_2 is switched. For $f_{\text{hpf,sc}} < 1\text{Hz}$, either the capacitor ratios have to be large or f_{clk} clock has to be very low. Moreover, an anti-alias filter is also be required which will lead to a higher power consumption. Hence this technique, too, is unsuitable for this application.

The cut-off frequency can also be implemented actively. Using a g_{m}-C stage is one such option. The cut-off frequency is then given by

$$f_{\text{hpf,gm}} = \frac{g_{\text{m}}}{2 \cdot \pi \cdot C_1} \tag{3.5}$$
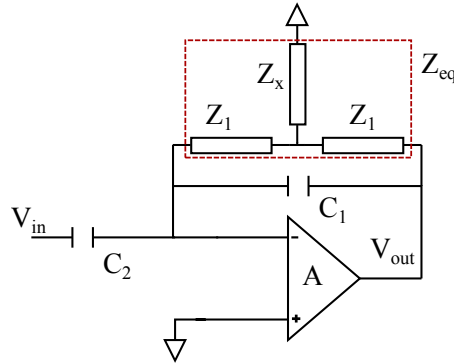
Figure 3.4: T-network impedance scaler

Considering a $C_1 = 10\text{pF}$, g_m required to obtain a $f_\text{hpf,gm} < 1\text{Hz}$ will be $<100\text{pS}$, which is unfeasible.

Large resistance is implemented by biasing mosfets in the linear regime in [42]. This method limits the value of achievable resistances to the order of few hundred MΩs to GΩs. Mosfets biased in the cut-off region are used by [25], [26]. They have termed such devices pseudo-resistors. Since the transistor is in cut-off region, the resistance offered can even exceed TΩs.

Fig. 3.5 shows an implementation of a simple pseudo-resistor. Two source-connected NMOSTs are placed in series. Although theoretically, one NMOS would be sufficient, two are connected for the sake of symmetry, so that the resistance seen during the positive and the negative half of the signal is the same. To analyse the working of a pseudo-resistor, it can be imagined as a mos-bipolar pair in series, as shown in Fig. 3.6. In the negative half of the signal, each device functions as diode connected PMOS transistor. In the positive half of the signal, the parasitic source-well-drain p-n-p bipolar junction transistor (BJT) is activated, and the device acts as a diode-connected BJT.
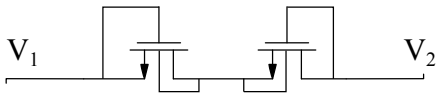
Figure 3.5: Analog Implementation of front-end of readout
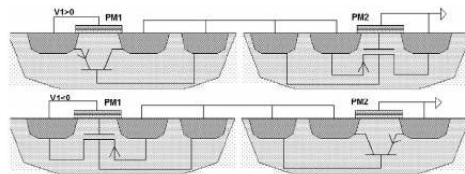
Figure 3.6: MOS-BIPOLAR view of a pseudo-resistor

Since, the gates of the transistors are connected to the sources, there is no bias current that flows through the pseudo-resistors and hence, not only the power consumed by them would be negligible but also their noise contribution.
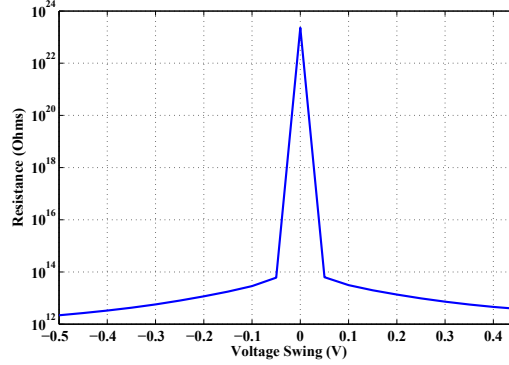
Figure 3.7: Incremental resistance vs voltage swing across pseudo-resistor
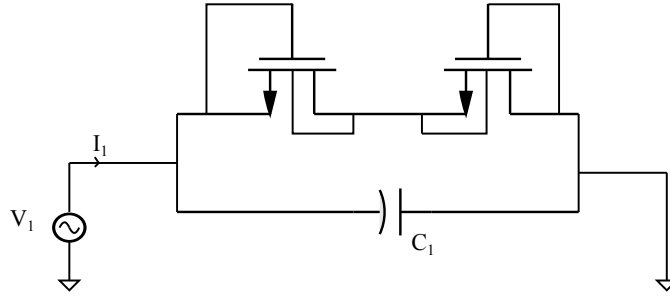
Figure 3.8: RC circuit using pseudo-resistor

The current across the source and drain of a mosfet biased in the sub-threshold region is [43]

$$I_{\text{pseudo}} \approx I_{\text{s}} \cdot e^{\frac{V_{\text{gs}} - V_{\text{t0}}}{U_{\text{t}}}} \cdot \left(1 - e^{-\frac{V_{\text{ds}}}{U_{\text{t}}}}\right) \tag{3.6}$$

where I_{s} is the scaling current, V_{t0} is the threshold voltage and U_{t} is the thermal voltage. For small V_{gs} i.e. $V_{\text{gs}} < 100\text{mV}$ and $V_{\text{ds}} > 2 \cdot U_{\text{t}}$, the resistance across the pseudo-resistor will be very high. This can also be seen in Fig. 3.7. It shows a plot of the resistance w.r.t voltage swing. When the voltage swing is less than 10mV, the resistance peaks to much greater than TΩs. Since the resistance depends exponentially on the voltage swing across the source and the drain, the cut-off frequency will keep on shifting according to the voltage swing. This behaviour manifests itself as dynamic distortion near the cut-off frequency.

To analyse the amount of distortion due to the pseudo-resistor, a simple RC circuit as shown in Fig. 3.8 is designed. The value of the capacitor, C_1 is chosen to be 100fF and the pseudo-resistor is sized such that the cut-off frequency ($f_{\text{hpf,pseudo}}$) is around 50mHz.

Fig. 3.9 plots the normalized magnitude of the current, I_1, for a voltage swing of 100mV and an input frequency of 50mHz. The distortion component is 40dB lower than that of the main signal component and hence it is not 10-bit linear. Fig. 3.10 plots the PSD of the current, I_1, for a voltage swing of 100mV and an input frequency of 1Hz.
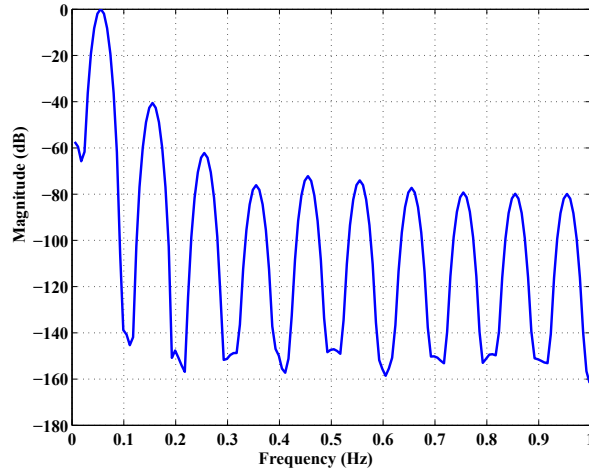
Figure 3.9: Distortion due to pseudo-resistor for 50mHz, 100mV signal swing, for $f_{\text{hpf,pseudo}}$= 50mHz
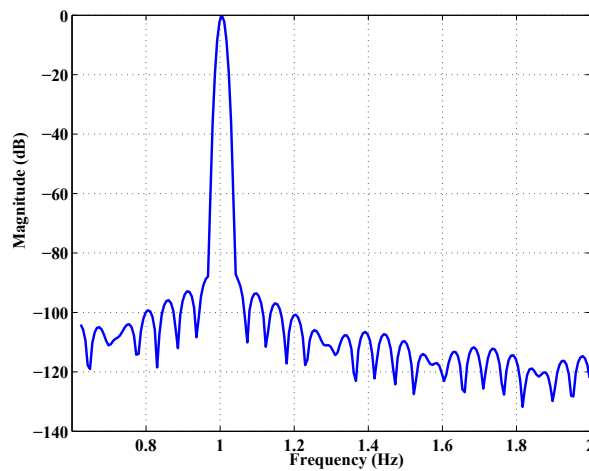
Figure 3.10: Distortion due to pseudo-resistor for 1Hz, 100mV signal swing for $f_{\text{hpf,pseudo}}$=50mHz

At frequencies higher than the cut-off frequency, the amount of distortion will mainly be decided by the capacitor, C_1 and hence will not be a bottleneck.

One can reduce distortion by reducing the voltage swing across the pseudo-resistor. However, this is undesirable as then the noise from the stages following the instrumentation amplifier will affect the SNR. It is possible to reduce the distortion by other methods.[44] biases pseudo-resistors using currents instead of voltages. [26] uses pseudo-resistors which are cross-coupled to each other to increase the symmetry and thus increase the 'flat region' in the resistance-voltage plot. However, even with these techniques, the resistance obtained by using pseudo-resistors is dependent on I_{s} and

exponentially dependent on V_{ds} and is thus still inaccurate and non-linear.

3.2 Mixed-Signal Feedback

3.2.1 Theory

Fig. 3.11 shows a generalized block diagram of mixed-signal feedback technique. It utilizes the fact that in general, the objective of any front-end is to convert the physiological signal to a digital one. Filtering can in principle be done in either the digital or the analog domain and would depend on the power budget and the DAC resolution.

This technique has been used by [28], [29] to reject DC-offsets, however with different ADCs. An 8-bit counting ADC and a 7-bit DAC and a digital IIR filter in the feedback is implemented in [28]. In this case, the linearity at the cut-off frequency will be limited by the DAC. A 12-bit incremental sigma-delta ADC, 1-bit DAC and an analog charge-pump filter has been implemented in [29]. Once again, here, the linearity near the cut-off frequency is limited by the fact that a 12-bit signal is converted to a 1-bit signal for feedback.

In this thesis, a sigma-delta ADC has been chosen. SAR ADC is generally the most widely used architecture for biomedical applications due to their low power consumption. Table 3.3 compares a sigma-delta ADC to a SAR ADC. The main advantage that the sigma-delta ADC has is that of implementing the feedback with 10-bit linearity using just a 1-bit DAC. This will be discussed in greater detail later in this section. It is first imperative to understand the basic functioning of a sigma-delta architecture.

Fig. 3.12 depicts a basic block diagram of a first-order sigma-delta architecture. It comprises an integrator, a 1-bit quantizer and a 1-bit DAC. The order denotes the number of integrators in the loop.

Since it is a non-linear system (due to the comparator) and a dynamic one (due to the memory of the integrator), the mathematical analysis of the functioning of the loop is a non-trivial one [45]. To gain a qualitative analysis into the working of the sigma-delta, the comparator can be linearized by assuming that the quantization noise
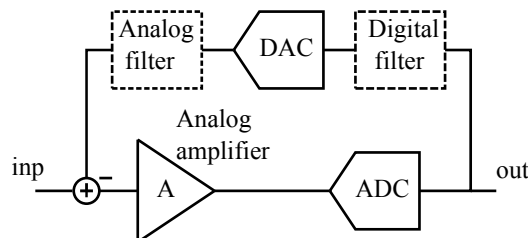
Figure 3.11: Generalized block diagram of the mixed-signal feedback technique

Table 3.3: Summary of choice of ADC

Name	Advantages	Disadvantages
SAR	Extremely low power, good linearity at low resolution	Matching issues in capacitors, area large
Sigma-delta	Extremely high resolution using simple analog structures, low area, no strict requirement on anti- alias filter, configurable resolution	Sampling frequency and power consumption higher
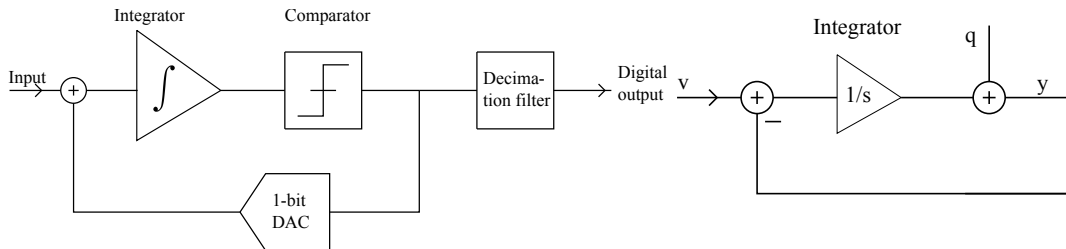
Figure 3.12: Block Diagram of First order Sigma-Delta Modulator

Figure 3.13: Linearized model of Sigma-Delta Modulator

is random. Also since the DAC is a 1-bit one, it is inherently linear. The corresponding s-domain equivalent model is shown in Fig. 3.13. The output of the comparator can be written as

$$v(s) \cdot \frac{1}{s+1} + q(s) \cdot \frac{s}{s+1} = y(s).$$ (3.7)

where v is the analog input signal, q is the quantization noise and y is the output of the sigma-delta modulator. It can be inferred from (3.7) that the input signal is transferred as is and the quantization noise is high-pass filtered. This can also be seen in Fig. 3.14, Fig. 3.15. The signal transfer function (STF) and the noise transfer function (NTF) have been simulated in MATLAB and plotted respectively. The final digital signal can be obtained by passing it through a digital filter to complete the analog-to-digital conversion.

The relation between the required signal-to-quantization noise ratio (SQNR) and oversampling ratio (OSR) for a first-order sigma delta modulator is given by [45]

$$SQNR = \frac{9 \cdot M^2 \cdot OSR^3}{2 \cdot \pi^2}$$ (3.8)

where M is the amplitude of the input sine wave. From (3.8), to achieve a 12-bit resolution, sampling frequency of 256kHz will be required for a corresponding Nyquist
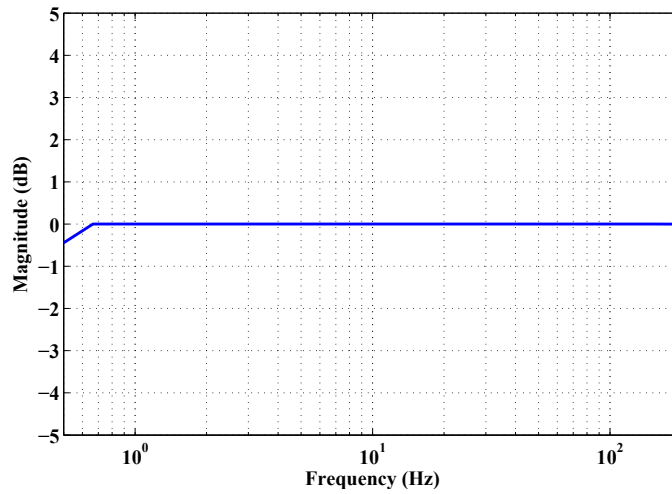
Figure 3.14: Signal Transfer Function of a conventional Sigma Delta Modulator
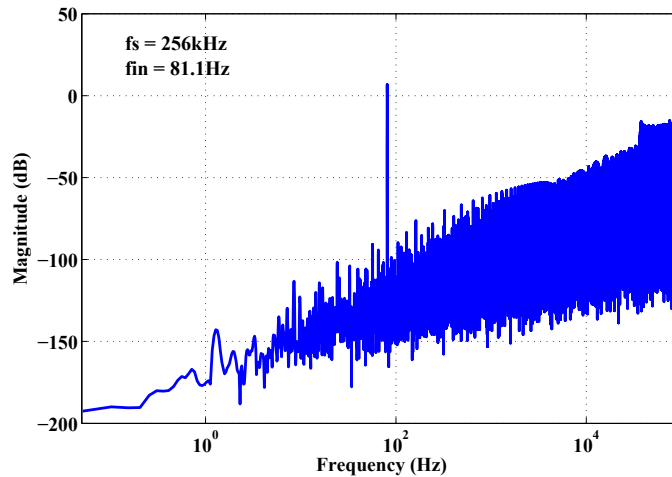
Figure 3.15: Noise Transfer Function of a conventional Sigma Delta Modulator

frequency of 500Hz. A nyquist frequency of 500Hz is chosen as the maximum frequency of our input signal is 200Hz.

Although the loop analysis was done in the s-domain, it could also have been done in the z-domain i.e. assuming a switched-capacitor integrator. Table 3.4 compares the continuous-time implementation of the loop filter to the discrete-time implementation of the sigma-delta architecture.

If a discrete-time implementation is chosen, apart from requiring a separate sample-and-hold circuit, the switched-capacitor integrator would need unity-gain bandwidth of approximately 4-5 times greater than the sampling frequency for it to settle properly i.e. around 2MHz. To meet this requirement, the opamp would need to consume a lot

Table 3.4: Comparison between continuous-time and discrete-time implementation of loop filter

Continuous-time loop filter	Discrete-time loop filter
Does not need a separate anti-alias filter and a sample and hold circuit as sampling is carried out by the comparator and thus high-pass filtered because of the loop	Needs a separate anti-alias filter and a sample and hold circuit as sampling needs to be done before implementation of the sigma-delta loop
Generally consumes less power	Consumes more power as stringent requirements on opamp settling require high unity-gain bandwidth
Not very accurate as time-constant depends on value of resistors and capacitors	Much more accurate as time-constant depends on ratios of capacitors
Prone to jitter	Relatively immune to clock jitter as the charge error on one capacitor in one cycle due to jitter would be compensated in the next cycle.

of power as compared to a g_m-C filter topology for a continuous time implementation. Moreover, in continuous time implementation, clock jitter will not be a bottleneck in achieving the resolution as the clock frequency is only 256kHz.

To obtain a high-pass characteristic for the input signal, one would need to add an integrator in the feedback loop. Consider the block diagram in Fig. 3.16 and its corresponding s-domain equivalent model in Fig. 3.17.

The s-domain equations for this block diagram are given by

$$v(s) \cdot \frac{s}{s^2 + s + a} + q(s) \cdot \frac{s^2}{s^2 + s + a} = y(s) \tag{3.9}$$

The STF has a zero at DC and two poles at

$$s = \frac{-1 \pm \sqrt{1 - 4a}}{2} \tag{3.10}$$

If a is very small, one pole will be near DC and one will be near the sampling frequency. The pole near DC will determine the high-pass cut-off frequency, f_hpf, as f_hpf is much smaller than the sampling frequency, f_s. Thus,

$$s = \frac{2 \cdot \pi \cdot f_\mathrm{hpf}}{f_\mathrm{s}} = -a \tag{3.11}$$
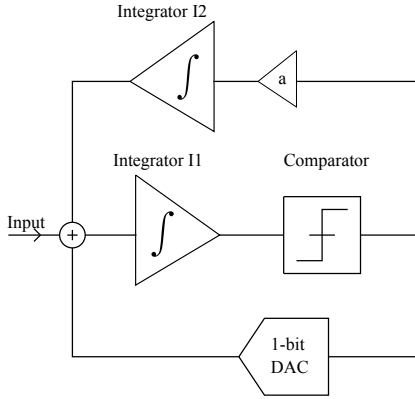
Figure 3.16: Sigma Delta ADC with second feedback loop
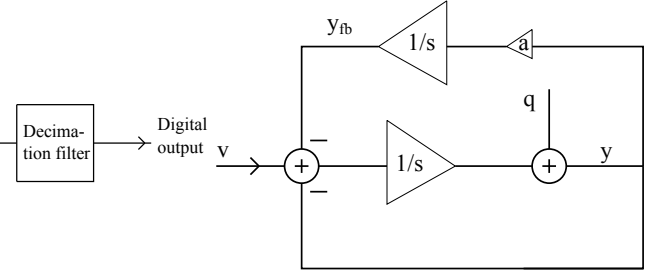
Figure 3.17: s-domain equivalent block diagram

By changing the scaling co-efficient, a, one can achieve the desired f_{hpf}.

The NTF, according to Eqn 3.9 would have a double zero at DC and a pole at $s = -a$ i.e. the quantization noise, q will be suppressed by 40dB/dec until f_{hpf}, after which, it will be suppressed by 20dB/dec. This can be seen in Fig. 3.19. This plot has been simulated with a sampling frequency of 256kHz and the value of a has been chosen such that $f_{\text{hpf}} = 20$Hz. Fig. 3.18 is a plot of the signal transfer function of the proposed block diagram. Both these plots have been obtained by simulating the above block diagram in MATLAB.

3.2.2 Small signal stability analysis

Since the sigma-delta architecture has a non-linear component, the comparator, conventional 'Bounded Input, Bounded Output' (BIBO) stability analysis cannot be applied here. Although there is no known fool-proof method for its stability analysis, a useful model for studying the small-signal stability is depicted in Fig. 3.20 [46].

The comparator is modeled as a block with a gain, k, and the DAC as a zero-order hold block. The laplace transform of a zero-order response is given by

$$\text{Zero-order hold response} = \mathcal{L}(u(t) - u(t - T)) \Leftrightarrow \frac{1 - e^{-\text{sT}}}{s} \tag{3.12}$$

where T = sampling time period. Equating the characteristic of the transfer function, $\frac{y(s)}{v(s)}$ to 0

$$s^2 + k \cdot \frac{1 - e^{-\text{sT}}}{s} \cdot (s + a) = 0 \tag{3.13}$$

This cannot be solved analytically as it is a non-linear equation. However, we can make an assumption. Since the frequency band of interest is much smaller than the
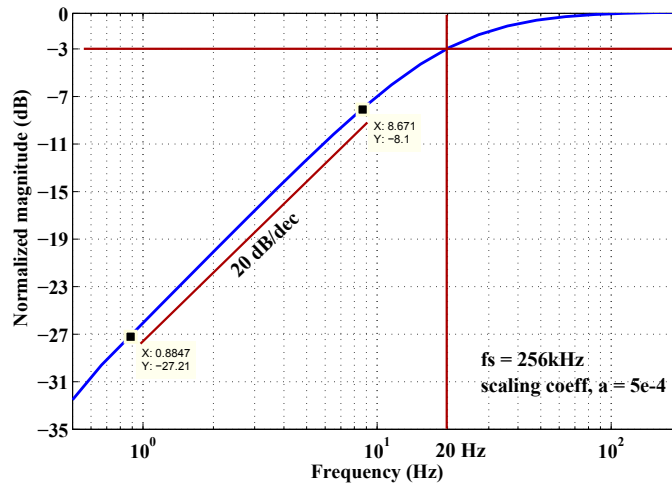
Figure 3.18: Signal Transfer Function for the proposed block diagram at $f_s = 256$kHz
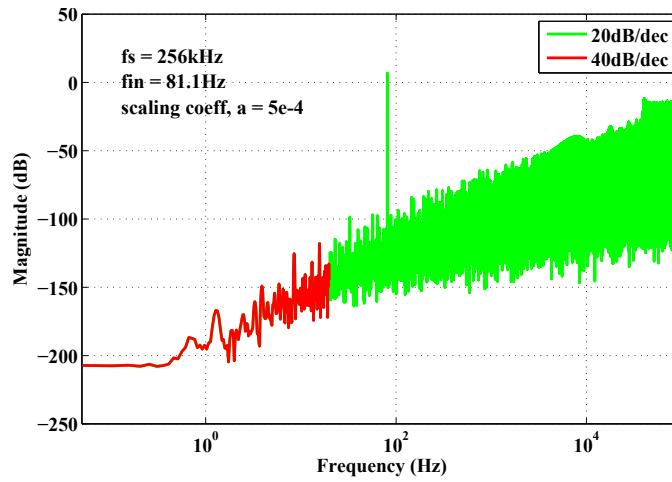
Figure 3.19: Noise Transfer Function for the proposed block diagram at $f_s = 256$kHz
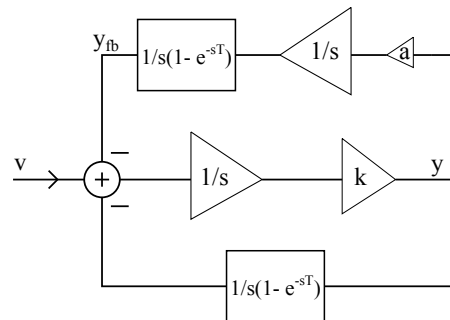
Figure 3.20: Model for analysing the stability of the sigma-delta loop
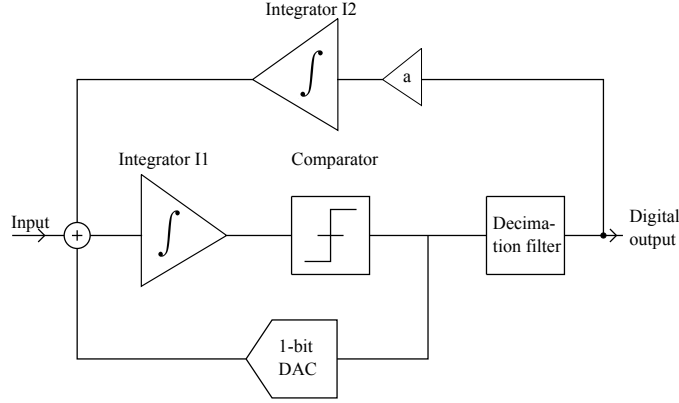
Figure 3.21: Alternative architecture wherein the feedback is taken after the decimation filter

sampling frequency, the exponential term can then be reduced to a linear one by Taylor approximation,

$$s^2 + k \cdot \frac{1 - (1 - sT)}{s} \cdot (s + a) = 0$$
$$s^2 + k \cdot T \cdot (s + a) = 0 \tag{3.14}$$

Since, there are only two poles in the characteristic equation, they will always stay in the left-half of the s-plane as k is varied from 0 to inf. Thus the modulator is stable for all values of the input to the comparator.

3.2.3 Comparison with alternative architectures

Fig. 3.21 and Fig. 3.22 show an alternative architecture wherein the feedback is taken after the digital decimation filter and its equivalent model respectively. This is similar to the structure proposed by [28] (although the ADC is different). Since we are interested in very low-frequency operation, the decimation filter is modeled as a unity-gain stage. q_1 represents the noise added while filtering the modulator output. The output of the comparator, y, is now given by

$$y(s) = v \cdot \frac{s}{s^2 + s + a} + q \cdot \frac{s^2}{s^2 + s + a} - q1 \cdot \frac{a}{s^2 + s + a}. \tag{3.15}$$

Comparing (3.9) and (3.15) shows that both the architectures are mathematically equivalent if the filtering is ideal and no noise is added by the decimation filter. However, the DAC in the feedback is no longer a single-bit one and therefore its non-linearity would also appear at the input along with that of I2. This limits the achievable resolution. Moreover, since the DAC D2 would now be a multi-bit one, it will also consume more power.

Fig. 3.23 and Fig. 3.24 plot the results if the resolution of the DAC D2 is lower than that of the ADC. In both these cases a sinc2 decimation filter and an ideal DAC has been used. A lower resolution DAC can be modeled as adding quantization noise to
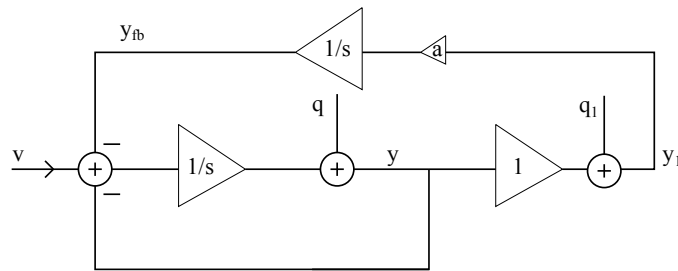
Figure 3.22: Equivalent s-domain model

the output of the decimation filter and thus can be incorporated in q_1 in (3.15). Since the characteristic equation of the signal frequency, v, and q_1 is the same, q_1 would be low-pass filtered with bandwidth given by (3.11). Thus the lower the resolution of the DAC D2, the greater the q_1 and hence lower the achievable resolution. The effect of q_1 can be reduced by making a smaller but that will also change the value of f_{hpf}.
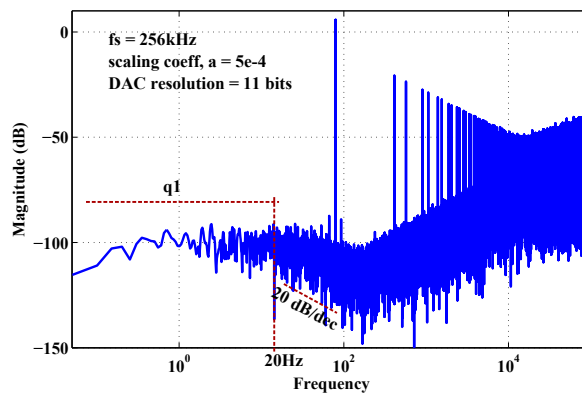
Figure 3.23: 12 bit ADC followed by a 11-bit DAC in the feedback
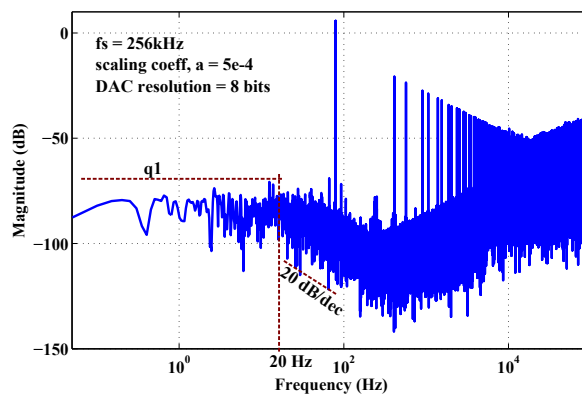
Figure 3.24: 12 bit ADC followed by a 8-bit DAC in the feedback

3.2.4 Block-level Implementation

Two popular types of continuous-time implementation of the integrator are the active-RC implementation and g_m-C implementation respectively. Table 3.5 compares these two topologies w.r.t linearity, power consumption and tunability i.e. three parameters pertinent to this application. In this table, the more the + signs, the more favourable the topology for that parameter.

Table 3.5: Comparison between a g_m-C and an active-RC implementation of the loop filter

	GmC	active RC
Linearity	+	+++
Power consumption	+++	+
Tunability mismatch	+++	+

Although active-RC offers a better linearity performance, a g_m-C implementation is chosen for lower power consumption. g_m-C filters are easier to tune compared to active-RC filters [47]. Moreover, resistances are relatively more difficult to implement on-chip.

The linearity of the g_m-C-stage depends on :

- input signal swing

- output signal swing

- output impedance

- region of operation

The reference voltage of the DAC has to be greater or equal to the amplitude of the signal available from the instrumentation amplifier. The worst-case signal swing that can be expected is when the input signal is $\approx V_\mathrm{ref}$ and that from the DAC feedback is $-V_\mathrm{ref}$ or vice-versa. Thus the signal swing at the input of the g_m-stage, in the worst case will be twice that of the output of the instrumentation amplifier. To reduce the signal swing, the g_m block can be brought outside the sigma-delta loop. To further reduce the signal swing at the input of the g_m-stage, a capacitive divider is also added at its input. The output signal swing can be reduced by increasing the capacitor, C_int. The output impedance can be increased by cascoding. Since, the current-voltage relationship is exponential in the sub-threshold region, biasing in this region will lead to a lot of distortion. Hence the g_m-stage is biased in the strong inversion region.

By moving the g_m-stage outside the sigma-delta loop, current is the physical quantity that is converted to digital by the modulator. This would require a current DAC. Table 3.6 compares this approach to that of a standard g_m-C sigma-delta modulator in terms of noise, distortion and power consumption.

Table 3.6: Voltage vs Current conversion

	Voltage conversion	**Current conversion**
Noise	Mathematically same	Mathematically same, however more freedom to choose between different values and implementations of transconductances
Distortion	Assuming a 100mV input signal and voltage reference, the signal swing at the input of g_mC filter would be 200mV which would lead to considerable distortion	Only the input signal present at the input of the gm-stage and hence distortion much lesser
Power consumption	To counteract the distortion due to high input voltage swing, more power would have to be consumed	Can be made very low power by using low currents and relatively-large valued capacitors

Since the overall system noise would primarily be decided by the instrumentation amplifier, using the current-based continuous-time sigma delta is possible for this application.

Fig. 3.25 and Fig. 3.26 show two possible methods of implementing the scaling coefficient and the integrator present in the mixed-signal feedback loop. In Fig. 3.25, the scaling and integration is implemented in two different stages. In the first stage the comparator output is scaled by using a resistive divider. A capacitive divider cannot be implemented as the scaling coefficient is very small and hence extremely large capacitor ratios would be needed. The integration is then achieved by using a switched capacitor (or continuous-time implementation). In Fig. 3.26, the scaling and integration function is done both by the charge-pump. The linearity of the scaling coefficient and the integrator will appear directly at the input of the sigma-delta modulator. Since the charge-pump implementation has fewer components, it leads to lower power consumption and an easier design for linearity. Hence a charge-pump implementation is chosen.

The voltage on the capacitor C_{fb} will be the scaled and integrated version of
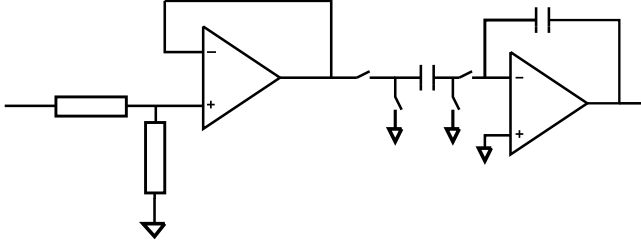
Figure 3.25: Scaling and Integration performed in two stages
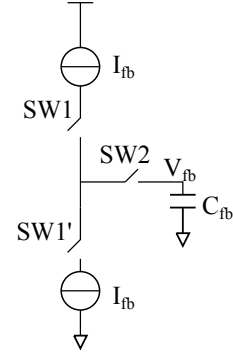
Figure 3.26: Scaling and Integration performed in a single-stage with a charge-pump

the output of the comparator. The comparator will decide whether C_{fb} is charged and discharged. SW2 will be turned on for time t_{sw2}, whenever the comparator output is available. Since a current mode sigma-delta is used, another g_m-stage will be required after the filter in the second feedback loop of the modulator as shown in Fig. 3.27. However, g_{m1} and g_{m2} can then be combined to lower the power consumption. The final system-level diagram is shown in Fig. 3.28 The scaling coefficient, a, will then be given by

$$g_m \cdot \frac{V_{fb}}{2} = a \cdot I_{ref}.$$ (3.16)

Implementation of a small scaling coefficient is challenging as it will be affected by non-ideal effects such as charge injection, clock feed-through as will be shown in the next chapter. According to 3.11, this value can be increased by decreasing the sampling frequency. To reduce the sampling frequency and keeping the output resolution the same, the order of the modulator needs to be increased. In such a case, the modulator would have three or more integrators within the loop (including the one in the feedback). Thus care has to be taken in designing the feedback and further zeros may need to be added to ensure stability. A second-order sigma-delta with additional feedback is presented as future work in Chapter 6. However, in this thesis, only a first-order modulator is considered.

The exact position of the high-pass cut-off frequency is determined by accuracy of the scaling coefficient. Since g_m and C are known to spread to as much as 40% [48] with process variation, the scaling coefficient and therefore the position of the cut-off frequency will also change by 40%. This will not have an effect on the noise-shaping property of the sigma-delta modulator as it is essentially a first-order one without any optimized NTF zeros. If the accuracy of position of the cut-off frequency is important, the values for g_m can be tuned either by tuning its bias current or in the digital domain. The design of tuning circuitry is assumed to be beyond the scope of this thesis.
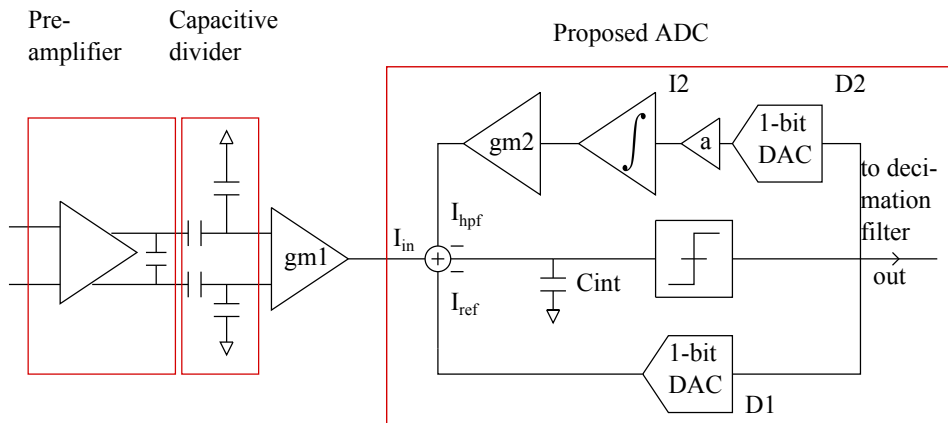
Figure 3.27: System-level diagram with two transconductance stage
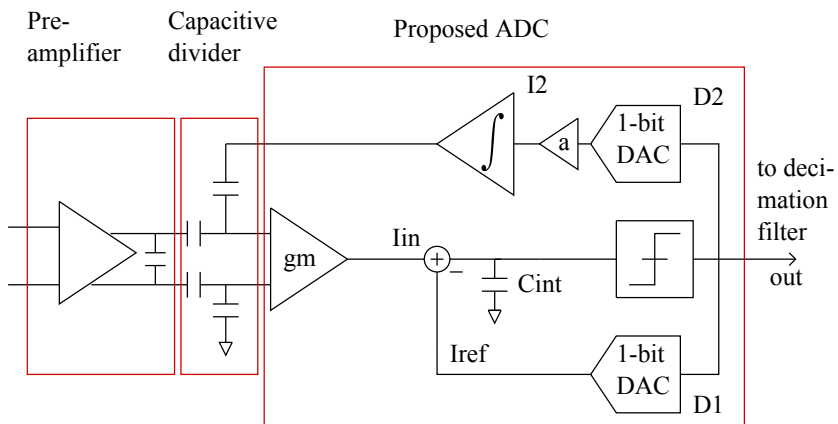
Figure 3.28: System-level diagram with just one transconductance stage

Circuit-Level Design

<div style="text-align: right; font-size: 3em;">4</div>

This chapter is organized as follows. Section 4.1 discusses the design of the instrumentation amplifier in detail. Section 4.2 presents the design of the comparator. Section 4.3 discusses the design of the DAC. Section 4.4 discusses the design of the input transconductance stage. Section 4.5 deals with the design of the charge-pump.

4.1 Design of Instrumentation Amplifier

The standard 3-opamp instrumentation amplifier is the most popular architecture for read-out of medical signals. However, a single differential amplifier will be sufficient for our application as common-mode rejection is not an issue.

As per the structured design methodology, the design for the amplifier is described in the following stages

- Design of feedback

- Design for noise

- Design of low-pass cut-off frequency

- Design for distortion

4.1.1 Design of feedback

Fig. 4.1, Fig. 4.2 and Fig. 4.3 depict three possible feedback configurations (transimpedance amplifier, voltage amplifier and transconductance amplifier). C_{in} is the input capacitance and C_f is the feedback capacitance. A capacitive feedback is chosen over resistive feedback to have a high input impedance, low noise and low power. The transfer function for each case is given by

$$\frac{V_{out}}{V_{in}} = A = -\frac{C_{in}}{C_f} \quad \text{(transimpedance amplifier)} \tag{4.1}$$

$$\frac{V_{out}}{V_{in}} = A = 1 + \frac{C_{in}}{C_f} \quad \text{(voltage amplifier)} \tag{4.2}$$

$$\frac{I_{out}}{V_{in}} = g_m = \frac{1}{Z_f} \quad \text{(transconductance amplifier)} \tag{4.3}$$

In the voltage amplifier stage, the DC-component is transferred to the output with a gain of one. This is undesirable as it might lead to saturation in the stages following the instrumentation amplifier. For the transconductance amplifier to be used in a
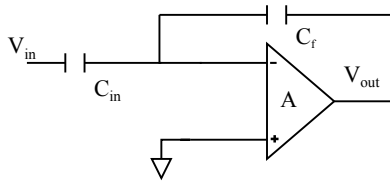
Figure 4.1: Transimpedance amplifier configuration
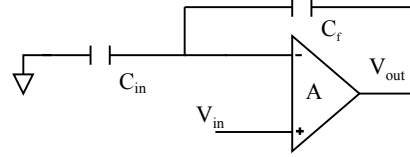
Figure 4.2: Voltage amplifier configuration
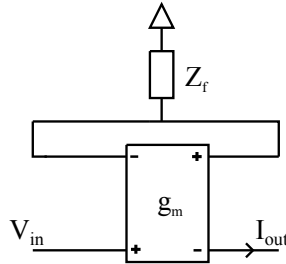
Figure 4.3: Transconductance Amplifier configuration

negative-feedback configuration and assuming 1μA of output signal current, a g_m of at least 50mS would be required which would lead to high power consumption. Hence, amongst the three feedback configurations, the transimpedance amplifier is the most promising one.

The capacitor values can be determined based on the gain and the input impedance of the amplifier. The input impedance of the transimpedance topology is given by

$$|Z_{in}| = |\frac{1}{s \cdot C_{in}}| = \frac{1}{2 \cdot \pi \cdot f \cdot C_{in}} \tag{4.4}$$

$C_{in} = 10$pF is chosen so that the input impedance >5MΩ for f$<$200Hz. $C_f = 100$fF is chosen so that gain $= 100$. A high gain is needed so as the noise from the stages following the instrumentation amplifier does not affect the SNR. However, the distortion in the following stages will also increase with increase in the gain.

4.1.2   Design for noise

Fig. 4.4 shows a conventional single-stage fully differential amplifier implementation. A PMOS input stage has been used as it exhibits lower flicker noise than an NMOS input stage.

Since we are not concerned with CMRR of the amplifier, a tail-current source is not required to bias the amplifier. We can use a voltage-source to bias it as shown in Fig. 4.5. The advantage of doing so would be a simpler common-mode feedback (CMFB) circuitry. Since the amplifier is ac-coupled (to reject the DC-offset) and fully differential, the common-mode voltages of the output and the input need to be set. Conventionally, if a tail-current source is used for biasing, the common-mode voltage
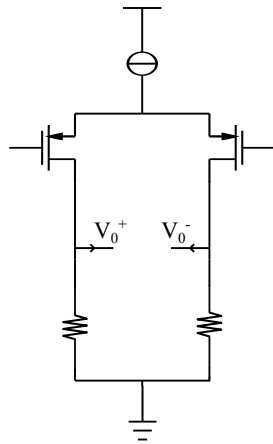
Figure 4.4: Conventional Differential Amplifier
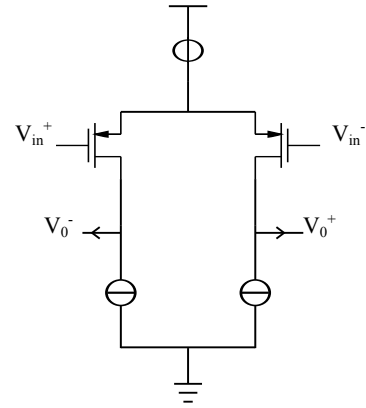
Figure 4.5: Proposed Differential Amplifier

of the outputs are set via techniques such as using large resistances or a triode-based differential amplifier or switched-capacitors [49]. If such techniques are unfavourable, one would need to resort to a differential-input, single-ended output amplifier as shown in Fig. 4.6. Whereas in the proposed biasing scheme for the differential amplifier, the output common-mode voltages can simply be set via a feedback resistor to the input terminal, as shown in Fig. 4.7. The feedback resistor can be implemented by pseudo-resistors. Their non-linearity will not be a concern as they are used for biasing purposes only. Thus a voltage-source biasing helps in simpler implementation of a fully-differential amplifier.

To achieve a closed loop gain of 100 and a loop gain >100, small-signal gain of
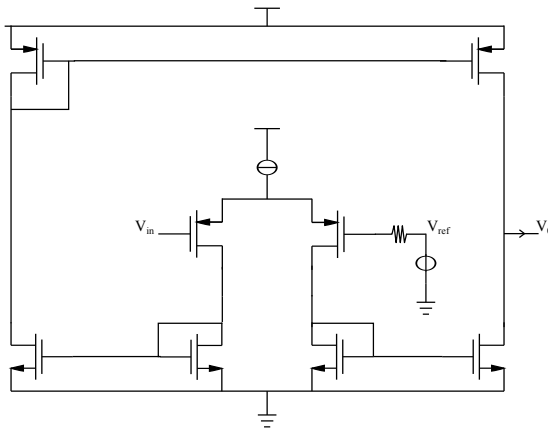
Figure 4.6: Single-sided Input, Single-sided Output Amplifier
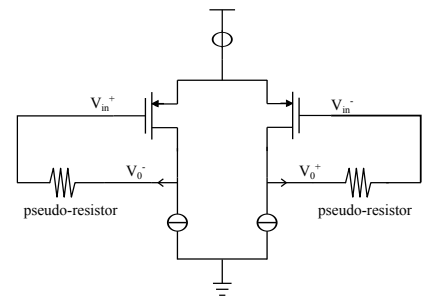
Figure 4.7: Biasing of the proposed differential amplifier

the amplifier, $gain_{ac}$ has to be greater than 10^4 or >80dB. Assuming that the amplifier is implemented by a single differential stage. Small-signal gain is then, given by

$$gain_{ac} = g_{m} \cdot (r_{o}//Z_{L}//Z_{f}) \approx g_{m} \cdot r_{o} \qquad (4.5)$$

where g_m is the transconductance of the input transistor, Z_L is the load impedance and Z_f is the impedance looking into the feedback. Since the load is capacitive and the signal bandwidth <200Hz, it can safely be assumed that $gain_{ac}$ will be decided by just its g_m and its intrinsic output resistance, r_o.

The gain can be obtained by biasing in their deep sub-threshold region. However, this will also result in a high input-referred noise. The input-referred noise of a differential stage and that of the corresponding instrumentation amplifier are [50]

$$S_{u,in} = 2 \left(\underbrace{\frac{2kT^1}{g_m}}_{\text{Thermal noise}} + \underbrace{\frac{K_f \cdot I_{bias}}{C_{ox} \cdot L^2 \cdot f \cdot g_m{}^2}}_{\text{Flicker noise}} \right) \tag{4.6}$$

$$S_{u,in,amp} \approx \left(\frac{C_{in} + C_f + C_{gs}}{C_{in}} \right)^2 \cdot S_{u,in} \tag{4.7}$$

where k is the Boltzmann's constant, T is the absolute temperature, K_f is the flicker noise coefficient, C_{gs} is the input capacitance of the transistor, I_{bias} is the bias current of each branch of the differential pair and C_{in} and C_f have the same meaning as defined earlier. The effect of input-referred noise current has been neglected. Flicker noise is dominant in the signal bandwidth. However, it can be reduced simply by increasing the area of transistor. In the subthreshold region it holds

$$g_m = g_{m,subthr} = \frac{I_{bias}}{n \cdot U_t} \tag{4.8}$$

where U_t is the thermal voltage and n is the subthreshold constant which varies from 1-1.4 [43]. By substituting (4.8) in (4.6), I_{bias} will appear in the denominator in (4.6) and therefore lowering it will lead to an increase in $S_{u,in}$ and $S_{u,in,amp}$. Thus, a trade-off exists between power consumption and noise. The Noise-efficiency factor (NEF) [52], is a figure-of-merit of this trade-off. It measures the amount of power consumed to achieve a certain input-referred noise. The NEF is

$$\begin{aligned} \text{NEF} &= \sqrt{S_{u,in} \cdot \Delta f \cdot \frac{2 \cdot I_{bias}}{\pi \cdot U_t \cdot 4kT \cdot \Delta f}} \\ &\approx \sqrt{\frac{2}{U_t} \cdot \frac{I_{bias}}{g_m}} \end{aligned} \tag{4.9}$$

The ideal NEF factor is 1, which occurs when a single BJT with no flicker noise is used. All other practical circuits have a higher NEF. Since power consumption is a major concern in this design, NEF is an important figure of merit.

---

[1]Although this is a widely accepted noise model for mosfets biased in weak-inversion, cadence spectre does not differentiate between regions of operation and uses the following model $S_{u,in,thermal} = \frac{4kT}{3 \cdot g_m}$ [51]. Thus the simulator will over-estimate the amount of noise. This is not an issue as it will lead to a little over-design.

Figure 4.8: Instrumentation Amplifier schematic

According to (4.6) and (4.9), to achieve a low noise and a low NEF factor, a high g_m and high $\left(\frac{g_m}{I_{bias}}\right)$ is required. $\left(\frac{g_m}{I_{bias}}\right)$ is the maximum in the subthreshold region [25]. Hence to reduce $S_{u,in}$ and the NEF simultaneously, the transistor has to be biased near the threshold voltage. However, $gain_{ac}$ in this region will not be >80dB. Therefore a second gain-stage (cascade) or a cascode is needed to boost it. In both the cases, the total small-signal gain will be the same but the small-signal output resistance of each case will be different. However, since the load and the feedback of the instrumentation amplifier are both capacitive, both the cascade and a cascode configurations will have almost the same performance in terms of achievable gain, input-referred noise, power consumption and frequency response. Since voltage swing is not a concern in this application, a cascode stage is chosen. Fig. 4.8 shows the schematic of the complete instrumentation amplifier. The small-signal gain will now be

$$gain_{ac} = g_{m1} \cdot r_{o1} \cdot g_{m3} \cdot r_{o3} \qquad (4.10)$$

and the input-referred noise of the amplifier will now be

$$S_{u,in} \approx \left(\frac{2kT}{g_{m1}{}^2}\right) \cdot (2g_{m1} + 2g_{m5}) + \left(\frac{I_{bias}}{C_{ox} \cdot f \cdot g_{m1}{}^2}\right) \cdot \left(\frac{2 \cdot K_{fp}}{L_1{}^2} + \frac{2 \cdot K_{fn}}{L_5{}^2}\right) \qquad (4.11)$$

where $g_{m1,3}$ are the transconductances of $M_{1,3}$, $r_{o1,3}$ are the output resistances of $M_{1,3}$, K_{fn} and K_{fp} are the NMOS and PMOS flicker noise coefficients respectively and $L_{1,5}$ are the lengths of transistors $M_{1,5}$ respectively. Since the output is taken differentially, the noise due to M_7 will not play a role. The noise due to PMOS current source transistors is neglected. Like earlier, flicker noise is reduced by increasing the area of the transistors. The thermal noise can be decreased by increasing I_{bias}. $\frac{W}{L}$ also needs to be simultaneously increased to keep the input transistors biased near the threshold voltage. This will lead to large input transistors and hence large input capacitance, too. C_{in} and C_f need to be increased so that the effect of C_{gs} in (4.7) can be neglected.

Another drawback of large input transistors is that the non-dominant pole due to the transconductance of the biasing current mirror will shift to lower frequencies as the area of the transistors is increased and reduce the phase-margin of the loop gain. Thus there is a trade-off between power, noise, area and stability.

Table 4.1 lists down the final values of all the parameters so as to achieve the required target of 60dB SNR for a frequency range of 50mHz-200Hz with a loop gain phase margin of approximately 60°. A frequency range of 50mHz - 200Hz is chosen for calculating the noise instead of 1Hz-200Hz as listed in Table 1.2 because as stated in Chapter 1, the design eventually needs to be made tunable. In such a case the worst-case high-pass cut-off frequency will be 50mHz and has thus been chosen for noise-analysis. The loop gain and the closed-loop response of the amplifier are shown in Fig. 4.9 and Fig. 4.10 respectively. The input-referred noise of the amplifier is shown in Fig. 4.11. The integrated noise over 50mHz - 200Hz is 0.58μVrms. For a 1mV_{pp} (0.7μVrms), this translates to an SNR $\approx$ 63dB.

Table 4.1: Operating points of components in the Instrumentation Amplifier

Component	Value	
I_{bias}	10μA	
$I_{\text{bias,casc}}$	200nA	
C_{f}	400fF	
C_{in}	40pF	
Transistor	$\frac{W}{L}$ (μm)	g_{m}
M_1, M_2	450/10	140μS
M_3, M_4	50/35	4μS
M_5, M_6	25/150	21μS
M_7	50/150	42μS

4.1.3   Design for low-pass cut-off frequency

The low-pass cut-off frequency is implemented by placing a load capacitance, C_{L}, at the output of the amplifier. The output node is chosen instead of the input or the feedback node because otherwise huge resistors would be required. This would also lead to an increase in the input-referred noise. The low-pass cut-off frequency, f_{lpf}, is given by

$$f_{\text{lpf}} = \frac{1}{2 \cdot pi \cdot C_{\text{L}} \cdot R_{\text{out}}} \tag{4.12}$$

R_{out}, the differential output resistance of the amplifier is

$$R_{\text{out}} = \frac{A}{g_{\text{m1}}} \tag{4.13}$$

By substituting the value of $g_{\text{m}} = 140\mu S$ from Table 4.1 shows that a $C_{\text{L}} = 1$nF will be required to achieve f_{lpf}= 200Hz, which is unpractical to implement on-chip. To decrease
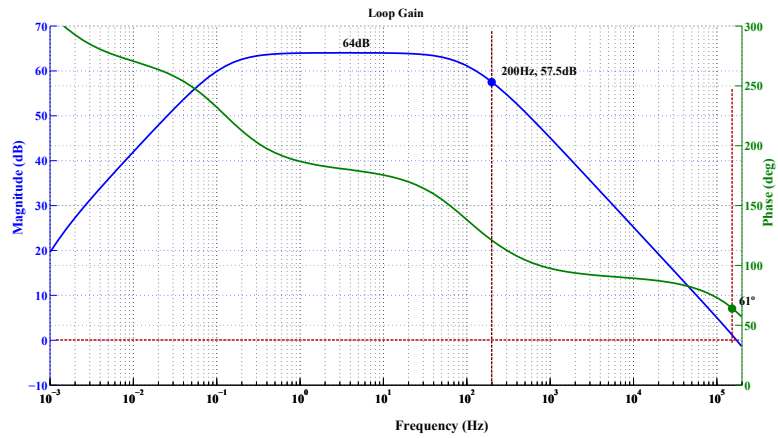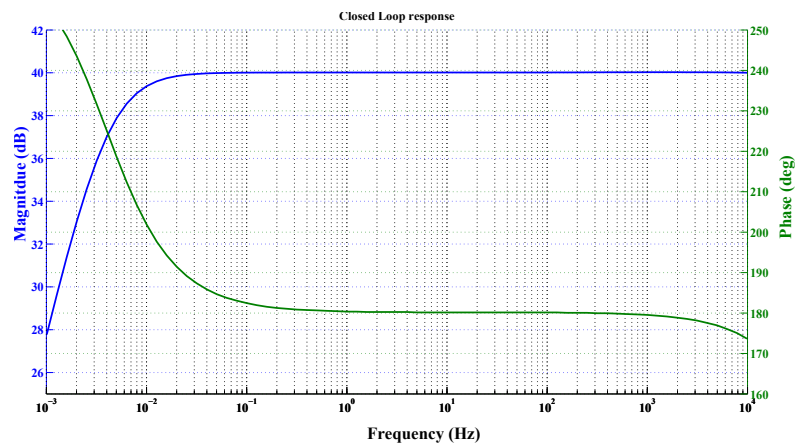
Figure 4.9: Loop Gain

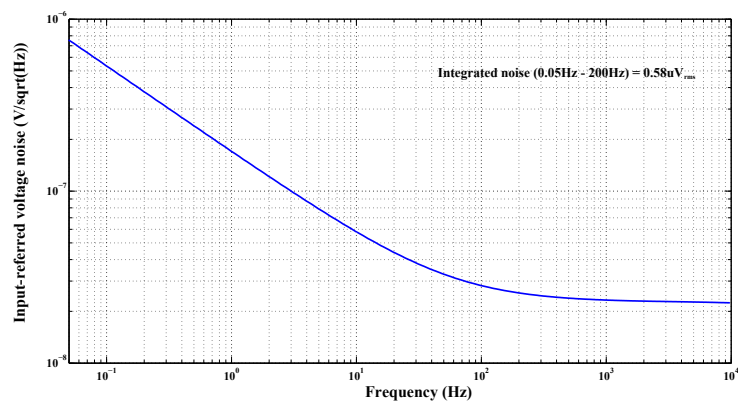Figure 4.10: Closed Loop response

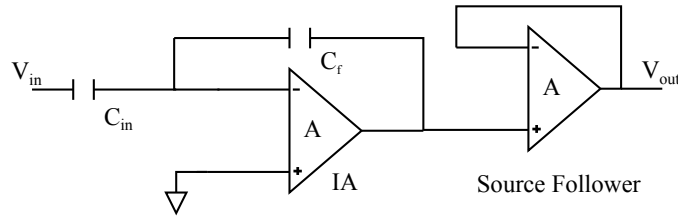Figure 4.11: Input-referred noise of the instrumentation amplifier

Figure 4.12: Indirect Feedback

the value of this capacitance either g_{m1} needs to be decreased, which is not possible as it is decided by the noise specification, or use the methods listed below -

- Current Division Technique [53]- In this technique, the signal current is divided into two. One part is dumped and the other is used for providing loop gain. This reduces the overall transconductance of the amplifier and thus increases the output resistance. Required noise performance can also be achieved by changing the area of the current-splitting transistor. However, this will require more power and moreover, the capacitance at the drain of the input transistor will also increase and thereby reducing the phase margin further.

- Indirect feedback by copying the output voltage [54]- In this technique, instead of feeding back the output voltage to the input, its copy is fed back. The instrumentation amplifier is followed by a "lousy" source follower i.e. a source follower with a high-impedance as shown in Fig. 4.12. Noise from the source follower does not affect the SNR as it appears after the instrumentation amplifier. However, the output resistance in (4.13) will now be decided by the transconductance of the source follower and not by that of the instrumentation amplifier. The power consumption will not be significant as an extremely low transconductance is required. The disadvantage of such an approach is that the distortion of the source follower will not be suppressed by the loop gain. However, it is seen that the required linearity is still achievable.

- Implement the filter in the digital domain- This method is the most convenient as a digital filter would already be present in a sigma-delta ADC. Since a continuous-time sigma-delta is designed, low-pass filtering before the ADC is not required.

However, since a digital filter has not been designed in this thesis, the indirect feedback technique is implemented. It is preferred over the current division technique due to power considerations. Fig. 4.13 shows the schematic of a simple source follower stage. $I_{\text{bias,src}}$ = 20nA so as the transconductances of M_8 and M_9 are very small. Now, for f_{lpf} = 200Hz, C_L = 20pF. Fig. 4.14 plots the magnitude and phase response of the instrumentation amplifier and the source follower. Table 4.2 lists the values of the parameters in the source follower. The transistors are extremely long so that they are biased in strong inversion to minimize the distortion from this stage.
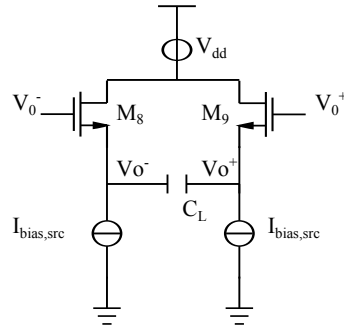
Figure 4.13: Schematic of the source follower
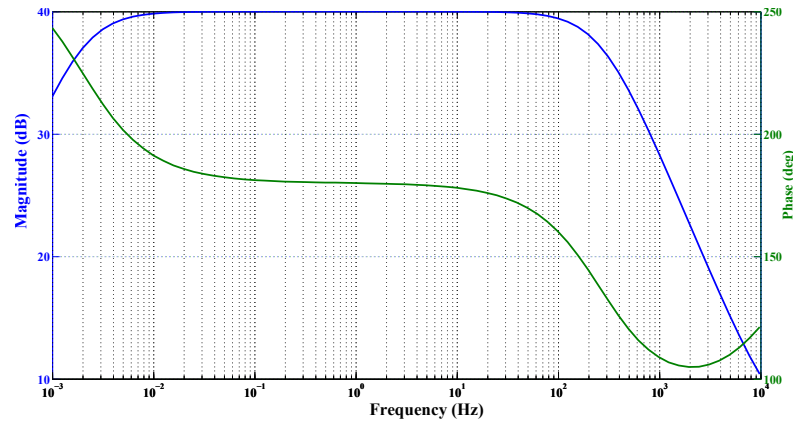
Figure 4.14: Magnitude and Phase response of the amplifier followed by the source follower

4.1.4 Distortion

There are two types of distortion viz. large signal distortion and weak distortion. Large signal distortion occurs when the transistors in the output stage move out of the saturation region due to the output voltage swing and slewing. In Fig. 4.8, $V_{ds3,4} = 770$mV and $V_{DSAT3,4} = 65$mV. Similar care has been taken while designing the source follower stage. For $g_{m1,2} = 140\mu$S and 1mV input signal, the maximum small signal current in one branch of the amplifier is 140nA. $I_{bias,casc} = 200$nA and therefore there will be no slewing. In the source follower, $g_{m8,9} = 70$nS. Therefore the maximum signal current

Table 4.2: Operating points of components in the Source follower

Component	Value	
$I_{bias,src}$	20nA	
C_L	20pF	
Transistor	$\frac{W}{L}$ (μm)	g_m
M_8. M_9	0.5/350	70nS
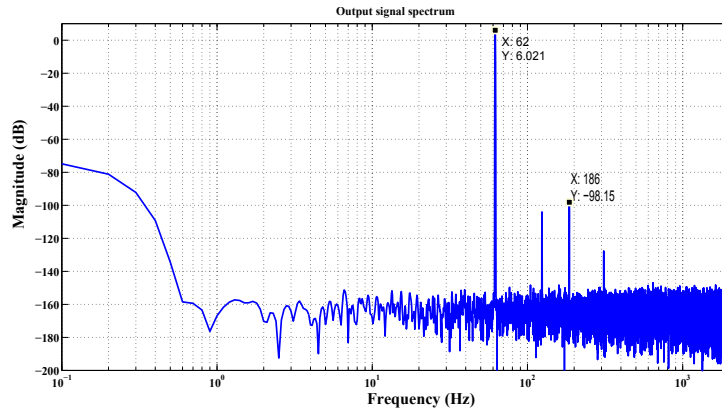
Figure 4.15: Frequency spectrum of the output of the amplifier for input frequency = 62Hz

will be 3.5nA. $I_{\text{bias,src}} = 20$nA and hence no slewing. Weak distortion can be minimized by increasing the loop gain. From Fig. 4.9, the loop gain of the amplifier >60dB (worst case, 57dB at 200Hz) which is sufficient for meeting the 60dB resolution requirement. Fig. 4.15 plots the frequency spectrum of the output of the amplifier for an input frequency of 62Hz. The main distortion component, 3rd harmonic, is 104dB lower than that of the main signal component.

4.2   Design of the comparator

The fundamental task of a comparator is to amplify the difference between its inputs to a digital value. There are three possible topologies for implementing a comparator [55]. Fig. 4.16, shows a chain of large-gain amplifiers. The total gain is such that the output of the last amplifier saturates to the rail voltages. Fig. 4.17 has a second amplifier in positive feedback configuration. The feedback amplifier has a much smaller gain than the one in the forward path and is used to add a threshold to the decision process. This is also known as hysteresis. Fig. 4.18 has a large gain amplifier in positive feedback to increase the speed of conversion. Due to the large positive feedback, a clock is required to reset the amplifier to a neutral state configuration.

In sigma-delta architectures, hysteresis is not a concern and thus the second topology is not needed. The latched comparator requires less power consumption for the same speed as compared to the chain of high gain amplfiers [55]. Hence the comparator

Figure 4.16: Chain of large-gain amplifiers

Figure 4.17: Amplifier with hysterisis
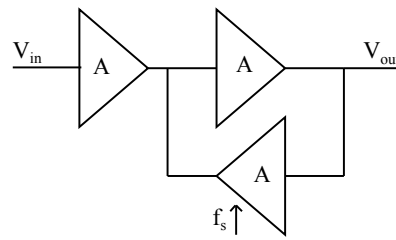
Figure 4.18: Latched amplifier

topology as shown in Fig.4.18 is chosen. Fig. 4.19 shows a popular architecture of such an architecture. The comparator has a g_{m}-stage followed by an inverter latch. V_{reset} short-circuits (resets) the comparator outputs for half the sampling time period i.e. 2μs.

The comparator should satisfy the following criterion -

- Speed: A decision should be made by half of the sampling time-period i.e. 2μs for our case
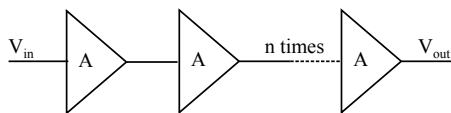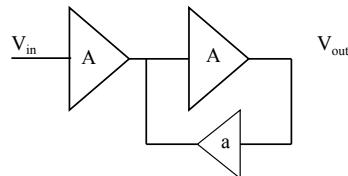
- Memory-less: The previous comparator decision should not affect the present decision

- Power: The comparator should consume less power, hopefully lesser than that of the instrumentation amplifier

The main non-idealities associated with a comparator are -

- Offset: The comparator offset will be suppressed by the loop and thus, is not a major concern in a sigma-delta architecture.

- Memory effect: The effect of memory is negated by using a reset switch. The comparator is reset for half of the clock period and operational for the other half. Thus the voltage nodes, $V_{01}{}^{+}$ and $V_{01}{}^{-}$ have 2μs to reset. This is easily achievable using simple MOS switches and therefore the comparator state in the previous clock cycle will not have an effect on the present decision. However, this reset technique comes at an expense of an increase in amount of charge kick-back. Techniques for reducing the charge kick-back are discussed later.

- Metastability: The comparator outputs switch between a digital '1' and a digital '0' depending upon the inputs. However, the response time varies with the input. The smaller the difference between the input voltages, the greater will be the comparator response time. This signal-dependent variation between the response times will affect the DAC response. This will lead to modulation of out-of-band noise into the signal spectrum. This effect has been reduced in the design by adding another cross-coupled inverter following the comparator. Another clock (V_{latch}) will latch the output of the comparator into this cross-coupled inverter just before the comparator is reset. Fig. 4.20 plots the effect of different input voltages vs. the response time. Here $V_{\mathrm{diff}} = V_{\mathrm{int}}{}^{+}$ - $V_{\mathrm{int}}{}^{-}$. As V_{diff} decreases, the response time of the comparator increases.
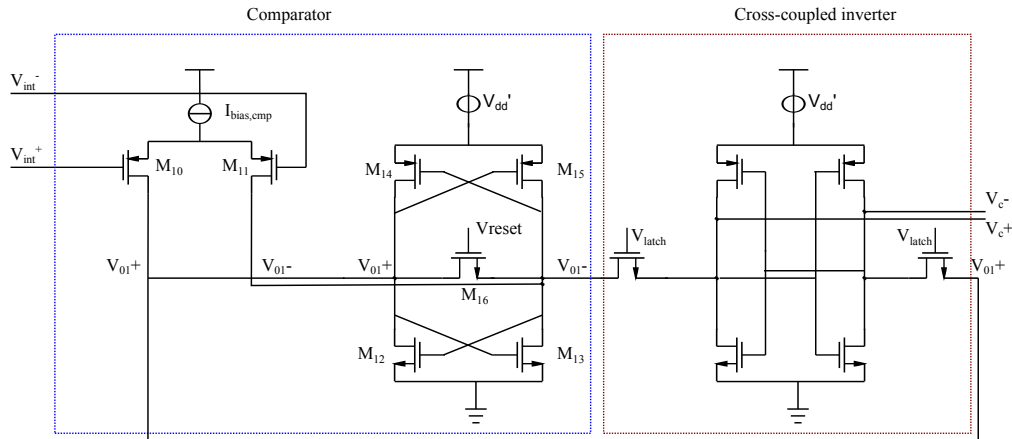
Figure 4.19: Schematic of a latched comparator
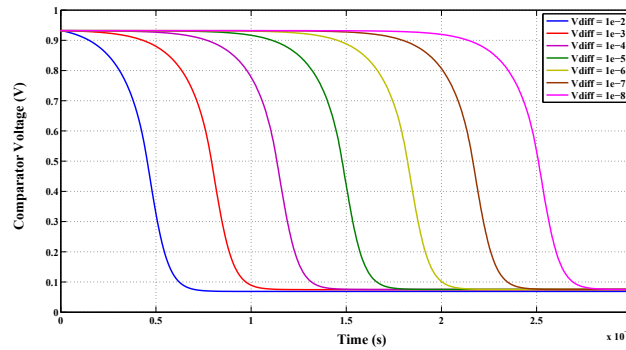
Figure 4.20: Response time variation of comparator to different input voltage differences

- Effect of charge kick-back: This can also be lowered by using a large C_{int} and a differential DAC structure (which leads to negligible even harmonics). Its effect can be reduced further by adding a pre-amplifier preceding the comparator. This will also aid in suppressing the comparator offset. However, it was observed that 10-bit linearity is obtainable without a pre-amplifier and hence is not used. This not only leads to lower power consumption but also to a faster decision [55].

To reduce the power consumption of the comparator

- The lengths of latch transistors M_{12} - M_{15} are increased. This will reduce the static power consumed by the comparator. This will also reduce the speed of conversion as it will increase the load capacitance seen by $M_{10,11}$ and thus decrease the overall unity-gain bandwidth of the comparator. However, the speed of the comparator will affect only the metastability, which has been taken care of by adding another cross-coupled inverter.

- The digital section of the ADC, i.e. the comparator and the digital filter, use a $V'_{\text{dd}} = 1.5\text{V}$. Designing a voltage reference that is half of the main voltage supply
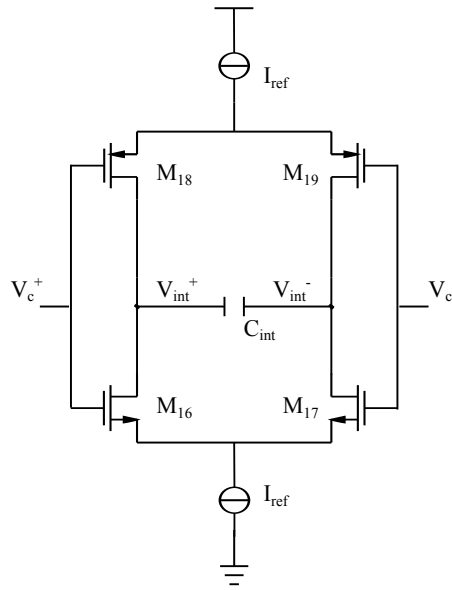
Figure 4.21: Schematic of the differential DAC implementation

can be easily achieved. It is assumed that the reference is available to us and its design is not dealt in this thesis.

The final sizes of the transistors and current sources are listed in Table 4.3.

Table 4.3: Operating points of components in the Comparator

Component	Value
$I_{\text{bias,cmp}}$	1μA
$V_{\text{dd}'}$	1.5V
Transistor	$\frac{W}{L}$ $(\mu$m$)$
M_{10}, M_{11}	5/0.35
M_{12}, M_{13}	0.5/7
M_{14}, M_{15}	1/1.75
M_{16}	1.5/0.35

4.3 Design of the DAC

Fig. 4.21 shows the schematic of the designed DAC. It is a standard differential current DAC. A differential structure has been chosen to reduce the effect of charge kick-back as discussed in the previous section.
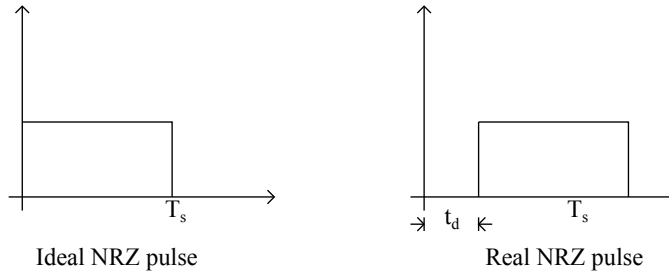
Figure 4.22: NRZ pulse response

4.3.1   Selection of DAC pulse waveform

There are numerous types of DAC pulse waveforms such as Non-Return-to-Zero (NRZ), Return-to-Zero (RZ), linear/quadratic decaying to name a few.

Fig. 4.22 shows the response of a NRZ type waveform. An NRZ-type implementation is chosen because it is easy to implement [47]. The output of the cross-coupled inverter in Fig. 4.19, can be used simply as switch voltages for the DAC without requiring any additional circuitry.

The main drawback of an NRZ-type waveform is the effect of excess delay, t_{d}, as shown on the right side of Fig. 4.22. A delay of t_{d} appears due to the finite response time of the switches. This, like metastability discussed previously, will modulate out-of-band noise within the signal band. However, it can be shown that for a sampling frequency of 256kHz, this delay is negligible. t_{d} can be written as [56]

$$t_{\mathrm{d}} = \rho_{\mathrm{d}} \cdot T_{\mathrm{s}} \tag{4.14}$$

where ρ_{d} is a constant and can be approximated by [56]

$$\rho_{\mathrm{d}} \approx n_{\mathrm{t}} \cdot \frac{f_{\mathrm{s}}}{f_{\mathrm{T}}} \tag{4.15}$$

where f_{s} is the sampling frequency and f_{T} is the transit frequency of a MOS transistor. In 0.35μm CMOS I3T25 technology, $f_{\mathrm{T}} \approx 20$GHz for an NMOS transistor at 1.5V. Substituting this value in (4.15) will lead to an extremely small ρ_{d} which can be neglected.

The common-mode voltage of nodes $V_{\mathrm{int}}{}^{+}$ and $V_{\mathrm{int}}{}^{-}$ are chosen to be equal to V'_{int} for the sake of convenience.

4.4   Design of input g_{m}-C stage

Fig. 4.23 shows the schematic of a cascoded g_{m}-stage along with the capacitive divider. V_{fb} is the feedback voltage from the charge-pump. As per the block diagram shown in Fig. 3.28, it is connected to the negative terminal of the g_{m}-block. As discussed in

Figure 4.23: Schematic of the cascoded gm-stage implementation

Chapter 3, the amplitude of V_int should not be too large so as to minimize the distortion. The worst-case voltage swing is given by

$$V_\text{int} \approx \frac{2 \cdot I_\text{ref} \cdot T_\text{s}}{C_\text{int}} \tag{4.16}$$
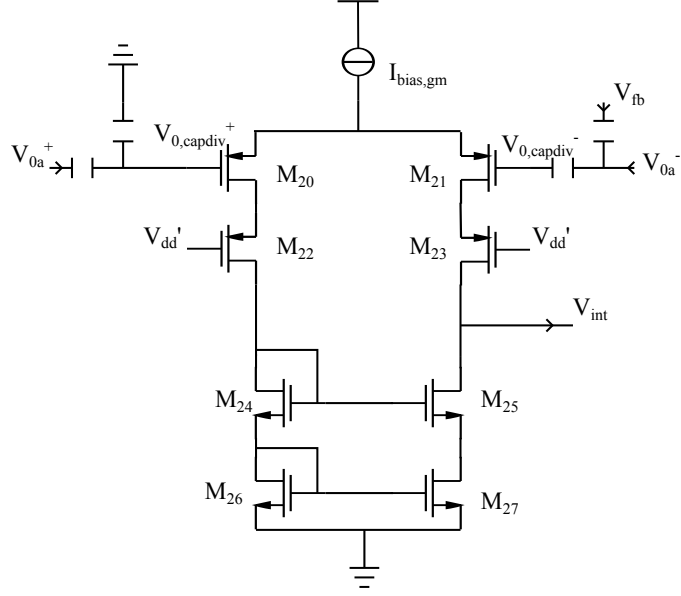
where I_ref is the reference current from the DAC and I_in is the input current to the sigma-delta modulator. Assuming a voltage swing of 20mV and $C_\text{int} = 50$pF. I_in cannot be greater than I_ref to ensure stability [45]. I_in is given by

$$I_\text{in} = 2 \cdot g_\text{m20} \cdot V_\text{o,capdiv}{}^+ \tag{4.17}$$

where g_m20 is the transconductance of the M_{20} and $V_\text{o,capdiv}{}^+$ is the output of the capacitive divider. Choosing $I_\text{ref} = 250$nA. As I_ref is lowered further, the power consumption reduces but I_in also needs to be simultaneously reduced. For $V_\text{o,capdiv}{}^+ = V_\text{o,capdiv}{}^- = 25$mV and $I_\text{in} = 200$nA, the required g_m20 would be equal to 4μS. This, however, leads to a problem. The feedback voltage, V_fb, is connected to just one of the input terminals of the g_m-stage. Such an architecture will face considerable 2nd-order distortion if V_fb is large i.e. $V_\text{fb} > 10$mV. Its amplitude depends on the value of g_m20, I_ref and the frequency of the input signal. From simulations, it is seen that for frequencies close to f_hpf and $g_\text{m20}= 4\mu$S, $V_\text{fb} \approx 20$mV, which is undesirable. Therefore, $g_\text{m20}= 2\mu$S is chosen. g_m20 is not reduced further for the following reasons -

- In a sigma-delta architecture, reducing the input signal w.r.t the reference signal leads to a drop in the SNR. This can also be seen in Fig. 4.24, in which the SNR of the output of modulator for various input currents (I_in) has been plotted. For $g_\text{m20} = 2\mu$S, $I_\text{in} = 100$nA. It can be seen that 10-bit resolution is obtainable with this value of I_in.
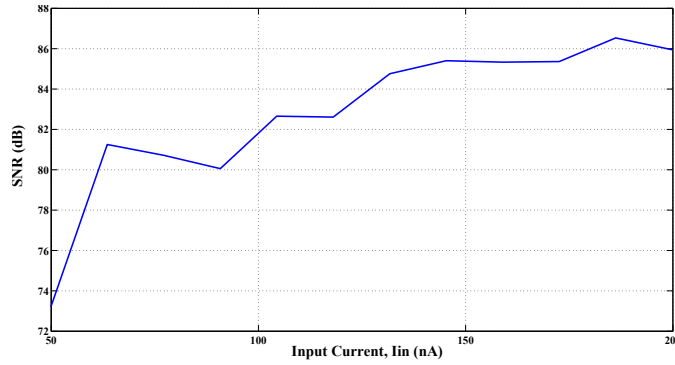
Figure 4.24: SNR vs the Input current to the modulator

- More complicated ultra-low g_m topologies will have to be designed.

The input transistors $M_{20,21}$ need to be biased in strong inversion for low enough distortion. V_{int} is biased at 1.5V. Once again, to simplify the biasing, the input transistors are also biased at 1.5V via pseudo-resistors. Since it is a cascoded structure, these transistors will be biased at the edge of saturation and triode region which emphasizes the need for a small output voltage swing. In the strong inversion, saturation region, it holds

$$g_{m1} = 2 \cdot \frac{I_{bias,gm1}}{V_{ov1}} \tag{4.18}$$

Assuming that the sources of $M_{20,21}$ are biased at 2.8V (keeping 200mV voltage headroom for $I_{bias,gm}$), then $V_{ov20} = 0.7$V. Substituting V_{ov20} and g_{m20} in (4.18) will give $I_{bias,gm} \approx 1.5\mu$A.

The final values of the parameters are specified in Table 4.4.

Table 4.4: Operating points of components in the integrator

Component	Value
$I_{bias,gm}$	1μA
$C_{int'}$	50pF
Transistor	$\frac{W}{L}$ $(\mu$m$)$
M_{20}, M_{21}	0.5/5
M_{22}, M_{23}	200/3.5
M_{24}, M_{25}	50/1.75
M_{26}, M_{27}	10/0.35

4.5   Design of charge pump

According to (3.11),for I_{fb}= 2.6nA, C_{fb}= 40pF and t_{sw2}= 100ns, $a = 5 \cdot 10^{-5}$. The main limiting factor in implementing the scaling coefficient and integration with a charge-

Figure 4.25: Charge Injection from MOS switch

pump is the effect of charge injection from the switches. Other limiting factors in a switched capacitor circuit in general are, clock feed-through effect and kT/C thermal noise. Since the instrumentation amplifier decides the noise behaviour of the circuit and that a relatively large C_{fb} has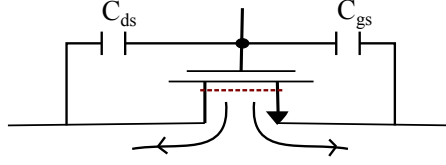 been chosen , the effect of kT/C thermal noise can be neglected. The clock feed-through will manifest itself as a constant offset [49]. Since the output of C_{fb} is connected to the g_{m1} block via a capacitive divider, this offset will not play any role. The magnitude of the offset is given by [49]

$$V_{\text{off,ckfeed}} = V_{\text{ck}} \cdot \frac{W C_{\text{ov}}}{W C_{\text{ov}} + C_{\text{fb}}} \tag{4.19}$$

where V_{ck} is the clock voltage which is 3V is our case, C_{ov} is the overlap capacitance of the MOS switch, W is the width of the MOS switch. Since $C_{\text{fb}} >> C_{\text{ov}}$, the magnitude of this offset will be very small. Hence only the effect of charge injection is considered.

Charge injection in the charge pump will have a two-fold effect on the output of the modulator :

- It will lead to a deviation from the designed scaling coefficient. This is not a critical effect as it will only lead to a change in the cut-off frequency, f_{hpf}, which can also be changed by tuning I_{fb}.

- It will lead to distortion for frequencies close to f_{hpf}. If not designed properly, the resulting linearity can be of the same order as that of a pseudo-resistor and thus nullifying the essence of such an approach.

To understand the effect of charge injection, Fig. 4.25 shows a typical implementation of a MOS switch, M_{sw}. The channel charge in M_{sw} needs a path to be sourced or dumped when the transistor is turned ON or OFF respectively. Let us assume that M_{sw} is being switched OFF. The total amount of charge in the channel depends on the parasitic capacitances of M_{sw}, C_{gd} and C_{gs}. After it is switched OFF, this charge needs to be dissipated. The amount of charge dissipating in each direction depends on the switching time and the impedances seen by the source and drain of M_{sw} [57].

If this amount of charge being dissipated in both the directions is constant every time M_{sw} is switched, the effect of charge injection can be easily compensated by adding dummy switches or using other complementary stages which use up this charge and do not let it reach C_{fb}.
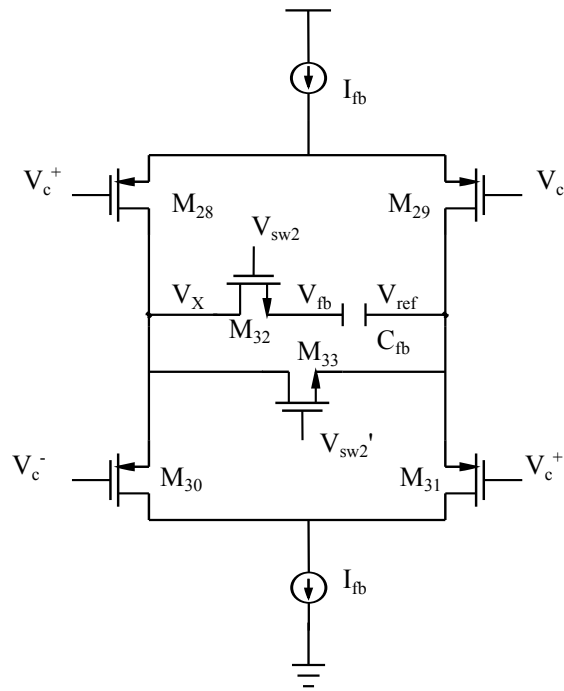
Figure 4.26: Charge Pump schematic

If either the switching time is comparable to f_T or the impedance at source and drain are identical, then the charge dissipation in each direction will be equal. If the charges are equal, charge injection can be compensated by simply adding dummy MOSFETs that are half the size of M_{sw} [57]. Since the f_T is around 20GHz, switching time can be assumed to be much smaller in our case. The impedances at the source and the drain of the switching transistor are asymmetrical in the case of the charge pump. This, therefore, will lead to unequal charge distribution in both directions and hence compensation of charge injection by dummy switches is not possible. Using a transmission gate as a switch also will not compensate for charge injection as the sizes of NMOS and PMOS transistors will be unequal and hence their parasitic capacitances too.

For compensation, a differential architecture, similar to that of the DAC, as shown in Fig. 4.26 is designed. M_{29} and M_{31} are used as the drains of $M_{28,30}$ are connected to current sources and need a path for the current to flow when $M_{29,30}$ are switched off respectively. Both the drains are biased at 1.5V. When V_{sw2} is switched low, the voltage of V_X will not be defined. M_{33} thus serves a dual purpose

- Keeps voltage V_X defined at 1.5V

- Compensates partly for charge injection from M_{32}. It cannot completely compensate due to the reasons stated earlier. However, it is seen that this is enough for a 10-bit requirement.

M_{28}-M_{31} are all PMOS switches to maintain symmetry. Like the DAC, here too, $V_{ref} = V'_{dd}$. to counteract the non-ideal effects, a slightly higher I_{fb}= 6.5nA has been chosen.

Simulation Results

<div style="text-align: right; font-size: 3em;">5</div>

This chapter is organized as follows. The first two sections functionally verify the working of the design. Section 5.1 and Section 5.2 present the results of the high-pass cut-off frequency and Effective Number of bits (ENOB) of the complete system. Section 5.3 presents the power consumption and efficiency results. This is also compared to existing work in literature. Section 5.4 presents the results of the behaviour of the design for process corners and various temperature. Section 5.5 lists down the total area consumption.

5.1 High-pass cut-off frequency

Fig. 5.1 plots the STF of the designed modulator. The signal at 1.1Hz is suppressed by approximately 3dB, as designed for. This is similar to the one obtained by system simulations in MATLAB in Fig. 3.14 except that the 3-dB frequency is different. Due to charge-injection, a slightly higher scaling coefficient, a, than the one predicted by (3.11) was needed.

5.2 ENOB

To obtain a 10-bit resolution, it is important that the total input-referred noise of the system and the distortion at the output are <60dB than the signal frequency.
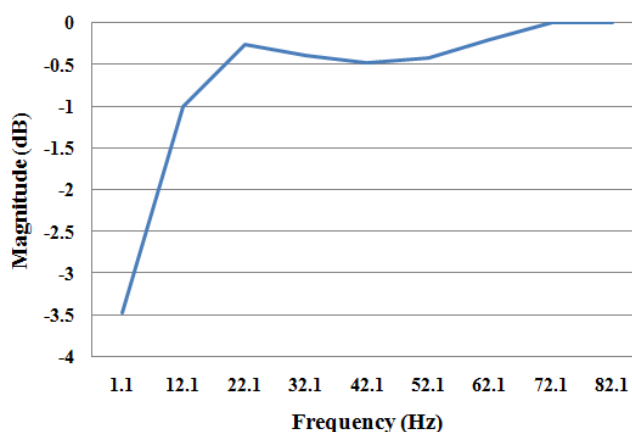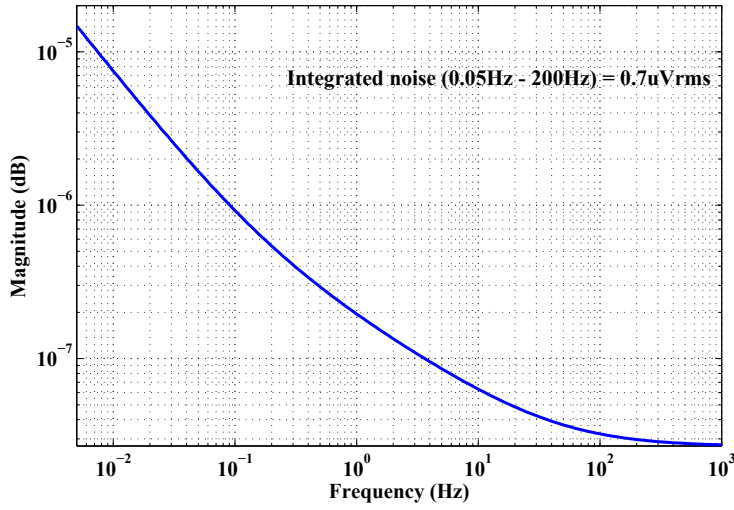

Figure 5.1: STF of the designed modulator

Figure 5.2: Input-referred noise of the whole system

Fig. 5.2 plots the input-referred noise of the whole system i.e. including the g_{m}-stage and the ADC. This verifies that the fact that the SNR of the system is decided mainly by the instrumentation amplifier.

Although, the STF of the system will be as shown earlier, the ENOB will vary with the input frequency. Fig. 5.3 and Fig. 5.4 plot the output of the modulator for input frequencies of 82.1Hz and 1.1Hz respectively. As expected, the 1.1Hz signal component is approximately 3dB lower than that of the 82.1Hz signal. Fig. 5.5 and Fig. 5.6 plot the output of the modulator for input frequencies of 2.1Hz and 3.1Hz respectively to examine the linearity of the proposed mixed-signal feedback technique at frequencies close to f_{hpf}. The 2nd and 3rd order harmonic components in modulator output for $f_{\mathrm{in}} = 82.1$Hz are approximately 74dB and 68dB lower than the main signal component respectively. However, in the modulator output for $f_{\mathrm{in}} = 2.1$Hz, 3.1Hz the 2nd order component is much higher. It is only approximately 61dB lower than that of the main signal component. This is, as discussed in chapter 4, due to the fact that the output of the charge pump, V_{fb}, is connected to just one input of the g_{m}-stage and due to charge-injection from the switches in the charge-pump. Therefore larger the V_{fb} signal swing, the greater the distortion will be.

Compared to Fig. 3.10, this is an improvement of 20dB or 10 times the linearity obtained by using a pseudo-resistor.

5.3   Power Consumption and Efficiency

The total static power consumption of the system is given by

$$P_{\mathrm{static,tot}} = 2 \cdot V_{\mathrm{dd}} \cdot (I_{\mathrm{ref}} + I_{\mathrm{fb}}) + P_{\mathrm{comparator}} + P_{\mathrm{gm}} + P_{\mathrm{amp}} \qquad (5.1)$$

Figure 5.3: Modulator output for $f_{in} = 82.1$Hz
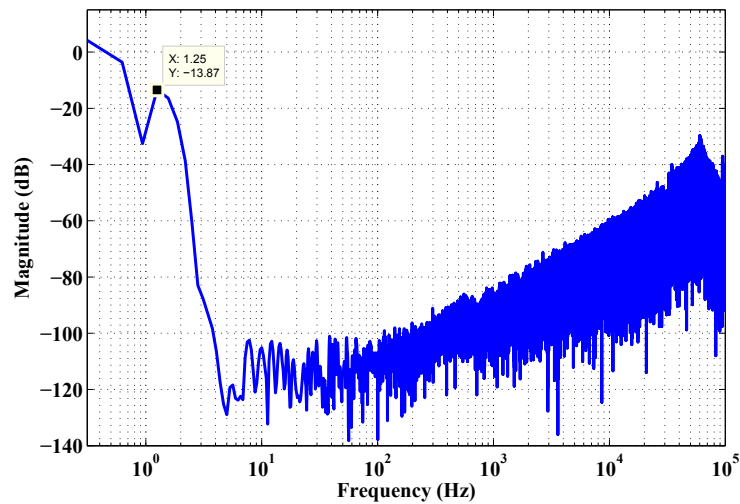
Figure 5.4: Modulator output for $f_{in} = 1.1$Hz

Table 5.1 lists down the power consumption of the different blocks in the system. The corresponding percentage-wise breakup is given in Fig. 5.7. The dynamic power consumption of the inverters/latches will depend on the capacitance and their switching frequency. For a ball-park estimate the dynamic power consumption for $f_{in} = 82.1$Hz is found by simulation and listed in Table 5.1. It is much smaller than the static power consumption because the frequency of operation is just 256kHz and the load capacitance is also since it consists of a inverters and mos-switches.

The instrumentation amplifier is by far the major power consuming block. The reason for this is that it has to meet a high SNR requirement at very low frequencies (where flicker noise is dominant).
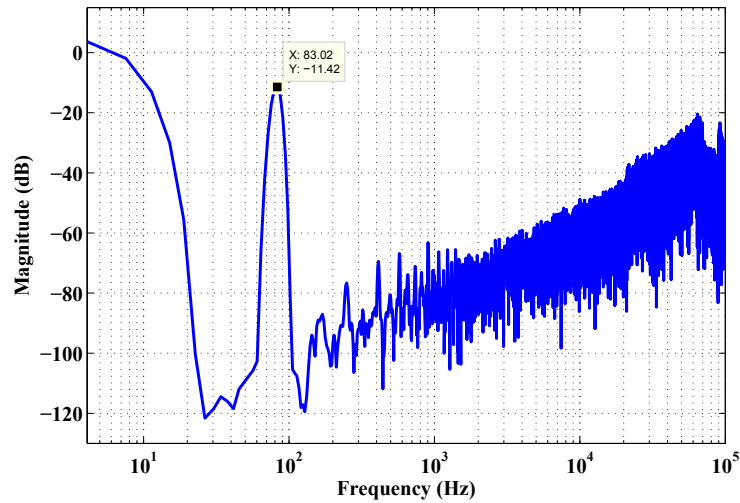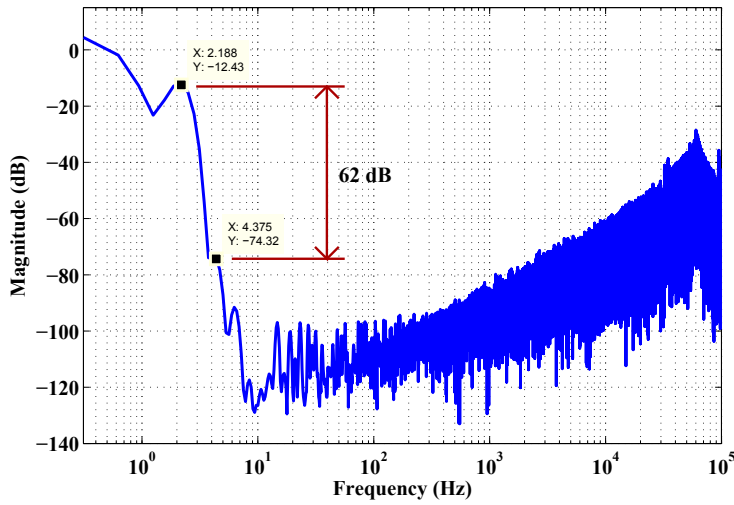
Figure 5.5: Modulator output for $f_{\text{in}} = 2.1\text{Hz}$
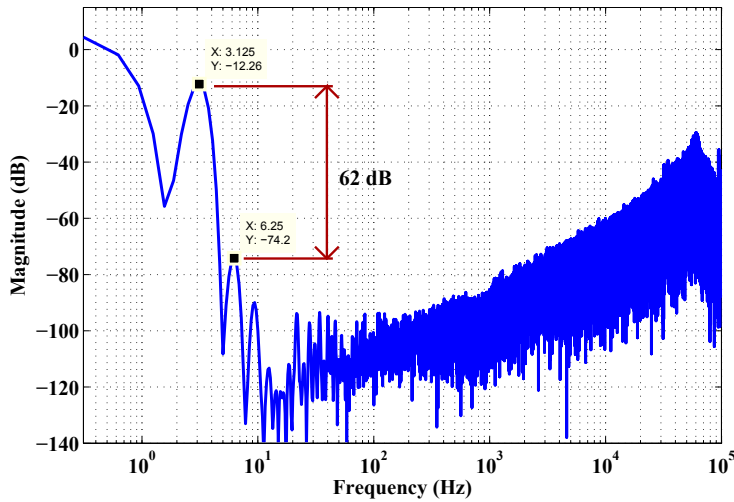
Figure 5.6: Modulator output for $f_{\text{in}} = 3.1\text{Hz}$

To examine the efficiency of this power consumption, Table 5.2 compares the NEF of the designed amplifier w.r.t other published biopotential instrumentation amplifiers. It has the highest SNR. Only [25] and [26] have a lower NEF. As discussed in Chapter 4, to lower the NEF, $\frac{g_{\text{m}}}{I_{\text{d}}}$ needs to be increased. In this design the input transistors are biased a little above the threshold voltage. $\frac{g_{\text{m}}}{I_{\text{d}}}$ at this operating point is 14. The maximum possible $\frac{g_{\text{m}}}{I_{\text{d}}}$ is around 27 as can be seen in Fig. 5.8. However, this value is obtained in the when the bias voltage is 50mV or more below the threshold voltage. To do so, $\frac{W}{L}$ of the input transistors will have to be further increased. This would reduce the phase margin. Hence a slightly higher NEF is kept at the expense of a higher phase margin.

Table 5.1: Block-wise break-up of power consumption

Block	Static Power consumption (μW)
Amplifier	60
g_m-C	3
DAC	1.5
Comparator	1.5
Charge-pump	0.024
Buffers	1.5
$P_{\text{static,tot}}$	$\approx$67.5
$P_{\text{dyn,tot}}$	≈ 0.062 (for f_{in}=82.1Hz)
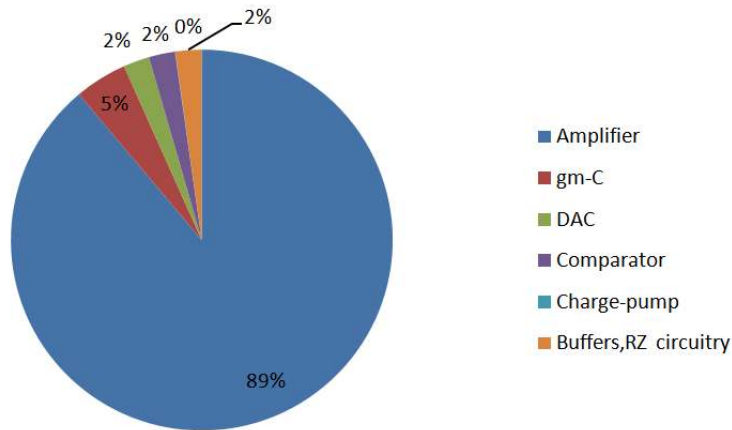
Figure 5.7: Block-wise break-up of power consumption

Fig. 5.9 plots the Power Supply Rejection Ratio (PSRR) of the amplifier. It is 80dB in the worst case i.e. for $f_{\text{in}} = 200$Hz.

5.4 Effect of Mismatch, Process Variation and Temperature

Fig. 5.10 plots the effect of mismatch between transistors on the transfer function of the amplifier. In this technology, the mismatch in capacitor ratios is very small ($\approx$0.1%). Hence the only effect that mismatch has is on the frequencies below f_{hpf} (the marked area in the figure) and hence not of any consequence.

Table 5.2: Comparison of NEF with existing biopotential instrumentation amplifiers

Work	Technology node	Bandwidth	Input-referred noise/(SNR)	NEF	Phase margin
[25]	1.5μm	7.2kHz	2.2μVrms (50dB)	2.9	52
[25] (EEG)	1.5μm	30Hz	1.6μVrms (52.8dB)	4.8	N/A
[26]	0.35μm	460Hz	2.5μVrms (48.9dB)	3.26	N/A
[23]	0.5μm	350Hz	1.12μVrms (55.9dB)	7.8	N/A
[42]	0.8μm	100Hz	0.98μVrms (57dB)	4.6	N/A
[58]	1.5μm	700Hz	3.6μVrms (45.7dB)	4.9	N/A
This work	0.35μm	200Hz	0.7μVrms (60dB)	4.1	61
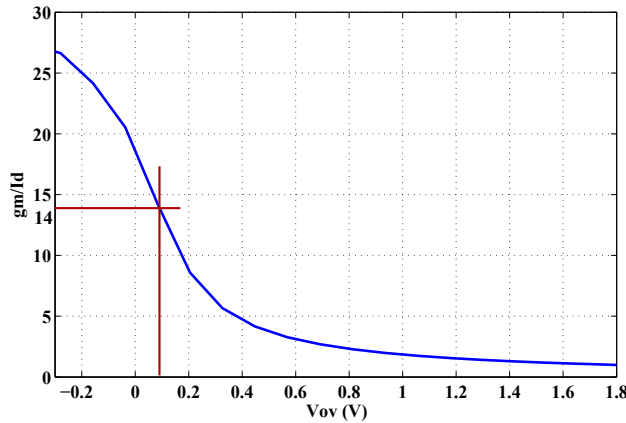
Figure 5.8: $\frac{g_{\mathrm{m}}}{I_{\mathrm{d}}}$ of the input transistor

Fig. 5.11 plots the effect of process variation will have on the transfer function of the amplifier. The transfer function of the amplifier is plotted for 3 types of process models available in I3T25 technology -

- typical

- AWCP - Absolute Worst Case Power or lowest possible threshold voltage. It is denoted as fast in the plot.
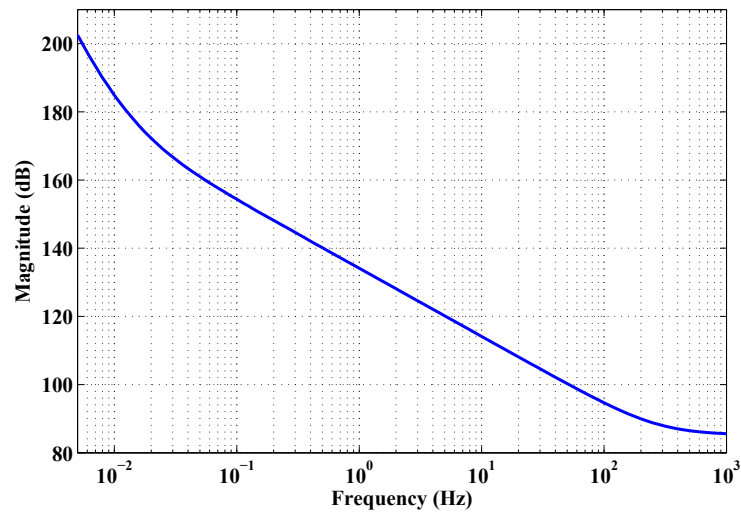
Figure 5.9: PSRR vs frequency of the amplifier
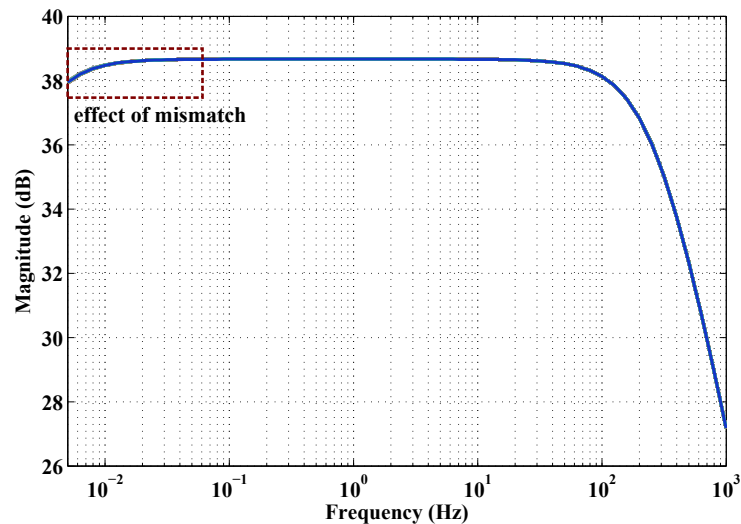
Figure 5.10: Effect of mismatch between components on the amplifier transfer function

- AWCS - Absolute Worst Case Speed or highest possible threshold voltage. It is denoted as slow in the plot.

The change in transconductance due to process variations will lead to a change in f_{hpf} and f_{lpf}. f_{lpf} varies from 160Hz to 230Hz in the extreme cases as compared to a typical case which is acceptable. Variation of f_{hpf} is also not of significance as it is out of the signal band of interest.

However, process variation does have a significant effect on the response of the modulator. Here too, 'fast', 'typ' and 'slow' have the same meaning as stated above. Fig. 5.12 plots the output of the modulator for $f_{in} = 82.1$Hz. In the 'slow' case, the
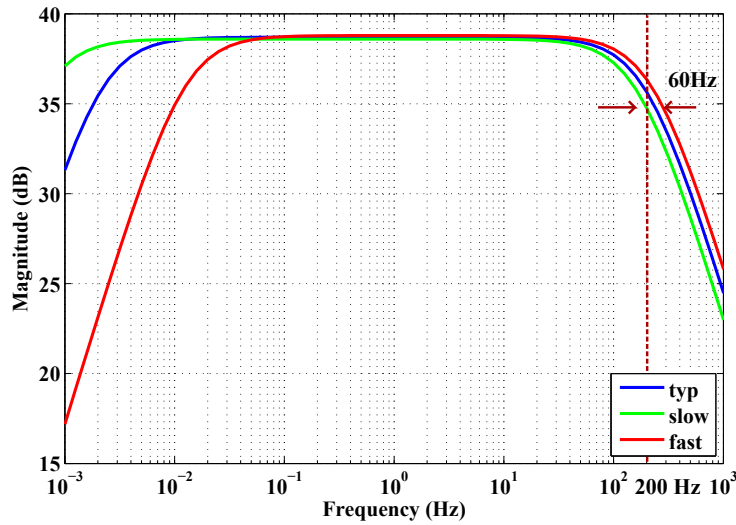
Figure 5.11: Effect of process variations on the amplifier transfer function
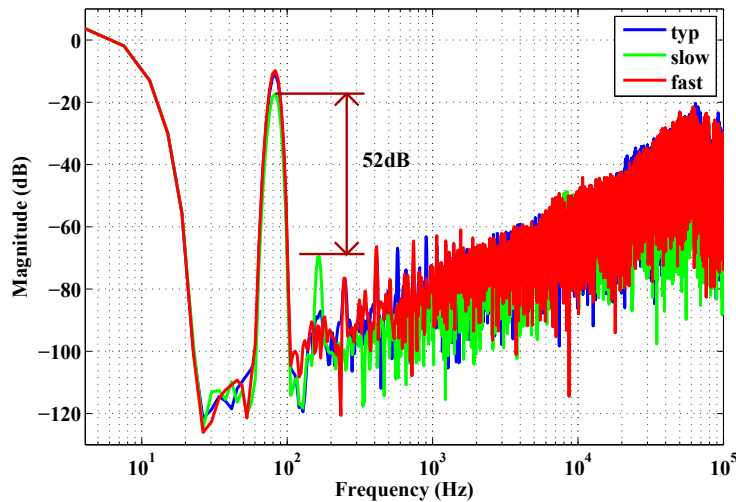
Figure 5.12: Effect of process variation on the Modulator for $f_{in} = 82.1$Hz

transconductance of the g_m-stage decreases and hence the main signal component has a lower magnitude. The 2nd-order distortion visibly increases in both the slow case as compared to the typical case and the SNR drops to 52dB. Fig. 5.13 plots the output of the modulator for $f_{in} = 1.1$Hz. Similar to the previous case, the distortion increases.

Since it is the 2nd-order distortion is increasing especially for $f_{in} = 82.1$Hz, it must be due to the fact that the effect of charge kick-back from the comparator is no longer canceled out as in the 'typ' case. Adding a pre-amplifier prior to the comparator will make the modulator design more robust. For $f_{in}=1.1$Hz, an increase in transconductance will lead to an increase in V_{fb} and effect of charge-injection and thus also lead to an increase the 2nd-order distortion.

Figure 5.13: Effect of process variation on the Modulator for $f_{\text{in}} = 1.1\text{Hz}$

Fig. 5.14 and Fig. 5.15 plot the transfer function of the amplifier and the total integrated noise of the instrumentation amplifier for the temperature range -40°C to 85°C respectively. Similar to the response of the amplifier to the process variation, the gain in the signal band is not affected. f_{lpf} varies about 60Hz over this temperature range, which is acceptable. f_{lpf} varies greatly but is outside the signal band of interest and hence, too, not significant. However, the variation of the high-pass cut-off frequency has an effect on the input-referred noise. As the temperature increases, the small-signal resistance offered by the pseudo-resistors will decrease and hence f_{hpf} will increase. When $f_{\text{hpf}} > 50\text{mHz}$, the gain at 50mHz will start decreasing which leads to an increase in the input-referred noise. Another reason for increase in the input-referred noise is that $g_{\text{m1,2}}$ will decrease with increase in temperature (as mobility decreases) as shown in Fig. 5.16. Hence this too will contribute to an increase in the input-referred noise.

Fig. 5.17 and Fig. 5.18 plot the effect of temperature variation on the output of the modulator for $f_{\text{in}} = 82.1\text{Hz}$, 1.1Hz respectively. Although, the distortion once again increases visibly for both the input frequencies, the effect of temperature is not as severe as that of process variation. The 10-bit requirement is still satisfied for the complete temperature range.

5.5 System Area

Table 5.3 gives a component-wise break-up of the area consumed and its corresponding percentage-wise break-up is given in Fig. 5.19. The capacitors use the majority of the area. Capacitors aside, the instrumentation amplifier uses up most of the area. This is due to the fact that to reduce the flicker noise, extremely huge transistors have to be used.
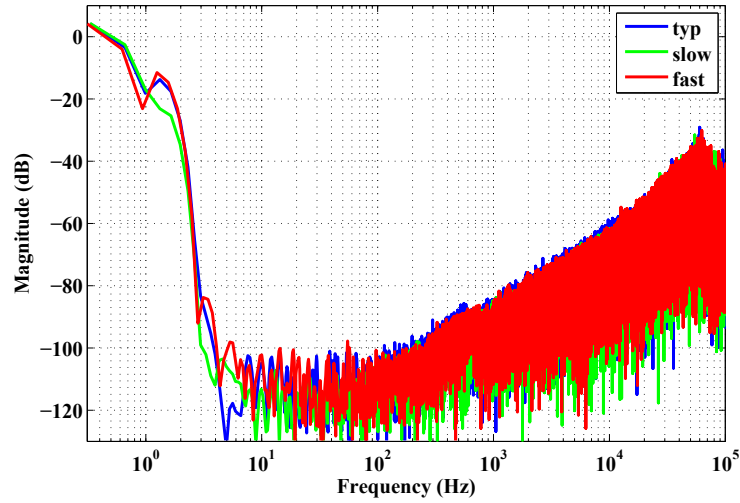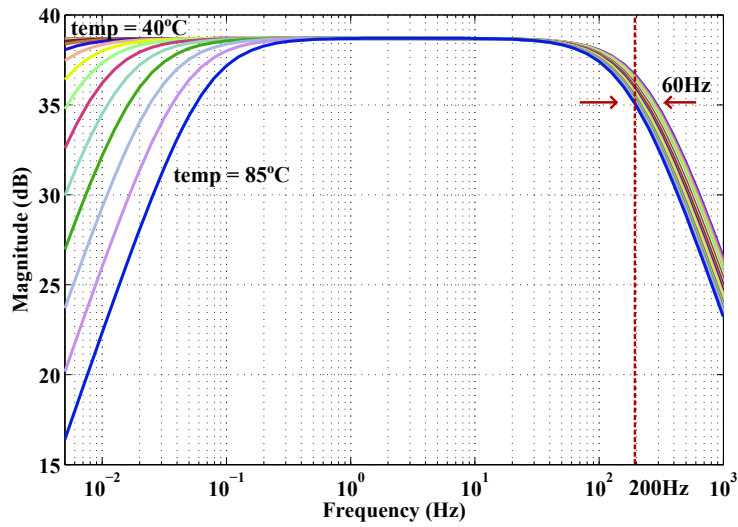
Figure 5.14: Effect of temperature on the amplifier transfer function
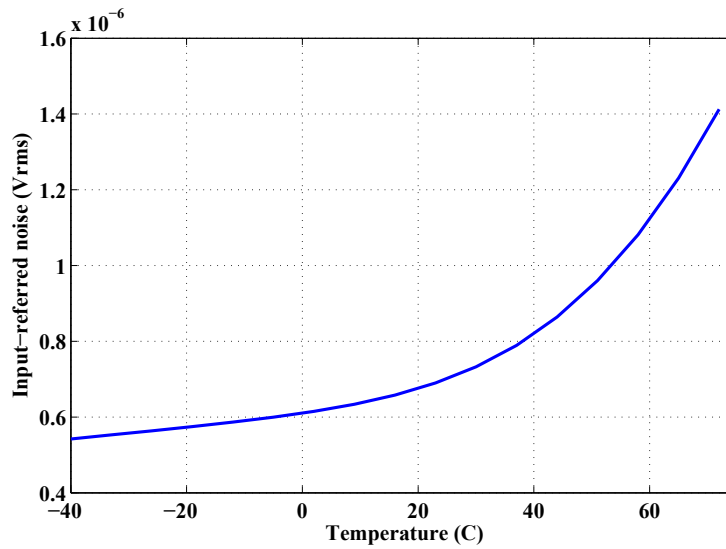
Figure 5.15: Effect of temperature on the integrated input-referred noise

Table 5.3: Block-wise break-up of area

Block	Area (mm^2)
Amplifier	0.028
g_m	0.000795
DAC	$0.7 \cdot 10^{-6}$
Comparator	$24.5 \cdot 10^{-6}$
Charge-pump	$21 \cdot 10^{-6}$
Buffers	$17.5 \cdot 10^{-6}$
Total Cap (175pF)	0.12
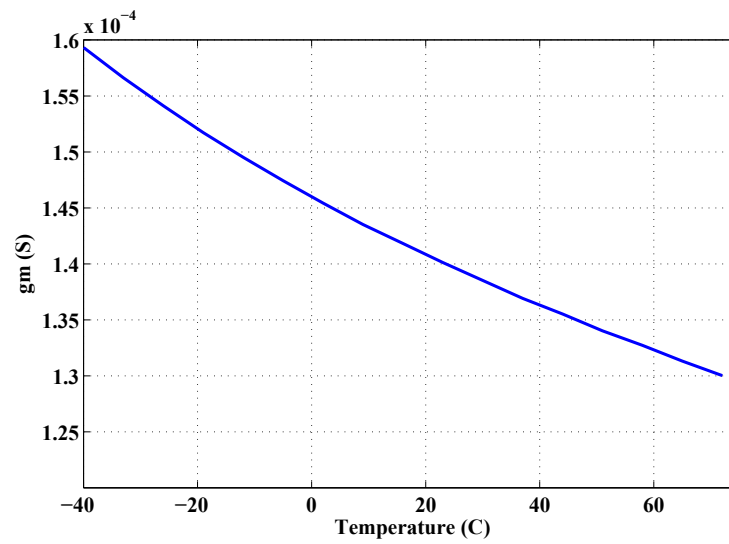
Figure 5.16: Effect of temperature on $g_{\mathrm{m}1,2}$
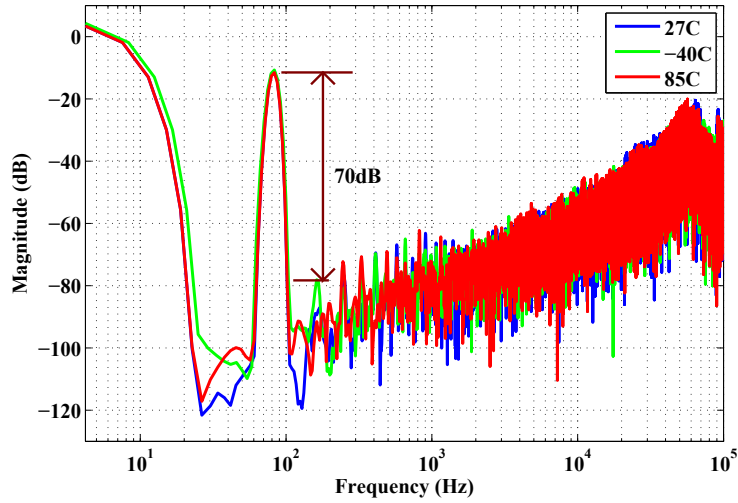
Figure 5.17: Effect of temperature on modulator output for $f_{\text{in}} = 82.1\text{Hz}$
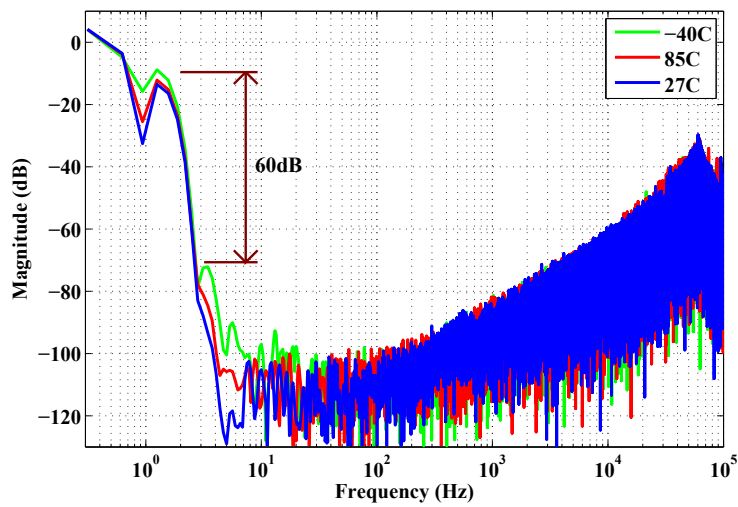
Figure 5.18: Effect of temperature on modulator output for $f_{\text{in}} = 1.1\text{Hz}$
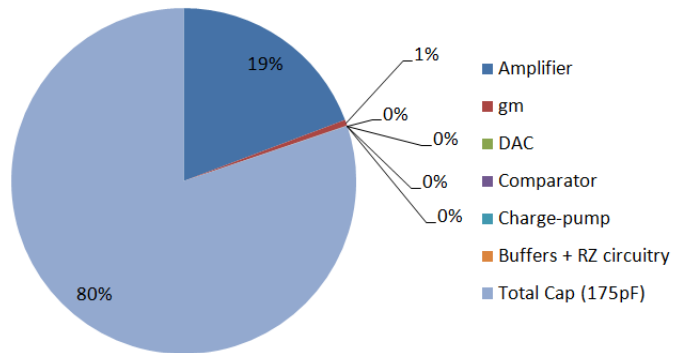
Figure 5.19: Block-wise break-up of area

Conclusion and Recommendation for Future Work

6

6.1 Conclusion and original scientific contribution

ECG devices or medical devices in general, require an instrumentation amplifier with a high CMRR to suppress common-mode noise due to coupling from power-line source. The specification for CMRR of the amplifier is usually the bottleneck for these designs. With increasing need for portable/implantable devices, there is a need to implement the whole ECG system on chip. This gives rise to another challenge i.e. integration of time-constants of the order of a few seconds required for meeting the signal bandwidth 1Hz-200Hz. Usually a 3-electrode or a 12-electrode system is used for ECG diagnosis. These devices also require that the number of electrodes needed for read-out of a signal be minimum i.e. two. Certain applications such as AMI can be diagnosed by detecting very small variation in signal amplitude and hence a 10-bit resolution is required.

This thesis deals with the design of a fully integrated analog front-end solution that meets the bandwidth and resolution requirements specifically for a portable 2-electrode device. It makes the following scientific contributions

- Effect of possible interference sources on the read-out of ECG signal has been studied. It has been shown that for a portable/integrated ECG system, a high CMRR is obtained from the fact that the coupling capacitance of the device is much smaller than that of the human-body. Hence, CMRR of the instrumentation amplifier is not required to be high as opposed to conventional front-end designs.

- The fact that CMRR of the amplifier was not a concern, a single differential-amplifier is sufficient instead of a 3-opamp instrumentation amplifier. Furthermore, this amplifier has been biased with a tail voltage source instead of tail-current source. This leads to a simpler biasing circuitry.

- To implement the high-pass cut-off frequency, a novel mixed-signal feedback technique using a sigma-delta ADC has been presented. This technique proposes feeding back a scaled and low-pass filtered comparator output to the previous analog stage.

- Small-signal stability of the presented technique was analysed and the system was shown to be unconditionally stable. This technique was also compared to other existing analog and mixed-signal feedback techniques. These existing methods are non-linear for frequencies near cut-off and give unpredictable time-constants. The advantages of the proposed technique include achieving a higher linearity

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Table 6.1: Resulting specification of the designed system

Parameters	Specification	Achieved
Input Amplitude	1mV	
Bandwidth	1Hz-200Hz	1Hz-200Hz
SNR	60dB	60dB
Distortion	~60dB (10-bit accuracy)	>10-bit accuracy for f>1Hz, ~10 bits accuracy for f~1Hz
Supply Voltage	3V	3V
Power consumption	less than 50μW	67μW
Input Impedance	>10MΩ	>10MΩ
CMRR	>60dB	>80dB
Process Technology	0.35μm I3T25 technology	0.35μm I3T25 technology

with simple analog components (such as 1-bit DAC and a charge-pump) and with negligible power consumption.

- To implement the low-pass cut-off frequency, an indirect feedback technique has been employed such that the noise specification of 60dB SNR is met while keeping the load capacitance of the order of a few tens of pFs.

- A first-order sigma-delta ADC with an oversampling ratio of 512 has been designed to meet the target 10-bit resolution. The main challenge in the design of the sigma-delta ADC had been reducing the effect of charge kick-back.

Table 6.1 lists down the results of the designed system vis-a-vis the required specifications listed in Table 1.2. The results show an improvement over the existing designs in the following areas

- A linearity of 10 bits has been obtained at frequencies close to the high-pass cut-off frequency by the proposed technique. This is an improvement of 20dB or $\approx$3 bits of resolution over pseudo-resistors, a widely-used method to implement large time-constants on-chip.

- A gain of 100, 61º of phase-margin, 60dB of SNR and an NEF (Noise-Efficiency Factor) of 4.1 for the instrumentation amplifier has been achieved. This is the highest reported SNR and phase margin and the 3rd lowest NEF.

6.2 Recommendation for Future Work

Based on the results presented in chapter 5, the following recommendations can be made to increase the robustness, linearity and performance specifications of the design -

Circuit-level

- Implement an active-RC integrator instead of a g_mC integrator for the sigma-delta implementation. This will lead to an improvement in linearity at the expense of power. Since the instrumentation amplifier consumes around 90% of the power, this should not be a major drawback. Moreover, an active-RC integrator will also be more robust to process corner.

- Implement a differential charge-pump architecture. This should cancel the effect of charge-injection and thus increase the allowable V_fb voltage swing. Thus, such an approach will improve linearity by decreasing 2nd order harmonics and also improve robustness to process corners.

- Incorporate tunability of frequency and gain into the design.

Block-level

- Implement a pre-amplifier before the comparator to reduce the effect of charge kick-back at all process corners.

- Investigate advantage of using a separate g_m-stage for the signal and the mixed-signal feedback. The required voltage swing of V_fb can be reduced by using a higher-g_m structure and thus improve linearity. This will be at the expense of increased power. However, mismatch between the two g_m-stages might also lead to distortion.

- Investigate feeding back V_fb to the input of the instrumentation amplifier instead of to the gm-stage. This also will reduce its voltage swing and thus improve linearity. However, the noise of the charge-pump and the 1-bit DAC in the feedback will appear directly at the input and thus decrease the SNR. Area of the transistors in these blocks will have to be considerably increased so as to minimize the dominant flicker noise. Thus there a trade-off will have to be made between area and linearity.

- Implement the digital decimation filter for the sigma-delta architecture.

Architecture/System-level

- Investigate use of chopping-technique to meet the required noise specification. This will lead to use of smaller capacitors and smaller transistors to decrease the area used at the expense of power consumption.

- Implement a higher-order sigma-delta modulator as first-order sigma-delta continuous-time modulators are generally not designed for most applications. This would not only decrease the required oversampling ratio but also decrease the required scaling coefficient. This might lead to a decrease in the effect of charge-injection and thus improve linearity.

- Investigate the advantages and challenges of feeding back the digital signal to the input of the instrumentation amplifier instead of the transconductance stage.

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