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Fully Integrated CMOS Fractional-N Frequency Divider for Wide-Band Mobile Applications With Spurs Reduction

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***Abstract*—A spurs reduction fractional-N frequency divider with a frequency range which is 3.5 times larger than that of a conventional fractional-N divider is presented in this paper. A 1.2-GHz quadrature voltage-controlled oscillator (VCO) is designed as the input source of the frequency divider. The circuit was fabricated using the 0.25-μm CMOS technology. The power consumption of the frequency divider and the quadrature VCO are 3 and 6 mW, respectively, at a 2-V supply.**

***Index Terms*—CMOS oscillator, quadrature oscillator, fractional-N and frequency synthesizer.**

I. Introduction

THE FRACTIONAL-N frequency divider has become increasingly popular in RF applications as it allows phase-locked loop (PLL) synthesizers to have a frequency resolution finer than the reference frequency. However, there are two main disadvantages in a fractional-N divider, namely, fractional spurs generation and frequency range limitation. Fractional spurs are generated due to the fixed pattern of the dual-modulus divider [1] and the frequency range of a fractional-N divider is equal to its reference frequency. This limits its usefulness especially in wide-band applications.

A dual-band PLL synthesizer for personal communications services (PCS) and cellular code division multiple access (CDMA) systems is demonstrated in [1]. This circuit uses a charge-averaging charge pump to solve the fractional spurs problem. However, this approach is only suitable for a small number of division ratios as it is limited by the complexity of the charge pump. As the frequency range of a dual-modulus fractional-N frequency synthesizer is equal to the reference frequency, e.g., 19.8 MHz as in [1], the operating band may not be fully covered.

This paper describes a new technique for reducing the fractional spurs while providing a wide frequency-coverage. The width of the maximum phase error's pulse [2] in the new design is a quarter of that of the conventional fractional-N divider. This is achieved through the introduction of a new division ratio $(N+1/4)$ in the divider. This frequency divider has a frequency range of 3.5 times larger than that of the conventional fractional-N divider, as its division modulus ranges from $(N-1.75)$ to $(N+1.75)$ while a conventional fractional-N divider has only a division modulus of N to $(N+1)$. This technique also reduces the magnitude of the fractional spurs to one quarter of the usual value.

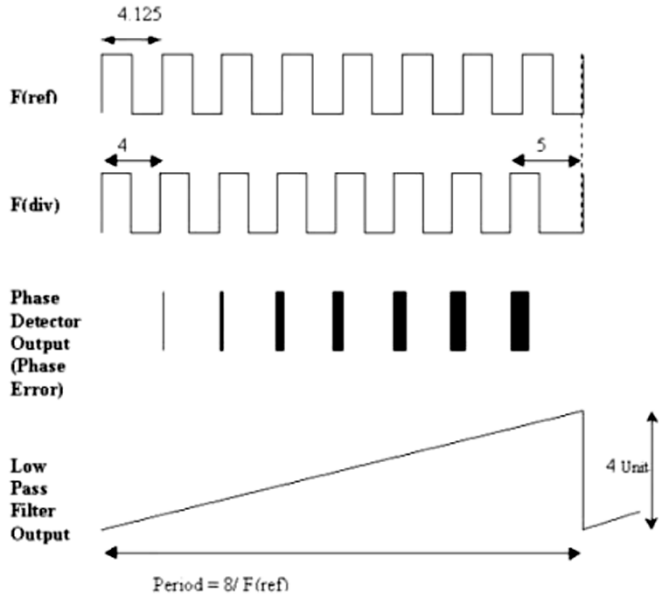

Fig. 1. Effect of unequal instantaneous frequencies.

In the modern transceiver design, quadrature voltage-controlled oscillator (VCO) is often needed to generate the quadrature signals for the local oscillator's inputs of either image-reject mixers [9] or frequency down converters with I/Q outputs. For multiple standard applications, the VCO needs to have a wide tuning range in order to cover the entire range of operation frequency. The quadrature VCO reported in [4] and [5] has a wide tuning range of 18.5% and 24%, respectively. The results show that the quadrature VCO is a good candidate for multiple standard applications. As the quadrature VCO is becoming more popular in modern communication systems [3]–[7], these quadrature outputs are used in this new frequency synthesizer.

II. Frequency Divider Topology

In a fractional-N frequency divider, a dual-modulus divider, divide-by-$(N/N+1)$ is used. The fractional division is obtained by periodically changing the division ratio. To achieve a divide-by-4.125 operation, seven divide-by-4 operations followed by one divide-by-5 operation are required. As shown in Fig. 1, each of the first seven cycles of the divided signal is slightly

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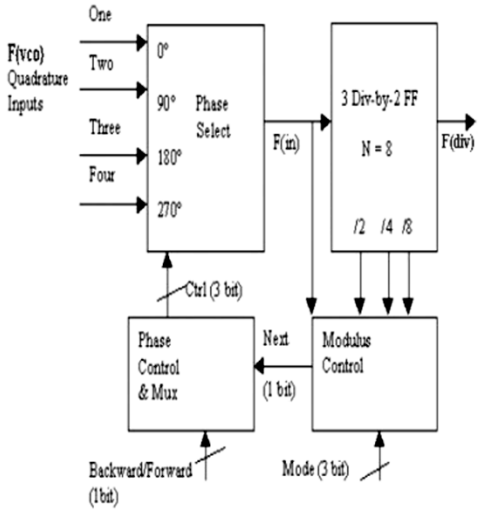

Fig. 2. Fractional-N frequency divider wit a divide-by-$(N + 1/4)$ operation.

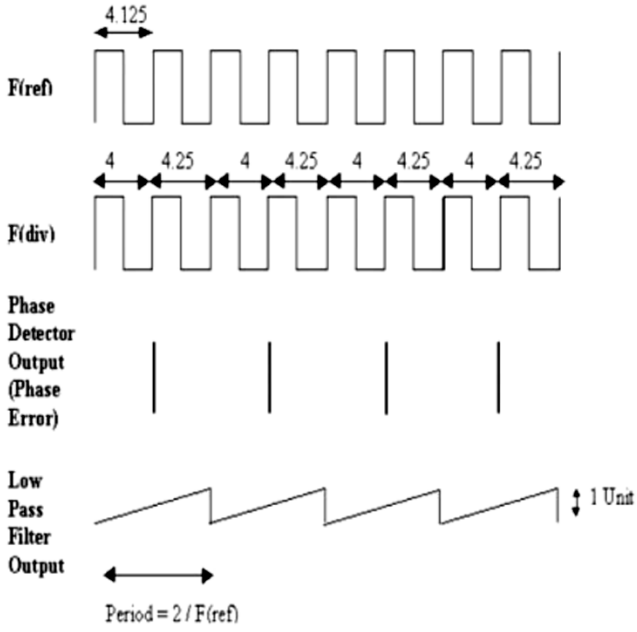

Fig. 3. Effect of the implementation of a divide-by-$(N + 1/4)$ operation.

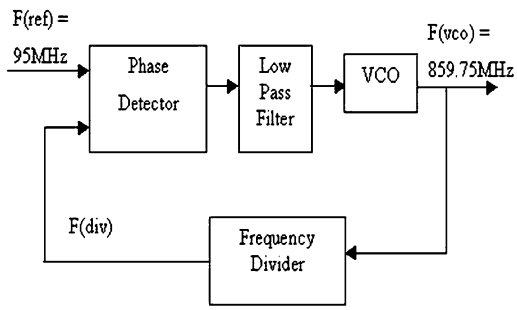

Fig. 4. Block diagram of the behavioral-level simulation setup of a PLL frequency synthesizer using conventional frequency divider and novel frequency divider.

shorter than the reference period. Consequently, the phase error between the reference and the feedback signal grows in every period of $F(\mathrm{ref})$ till it returns to zero when the divide-by-5 operation occurs. Thus, the phase detector produces progressively wider error pulses, creating a ramp at the filter output of the PLL.

Here, it can be concluded that if the VCO output is to be equal to $(N + \alpha)F(\mathrm{ref})$, (e.g., $\alpha = 1/8$ and $N = 4$ in Fig. 1), the output of the low-pass filter (LPF) will be a repetitive ramp waveform with a period of $1/(\alpha F(\mathrm{ref}))$. If the loop is closed, such a waveform would modulate the VCO, creating sidebands at $\alpha F(\mathrm{ref})$, $2\alpha F(\mathrm{ref})$, etc. with respect to the center frequency. Such sidebands are called fractional spurs. For example, for $\alpha = 1/8$, the output of the LPF will be a periodic ramp waveform with a period of$8/F(\mathrm{ref})$, creating sidebands at $0.125F(\mathrm{ref})$, and $0.25F(\mathrm{ref})$, etc. with respect to the center frequency.

The new fractional-N frequency divider with $(N+1/4)$ modulus is shown in Fig. 2. The operation of the $(N+1/4)$ division fractional-N frequency divider will be discussed in Section IV. The inputs of the frequency divider F(vco) are from a quadrature VCO. With inputs from the quadrature VCO, a new division ratio of $(N + 1/4)$ can be achieved, as the phase difference between the consecutive outputs of the quadrature VCO is 90°. The new divider reduces the generation of fractional spurs by the introduction of the new division ratio of $(N + 1/4)$.

In Fig. 3, to achieve a divide-by-4.125 operation, one divide-by-4 operation is made for each one divide-by-4.25 operation, so the total time for one correct comparison is $2/F(\mathrm{ref})$. This effectively reduces the period of the periodic ramp at the output of the LPF from $8/F(\mathrm{ref})$ to $2/F(\mathrm{ref})$. Thus, the sidebands created now are at $0.5F(\mathrm{ref})$, $F(\mathrm{ref})$, etc., with respect to the center frequency, which are four times the distance as in the case of a conventional divider. The magnitude of the sidebands is now a quarter of the magnitude of that in the conventional divider as shown in Fig. 1. The reason is that the time to accumulate the charge at the output of the LPF is now a quarter of that of a conventional divider.

To further illustrate the effect of the new division ratio, simulations to achieve the division ratio of 9.05 were done for a PLL frequency synthesizer as shown in Fig. 4. Fig. 4 shows the block diagram of the behavioral-level simulation setup of a PLL frequency synthesizer using conventional frequency divider and novel frequency divider. The output frequency $F(\mathrm{vco})$ and the reference frequency $F(\mathrm{ref})$ of the PLL frequency were 859.75 and 95 MHz, respectively.

In order to achieve a division ratio of 9.05, for the conventional frequency divider, 19 divide-by-9 operations are needed before one divide-by-10 operation. For the new frequency divider, 4 divide-by-9 operations are required before one divide-by-9.25 operation. In Fig. 5, it is observed that the fractional spurs of the new fractional divider are much smaller than those of the conventional divider and four times further from the carrier as compared to those of the conventional divider.

III. Circuit Description

A. Modulus Control

Fig. 6 shows the modulus control circuitry. The 3-bit division modulus control word, Mode, determines the division modulus by generating 1, 2, or 4 pulses depending on the settings of the control bits Mode1, Mode2, and Mode3. For example, when Mode is 100, where Mode3 is high, while Mode1 and Mode2

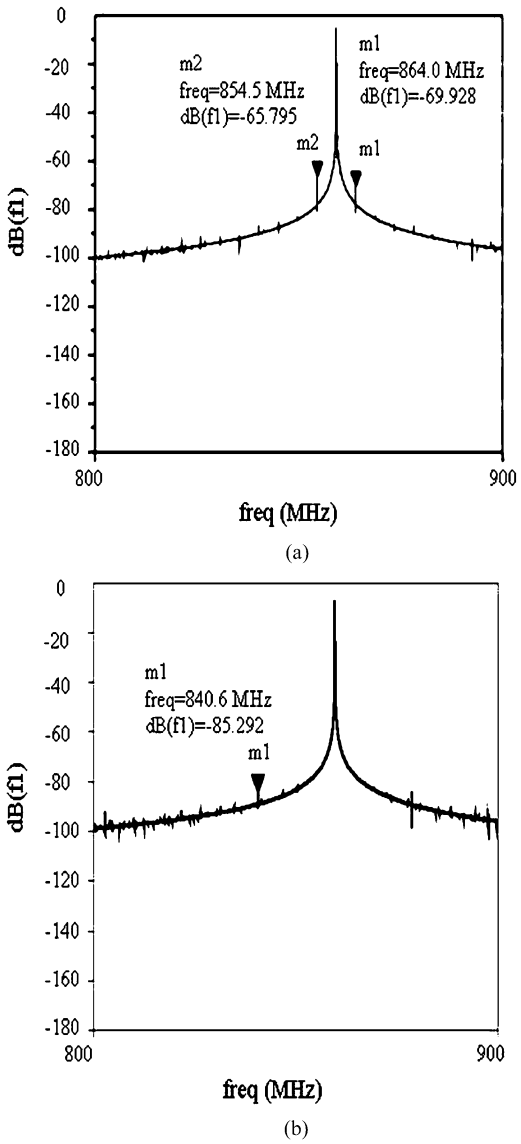

Fig. 5. Output spectrums of a PLL frequency synthesizer using (a) conventional frequency divider and (b) e new frequency divider.

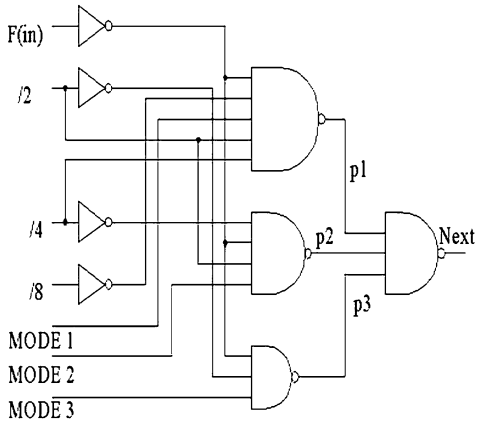

Fig. 6. Modulus control circuitry.

are low, four pulses will be generated at the output Next [8]. The inputs $F(\mathrm{in})/2, /4$, and $/8$ correspond to the output of the phase select circuitry and the outputs of the three divide-by-2 flip-flops, respectively, as shown in Fig. 2.

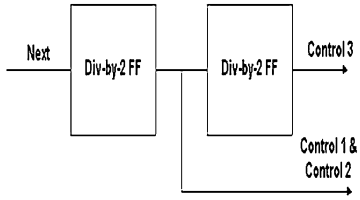

Fig. 7. Phase control circuitry.

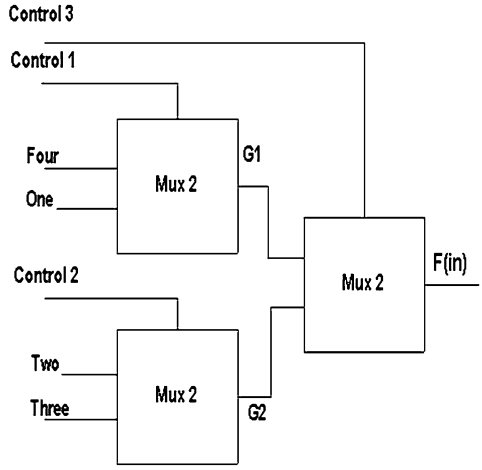

Fig. 8. Phase select circuitry.

B. Phase Control Circuitry

The phase control circuitry is needed to convert the signal next generated from the modulus control circuitry to the 3-bit control signal in the phase select circuitry. The 3-bit control signal Ctrl is generated by two divide-by-2 flip-flops as shown in Fig. 7.

C. Phase Select

A phase select circuitry is needed to switch the inputs from One to Two, Two to Three, Three to Four, and then back from Four to One, whenever the Ctrl signal changes. The multiplexer in the phase select circuitry is implemented using pass transistors as shown in Fig. 8. In this design, Control 1 and Control 2 are the same signal, so they can be combined into one single bit. When Ctrl is equal to 10 (Control 3 Control 1/2), the output of the phase select circuitry $F(\mathrm{in})$ is connected to One. If Ctrl is 01, $F(\mathrm{in})$ is connected to Two. If Ctrl is 00, $F(\mathrm{in})$ is connected to Three. Lastly, when Ctrl is 11, $F(\mathrm{in})$ is connected to Four.

Fig. 9 shows the timing diagram of the phase select circuitry operation, where T is the period of the input VCO frequency $F(\mathrm{vco})$, square wave input signals are used for better illustration purpose. For control $3 = 0$, when Control 2 changes from 1 to 0, $F(\mathrm{in})$ which previously connected to Two now is switched to Three. With each switching of the input signal, for example, Two to Three, Three to Four, an extra 0.25 T is added to the output period $F(\mathrm{in})$.

When Control 2 changes from 1 to 0, Two can be deselected before Three is low enough. This causes a small spike in the $F(\mathrm{in})$ as shown in Fig. 9. If the control signal Control 2 has a

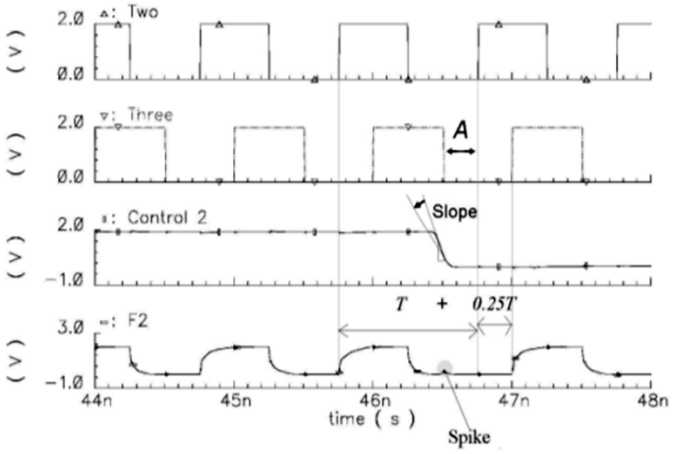

Fig. 9. Timing diagram of the phase select circuitry operation.

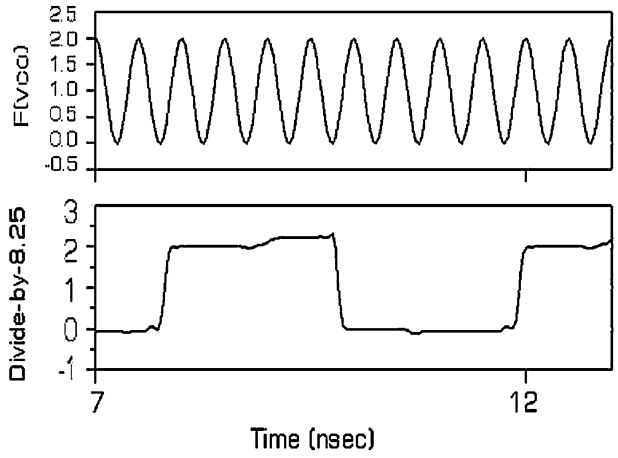

Fig. 10. Divide-by-8.25 operation at 2 GHz.

very steep slope, this will cause large spike to occur, which will jeopardize the proper operation of the circuit. Thus, the steepness of the control signals slope has to be reduced to minimize the spike. In order to reduce the steepness of the slope, a small buffer with a large rise time and fall time can be used to drive the control signals. Another possible solution to prevent the generation of the spike is to provide delay to the control signal. As shown in Fig. 9, if the transition from 1 to 0 of the signal Control 2 is delayed such that it falls into the time region denoted by ***A***, then no spike will be generated. The delay can be implemented using buffer. However, in order to guarantee the proper operation of the circuit, simulation has to be done for all possible transistor process variations and operating temperatures.

IV. Circuit Operation

For forward propagation division, the new divider operates as follows. As shown in Fig. 2, the input signals namely, One, Two, Three, and Four, are fed to the phase select circuitry. When the 3-bit signal Mode is 000, the phase control block is disabled and its output signal $F(\mathrm{in})$ is not changed. This means that the output of the multiplexer will be taken from the same input as the previous clock. Hence, $F(\mathrm{div})$ is eight times smaller than the input frequency $F(\mathrm{in})$ due to the three divide-by-2 flip-flops.

Depending on the required modulus, the control signal Ctrlwill change in such a way that the division control block will connect $F(\mathrm{in})$ to the signal that is 90° phase shifted with respect to the present signal, e.g., from 0° to 90° or 90° to 180°. For example, for a division of 8.25, Mode is equal to 001. Hence, one pulse will be generated at Next. If $F(\mathrm{in})$ is initially connected to One, after Ctrl changes, a connection will be made to Two. Hence, a division of 8.25 is achieved as shown in Fig. 10, where the input frequency in this simulation is 2 GHz.

In this design, all the division modulus from 8 to 9.75 for $N = 8$ can be achieved. In Fig. 11, a divide-by-9.75 operation was simulated at 1 GHz. In order to achieve a divide-by-9.75 operation, Mode must be set to 111. Thus, seven pulses will be generated at Next. When $F(\mathrm{in})$ is initially connected to One, after Ctrl changes, a connection will be made to Two. As there are seven pulses, Ctrl will change seven times in one divide-by-9.75

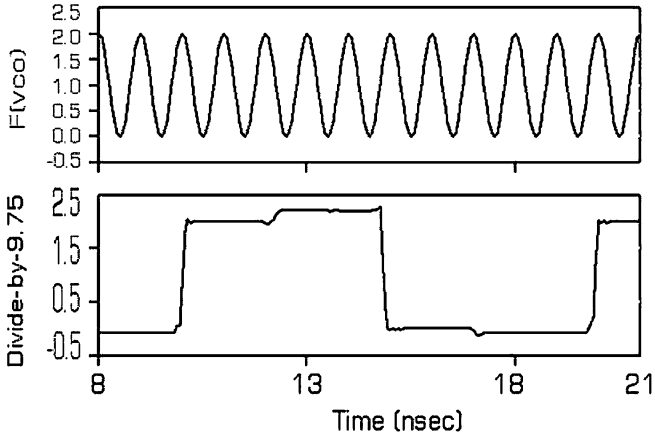

Fig. 11. Divide-by-9.75 operation at 1 GHz.

TABLE I
Forward and Backward Sequences of Phase Select Circuitry

Input	Control 3	Control 1 and 2	Forward	Backward
1st Input of 1st Mux	1	1	Four	One
2nd Input of 1st Mux	1	0	One	Four
1st Input of 2nd Mux	0	1	Two	Three
2nd Input of 2nd Mux	0	0	Three	Two

operation period. In each sequence, $F(\mathrm{ref})$ will consecutively connect to One, Two, Three, Four, then go back to One, Two, Three, and lastly to Four.

The backward propagate division is implemented by using the sequences of the forward and backward propagation of the phase select circuitry as shown in Table I. Essentially, for backward propagation, both the signals for Control 1 and 2 are inverted. Hence, the range of the division ratio for the frequency divider is increased by two times, which ranges from $(N - 1.75) = 6.25$ to $(N + 1.75) = 9.75$ for $N = 8$.

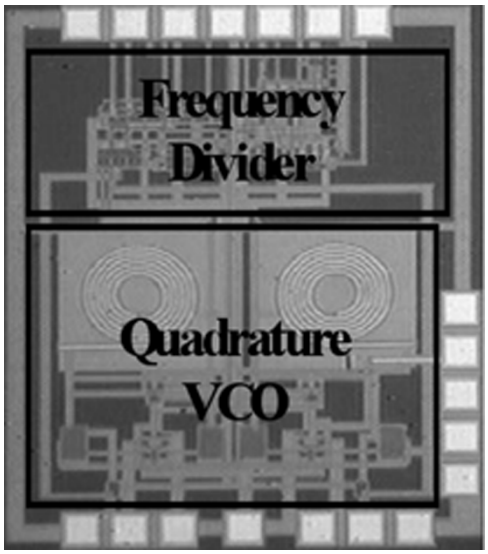

Fig. 12. Microphotograph of the frequency divider and the 1.2-GHz quadrature VCO.

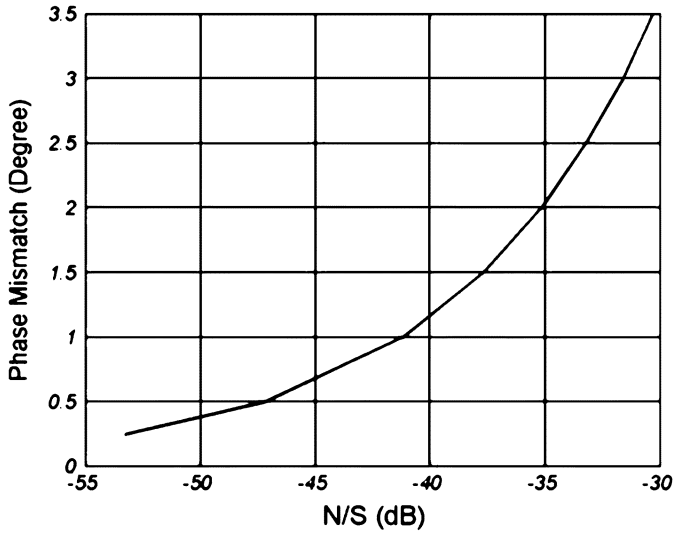

Fig. 13. Phase mismatch versus noise-to-signal ratio.

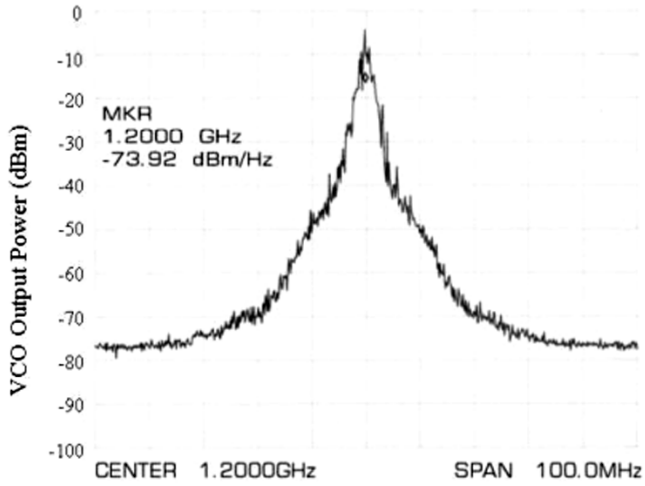

Fig. 14. Power spectrum of the VCO output at 1.2 GHz.

V. Experimental Results and Conclusion

The frequency divider in Fig. 2 was designed and fabricated using the CMOS 0.25-μm process. A 1.2-GHz frequency quadrature VCO was designed to generate the quadrature signals into the frequency divider. The quadrature VCO was designed using the parasitic-compensated quadrature VCO technique [10]. The active chip area is 1200 μm $\times$ 1600 μm. The frequency divider and the quadrature VCO consume 3 and 6 mW, respectively, at 2-V supply. Fig. 12 shows a microphotograph of the frequency divider with the quadrature VCO.

An important consideration in the design of this frequency divider is the accuracy of the quadrature signals, or more specifically the phase mismatches between the in-phase and the quadrature phase. The relationship between the amplitude and phase mismatches with the noise-to-signal ratio is given by [11]

$$\frac{N}{S} = \frac{A + \frac{1}{A} - 2\cos(\Delta\Phi)}{A + \frac{1}{A} + 2\cos(\Delta\Phi)} \tag{1}$$

where A and $\Delta\Phi$ are given by

$$A = \frac{A_I}{A_Q} \tag{2}$$

$$\Delta\Phi = \Phi_I - \Phi_Q \tag{3}$$

where A_I and A_Q are amplitudes of I (in-phase) and Q (quadrature) signals, respectively, and Φ_I and Φ_Q are phases of the I and Q signals in degree. As A_I and A_Q do not directly cause spurious tones generation, A_I and A_Q are considered to be the same. Using (1), the phase mismatch (in degree) versus noise to signal ratio (in decibles) was plotted.

It is common for an *LC* quadrature VCO to achieve quadrature phase mismatch of less than 1° [3]. The measured quadrature phase mismatch of the VCO is smaller than 0.5° at 1.2-GHz carrier frequency. The small quadrature phase mismatch of this frequency divider is achieved through symmetrical layout using common centroid technique [12].

In order to see the effect of the phase mismatch on the frequency divider, this frequency divider is used in a frequency synthesizer with 28-MHz reference frequency, and the fractional dividing ratio α is set to 1/8. From Fig. 13, a spurious tone of at least $-$ 47 dBc/Hz is expected to appear at 3.5 MHz (28 MHz/8) offset from the carrier frequency. It is obvious that it is important to have a quadrature phase mismatch as small as possible. Further improvement on the quadrature phase matching can be achieved through calibration technique such as proposed in [13].

Fig. 14 shows the power spectrum of the VCO output at 1.2 GHz. A divide-by-9.75 operation is implemented through forward propagation of the phase select circuitry, which results in an output frequency of 1.2 GHz/9.75=123.1 MHz. Fig. 15 shows the power spectrum of the divider output at 123.1 MHz. This frequency coincides for a divide-by-9.75 operation with a 1.2-GHz input signal, which shows the feasibility of $(N+1/4)$ division. With the $(N + 1/4)$ division, the generation of the fractional spurs in a fractional-N frequency divider will be reduced.

A divide-by-7.75 operation is implemented through backward propagation of the phase select circuitry, which results in an output frequency of 1.2 GHz/7.75=154.8 MHz. Fig. 16

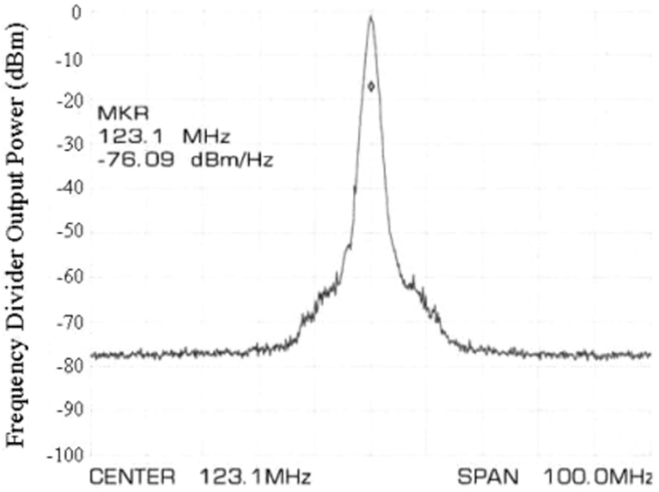

Fig. 15. Power spectrum of the frequency divider output at 123.1 MHz.

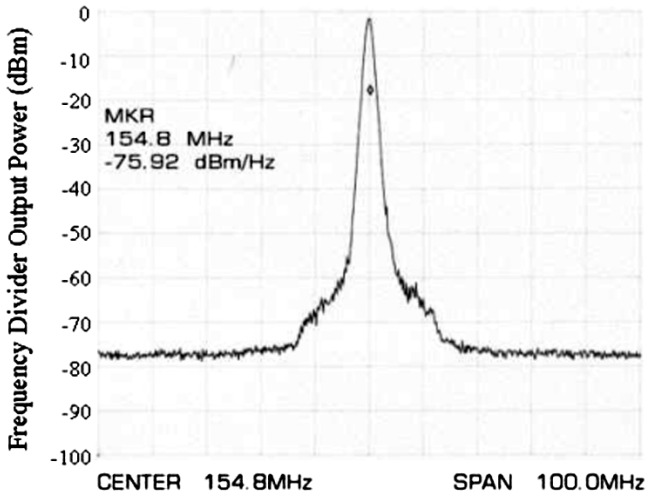

Fig. 16. Power spectrum of the frequency divider output at 154.8 MHz.

shows the power spectrum of the divider output at 154.8 MHz. This frequency coincides for a divide-by-7.75 operation with a 1.2-GHz input signal, thus proof the feasibility of the backward propagation technique. Using the backward propagation technique, the range of the division ratio for the frequency divider is increased by two times.

A new multiple modulus fractional-N frequency divider was presented. This frequency divider provides a new division of $(N + 1/4)$, which reduces the generation of fractional spurs. In addition, it has a large range of multiple modulus division from $(N - 1.75)$ to $(N + 1.75)$, as shown in the above example it ranges from 6.25 to 9.75 for $N = 8$. This will enable the frequency divider to support multiple standard applications for fixed and mobile radios that operate over a wide range of frequency.

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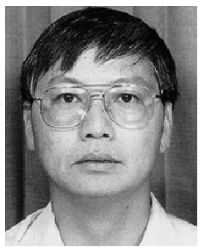

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