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Citation	Chen, Xiangyu et al. "Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics." IEEE Transactions on Electron Devices 57.11 (2010): 3137-3143. © Copyright 2010 IEEE
As Published	http://dx.doi.org/10.1109/TED.2010.2069562
Publisher	Institute of Electrical and Electronics Engineers (IEEE)
Version	Final published version
Citable link	http://hdl.handle.net/1721.1/72125
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Fully Integrated Graphene and Carbon Nanotube Interconnects for Gigahertz High-Speed CMOS Electronics

Xiangyu Chen, *Student Member, IEEE*, Deji Akinwande, *Member, IEEE*, Kyeong-Jae Lee, *Student Member, IEEE*, Gael F. Close, *Member, IEEE*, Shinichi Yasuda, *Member, IEEE*, Bipul C. Paul, *Senior Member, IEEE*, Shinobu Fujita, Jing Kong, and H.-S. Philip Wong, *Fellow, IEEE*

Abstract—Carbon-based nanomaterials such as metallic single-walled carbon nanotubes, multiwalled carbon nanotubes (MWCNTs), and graphene have been considered as some of the most promising candidates for future interconnect technology because of their high current-carrying capacity and conductivity in the nanoscale, and immunity to electromigration, which has been a great challenge for scaling down the traditional copper interconnects. Therefore, studies on the performance and optimization of carbon-based interconnects working in a realistic operational environment are needed in order to advance the technology beyond the exploratory discovery phase. In this paper, we present the first demonstration of graphene interconnects monolithically integrated with industry-standard complementary metal–oxide–semiconductor technology, as well as the first experimental results that compare the performance of high-speed on-chip graphene and MWCNT interconnects. The graphene interconnects operate up to 1.3-GHz frequency, which is a speed that is commensurate with the fastest high-speed processor chips today. A low-swing signaling technique has been applied to improve the speed of carbon interconnects up to 30%.

Index Terms—Carbon nanotubes, graphene, high speed, interconnect, on-chip.

I. INTRODUCTION

INTERCONNECT wires have always been one of the major technology components of modern high-speed integrated

Manuscript received April 4, 2010; revised July 9, 2010; accepted July 30, 2010. Date of publication September 16, 2010; date of current version November 5, 2010. This work was supported in part by Toshiba Corporation. The work of D. Akinwande was supported in part by the Stanford DARE Fellowship, by the Ford Foundation, and the Alfred P. Sloan Foundation Graduate Fellowships. The review of this paper was arranged by Editor M. A. Reed.

X. Chen and H.-S. Philip Wong are with the Center of Integrated Systems, Stanford University, Stanford, CA 94305 USA (e-mail: hspwong@stanford.edu).

D. Akinwande was with the Center of Integrated Systems, Stanford University, Stanford, CA 94305 USA. He is now with the University of Texas at Austin, Austin, TX 78712 USA.

K.-J. Lee and J. Kong are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

G. F. Close was with the Center of Integrated Systems, Stanford University, Stanford, CA 94305 USA. He is now with the Zurich Research Laboratory, IBM Research, 8803 Rüschlikon, Switzerland.

S. Yasuda and S. Fujita are with Toshiba Corporation, Kawasaki 210-8520, Japan.

B. C. Paul is with Toshiba America Research, San Jose, CA 95131 USA.

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Digital Object Identifier 10.1109/TED.2010.2069562

circuits (ICs). In the most advanced IC technology, the capacitance associated with interconnects typically accounts for about 50% of the active processor power consumption [1], and the associated signal delay along interconnects is one of the main bottlenecks for the routing of high-speed signals. With the progressive miniaturization of semiconductor devices, the need for longer, thinner, and faster interconnects with lower power consumption is becoming more pronounced. Conventional interconnect materials such as copper are facing great challenges to satisfy requirements when physical dimensions are scaled down to the nanoscale range. First, the conductance of copper significantly decreases when the lateral dimension is scaled down: the resistivity of local interconnects is increased by about 50% when wire pitch decreased from 100 to 50 nm due to increased electron scattering at the grain boundaries and wire surfaces [2], which increases the circuit signal delay; equally important is that the reliability of copper wires suffers when the current density increases due to the miniaturization. Increased wire resistivity leads to increased Joule heating and degraded electromigration lifetime, which result in decreased maximum allowed current density in copper wires [2]–[4]. Therefore, alternative interconnect materials are being actively researched to improve on-chip interconnect performance [5].

In recent years, graphene has gained a lot of attention for being a promising new material for high-speed electronics [6]–[9], since it not only shares the same outstanding transport properties as carbon nanotubes [10]–[13], such as high mean free path and high current-carrying capacity but also offers potential advantages such as simpler fabrication process, better material control, and better reproducibility [14]. Researchers have demonstrated graphene transistors with intrinsic cutoff frequency as high as 100 GHz [7], graphene nanomechanical resonators operating at 50–80 MHz [8], and microwave switches operating at gigahertz (GHz) range [9]. When used as interconnects, graphene also showed a great potential: previous theoretical calculations have shown that the conductivity of metallic graphene nanoribbons (GNR) would outperform copper wires with unity aspect ratio when interconnect width is scaled down below 8 nm [15]. The theory also predicts that high-quality doped GNRs offer smaller signal delay than copper at the 11-nm technology node when used as global wires [16]. DC experimental characterizations showed that the resistivity of good-quality GNRs in the width range from 18

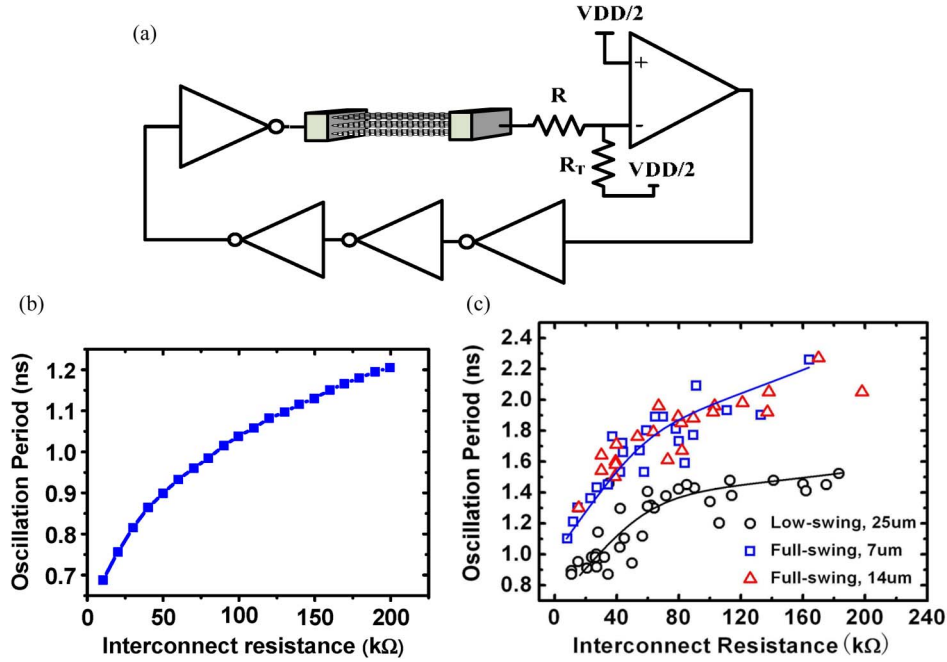


Fig. 1. Application of low-swing oscillator circuitry for interconnect performance improvement. (a) Circuit diagram of a five-stage low-swing ring oscillator with a differential amplifier at the receiver end of the inverter chain. The line is terminated by a termination resistor ($R_T = 20$ kΩ, $R \sim 0.5R_T$ is a value determined by the tradeoff between speed improvement brought by low-swing signaling and the sensitivity of the differential amplifier at the receiving end) to a midsupply voltage; hence, the signal swing at the receiver end is reduced to $V_{DD} \times R/R_T$, whereas the speed is increased by a factor R/R_T . (b) Modeling results of signal delay along 30- μ m-long MWCNT interconnects integrated with a low-swing oscillator circuit. The signal delay increases with increasing MWCNT resistance, as expected. For a good-quality MWCNT (lower resistivity), signal delay as low as 0.7 ns can be expected. (c) Experimental performance comparison of MWCNT interconnects integrated on both full- and low-swing circuits. We can see that, even with an increased length, the MWCNT interconnect integrated with a low-swing circuit still shows a significant signal delay improvement of about 30% at the same resistance value. (Symbols) Experimental data. (Solid lines) Visual guides.

to 50 nm is smaller than $10 \mu\Omega \cdot \text{cm}$, which is comparable with copper wires with the same physical dimensions [17]. Furthermore, GNRs have breakdown current density on the order of 10^8 A/cm², which is ten times higher than the maximum permissible current density of copper [18]. However, despite the favorable theoretical and dc characterization results of graphene interconnects, experimental demonstration of high-speed signaling using graphene interconnects has not yet been made, and there is no report of integration of graphene with standard CMOS technology, which is a key requirement for future integrated graphene electronics. We address these topics by presenting the first experimental demonstration of high-speed graphene interconnects integrated with a five-stage standard CMOS low-swing ring oscillator circuit operating above 1 GHz, which is a major milestone for graphene electronics.

II. LOW-SWING CIRCUITRY

The CMOS five-stage ring oscillator circuit is fabricated using standard 0.25- μ m CMOS technology.¹ Each ring oscillator is designed with a missing interconnect wire onto which a graphene interconnect wire was subsequently integrated. Only one graphene interconnect is integrated with each ring oscillator, so that we can characterize each graphene interconnect individually while maintaining the high oscillation speed. A low-swing signaling technique is implemented for the ring

oscillator circuit to serve as a method to investigate the high-frequency performance of interconnects. A lower input-signal swing shortens the time needed to charge up the load capacitance, thereby improving the ring oscillator speed substantially. Since the main focus of this paper is interconnect performance, the possible extra chip area and power cost of introduction of a low-swing receiver is not discussed here but has been previously studied elsewhere [19]. Fig. 1(a) shows the ring oscillator circuit diagram. The differential amplifier at the receiving end provides higher signal sensitivity than a simple inverter stage. Simulation shows that the signal delay of 30- μ m-long multiwalled carbon nanotube (MWCNT) interconnects (diameter ~ 30 nm and resistivity $\sim 650 \mu\Omega \cdot \text{cm}$) in this low-swing ring oscillator loop can be on the order of 100 ps [see Fig. 1(b)].

To demonstrate the speed improvement brought by the improved ring oscillator circuit design, we integrated, using dielectrophoresis, the same kind of MWCNT interconnects onto both the low-swing CMOS ring oscillators and the standard full-swing CMOS oscillators. The fabrication process was detailed in [20]. The experimental characterization result shows a significant 30% average speed improvement for the same wire resistance [see Fig. 1(c)].

III. GRAPHENE INTERCONNECT DEVICE FABRICATION

The process flows of graphene growth/transfer and post-CMOS fabrication are shown in Fig. 2. First, large-area multilayered graphene (average thickness of about 15–20 nm,

¹The 0.25- μ m ring oscillator CMOS platforms were fabricated by Taiwan Semiconductor Manufacturing Company.

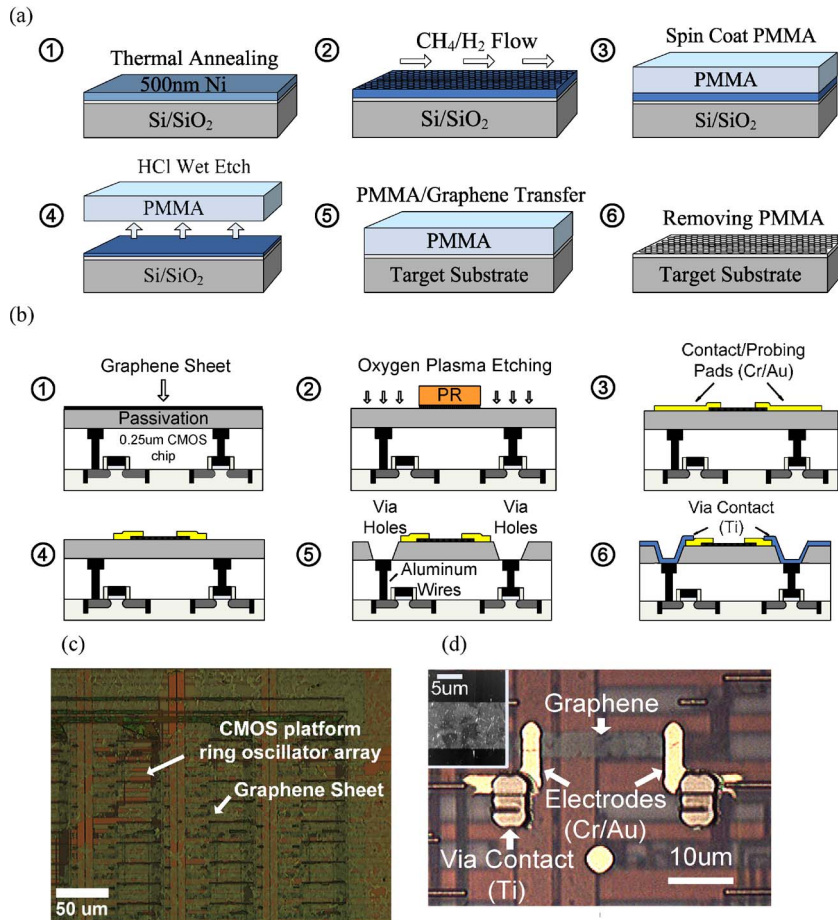


Fig. 2. Device fabrication process flows and images of as-fabricated on-chip graphene interconnects. (a) Process flow of CVD graphene growth and PMMA-assisted transferring. (b) Process flow of the posttransfer fabrication process for integrating graphene with underneath CMOS circuitry. (c) Optical image of graphene after being transferred on top of the CMOS ring oscillator array. (d) Optical image of one fabricated graphene interconnect on top of the CMOS ring oscillator array. The lines that appear black in the middle of Ti via contacts are M3 Al lines. (Inset) AFM image of graphene stripes on the SiO₂/Si test substrate.

which is measured using atomic force microscopy) is grown using chemical vapor deposition (CVD) on a 500-nm electron-beam-evaporated nickel layer and then transferred to a 5 mm × 5 mm CMOS chip with the low-swing circuitry as previously described. The CVD growth is carried out for 5 min at 1000 °C, with 5 sccm of methane and 1300 sccm of hydrogen [21]. After the growth is completed, a thin layer of polymethyl methacrylate (PMMA) is spin coated on top of the graphene/nickel substrate, and a 10% HCl aqueous solution is used to lift off the PMMA-graphene layer from the underneath nickel layer. Then, the PMMA-graphene film is placed on the target substrate, and the PMMA is subsequently washed off using acetone. An average sheet resistance of about 700 Ω/sq is extracted for graphene before post-CMOS processing by transferring graphene on top of the Si/SiO₂ substrate. In principle, this method is scalable to transferring arbitrary large areas of graphene from arbitrary substrates to CMOS substrates. For this reason, it is an attractive option for integrating wafer-scale graphene with wafer-scale CMOS substrates to facilitate very large scale integrated (VLSI) graphene/Si electronics.

After the graphene transfer, all processing steps are done using standard CMOS-compatible fabrication techniques. First, graphene is patterned into stripes of different widths/lengths

using optical lithography and oxygen plasma etching. The interconnect width ranges from 3 to 5 μm, whereas the length ranges from 5 to 145 μm. Cr/Au electrodes are deposited as contacts to graphene. Then, via holes are formed by etching through the passivation layer, reaching down to the topmost metal layer of the CMOS chip. Finally, the via contacts between graphene interconnects and underlying CMOS circuitry are made by filling the via holes with Ti.

IV. CHARACTERIZATION RESULTS

To see whether the quality of this novel nanomaterial is significantly degraded by going through the standard CMOS fabrication process, we measured the sheet resistance of graphene before and after the standard CMOS fabrication process, Fig. 3(a) shows that the average sheet resistance of graphene remains to be 700 Ω/sq on average, which indicates that the quality of graphene is generally preserved during device fabrication. The *I*-*V* characteristics of the fabricated graphene interconnect in Fig. 3(a) indicate that we have achieved an ohmic contact between graphene and metal. At the same time, the linear *I*-*V* curves show that the contact between graphene and metal is ohmic. Contact resistance is negligible compared with

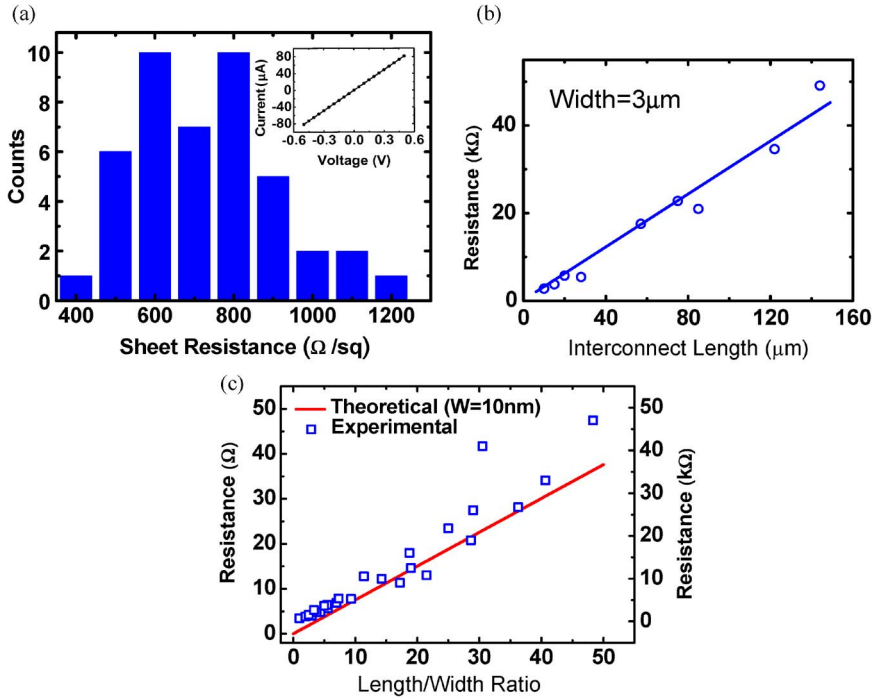


Fig. 3. DC characterization results for graphene interconnects. (a) Sheet resistance distribution. The average sheet resistance is $R_s \sim 711 \Omega/\text{sq}$. The wide distribution was due to variation in the number of layers and surface defects. (Inset) I - V curve of a graphene interconnect showing an ohmic contact ($L/W = 28 \mu\text{m}/3 \mu\text{m}$, $R = 6.15 \text{ k}\Omega$). (b) Interconnect resistance as a function of length, indicating diffusive transport. The intercept on the y -axis gives the contact resistance between graphene and metal. It is negligible compared with the interconnect resistance. (c) Comparison between theoretical and experimental results for interconnect conductance for the same length/width ratio. (Experimental results are obtained using interconnects with varied widths.) Theoretical results are derived using the model proposed in [16].

interconnect resistance [see Fig. 3(b)]. Theoretical conductance calculation is done based on the multilayer graphene conductivity model proposed in [16] using the material mean free path derived from our sheet resistivity data. Comparison with experimental measurement is shown in Fig. 3(c). To demonstrate the high-speed signal routing capability of graphene interconnects, we characterized the ring oscillator frequencies and amplitudes by wire bonding the postprocessed CMOS chip to a pin grid array package and mounting the package into a printed circuit board for high-frequency electrical testing [see Fig. 4(a)]. Gigahertz oscillation frequency is observed for ring oscillators with graphene interconnects as long as $80 \mu\text{m}$, which confirms the great potential of graphene for future VLSI interconnects. The oscillation frequency of the ring oscillator circuit is determined by the total circuit RC delay as in (1) (f is the circuit oscillation frequency, R is the total resistance of the circuit dominated by graphene interconnect resistance, C_{tot} is the total capacitance of the circuit, ρ_s is the sheet resistivity of graphene, L is the interconnect length, and W is the interconnect width), which agrees with our experimental characterization results shown in Fig. 4(b) and (c): the circuit oscillation frequency is directly correlated with the interconnect width and inversely correlated with the length/width ratio. Thus

$$f \propto \frac{1}{RC_{\text{tot}}} \propto \frac{1}{\rho_s \left(\frac{L}{W}\right) \cdot C_{\text{tot}}} \quad (1)$$

By integrating graphene and the MWCNT with the same type of low-swing CMOS ring oscillator, we directly compared the RF performances of the two materials. Fig. 4(d) shows that graphene offers a higher oscillation frequency because of its lower resistivity, and the ring oscillator with best performance graphene wire has an oscillation frequency that is comparable with the reference oscillators with aluminum wire. However, at the same resistance value, the MWCNT has better signal delay performance. This may be due to the larger total capacitance associated with our wide graphene stripes: using the Predicative Technology Model [22], the wire-to-ground electrostatic capacitance for a $1\text{-}\mu\text{m}$ -wide graphene wire is around $0.118 \text{ fF}/\mu\text{m}$ (dielectric thickness = 500 nm), whereas a 30-nm -wide MWCNT wire has capacitance around $0.0345 \text{ fF}/\mu\text{m}$. When graphene is scaled down to similar physical dimensions as the MWCNTs (width $\sim 30 \text{ nm}$), the estimated single graphene wire electrostatic capacitance is about $0.01 \text{ fF}/\mu\text{m}$, similar to that of the MWCNT wire estimated using the 1-D transmission line model [23]. However, while scaling down the width of graphene decreases the interconnect capacitance, it brings other issues like increased contact resistance and increased wire resistivity due to limited material quality and edge roughness. Although study has shown that it is possible to fabricate chirality-controlled graphitic nanoribbons [24] and that optimizing contact figuration can help achieve an ohmic contact between GNRs and metal, more research needs to be done to make high-frequency operation of GNR interconnects practical.

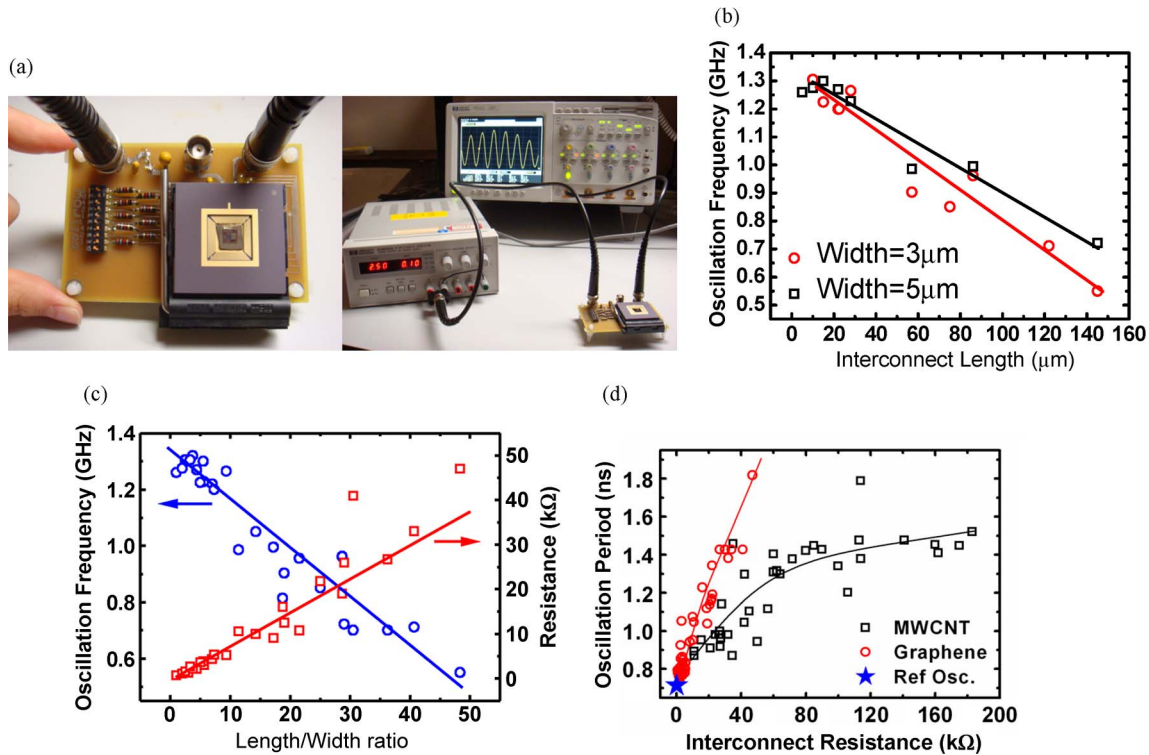


Fig. 4. RF characterization of graphene on-chip interconnects. (a) Printed circuit board and setup for RF measurements. (b) Oscillation frequency for various interconnect lengths and widths. Gigahertz range operation frequency is observed for interconnects up to $\sim 80 \mu\text{m}$ long. (c) Oscillation frequency and resistance as functions of L/W ratio indicative of the number of squares. (Symbols) Experimental data. (Bold lines) Visual guides. (d) Oscillation period as a function of interconnect resistance for the CMOS reference interconnects (aluminum), MWCNTs, and graphene. For the same ring oscillator circuit, graphene offers higher speed operation compared with MWCNTs. However, at the same resistance values, MWCNT interconnects are faster most likely due to their smaller capacitance. (Symbols) Experimental data. (Bold lines) Visual guides.

V. CONCLUSION

In summary, we have successfully demonstrated the first integration of graphene interconnects with standard CMOS technology. Gigahertz operation frequency is observed for graphene interconnects as long as $80 \mu\text{m}$. By using the low-swing signaling technique, wire signal delay performance is further improved by about 30%. Along with recent reports on large-scale [25] transfer-free [26] low-temperature [27] graphene synthesis techniques, the future of graphene interconnects in VLSI technology appears increasingly promising, although advances in the controlled synthesis of continuous sheets of graphene and understanding of graphene interconnect performance limits require further research.

ACKNOWLEDGMENT

X. Chen, G. F. Close, K. J. Lee, J. Kong, and H.-S. P. Wong would like to thank Interconnect Focus Center, which is one of the Semiconductor Research Corporation/DARPA Focus Centers, for the support. Part of the work in this paper was performed at the Stanford Nanofabrication Facility.

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Deji Akinwande (M'98) received the B.S. and M.S. degrees in electrical engineering and applied physics from Case Western Reserve University, Cleveland, OH, and the Ph.D. degree in electrical engineering from Stanford University, Stanford, CA, where he conducted research on the experimental synthesis, device physics, and circuit applications of carbon nanotubes and graphene. His Master's research involved the design, development, and characterization of evanescent microwave probes for nondestructive imaging of materials.

He is currently an Assistant Professor with the University of Texas, Austin. He is a co-inventor of a high-frequency bondwire interconnect.

Prof. Akinwande was the recipient of the "2005 Stanford Cheesy Award" for outstanding LNA design and the Ford Foundation, Alfred P. Sloan Foundation, and Stanford future-faculty DARE Fellowships.



Kyeong-Jae Lee (S'05) received the B.S. degree in computer engineering from the University of Virginia, Charlottesville, VA, in 2005 and the S.M. degree in electrical engineering and computer science, in 2007, from Massachusetts Institute of Technology, Cambridge, where he is currently working toward the Ph.D. degree in the Department of Electrical Engineering and Computer Science.

From June 2007 to August 2007, he was with the Microprocessor Technology Laboratory, Intel Corporation, Hillsboro, OR, measuring high-frequency properties of carbon nanotube devices. His research interests include the development of integrated systems for CMOS and emerging technologies, such as carbon nanotubes and graphene devices.

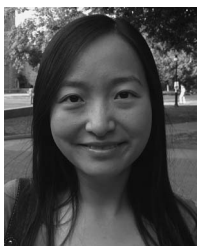
Mr. Lee was a corecipient of the 2008 DAC/ISSCC Student Design Contest Award.



Gael F. Close (M'03) received the B.Sc. (Eng.) degree in 2003 from the University of Liege, Liege, Belgium, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 2004 and 2008, respectively, all in electrical engineering.

In 2008, he joined the Zurich Research Laboratory, IBM Research, Rüschlikon, Switzerland, where he is currently a Research Staff Member. His research interests include the development of prototype semiconductor memory chips exploiting new technology.

Dr. Close was the recipient of a Belgian American Educational Foundation Fellowship during 2003–2004 for his study in the United States and the 2006–2007 Intel Graduate Foundation Fellowship to support his doctoral research at Stanford.

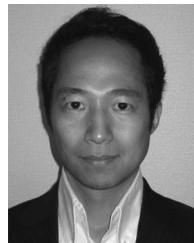


Xiangyu (Helen) Chen (S'09) received the B.S. degree in physics from Nanjing University, Nanjing, China, in 2007. She is currently working toward the Ph.D. degree in physics in Prof. H.-S. P. Wong's group in the Center of Integrated Systems, Stanford University, Stanford, CA.

From June to September 2010, she worked on mobility study of 110-channel MOSFETs and device characterization for 20-nm low-power technology development in the 20-nm bulk device team at IBM East Fishkill. Her research interests include device

physics, fabrication and applications of carbon nanotubes, graphene transistors, and carbon interconnects, and transport physics at the interface of carbon nanomaterial and metals.

Ms. Chen was the recipient of the Stanford Graduate Fellowship for year 2010–2012.



Shinichi Yasuda (M'04) received the B.S. degree in applied physics and the M.S. degree in advanced materials science from the University of Tokyo, Tokyo, Japan, in 1999 and 2001, respectively.

He joined the Research and Development Center, Toshiba Corporation, Kawasaki, Japan, in 2001. He has been engaged in the research of circuit and system technology with silicon nanoscale devices and emerging devices.



Bipul C. Paul (S'97–M'01–SM'05) received the B.Tech. and M.Tech. degrees in radiophysics and electronics from the University of Calcutta, Calcutta, India, and the Ph.D. degree from Indian Institute of Science (IISc), Bangalore, India.

He is currently a Senior Research Scientist with Toshiba America Research, San Jose, CA. Earlier, he was with Alliance Semiconductor (India), where he worked on synchronous DRAM design. From 2000 to 2005, he was with Purdue University, West Lafayette, IN, as a Postdoctoral Research Associate,

where he developed several device models and statistical design techniques for nanoscale circuits and memory. He has also developed several device and circuit optimization techniques for ultralow-power digital subthreshold operation. In 2005, he joined Toshiba America Research. He is also a Visiting Scientist with Stanford University, Stanford, CA. He is currently in the Editorial Board of the *ACM Journal of Emerging Technology and Computing*, *IEEE Computers and Digital Techniques*, and *Journal of Low Power Electronics*. He also served as Guest Editor for *IEEE Computers and Digital Techniques* on a Special Issue entitled "Advances in Nanoelectronics Circuits and Systems" in 2009. He has published more than 70 technical papers in international journals and conference proceedings. He is the holder of five U.S. patents (pending). His research interests include device and circuit design for emerging nanotechnology, statistical design for yield and reliability (NBTI), 3D nanoarchitecture, ROM-based design for high-performance logic, and ultralow-power design.

Dr. Paul received National scholarship (India) in 1984, the Senior Research Fellowship Award from CSIR (Government of India) in 1995, the Best Thesis of the Year Award in 1999, and the IEEE Circuits and Systems Society VLSI Transactions Best Paper Award in 2006. He has served in the technical program committees of several international conferences, including DATE, IOLTS, GLSVLSI, and TTEP.

Shinobu Fujita, photograph and biography not available at the time of publication.



Jing Kong received the B.S. degree from Peking University, Beijing, China, in 1997 and the Ph.D. degree from Stanford University, Stanford, CA, in 2002, both in chemistry.

In 2004, she joined Massachusetts Institute of Technology, Cambridge, where she is currently an Associate Professor with the Department of Electrical Engineering and Computer Science. She has worked in the field of carbon nanotubes for more than ten years and has published numerous papers on this subject. She and her colleagues at Stanford

were among the first to develop the chemical vapor deposition method for synthesizing individual single-walled carbon nanotubes, and they also initiated the research on carbon nanotube chemical sensors. The research activity in her current group involves controlled synthesis of carbon nanotubes and graphene, investigation of their electronic and optical properties, and integration with the CMOS circuits.



H.-S. Philip Wong (S'81–M'82–SM'95–F'01) received the B.Sc. (Hons.) degree from the University of Hong Kong, Pokfulam, Hong Kong, in 1982, the M.S. degree from the State University of New York at Stony Brook, Stony Brook, in 1983, and the Ph.D. degree from Lehigh University, Bethlehem, PA, in 1988, all in electrical engineering.

In 1988, he joined the IBM T. J. Watson Research Center, Yorktown Heights, NY. In September 2004, he joined the Center of Integrated Systems, Stanford University, Stanford, CA, as a Professor of electrical

engineering. While at IBM, he worked on CCD and CMOS image sensors, double-gate/multigate MOSFET, device simulations for advanced/novel MOSFET, strained silicon, wafer bonding, ultrathin-body SOI, extremely short gate FET, germanium MOSFET, carbon nanotube FET, and phase change memory. He held various positions from research staff member to manager, and senior manager. While he was Senior Manager, he had the responsibility of shaping and executing IBM's strategy on nanoscale science and technology, as well as exploratory silicon devices and semiconductor technology. His research interests include nanoscale science and technology; semiconductor technology; solid-state devices; electronic imaging; exploration of new materials, novel fabrication techniques, and novel device concepts for future nanoelectronics systems; and explorations into circuits and systems that are device driven. Novel devices often enable new concepts in circuit and system designs. His current research interests include carbon nanotubes, semiconductor nanowires, self-assembly, exploratory logic devices, nanoelectromechanical devices, novel memory devices, and biosensors.

From 2001 to 2006, he served on the IEEE Electron Devices Society as an elected AdCom member. He served on the IEDM committee from 1998 to 2007 and was the Technical Program Chair in 2006 and General Chair in 2007. He served on the ISSCC program committee from 1998 to 2004 and was the Chair of the Image Sensors, Displays, and MEMS subcommittee from 2003 to 2004. He serves on the Executive Committee of the Symposia of VLSI Technology and Circuits. He was the Editor-in-Chief for the *IEEE Transactions on Nanotechnology* during 2005–2006. He has been a Distinguished Lecturer of the IEEE Electron Devices Society (since 1999) and was a Distinguished Lecturer of the Solid-State Circuit Society (during 2005–2007).