Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System

Engin Ozdemir, *Senior Member, IEEE*, Sule Ozdemir, *Member, IEEE*, and Leon M. Tolbert, *Senior Member, IEEE*

***Abstract*—This paper presents a fundamental-frequency-modulated diode-clamped multilevel inverter (DCMLI) scheme for a three-phase stand-alone photovoltaic (PV) system. The system consists of five series-connected PV modules, a six-level DCMLI generating fundamental-modulation staircase three-phase output voltages, and a three-phase induction motor as the load. In order to validate the proposed concept, simulation studies and experimental measurements using a small-scale laboratory prototype are also presented. The results show the feasibility of the fundamental frequency switching application in three-phase stand-alone PV power systems.**

***Index Terms*—Fundamental switching, harmonic elimination, multilevel inverter, photovoltaic (PV) system.**

I. Introduction

SOLAR ENERGY is one of the favorable renewable energy resources, and the multilevel inverter has been proven to be one of the important enabling technologies in photovoltaic (PV) utilization. Multilevel voltage-source inverters offer several advantages compared with their conventional counterparts. By synthesizing the ac output terminal voltage from several levels of voltages, staircase waveforms can be produced, which approach the sinusoidal waveform with low harmonic distortion, thus reducing filter requirements. The need of several sources on the dc side of the converter makes multilevel technology attractive for PV applications [1]. While the multilevel inverter requires more components than conventional two-level inverters, lower voltage-rated devices can be used, and the multilevel inverter offers advantages such as the possibility of lower switching frequency (which leads to higher efficiency) and lower electromagnetic interference (EMI).

Several configurations and new trends of PV power conditioning systems, employing various static converter topologies, can be found in technical literature [2], [3]. Cascaded H-bridge multilevel inverter for PV power supply system is proposed in the papers for stand-alone and grid-connected operations [4]–[8]. However, H-bridge multilevel inverters require too many separate dc sources for each phase; hence, as an alternative, diode-clamped multilevel inverters (DCMLIs) share the same dc level for each of the three phases which decreases dc cabling and losses on the dc side. Most of the proposed recent power conversion units [9]–[11] for PV applications require dc–dc converter, conventional inverter, and/or transformer that increase the losses and reduce the efficiency of the whole PV power system. Some of the proposed single-phase topologies also require string inverters and multiple stages or complex algorithms for grid-connected operations [12]–[17]. Recent three-phase PV applications have used conventional inverter topologies and/or transformers [18], [19]. The Z-source inverter developed for split-phase residential PV applications may also have efficiency problems because of the losses in the inductors [20]. Issues such as reliability, high efficiency, small size and weight, and low price are of great importance to the conversion stage of the PV system.

A single-stage dc-to-ac multilevel inverter for three-phase stand-alone PV power supply system is presented in this paper. Diode-clamped type of multilevel inverter is also suitable for operation with multiple inputs such as different types of PV arrays, fuel cells, and wind turbines, as proposed in [21] and [22]. The objective is to develop a low-cost, reliable, and efficient PV power supply unit for three-phase domestic or industrial applications. A six-level diode DCMLI configuration using low-voltage MOSFETs as switching devices is used in the proposed topology. This configuration results in sinusoidal output voltages with step modulation and fundamental frequency switching. The proposed configuration and fundamental frequency modulation have reduced conduction and switching losses in the inverter and increase the system efficiency that is very important in PV applications. This design is not suitable for boosting the voltage, and thus, the system must be designed such that there is a high-enough voltage level at the input that voltage boosting is not required.

II. PV-Powered DCMLI

Several proposed arrangements of PV power systems have been made. Fig. 1 shows the proposed DCMLI for stand-alone PV power system configuration. The six-level DCMLI powered by five PV panels drives a three-phase induction motor. In actual implementation, several storage units (such as battery and ultracapacitor) would be in parallel with the PV panels in order to maintain energy storage capability for continuous operation of the PV system.

Manuscript received October 2, 2007; revised June 17, 2008. First published July 9, 2008; current version published October 9, 2009. The work of E. Ozdemir was supported by TUBITAK 2219 under a research grant.

E. Ozdemir and S. Ozdemir are with the Faculty of Technical Education, Kocaeli University, Kocaeli 41380, Turkey (e-mail: eozdemir@kocaeli.edu.tr; sozaslan@kocaeli.edu.tr).

L. M. Tolbert is with the Department of Electrical Engineering and Computer Science, University of Tennessee, Knoxville, TN 37996 USA, and also with Oak Ridge National Laboratory, Knoxville, TN 37932 USA (e-mail: tolbert@utk.edu).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIE.2008.928096

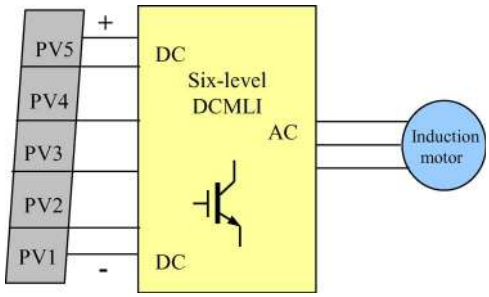


Fig. 1. DCMLI-based stand-alone PV power system configuration.

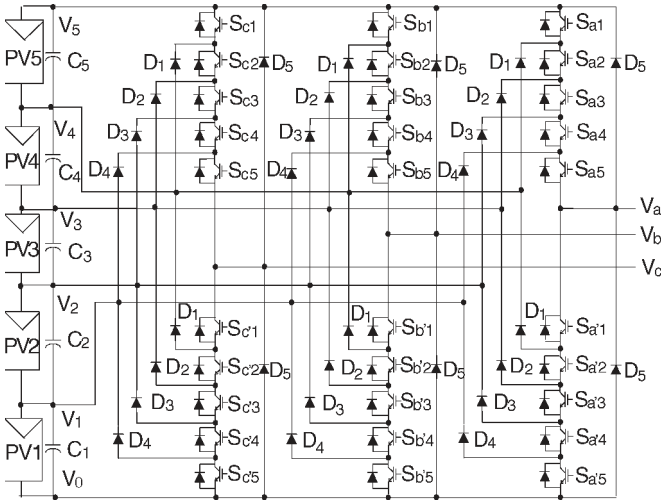


Fig. 2. PV module connected to a three-phase six-level DCMLI topology.

TABLE I
DCMLI VOLTAGE LEVELS AND SWITCHING STATES

Voltage V_a	Switch State									
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$	$S_{a'5}$
$V_5=5V_{DC}$	1	1	1	1	1	0	0	0	0	0
$V_4=4V_{DC}$	0	1	1	1	1	1	0	0	0	0
$V_3=3V_{DC}$	0	0	1	1	1	1	1	0	0	0
$V_2=2V_{DC}$	0	0	0	1	1	1	1	1	0	0
$V_1=V_{DC}$	0	0	0	0	1	1	1	1	1	0
$V_0=0$	0	0	0	0	0	1	1	1	1	1

An m-level DCMLI typically consists of $(m-1)$ power supplies on the dc bus and produces m levels of the phase voltage [23]. Five series PV modules connected on the dc bus with a three-phase six-level structure of the DCMLI are shown in Fig. 2. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by five PV panels into six levels. The voltage across each PV module is $V_{\rm dc}$, and the voltage stress across each switching device is limited to $V_{\rm dc}$ through the clamping diodes.

Table I lists the output-voltage levels possible for one phase of the inverter, with the negative dc rail voltage V_0 as a reference. State condition 1 means that the switch is on, and 0 means that the switch is off. Each phase has five complementary switch pairs such that turning on one of the switches of the pair requires that the other complementary switch be turned off. The complementary switch pairs for phase leg a are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, and $(S_{a5}, S_{a'5})$. Table I also shows that, in a diode-clamped inverter, the switches that are on for a particular phase leg are always adjacent and in series.

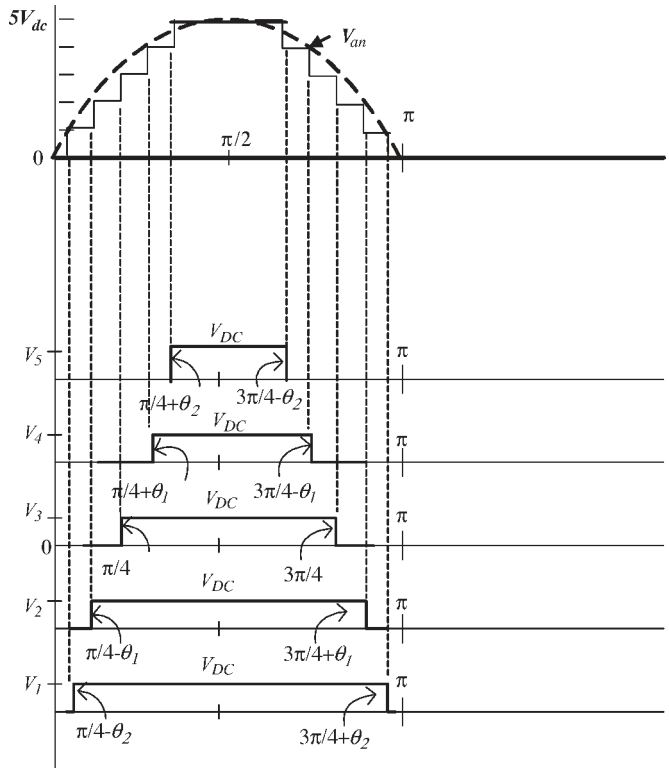


Fig. 3. Line-neutral voltage waveform for a six-level DCMLI.

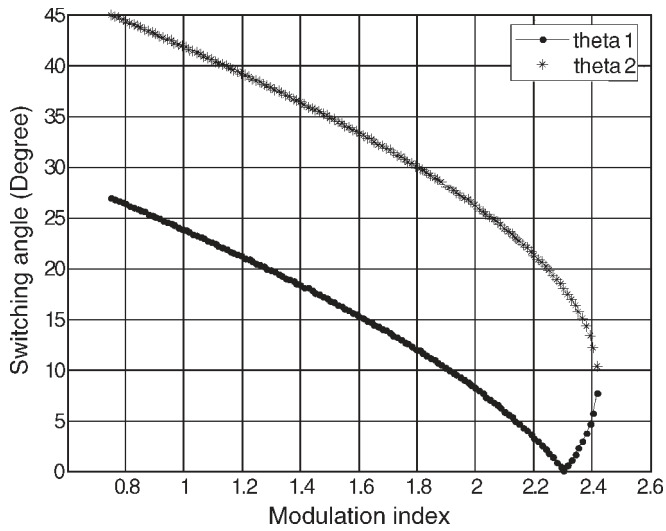


Fig. 4. Switching-angle (θ_1 and θ_2) solutions versus modulation index.

Fig. 3 shows one of the three line-neutral voltage waveforms for a six-level DCMLI. The line voltage V_{ab} consists of a phase-leg a voltage and a phase-leg b voltage. The resulting line voltage is an 11-level staircase waveform. This means that an m-level diode-clamped inverter has an m-level output phase voltage and a $(2m-1)$-level output line voltage.

The simplest way to control a multilevel converter is to use a fundamental frequency switching control where the switching devices generate an m-level staircase waveform that tracks a sinusoidal waveform. In this control, each switching device

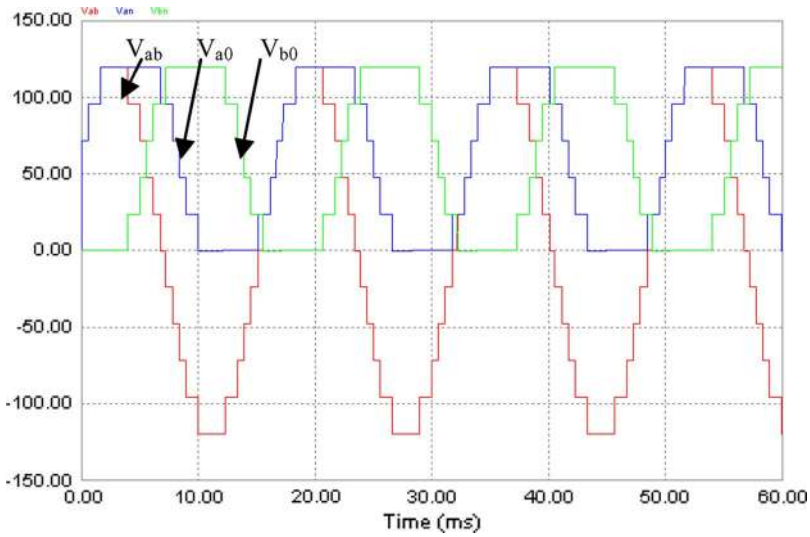


Fig. 5. Line and phase-leg voltage waveforms.

only needs to switch one time per fundamental cycle, which results in low switching losses and low EMI. Considering the symmetry of the waveform, there are only two switching angles (θ_1 and θ_2) that need to be determined in this control strategy, as shown in Fig. 3.

Because there is no neutral connection of the dc side of the six-level DCMLI and in order to create balanced line voltage at the output of the inverter, phase-voltage switching angles (θ_1 and θ_2) must be selected with a value less than 45°, as shown in Fig. 3. The proposed switching-angle calculation method is given in Section III.

III. Proposed Switching Method for Six-Level DCMLI

An important issue in multilevel inverter design is that the voltage waveform is near sinusoidal and the lower order harmonics are eliminated. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the fundamental voltage and not generate specific higher order harmonics. Often, iterative techniques are used to calculate the switching angles, although such an approach does not guarantee finding all the possible solutions. Some other fundamental modulation techniques were presented in [24], [25], and [26]. Previous work in [27] has shown that the transcendental equations characterizing the harmonic content can be converted into polynomial equations, which are then solved using the method of resultants from elimination theory. The work presented here is based on the previous work in [28] for cascaded H-bridges. However, in this paper, the proposed calculation method is adopted for switching of the DCMLI.

As shown in Fig. 3, a multilevel inverter can produce a quarter-wave symmetric voltage waveform synthesized by several dc voltages. By applying Fourier series analysis, the instantaneous output voltage can be expressed as

$$V(t) = \sum_{n=1,3,5,\ldots}^{s} \frac{4V_{\mathrm{DC}}}{n\pi} \left(\cos(n\phi_1) + \cos(n\phi_2) + \cdots + \cos(n\phi_s)\right) \sin(n\omega t) \quad (1)$$

where s is the number of dc sources and V_{dc} is the level of each dc voltage. The switching angles must satisfy the condition $0 < \phi_1 < \phi_2 \cdots < \phi_s < \pi/4$. In order to minimize the harmonic distortion and to achieve adjustable amplitude of the fundamental component, up to $(s-1)$th harmonic can be removed from the voltage waveform. In general, the most significant low-frequency harmonics are chosen for elimination by properly selecting angles among different level inverters, and high-frequency harmonic components can be readily removed by using additional filter circuits. To keep the number of eliminated harmonics at a constant level, for the six-level DCMLI, all switching angles must satisfy the condition $0 < \theta_1 < \theta_2 < \pi/4$, or the total harmonic distortion (THD) increases dramatically. Considering the symmetry of the waveform, only two switching angles need to be determined in this strategy, which are θ_1 and θ_2 shown in Fig. 3. For a six-level DCMLI, the voltage equations are given as

$$\begin{aligned} \frac{1}{2} + \cos(\theta_1) + \cos(\theta_2) &= m_a \\ \frac{1}{2} + \cos(5\theta_1) + \cos(5\theta_2) &= 0 \end{aligned} \quad (2)$$

where modulation index is $m_a = \pi V_{\mathrm{o1}}/(4V_{\mathrm{DC}})$. By defining $x_1 = \cos(\theta_1)$, $x_2 = \cos(\theta_2)$, and V_{o1} to be the rms fundamental component in the output voltage, then using the trigonometric identity given hereafter

$$\cos(5\theta) = 5\cos(\theta) - 20\cos^3(\theta) + 16\cos^5(\theta) \quad (3)$$

the polynomial equations given next are used for calculation of two switching angles (θ_1 and θ_2)

$$\begin{aligned} p_1(x_1, x_2) &= \sum_{n=1}^{2} x_n - m = 0 \\ p_5(x_1, x_2) &= \sum_{n=1}^{2} \left(5x_n - 20x_n^3 + 16x_n^5\right) = 0. \end{aligned} \quad (4)$$

The switching angles of the DCMLI were determined such that the fifth-order harmonic was eliminated while, at the same time, controlling the value of the fundamental. The appropriate polynomial harmonic equations were first derived as given earlier, and the equations are solved, and a table of modulation indices versus switching angles (θ_1 and θ_2) was calculated. Therefore, the lowest THD solution can be used for practical application for the best control performance. The proposed fundamental modulation technique features low switching losses due to the fact that all the switches operate at the fundamental frequency, and the technique additionally allows the converter to operate over a wide range of modulation indices based on selective harmonic elimination.

An m-file in Matlab was used to perform all of the aforementioned calculations. The switching angles' solutions versus the modulation index m_a are shown in Fig. 4. Also, some modulation indices have more than one set of solutions with different values for their residual harmonics and, thus, THD. For practical applications, the set of switching angles with the lowest THD is used for the simulation study and real-time implementation. In order to understand phase-leg and line-voltage relation, phase-leg voltages (V_{a0}, V_{b0}) and the resulting line–line-voltage (V_{ab}) waveforms are shown in Fig. 5

$$V_{ab} = V_{a0} - V_{b0}. \tag{5}$$

IV. Simulation Results

Matlab/Simulink and PSIM software packages were linked to run concurrently to perform this simulation implementation. Blocks in Matlab/Simulink generate the proposed fundamental switching pattern. SimCoupler module, an add-on module to the PSIM software, provides an interface between Matlab/Simulink and PSIM software packages for cosimulation [29]. First, the DCMLI power circuit is simulated in PSIM, and the switching control is also simulated in Matlab/Simulink. The reason for using PSIM is that it is circuit-based simulation software, and it conveniently interfaces with Matlab–Simulink via the toolbox called Simcouple for cosimulation. The simulation validation block diagram based on Simulink and PSIM model is shown in Fig. 6. In the Simulink model, different output-frequency values were tested in order to get dynamic response of the proposed technique. It should be noted that the similar Simulink model is used in both simulation and experiment.

The three-phase line voltages and motor current waveforms shown in Fig. 7 demonstrate that the current shape is almost sinusoidal. The harmonic spectrum of the DCMLI output voltage for 60 Hz revealed elimination of the fifth-order harmonic, as shown in Fig. 8.

V. Experimental Results

A prototype was built to verify the operation of the proposed method. A picture of the laboratory experimental setup is shown in Fig. 9 that includes PV-module connections, six-level DCMLI circuit, three-phase induction motor, and measurement equipment. The PV-powered DCMLI prototype employed 100-V 100-A MOSFETs and supplies an induction motor with

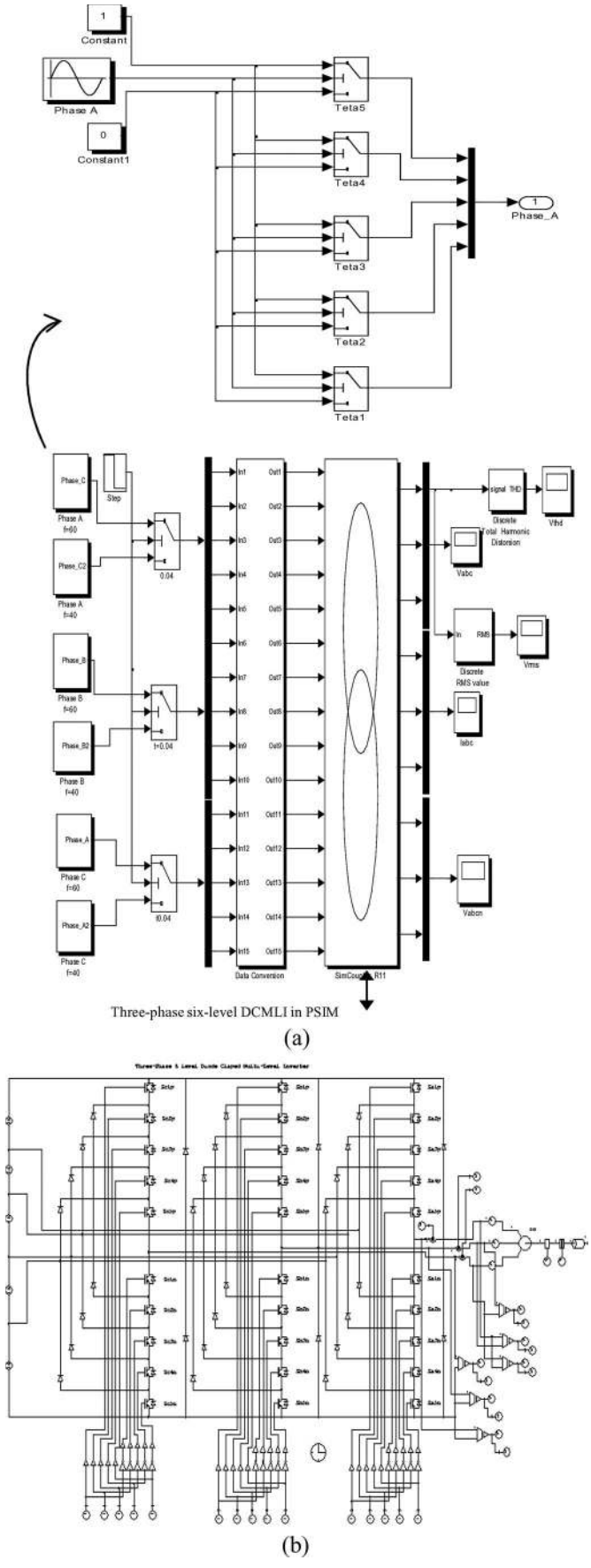


Fig. 6. (a) Simulation block diagram with (b) PSIM performing power circuit of the six-level DCMLI.

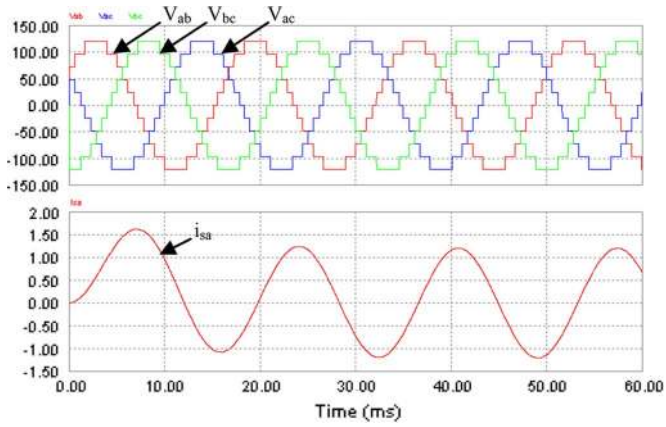


Fig. 7. Line voltage and motor current waveforms of the DCMLI output for 60 Hz.

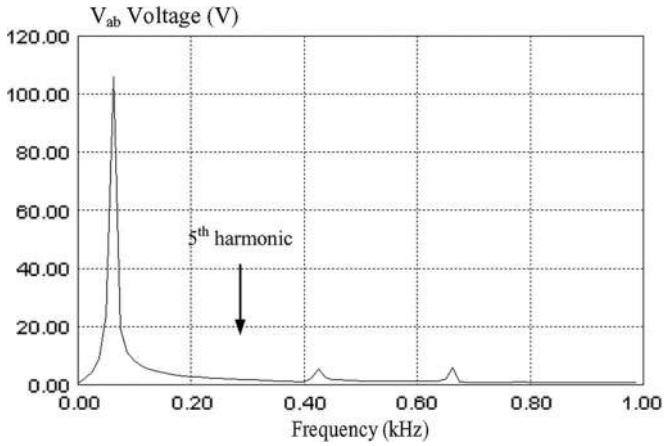


Fig. 8. Harmonic spectrum of line voltage for 60 Hz.

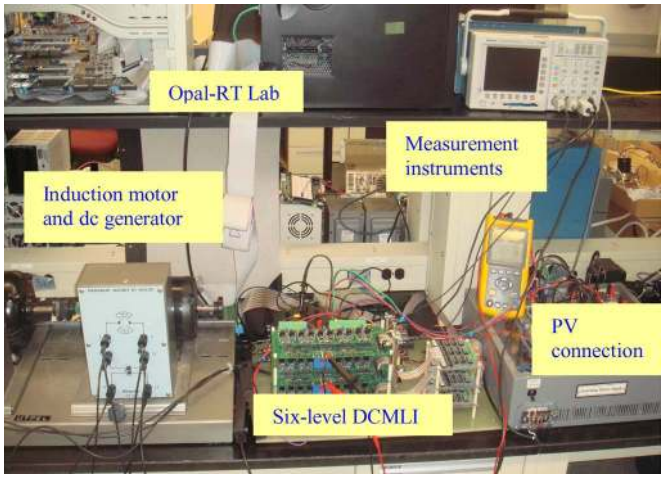


Fig. 9. Six-level DCMLI experimental setup.

a rated horsepower of 250 W, a rated speed of 1725 r/min, a rated current of 1.5 A, and a rated voltage of 208 V coupled with a dc generator (250 W) as a load of the induction motor.

In this paper, the RT-LAB real-time computing platform from Opal-RT Technologies Inc. [30] was used to interface the

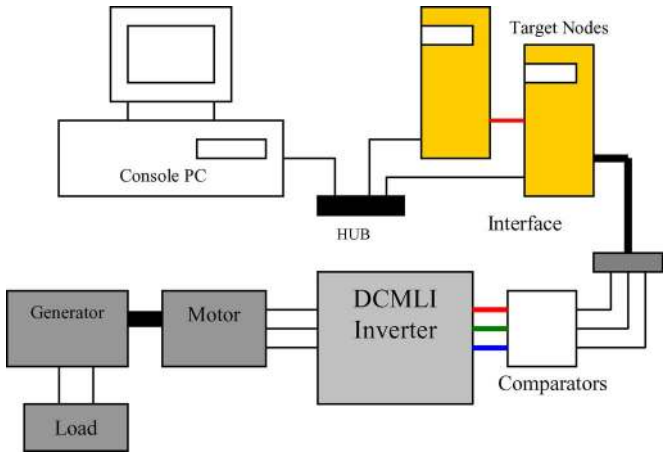


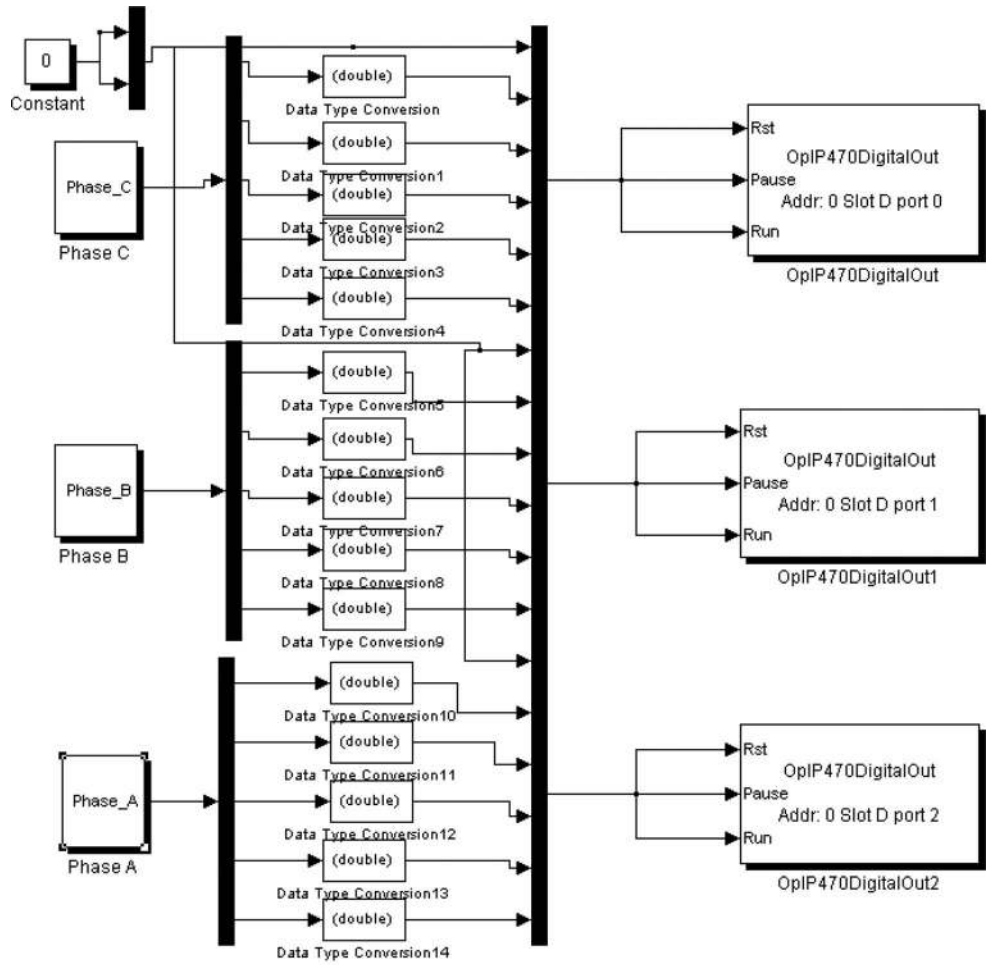
Fig. 10. Hardware components for the Opal RT-LAB configuration.

computer to the six-level DCMLI. The Opal RT-LAB system is utilized to generate gate drive signals and interfaces with the gate drive board. This system allows one to implement the switching algorithm in Simulink which is then converted to C code using real-time workshop from The MathWorks. The Opal RT-LAB software provides icons to interface the Simulink model to the digital I/O board and converts the C code into executables. Hardware components for the Opal RT-LAB configuration are shown in Fig. 10.

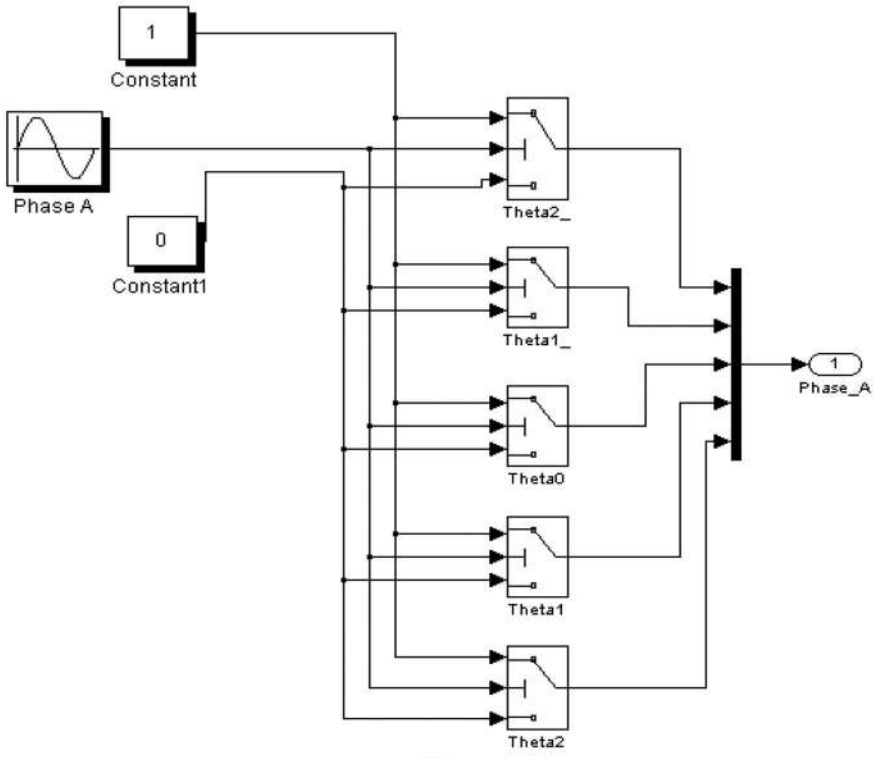
The step size for the real-time implementation was 10 ms, which was used to obtain an accurate resolution for implementing the switching times. The real-time implementation is accomplished by placing the data in a lookup table and therefore does not require high computational power for implementation. The Simulink model shown in Fig. 5 is also used for experimental verification. The model output nodes in Simulink connected to the SimCoupler module are coupled to the output nodes of Opal RT-LAB icons to produce gate signals of DCMLI, as shown in Fig. 11.

Fig. 12 shows the photograph of PV-module arrangements that supply the multilevel inverter. Each PV module has a rated power of 10 W with voltage variation of 16–21 V (nominal 18 V), depending on the operating conditions such as insolation, temperature, etc. Four PV modules are used for one PV array: Two PV modules are connected in series, and two of them are connected in parallel in order to get a nominal voltage of 36 V and a 40-W power for each dc level of the multilevel inverter. There are five identical units (PV1 to PV5) in the proposed PV power supply system with an installed power generation capacity of 200 W from a total of 20 PV panels. The PV panels are mounted outside such that the panels receive maximum solar energy during most of the day.

The conversion efficiency of the inverter, which was measured with a Yokogawa PZ4000 power analyzer, at low power levels is more than 95%, and the maximum efficiency is about 98.5%, which is comparatively higher than that of conventional inverters. Negligible switching losses occur for this system due to the low switching frequency employed. In the present case, the main causes of inverter losses are related to semiconductor conduction losses. Each switch in the inverter switches



(a)



(b)

Fig. 11. (a) DCMLI gate-signal production block diagram in Simulink for the Opal RT-LAB interface. (b) Phase-leg a block diagram.

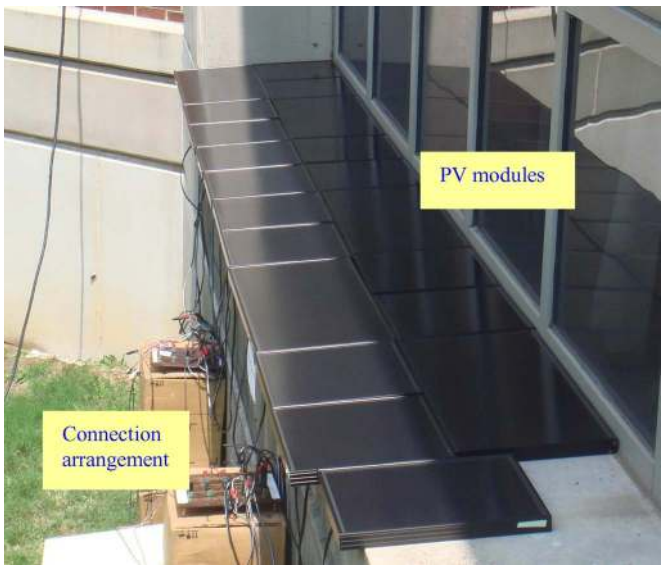


Fig. 12. Photograph of PV-module arrangements comprised of 20 PV modules.

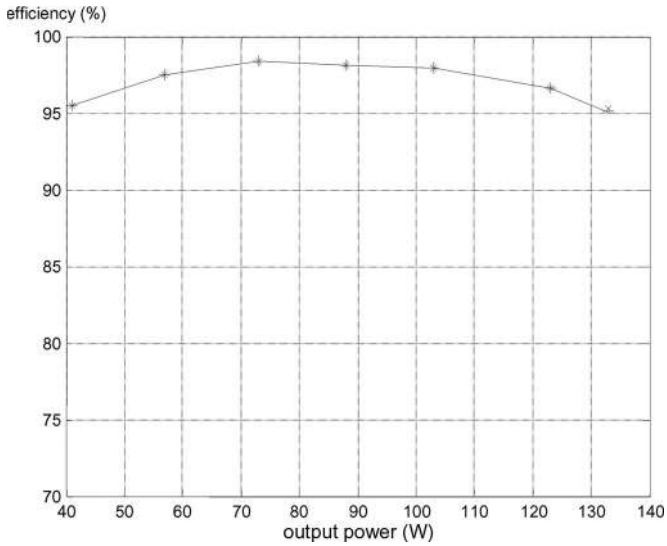
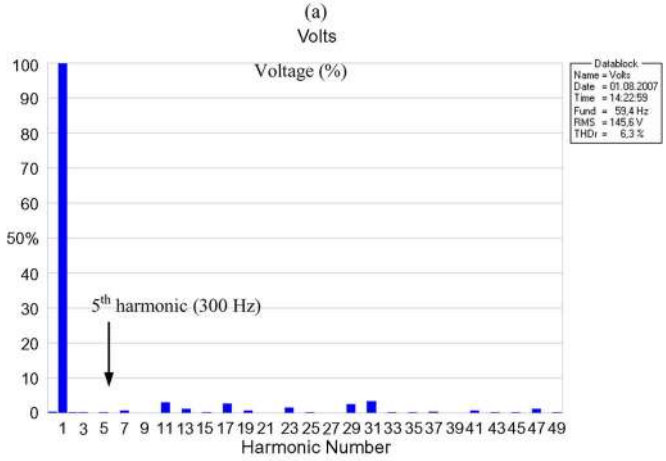


Fig. 13. Conversion efficiency of the six-level DCMLI under different output powers.

TABLE II
SPECIFICATIONS OF PV POWER SYSTEM IN LABORATORY

PV Modules Shell ST10		DCMLI	
Rated Power	10 W	Level	6
Open circuit voltage	22.9 V	Number of DC Source	5
Short circuit current	0.77 A	Output voltage (AC)	120 V
Rated power of PV system	200 W	DC voltage (V_{DC})	36 V

(a)



(b)

Fig. 14. Experimental waveforms. (a) Three-phase line voltage. (b) FFT spectrum of the six-level DCMLI output voltage.

only once per cycle when performing fundamental frequency switching; this results in high efficiency. Fig. 13 summarizes the experimental conversion efficiency of the three-phase six-level DCMLI under different output powers.

Total 200-W peak-power PV modules and a six-level multilevel inverter have been developed in laboratory. Specifications of the main components of the PV power system in laboratory are shown in Table II. It is important to comment that all components of the six-level DCMLI are oversized due to the laboratory component availability. The DCMLI switching frequency has been chosen as fundamental in order to achieve low switching losses.

Fig. 14(a) shows the experimental three-phase line-to-line voltage waveforms, and Fig. 14(b) shows its corresponding fast-Fourier-transform (FFT) spectrum viewing that the 5th, 13th, and triplen harmonics are absent from waveform. The output voltage has a staircase waveform with 11 levels, and the wave shape is near sinusoidal. The THD level of the line-to-line voltage was computed using the data in Fig. 14(a) and was found to be 6.3%. Because the magnitude of the lower order harmonics is very low, there is no need for a large filter circuit. Experimental verification that the low-order harmonics are indeed eliminated is also presented by driving a three-phase induction motor from a six-level DCMLI. Because the six-level DCMLI can generate 11-level line-to-line staircase waveform, the generated voltage and current waveforms are sinusoidal shape even at fundamental switching frequency. The induction motor input voltage and current are shown in Fig. 15, and the input-current FFT spectrum is shown in Fig. 16. The THD level of the output current of the inverter was as low as 1.2% at full load with fundamental frequency switching.

Experimental waveforms, efficiency, and harmonic measurements obtained from a small-scale laboratory prototype have been used to validate the proposed fundamental switching

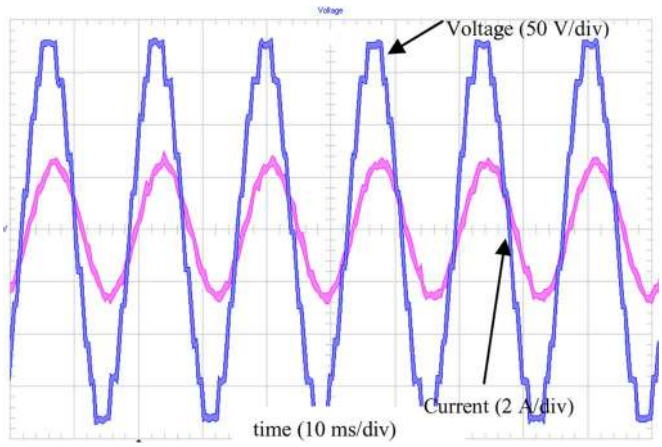


Fig. 15. Experimental induction-motor input-voltage and current waveforms.

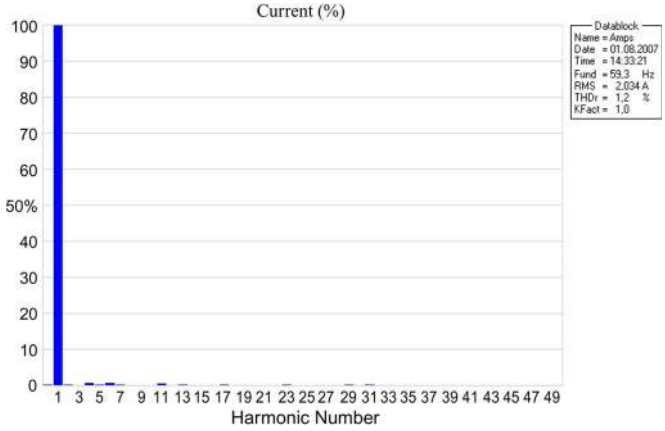


Fig. 16. Induction-motor input-current FFT spectrum.

modulation method and the feasibility of the application of the fundamental-frequency-modulated three-phase six-level DCMLI. The proposed technique, while maintaining switching at fundamental frequency, is simple and requires relatively simple control circuitry, and the output-power quality becomes better as the number of levels increases. The proposed fundamental-frequency-operated DCMLI-based PV power system presented a good performance concerning efficiency and power quality. The proposed configuration has several attractive features such as the output voltage is compatible with the load and, hence, output transformer is not needed. Also, the magnitude of the lower order harmonics is very low; hence, there is no need for a large filter circuit, which makes the inverter cheaper, lighter, and more compact.

In this paper, PV-powered six-level DCMLI switching at the fundamental frequency is proposed for a stand-alone PV system. The lower order harmonics are eliminated, choosing the switching angles that do not generate specifically chosen harmonics. In this paper, a harmonic elimination technique is presented that allows one to control a multilevel inverter in such a way that it is an efficient low-THD inverter that can be used to interface distributed dc energy sources with a main ac grid or as an interface to a traction drive with fuel cells, batteries, or ultracapacitors.

Although the developed PV-based power generation system belongs to a stand-alone power generation approach, it can further merge maximum-power-point-tracking and modified multilevel-inverter control algorithms that can be applied to form a grid-connected generation framework in the future.

VI. Conclusion

In this paper, a fundamental-frequency-modulated DCMLI fed by PV modules is proposed for stand-alone application. It is dedicated to rural areas where there is no connection to the utility network. High-efficiency converters are desirable for renewable energy systems, specifically those related with PV applications. The aim is to have a simple, robust, free-maintenance, and highly efficient PV system. The maximum overall efficiency of the multilevel inverter experimentally verified by a prototype stand-alone PV power system is about 98.5%, which is comparatively higher than that of conventional inverters.

The proposed six-level DCMLI has been applied in a three-phase stand-alone PV system and presents several promising advantages. First, it can convert power for ac utility from relatively low dc voltage sources by itself. Second, it increases output-voltage levels without any transformer so that it has higher efficiency and lower weight for the overall system. Third, in the case of a six-level multilevel inverter, it does not require an output filter because high-order harmonics are effectively filtered off, owing to the reactance of the induction motor load; therefore, it can produce a staircase voltage waveform with lower harmonics eliminated such that higher order harmonics can be easily filtered off if needed for that particular application. Finally, it reduces stresses on power switching devices, resulting in low audio and radio-frequency (RF) noise, EMI, or less electromagnetic compatibility problems, because the multilevel inverter operates with a low switching frequency.

References

[1] M. Calais and V. G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems—An overview," in *Proc. ISIE*, 1998, vol. 1, pp. 224–229.

[2] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. PortilloGuisado, M. A. M. Prats, J. I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Aug. 2006.

[3] L. Quan and P. Wolfs, "Recent development in the topologies for photovoltaic module integrated converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 18–22, 2006, pp. 1–8.

[4] A. R. Beig, U. R. Y. Kumar, and V. T. Ranganathan, "A novel fifteen level inverter for photovoltaic power supply system," in *Conf. Rec. 39th IEEE IAS Annu. Meeting*, Oct. 3–7, 2004, vol. 2, pp. 1165–1171.

[5] F. S. Kang, S. J. Park, S. E. Cho, C. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power system," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[6] J. J. Negroni, F. Guinjoan, C. Meza, D. Biel, and P. Sanchis, "Energy-sampled data modeling of a cascade H-bridge multilevel converter for grid-connected PV systems," in *Proc. 10th IEEE Int. Power Electron. Congr.*, Oct. 2006, pp. 1–6.

[7] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. 34th IEEE Annu. Power Electron. Spec. Conf.*, Jun. 15–19, 2003, vol. 2, pp. 731–735.

[8] H. Valderrama-Blavi, M. Munoz-Ramirez, J. Maixe, R. Giral, and J. Calvente, "Low frequency multilevel inverters for renewable energy systems," in *Proc. IEEE Int. Symp. Ind. Electron.*, Jun. 20–23, 2005, vol. 3, pp. 1019–1024.
[9] R. L. Wai, L. C. You, and W. Hung, "Novel power control scheme for stand-alone photovoltaic generation system," in *Proc. IEEE Ind. Electron. Conf.*, Nov. 2006, pp. 97–102.
[10] R. Gonzalez, J. Lopez, P. Sanchis, and L. Marroyo, "Transformerless inverter for single-phase photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 693–697, Mar. 2007.
[11] R. W. Geoffrey and P. C. Sernia, "Cascaded DC–DC converter connection of photovoltaic modules," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 1130–1139, Jul. 2004.
[12] X. Zhang, H. Ni, D. Yao, R. X. Cao, and W. X. Shen, "Design of single phase grid-connected photovoltaic power plant based on string inverters," in *Proc. IEEE Conf. Ind. Electron. Appl.*, May 2006, pp. 1–5.
[13] E. Roman, R. Alonso, P. Ibanez, S. Elorduizapatarietxe, and D. Goitia, "Intelligent PV module for grid-connected PV systems," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1066–1073, Jun. 2006.
[14] C. Meza, J. J. Negroni, F. Guinjoan, and D. Biel, "Inverter configurations comparative for residential PV-grid connected systems," in *Proc. 32nd IEEE Annu. Conf. Ind. Electron.*, Nov. 2006, pp. 4361–4366.
[15] J. M. Kwon, K. H. Nam, and B. H. Kwon, "Photovoltaic power conditioning system with line connection," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1048–1054, Jun. 2006.
[16] J. M. Chang, W. N. Chang, and S. J. Chung, "Single-phase grid-connected PV system using three-arm rectifier–inverter," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 42, no. 1, pp. 211–219, Jan. 2006.
[17] I. S. Kim, M. B. Kim, and M. J. Youn, "New maximum power point tracker using sliding-mode observer for estimation of solar array current in the grid-connected photovoltaic system," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1027–1035, Jun. 2006.
[18] R. Gonzalez, H. R. Jimenez, J. M. Huacuz, and G. Munguia, "First 3-phase grid-connected photovoltaic system in Mexico," in *Proc. 3rd Int. Conf. Elect. Electron. Eng.*, Sep. 2006, pp. 1–4.
[19] T. Ostrem, W. Sulkowski, L. E. Norum, and C. Wang, "Grid connected photovoltaic (PV) inverter with robust phase-locked loop (PLL)," in *Proc. IEEE Transmiss. Distrib. Conf. Expo., Latin America*, Aug. 2006, pp. 1–7.
[20] Y. Huang, M. Shen, F. Z. Peng, and J. Wang, "Z-source inverter for residential photovoltaic systems," *IEEE Trans. Power Electron.*, vol. 21, no. 6, pp. 1776–1782, Nov. 2006.
[21] Y. M. Chen, T. C. Liu, S. C. Hung, and C. S. Cheng, "Multi-input inverter for grid-connected hybrid PV/wind power system," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1070–1077, May 2007.
[22] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," in *Proc. IEEE Power Eng. Soc. Summer Meeting*, Jul. 16–20, 2000, vol. 2, pp. 1271–1274.
[23] S. Khomfoi and L. M. Tolbert, "Multilevel power converters," in *Power Electronics Handbook*, 2nd ed. Amsterdam, The Netherlands: Elsevier, 2007, pp. 451–482.
[24] J. Wang, R. Wei, Q. Ge, and Y. Li, "The harmonic selection elimination of multilevel converters," in *Proc. IEEE Int. Conf. Elect. Mach. Syst.*, 2003, vol. 1, pp. 419–422.
[25] E. Y. Guan *et al.*, "Fundamental modulation: Multi-pattern scheme with an entire range of modulation indices for multilevel cascaded converters," in *Proc. IEEE Ind. Electron. Appl. Conf.*, 2006, pp. 1–6.
[26] Z. Pan, F. Z. Peng *et al.*, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Trans. Ind. Appl.*, vol. 41, no. 6, pp. 1698–1706, Dec. 2005.
[27] J. Chiasson, L. M. Tolbert, K. J. Mckenzie, and Z. Du, "Control of a multilevel converter using resultant theory," *IEEE Trans. Control Syst. Technol.*, vol. 11, no. 3, pp. 345–354, May 2003.
[28] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.
[29] *PSIM User's Guide Version 6*, Powersim Inc., Woburn, MA, 2003. [Online]. Available: http://www.powersimtech.com
[30] *RT-LAB User's Manual*, Opal-RT Technol. Inc., Montreal, QC, Canada, 2001. Version 6. [Online]. Available: http://www.opal-rt.com

Engin Ozdemir (S'98–M'00–SM'07) was born in Izmit, Turkey. He received the M.Sc. degree in electrical engineering from Yildiz Technical University, Istanbul, Turkey, in 1994, and the Ph.D. degree in electrical engineering from Kocaeli University, Kocaeli, Turkey, in 1999.

In 2007, he was a Visiting Professor with The University of Tennessee, Knoxville, where he also worked on a project at Oak Ridge National Laboratory, Oak Ridge, TN. Since 1999, he has been a Professor with the Faculty of Technical Education, Kocaeli University. His research interests include renewable energy system and power electronics interface, multilevel converters, active power filters, and power quality.

Sule Ozdemir (M'07) was born in Turkey. She received the M.Sc. and Ph.D. degrees from Kocaeli University, Kocaeli, Turkey, in 1999 and 2003, respectively.

In 2007, she was a Visiting Professor with The University of Tennessee, Knoxville. Since 2004, she has been an Assistant Professor with the Faculty of Technical Education, Kocaeli University. Her present research interests include multilevel converters, static var compensation, active power filters, and power quality.

Leon M. Tolbert (S'89–M'91–SM'98) received the B.E.E., M.S., and Ph.D. degrees in electrical engineering from the Georgia Institute of Technology, Atlanta, in 1989, 1991, and 1999, respectively.

He was with Oak Ridge National Laboratory, Oak Ridge, TN, in 1991, and worked on several electrical distribution projects at the three U.S. Department of Energy plants in Oak Ridge. In 1999, he was an Assistant Professor with the Department of Electrical Engineering and Computer Science, The University of Tennessee, Knoxville, where he is currently an Associate Professor. He is an Adjunct Participant at Oak Ridge National Laboratory and conducts joint research at the National Transportation Research Center. He does research in the areas of electric power conversion for distributed energy sources, motor drives, multilevel converters, hybrid electric vehicles, and application of SiC power electronics.

Dr. Tolbert is a registered Professional Engineer in the state of Tennessee. He is an Associate Editor for the IEEE TRANSACTIONS ON POWER ELECTRONICS.