Fundamental Logics Based On Two Phase Clocked Adiabatic Static CMOS Logic

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***Abstract*—This paper demonstrates some fundamental logic gates employing two phase clocked adiabatic static CMOS logic (2PASCL) circuit techniques. We design and simulate NOT, NAND, NOR, and XOR logic gates on the basis of the 2PASCL topology using SPICE implemented using 0.18 μm CTX CMOS technology. For NOT circuit, analytical and simulation values are compared. From the simulation results, we find that 2PASCL inverter logic can save up to 97% of dissipated energy as compared to that with a static CMOS logic at transition frequencies of 10 to 100 MHz. Further, the power dissipation is the lowest when compared with other proposed simple adiabatic logic inverters. 2PASCL also achieves the highest fan-out performance. The results indicate that 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.**

I. Introduction

With the widespread use of mobile and wireless devices and the increase of clock and logic speeds in meeting the new performance requirements, energy efficiency has become a key design aspect in the field of integrated circuits (ICs). For digital circuits, which mostly utilize complementary metal-oxide-semiconductor (CMOS), voltage scaling is one of the main strategies as the power consumption is proportional to the square of the power supply voltage. To maintain high transistor drive current and thus achieve performance improvements, transistor thresholds must be scaled along with the supply voltage. However, threshold voltage, V_t scaling results in a substantial increase in subthreshold leakage current [1].

In recent years, studies on adiabatic computing have been utilized for low-power systems and several adiabatic logic families have been proposed [2]– [9]. However, we have observed several weaknesses of the diode based logics such as low output amplitude and the power dissipation of the diodes at the charging path.

In this study, we design, simulate, and compare the power consumption of NOT, NAND, XOR and NOR logics using 2PASCL [10] and CMOS circuit technologies. A novel method for reducing the power dissipation in a 2PASCL circuit involves; the design of a charging path without diodes. In such a case, current flows only through the transistor during the charging. Thus, a 2PASCL circuit is different from other diode-based adiabatic circuits, in which current flows through both the diode and transistor. By using the aforementioned 2PASCL circuit, we can achieve high output amplitudes and reduce power dissipation. In addition, in order to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

II. CMOS vis-a-vis Adiabatic Logic

A. CMOS

Power dissipation in conventional CMOS circuits primarily occurs during device switching. When the logic level in the system is "1," there is a sudden flow of current through channel resistance R. $Q = C_L V_{dd}$ is the charge supplied by the positive power supply rail for charging C_L to V_{dd}. C_L is the node capacitance, which is referred to as the load capacitance in this paper. Hence, the energy drawn from the power supply is $Q \cdot V_{dd} = C_L V_{dd}^2$ [3]. If it is assumed that the energy drawn from the power supply is equal to that supplied to C_L, the energy stored in C_L becomes one-half the supplied energy, i.e., $E_{stored} = (\frac{1}{2}) C_L V_{dd}^2$. The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is:

$$E_{charge} + E_{discharge} = \frac{1}{2} C_L V_{dd}^2 + \frac{1}{2} C_L V_{dd}^2 = C_L V_{dd}^2. \quad (1)$$

From the above equation, it is apparent that the energy consumption in a conventional CMOS circuit can be reduced by reducing V_{dd} and/or C_L. By decreasing the switching activity in the circuit, the power consumption ($P = \frac{dE}{dt}$) can also be proportionally suppressed.

B. Adiabatic Logic

As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the used of a time-varying voltage source instead of a fixed voltage supply. By spreading out the charge transfer more evenly over the entire time available, peak current is greatly reduced. Consequently, by taking $\hat{I}$ as the average of the current flows to the load capacitance, the overall energy dissipated in the transition has been reduced to being proportional to

$$\hat{I}^2 RT_p = \left(\frac{C_L V_{dd}}{T_p}\right)^2 RT_p = \left(\frac{RC_L}{T_p}\right) C_L V_{dd}^2. \quad (2)$$

For adiabatic charging, theoretically, when T_p, which means the time for the driving voltage to change from 0 V to V_{dd} is long, the energy dissipation is nearly zero.

When the driving voltage $V\overline{\phi}$ changes from HIGH to LOW in pull down network, the discharging via nMOS transistor occurs. From Eq. 2, by minimizing the dissipation through slowing down the logic transition speed, the system reclaims some of the energy that is stored in their capacitors during a computation and reuses it on subsequent computations. This is the theory of charge recovery where these systems are not necessarily reversible.

III. 2PASCL

A. Circuit Operation

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter [10]. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches. By using these two split-level sinusoidal waveforms, which have peak-to-peak voltages of 0.9 V, the voltage difference between the current-carrying electrodes can be minimized, consequently power consumption can be suppressed. The substrates of the pMOS and nMOS transistors are connected to ϕ and GND respectively.

Since the criteria for maintaining thermal equilibrium, in which the voltage between the current-carrying electrodes is zero when the transistors are in the ON state [4] are satisfied, the energy accumulated in C_L is not dissipated. Moreover, sinusoidal waveforms can be generated with a higher energy efficiency than trapezoidal waveforms [7].

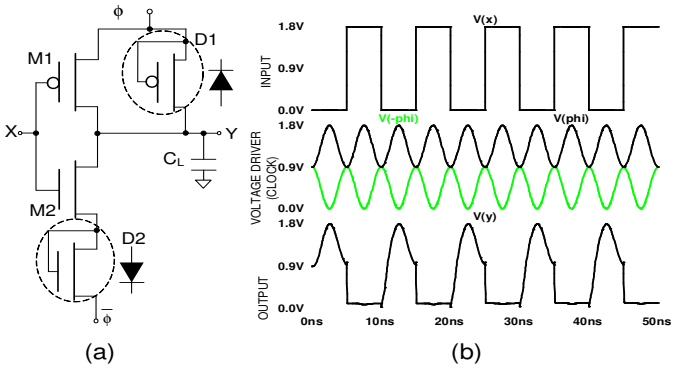

Fig. 1. (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency X=100 MHz, $V_\phi = V\overline{\phi}$ = 200 MHz.

From the operation of 2PASCL [11], less dynamic switchings are seen as circuit nodes are not necessarily charging and discharging at every clock cycle which reduces the node switching activities significantly. The lower the switching activity, the lower its energy dissipation. One of the benefits is that the logic behaves like a static logic.

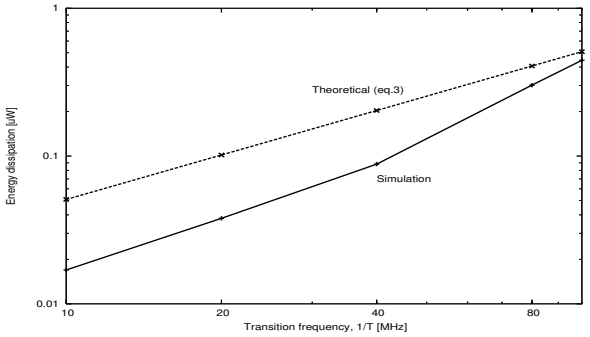

Fig. 2. Power dissipation per cycle comparison of the simulation results and theoretical values of 2PASCL-based inverter gate.

B. Theoretical Analysis

In adiabatic circuits, energy dissipation occurs through the threshold voltage and transistor channel resistance. To estimate the energy consumption in adiabatic circuits, we utilize an RC model with a threshold voltage V_t. The energy dissipation in a 2PASCL inverter is as follows [12]:

$$\begin{aligned} E_{2PASCL} &= E_{chrg(M1)} + E_{dischrg(D1)} + E_{dischrg(M2,D1)} \\ &= \frac{1}{2}C_L V_{tp}^2 + \frac{1}{2}C_L V_{\phi p-p} \mid V_{tp} \mid + \frac{1}{2}C_L (V_{\overline{\phi}p-p} - V_{tn}) V_{tn} \\ &= \frac{1}{2}C_L \left(V_{tp}^2 + V_{\phi p-p} \mid V_{tp} \mid + (V_{\overline{\phi}p-p} - V_{tn}) V_{tn} \right), \end{aligned} \quad (3)$$

where C_L is the load capacitance; V_{tp} the threshold voltage of pMOS; V_{tn} the threshold voltage of nMOS; and $V_{\phi p-p}$ and $V_{\overline{\phi}p-p}$ the voltage supplies.

By assuming C_L=0.01 pF, $\mid V_{tp} \mid$=0.58 V, V_{tn}=0.24 V, and $V_{\phi p-p} = V_{\overline{\phi}p-p}$= 0.9 V, the theoretical calculations are plotted. As shown in Fig. 2, the power dissipation at each transition frequency is compared. The unmatched values of the simulation and analytical results are primarily because of the shape factor of voltage drivers which are not considered in the theoretical calculations. However, we have understood the fundamental factors that contributed to the power dissipation in the 2PASCL inverter from this analytical analysis. From Eq. 3, by applying $V_{\phi p-p}$ and $V_{\overline{\phi}p-p}$ as split-level sinusoidal waveforms, with each peak-to-peak voltage being 0.9 V, we have saved approximately 50% of the energy, as compared to non-split-level waveforms.

C. Inverter Circuit

The paper starts by examining the logic function and energy dissipation of a simple logic gate, an inverter of 2PASCL.

1) Simulation Condition: The simulations in this paper utilize SPICE circuit simulator with a 0.18 μm, 1.8 V standard CMOS process. The W/L of nMOS and pMOS logic gates used are 0.6 μm/0.18 μm. A capacitive load C_L, of 0.01 pF is placed at the output node Y. The frequency of power supply

clock is set to be exactly two times higher than the transition frequency. The simulations are as follows;

a) Inverter logic function evaluation: The simulation to evaluate logic function for the 2PASCL inverter at 100 MHz transition frequency is carried out.

b) Energy dissipation comparison: Next, energy dissipation per cycle is compared to CMOS and other simple adiabatics inverter logic i.e. 1n1p with split-level driving pulse [5], 1n1p quasi adiabatic [6], Quasi-Static Energy Recovery Logic (QSERL) [7], Adiabatic Dynamic CMOS Logic (ADCL) [8] and 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL) [9] at transition frequencies of 10, 20, 40, 80 and 100 MHz.

c) Load capacitance evaluation: Then, by changing the load capacitance from 0.01, 0.02, 0.05, 0.1, 0.2, 0.3, 0.4 and 0.5 pF, energy dissipation of 2PASCL is once again compared to CMOS and previously mentioned simple adiabatic inverters.

2) Simulation Results:

a) Inverter logic function: The SPICE simulation results obtained for the 2PASCL inverter are shown in Fig. 1 (b). The top graph demonstrates the input signal which is a CMOS-compatible rectangular pulses. The middle graph shows the driving voltage of the split-level sinusoidal supply clock, and the last graph shows the output waveform. The energy dissipation is calculated by integrating the product of voltage and current as follows:

The energy dissipation is calculated by integrating the voltage and current product value as follows:

$$E = \int_0^T \left(\sum_{i=1}^{n} (V_{pi} \times I_{pi}) \right) dt, \tag{4}$$

where T is the period of the primary input signal; V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [9]. The energy in joule is then converted to watt by multiplying it with the input frequency.

b) Comparison of energy dissipation: The graph shown in Fig. 3 reveals that with the 2PASCL inverter, up to 97% of the power dissipated from the CMOS inverter can be saved. It also show that the 2PASCL inverter offers the lowest power dissipation among all the other adiabatic inverter logic circuits.

c) Power dissipation at different value of C_L: The simulation results show that the power dissipation in the 2PASCL inverter is 63% lower than that of CMOS static when the C_L values are changed from 0.01 to 0.5 pF, as shown in Fig. 4. It is also shown that the energy dissipated from 2PASCL at various load capacitance is the lowest compared to other adiabatic circuits. It shows a significantly lower energy dissipation from 0.01 to 0.1 pF. The difference compared to QSERL at this range exceeds 100 times.

IV. Applications of Proposed Circuit

The first combination circuit examined in this study is NAND logic. Our proposed schematic is shown in Fig. 5. The logic function of the circuit as shown on the right graph is confirmed. From the comparison study with CMOS, we find

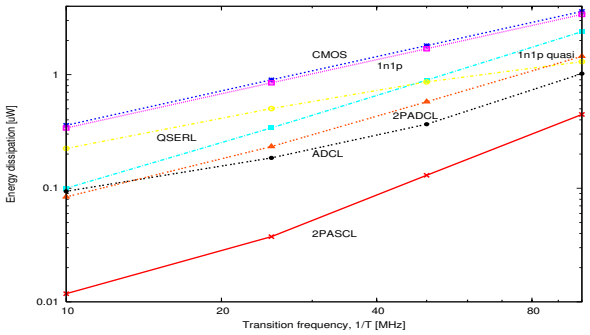

Fig. 3. Power dissipation comparison of 2PASCL, CMOS and other simple adiabatic circuits.

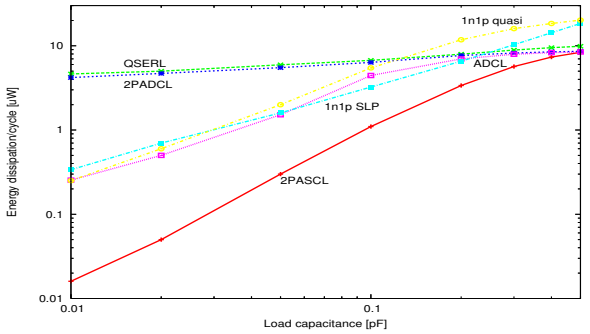

Fig. 4. Energy dissipation comparison of adiabatic logics at different load capacitance.

that a 2PASCL-based NAND circuit can save up to 62% at transition frequencies of 10 to 100 MHz. From the graph, power can be saved the most at low transition frequencies.

We then simulated two combination logic circuits; 2PASCL-based XOR and NOR circuits. Both the schematics are demonstrated in Fig. 6 and Fig. 7. By using the split-level sinusoidal driving clocks, the proposed XOR and NOR have 47% and 36% lower energy than conventional static CMOS, respectively. A significant power saving can be seen at low transition frequencies. As shown in Fig. 6, the scheme for a 2PASCL XOR has no diodes at the output Y. The discharging diodes of pMOSs are placed only at the inverter site of the circuit. However, in the case of an nMOS diode, it remains adjacent to the nMOS logic circuit and $\overline{\phi}$.

V. Discussion

The logic swings at the output at high state have been solved when simulation is carried out using 0.1 pF load capacitance. By taking lower power dissipation and higher fan-out as its strength, the weakness of 2PASCL is related to leakage current as the gates are slowly switched. Further analysis will be carried out in the next evaluation to solve these problems.

VI. Conclusion

The NOT, NAND, XOR and NOR logic using 2PASCL topology has offered more energy savings compared to conventional CMOS. As it dissipates less energy than other proposed adiabatic inverter circuits, 2PASCL is a promising

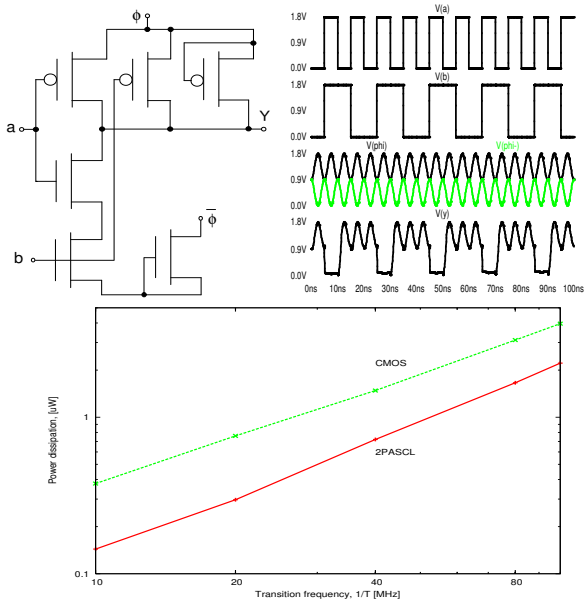

Fig. 5. Scheme for 2PASCL-based NAND logic (top left), waveforms from the simulation at X=100 MHz where the output $Y = \overline{a \cdot b}$ (top right), and power dissipation compared to conventional NAND gate (bottom).

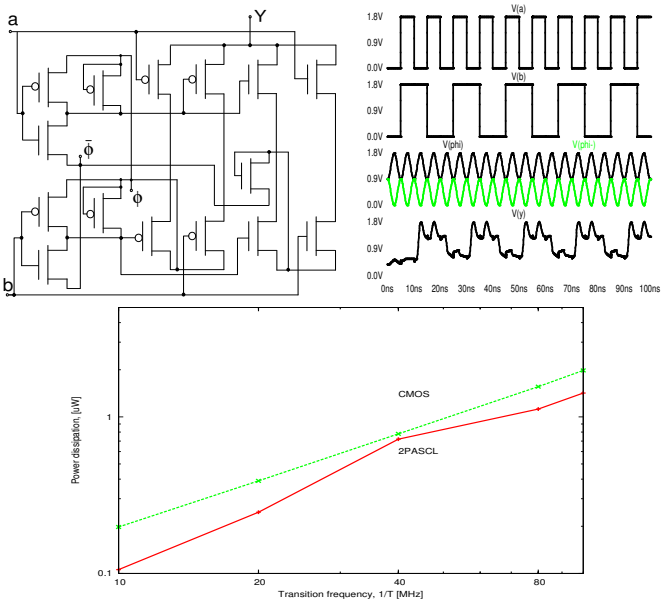

Fig. 6. (top left) Scheme for 2PASCL based XOR logic, (top right) waveforms from the simulation where the output $Y = a \oplus b$ and (bottom) energy dissipation compared to conventional ExOR gate.

candidate for low-power circuits at the frequency range in which signals are digitally processed.

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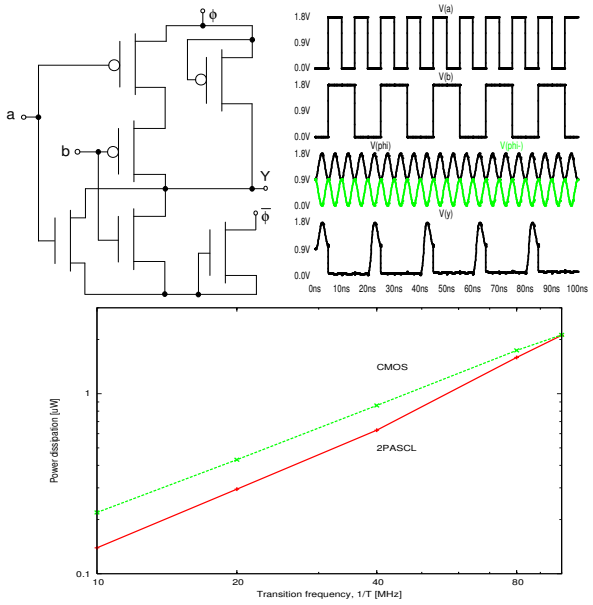

Fig. 7. (top left) Scheme for 2PASCL based NOR logic, (top right) waveforms from the simulation where the output $Y = \overline{a + b}$ and (bottom) energy dissipation compared to conventional NOR gate.

REFERENCES

[1] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand, "A leakage current mechanism and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol.91, no.2, pp.305–327, Feb. 2003.

[2] S. Kim, C.H. Ziesler, and M.C. Papaefthymiou, "Charge-recovery computing on silicon," *IEEE Trans. Computers*, vol.54, no.6, pp.651–659, June 2005.

[3] J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic – a proposal for digital low power applications," *J. VLSI Signal Processing*, vol.27, no.27, pp.253–268, Feb. 2001.

[4] V.I. Starosel'skii, "Adiabatic logic circuits: A review," *Russian Microelectronics*, vol.31, no.1, pp.37–58, 2002.

[5] K.A. Valiev and V.I. Starosel'skii, "A model and properties of a thermodynamically reversible logic gate," *Mikroelektronika*, vol.29, no.2, pp.83–98, 2000.

[6] V.I. Starosel'skii, "Reversible logic," *Mikroelektronika*, vol.28, no.3, pp.213–222, 1999.

[7] Y. Ye and K. Roy, "QSERL: Quasi-static energy recovery logic," *IEEE J. Solid-States Circuits*, vol.36, no.2, pp.239–248, Feb. 2001.

[8] K. Takahashi and M. Mizunuma, "Adiabatic dynamic CMOS logic circuit," [*IEICE Trans. Electron. (Japanese Edition)*], vol.J81-CII, no.10, pp.810–817, Oct. 1998 (Electronics and Communications in Japan Part II (English Translation), vol.83, no.5 , pp.50–58, April 2000).

[9] Y. Takahashi, Y. Fukuta, T. Sekine and M. Yokoyama, "2PADCL : Two phase drive adiabatic dynamic CMOS logic," *Proc. IEEE APCCAS*, pp.1486–1489, Dec. 2006.

[10] N. Anuar, Y. Takahashi and T. Sekine, "Adiabatic logic versus CMOS for low power applications," *Proc. ITC–CSCC 2009*, pp.302–305, Jul. 2009.

[11] N. Anuar, Y. Takahashi and T. Sekine, "4-bit ripple carry adder of two-phase clocked adiabatic static CMOS logic: a comparison with static CMOS," *Proc. IEEE ECCTD 2009*, pp.65–68, Aug. 2009.

[12] N. Anuar, Y. Takahashi and T. Sekine, "4-bit ripple carry adder using two-phase clocked adiabatic static CMOS logic," *Proc. IEEE TENCON 2009* (accepted).