

Serge Oktyabrsky • Peide D. Ye
Editors

Fundamentals of III-V Semiconductor MOSFETs

 Springer

Contents

1 Non-Silicon MOSFET Technology: A Long Time Coming	1
Jerry M. Woodall	
1.1 Introduction	1
1.2 Brief and Non-Comprehensive History of the NSMOSFET	2
1.3 Surface Fermi Level Pinning: The Bane of NSMOSFET Technology Development	3
1.4 Concluding Remarks	6
References	6
2 Properties and Trade-Offs of Compound Semiconductor MOSFETs	7
Tejas Krishnamohan, Donghyun Kim and Krishna C. Saraswat	
2.1 Introduction	7
2.2 Simulation Framework	10
2.3 Power-Performance Tradeoffs in Binary III-V Materials (GaAs, InAs, InP and InSb) vs. Si and Ge	15
2.4 Power-Performance of Strained Ternary III-V Material ($\text{In}_x\text{Ga}_{1-x}\text{As}$)	19
2.5 Strained III-V for p-MOSFETs	22
2.6 Novel Device Structure and Parasitics	24
2.7 Conclusion	27
References	27
3 Device Physics and Performance Potential of III-V Field-Effect Transistors	31
Yang Liu, Himadri S. Pal, Mark S. Lundstrom, Dae-Hyun Kim, Jesús A. del Alamo and Dimitri A. Antoniadis	
3.1 Introduction	31
3.2 InGaAs HEMTs	32
3.3 Discussion	36
3.4 Conclusions	46
References	47

4	Theory of HfO_2-Based High-k Dielectric Gate Stacks	51
	Alexander A. Demkov, Xuhui Luo and Onise Sharia	
4.1	Introduction	51
4.2	Theoretical Background	52
4.3	Properties of Bulk Hafnia and Zirconia	57
4.4	Surfaces	71
4.5	Band Alignment at Hafnia Interfaces	81
4.6	Conclusions	89
	References	89
5	Density Functional Theory Simulations of High-k Oxides on III-V Semiconductors	93
	Evgueni A. Chagarov and Andrew C. Kummel	
5.1	Introduction	93
5.2	Methodology of DFT Simulations of High-k Oxides on Semiconductor Substrates	96
5.3	DFT Simulations of High-k Oxides on Si/Ge Substrates	106
5.4	Generation of Amorphous High-k Oxide Samples by Hybrid Classical-DFT Molecular Dynamics Computer Simulations	112
5.5	The Current Progress in DFT Simulations of High-k Oxide/III-V Semiconductor Stacks	118
5.6	Summary	126
	References	126
6	Interfacial Chemistry of Oxides on III-V Compound Semiconductors	131
	Marko Milojevic, Christopher L. Hinkle, Eric M. Vogel and Robert M. Wallace	
6.1	Introduction	131
6.2	Surfaces of III-V MOSFET Semiconductor Candidates	132
6.3	Oxide Formation (Native and Thermal)	138
6.4	Oxide Deposition on III-V Substrates	146
6.5	Electrical Behavior of Oxides on III-V and Interfacial Chemistry	156
6.6	Conclusions	165
	References	165
7	Atomic-Layer Deposited High-k/III-V Metal-Oxide-Semiconductor Devices and Correlated Empirical Model	173
	Peide D. Ye, Yi Xuan, Yanqing Wu and Min Xu	
7.1	Introduction	173
7.2	History and Current Status	174
7.3	Empirical Model for III-V MOS Interfaces	178
7.4	Experiments on High-k/III-V MOSFETs	181
7.5	Conclusion	188
	References	189

8	Materials and Technologies for III-V MOSFETs	195
	Serge Oktyabrsky, Yoshio Nishi, Sergei Koveshnikov, Wei-E Wang, Niti Goel and Wilman Tsai	
8.1	Introduction	195
8.2	III-V HEMTs for Digital Applications	196
8.3	Challenges for III-V MOSFETs	207
8.4	Mobility in Buried Quantum Well Channel	208
8.5	Interface Passivation Technologies	210
8.6	Summary	237
	References	238
9	InGaAs, Ge, and GaN Metal-Oxide-Semiconductor Devices with High-k Dielectrics for Science and Technology Beyond Si CMOS	251
	M. Hong, J. Kwo, T. D. Lin, M. L. Huang, W. C. Lee and P. Chang	
9.1	Introduction	251
9.2	Material Growth, Device Fabrication, and Measurement	253
9.3	Devices	255
9.4	Interfacial Chemical Properties	266
9.5	Energy-Band Parameters	268
9.6	Thickness Scalability of Ga ₂ O ₃ (Gd ₂ O ₃) on InGaAs with Low D _{it} , Low Leakage Currents, and High-Temperature Thermodynamic Stability	272
9.7	Interface Trap Densities and Efficiency of Fermi-Level Movement	274
9.8	Conclusion	279
	References	280
10	Sub-100 nm Gate III-V MOSFET for Digital Applications	285
	K. Y. (Norman) Cheng, Milton Feng, Donald Cheng and Chichih Liao	
10.1	Introduction	285
10.2	MOSFET Figures of Merit for Digital Applications	286
10.3	Selection of III-V Channel Materials	290
10.4	Self-Aligned III-V MOSFET Structures	294
10.5	Benchmark of III-V FET with Si CMOS	299
10.6	Outlook and Conclusions	302
	References	303
11	Electrical and Material Characteristics of Hafnium Oxide with Silicon Interface Passivation on III-V Substrate for Future Scaled CMOS Technology	307
	Injo Ok and Jack C. Lee	
11.1	Introduction	307
11.2	MOSCAPs and MOSFETs on GaAs with Si, SiGe Interface Passivation Layer (IPL)	309
11.3	MOSCAPs and MOSFETs on InGaAs with Si IPL	334

11.4	MOSCAPs and Self-Aligned n-channel MOSFETs on InP Channel Materials with Si IPL	342
11.5	Conclusions	346
	References	347
12	p-type Channel Field-Effect Transistors	349
	Serge Oktyabrsky	
12.1	Introduction	349
12.2	Low-Field Hole Mobility in Bulk Semiconductors	351
12.3	p-channel: Figures of Merit with Scaling of Channel Length ...	353
12.4	Strained Quantum Wells	355
12.5	p-channel HFETs	364
12.6	p-type MOSFETs	370
12.7	Conclusions	372
	References	372
13	Insulated Gate Nitride-Based Field Effect Transistors	379
	M. Shur, G. Simin, S. Romyantsev, R. Jain and R. Gaska	
13.1	Introduction	379
13.2	Materials Growth and Deposition Technologies	381
13.3	Transport Properties	389
13.4	Device Design and Fabrication	395
13.5	Device Characteristics	397
13.6	Non-Ideal Effects and Reliability	404
13.7	Applications and Performance	406
13.8	Future Trends: From Megawatts to Terahertz	414
	References	416
14	Technology/Circuit Co-Design for III-V FETs	423
	Jaydeep P. Kulkarni and Kaushik Roy	
14.1	Introduction	423
14.2	Device/SPICE Models	425
14.3	Logic Circuit Analysis	428
14.4	Memory Circuit Analysis	435
14.5	Application Space of III-V QWFETs	439
14.6	Conclusions	439
	References	440
	Index	443