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Fundamentals of low-noise analog circuit design — Source link

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Published on: 01 Oct 1994

Topics: Noise (electronics), Circuit design, Analogue electronics, Integrated circuit and Electronic circuit

Fundamentals of Low-Noise Analog Circuit Design

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This paper presents a tutorial treatment of the fundamentals of noise in solid-state analog electronic circuits. It is written for upper division students and practicing engineers who wish to gain a basic knowledge of the theory of electronic noise and techniques for low-noise circuit design. The paper presents an overview of noise fundamentals, a description of noise models for passive devices and active solid-state devices, methods of calculating the noise performance of amplifiers, and techniques for minimizing noise in circuit design. The theory and methods are applicable to both discrete and integrated circuits.

I. Introduction

With modern solid-state devices and integrated circuits, it is possible to realize amplifiers that exhibit an extremely high voltage gain. Indeed, a gain of almost any desired magnitude can be obtained by cascading stages. This might seem to imply that an arbitrarily small signal can be amplified to any desired level. This is not true because there is always a limit to the smallest signal that can be amplified. This limit is determined by electronic noise. If a signal is so small that it is masked by the noise in an amplifier, it is impossible to recover the signal by amplification.

Noise is present in all electronic circuits. It is generated by the random motion of electrons in a resistive material, by the random recombination of holes and electrons in a semiconductor, and when holes and electrons diffuse through a potential barrier. The theoretical basis for the analysis of noise lies in the areas of semiconductor device physics and probability theory [1]–[3]. The circuit designer can easily be intimidated by some of this theory. For this reason, low-noise circuit design is perceived by some as being an esoteric area. However, it can be straightforward if the device noise models are understood. These models are quite simple and no special knowledge of semiconductor device physics or probability theory is required to use them.

This paper gives a tutorial introduction to the subject of noise in analog electronic circuits. The material is applicable to both discrete and integrated circuits. The principal sources of noise are described and models for the sources are given. The general characteristics of noise are described and methods for its measurement are discussed. Noise models for the bipolar junction transistor (BJT) and the field-effect transistor (FET) are given. These devices are analyzed by reflecting all noise sources into an equivalent noise voltage in series with the device input. The conditions for minimum noise in each are derived. To illustrate the principles, a design example is presented where the theoretically predicted noise performance is compared to that predicted by a SPICE simulation.

The notations for voltages and currents correspond to the following conventions: dc quantities are indicated by an upper case letter with upper case subscripts, e.g., I_C, I_D, etc. Small-signal ac quantities are indicated by a lower case letter with lower case subscripts, e.g., v_s, i_t, etc. Root mean square (rms) or effective values are indicated by an upper case letter with lower case subscripts, e.g., V_s, I_t, etc. Phasor quantities are indicated by a bold-face upper case letter and bold face lower case subscripts, e.g., $\boldsymbol{V}_s$, $\boldsymbol{I}_t$, etc. Circuit symbols for independent sources are circular and those for controlled sources have a diamond shape. Voltage sources have a $\pm$ sign within the symbol and current sources have an arrow. Noise sources are represented as independent sources having a smaller circular symbol than signal sources. In the numerical evaluation of noise equations, the following values are used: Boltzmann's constant $k = 1.38 \times 10^{-23}$ J/K, absolute temperature $T = 300$ K, electronic charge $q = 1.60 \times 10^{-19}$ C, and thermal voltage $V_T = 0.0259$ V.

II. Thermal Noise

A noise voltage called *thermal noise* is generated when thermal energy causes free electrons to move randomly in a resistive material [2], [4], [5]. The phenomenon was discovered (or anticipated) by Schottky in 1928 and first measured and evaluated by Johnson in the same year. It is also referred to as *Johnson noise*. Shortly after its discovery, Nyquist used a thermodynamic argument to show that the open-circuit rms thermal noise voltage across a resistor is given by

$$V_t = \sqrt{4kTR\Delta f} \tag{1}$$

Manuscript received January 28, 1993; revised March 29, 1994.

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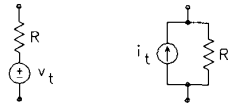
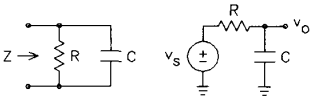
IEEE Log Number 9404667.



(a) (b)

Fig. 1. (a) Thevenin noise model of resistor. (b) Norton noise-model of resistor.



(a) (b)

Fig. 2. (a) Parallel RC network. (b) Single pole RC low-pass filter.

where k is Boltzmann's constant, T is the absolute temperature, R is the resistance, and Δf is the bandwidth in hertz over which the noise is measured.

The power in thermal noise is proportional to the square of V_t which is independent of frequency for a fixed bandwidth. The power between 100 and 200 Hz is the same as it is between 10100 and 10200 Hz. Such noise is said to have a *uniform* or *flat* power distribution and is called *white noise*. It is called this by analogy to white light which also has a flat power distribution in the optical band.

Equation (1) is the basis for two resistor noise models—the Thevenin model and the Norton model. These are shown in Fig. 1. The short-circuit rms thermal noise current in the Norton model of Fig. 1(b) is given by

$$I_t = \frac{V_t}{R} = \sqrt{\frac{4kT\Delta f}{R}}. \tag{2}$$

Because noise is random, the source polarities in the figure are arbitrary. In general, the polarities must be labeled when writing circuit equations. The total rms noise in a circuit is independent of the assumed polarities.

Thermal noise is present in all circuit elements containing resistance. The noise is independent of the composition of the resistance. It is modeled the same way in discrete-circuit resistors and in integrated-circuit monolithic and thin-film resistors [4]. A carbon composition resistor generates the same amount of thermal noise as a metal film resistor of the same value. However, an additional noise component called flicker noise may be present in the carbon composition resistor. It results from the variable contact between the carbon particles of the resistive material. This noise is present only when a direct current flows in the resistor. It is discussed in more detail in Section IV.

Equation (1) shows that thermal noise voltage is proportional to the square root of the product of the absolute temperature, the resistance value, and (to the highest measurable frequencies) the bandwidth over which the noise is measured. For a fixed temperature, the thermal noise voltage in a circuit can be reduced by minimizing the resistance and the bandwidth. Further reduction can only be obtained by operating the circuit at lower temperatures.

The *crest factor* for thermal noise is defined as the ratio of the peak value to the rms value. Although the rms value can be calculated, the peak value cannot because it is random. A common definition for the peak value is the level that is exceeded only 0.01% of the time [5]. To relate this to the rms value, a statistical model for the amplitude distribution is required. It is common to assume that the amplitude distribution of thermal noise can be modeled by a Gaussian or normal probability-density function. For a Gaussian random variable, the probability that the instantaneous value exceeds four times the rms value is approximately 0.01%. Thus the crest factor is approximately 4.

In any circuit containing resistors, capacitors, and inductors, only the resistors generate thermal noise. (The winding resistance of an inductor must be modeled as a separate resistor.) Let Z be the complex impedance of a two-terminal network. The open-circuit rms thermal noise voltage generated by the network in the frequency band from f_1 to f_2 is given by

$$V_t = \left[4kT \int_{f1}^{f_2} \mathrm{Re}\,(Z)\, df\right]^{1/2} \tag{3}$$

where $\mathrm{Re}\,(Z)$ is the real part of Z and f is the frequency in hertz. Let $f_2 = f_1 + \Delta f$. If Δf is sufficiently small, the noise voltage divided by the square root of the bandwidth can be solved for to obtain

$$\frac{V_t}{\sqrt{\Delta f}} = \sqrt{4kT\,\mathrm{Re}\,(Z)}. \tag{4}$$

This equation defines what is called the *spot noise voltage* generated by the impedance. The units are read "*volts per root hertz*".

The total noise voltage generated by any resistor is limited by its shunt capacitance. For a physical resistor, this capacitance can never be zero. Figure 2(a) shows a parallel RC circuit. The complex impedance and its real part, respectively, are given by

$$Z = R\|(1/j2\pi fC) = R/(1 + j2\pi fRC)$$

and

$$\mathrm{Re}\,(Z) = R/[1 + (2\pi fRC)^2].$$

It follows from (3) that the total rms open-circuit thermal noise voltage is given by

$$V_t = \left[4kT \int_0^\infty \frac{R\,df}{1 + (2\pi fRC)^2}\right]^{1/2} = \sqrt{\frac{kT}{C}}. \tag{5}$$

It can be concluded that the total noise voltage generated by a resistor is a function only of the temperature and the total shunt capacitance across the resistor.

III. Shot Noise

Shot noise is generated when a current flows across a potential barrier [1], [4], [5]. It is caused by the random fluctuation of the current about its average value and occurs in vacuum tubes and in semiconductor devices. In vacuum tubes, it is generated by the random emission of electrons from the cathode. In semiconductors, it is generated by the random diffusion of holes and electrons through a p-n junction and by the random generation and recombination of hole–electron pairs.

The shot noise generated by a device is modeled by a parallel noise current source. The rms shot-noise current in the frequency band Δf is given by

$$I_{\text{sh}} = \sqrt{2qI\Delta f} \tag{6}$$

where q is the electronic charge and I is the dc current flowing through the device. This equation was derived by Shottky in 1928 and is known as the *Shottky formula.* For a fixed bandwidth, the noise current is independent of frequency so that shot noise has a flat power distribution, i.e., it is white noise. It is commonly assumed that the amplitude distribution of shot noise can be modeled by a Gaussian or normal distribution. Therefore, the relation between the crest factor and rms value for shot noise is the same as it is for thermal noise.

IV. Flicker Noise

The imperfect contact between two conducting materials causes the conductivity to fluctuate in the presence of a dc current [4], [5]. This phenomenon generates what is called *flicker noise* or *contact noise*. It occurs in any device where two conductors are joined together, e.g., the contacts of switches, potentiometers, relays, etc. In resistors, it is caused by the variable contact between particles of the resistive material and is called *excess noise* [6]. Metal film resistors generate the least excess noise, carbon composition resistors generate the most, with carbon film resistors lying between the two. Flicker noise in BJT's occurs in the base bias current. In FET's, it occurs in the drain bias current.

Flicker noise is modeled by a noise current source in parallel with the device. The rms flicker noise current in the frequency band Δf is given by

$$I_f = \sqrt{\frac{K_f I^m \Delta f}{f^n}} \tag{7}$$

where I is the dc current, $n \simeq 1$, K_f is the flicker-noise coefficient, and m is the flicker-noise exponent. In modeling JFET noise at low temperatures, n is not fixed [7]. In modeling base-current flicker noise in the BJT, m is typically in the range $1 < m < 3$ [8]. To simplify the analyses in the following, it is assumed that $n = m = 1$ in all flicker-noise equations. It is straightforward to modify the results for other values of n and m.

In BJT's, flicker noise can increase significantly if the base-to-emitter junction is subjected to reverse breakdown [9]. This can be caused during power supply turn-on or by the application of too large an input voltage. A diode in parallel with the base-to-emitter junction is often used to prevent it. For example, the MAT-02 and MAT-03 low-noise matched dual monolithic BJT pairs have the diodes fabricated as part of the devices.

The power in flicker noise is proportional to the square of I_f which is inversely proportional to the frequency. Because of this, flicker noise is commonly referred to as $1/f$ *noise*, read *"one-over-f noise."* Because it increases at low frequencies, it is also referred to as *low-frequency noise*. Another name that is sometimes used is *pink noise* [10]. This name comes from the optical analog of pink light which has a power density that increases at the longer wavelengths, i.e., at the lower frequencies.

V. Burst Noise

Burst noise is caused by a metallic impurity in a p-n junction [4], [5], [6]. Because it is caused by a manufacturing defect, it is minimized by improved fabrication processes. When burst noise is amplified and reproduced by a loudspeaker, it sounds like corn popping. For this reason, it is also called *popcorn noise*. When viewed on an oscilloscope, burst noise appears as fixed-amplitude pulses of randomly varying width and repetition rate. The rate can vary from less than one pulse per minute to several hundred pulses per second. Typically, the amplitude of burst noise is 2 to 100 times that of the background thermal noise [5]. Burst noise in BJT's is discussed in [11] and [12].

VI. Noise Bandwidth

When a noise voltage is measured, the observed value is dependent on the bandwidth of the measuring voltmeter unless a filter is used to limit the bandwidth to a value that is less than that of the voltmeter. It is common to use such a filter in making noise measurements. The *noise bandwidth* of a filter is defined as the bandwidth of an ideal filter which passes the same rms noise voltage as the filter, where the input signal is white noise [5], [6]. The filter and the ideal filter are assumed to have the same gains.

To express the noise bandwidth of a filter analytically, let $A(f)$ be its voltage gain transfer function and let A_0 be the maximum value of $|A(f)|$, where f is the frequency in hertz. The noise bandwidth B in hertz is given by

$$B = \frac{1}{A_0^2} \int_0^\infty |A(f)|^2 \, df. \tag{8}$$

This equation is interpreted graphically in Fig. 3 for both a low-pass filter and a band-pass filter. In each case, the actual filter response and the response of an ideal filter having the same noise bandwidths are shown. For the noise bandwidths to be the same, the area under the actual filter curve must be equal to the area under the ideal filter curve. For the low-pass case, this makes the two indicated areas equal. A similar interpretation holds for the band-pass case.

There are two classes of low-pass filters which are often used in making noise measurements. The first has n real poles, all with the same frequency. The second is an n-

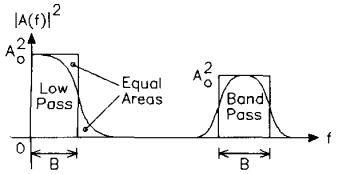


Fig. 3. Graphical interpretation of noise bandwidth for low-pass and band-pass filters.

Table 1. Noise Bandwidth B of Low-Pass Filters

Number of Poles	Slope dB/dec	Real Pole B		Butterworth B
1	20	$1.571f_0$	$1.571f_3$	$1.571f_3$
2	40	$0.785f_0$	$1.220f_3$	$1.111f_3$
3	60	$0.589f_0$	$1.155f_3$	$1.042f_3$
4	80	$0.491f_0$	$1.129f_3$	$1.026f_3$
5	100	$0.420f_0$	$1.114f_3$	$1.017f_3$

pole Butterworth filter. Table 1 gives the noise bandwidth B for each filter as a function of the number of poles n for $1 \leq n \leq 5$. For the real-pole filter, the noise bandwidth is given as a function of both the pole frequency f_0 and the upper -3-dB cutoff frequency f_3. For the Butterworth filter, the noise bandwidth is given as a function of the upper -3-dB frequency. The table shows that the noise bandwidth approaches the -3-dB frequency as the number of poles is increased.

A simple RC low-pass filter such as the one shown in Fig. 2(b) is an example single-pole filter that is often used to limit the bandwidth of noise. This filter has the transfer function $A(f) = 1/(1 + j2\pi fRC)$. The pole frequency is $f_0 = 1/2\pi RC$. From Table 1, the noise bandwidth is given by $B = 1.571/2\pi RC = 1/4RC$.

Band-pass filters are used in making spot noise measurements. The filter bandwidth must be small enough so that the input noise voltage as a function of frequency is approximately constant over the filter bandwidth. The spot noise voltage is obtained by dividing the filter noise output voltage by the square root of its noise bandwidth. A filter that is often used for these measurements is a second-order band-pass filter. Such a filter has a -3-dB bandwidth of f_c/Q, where f_c is the center frequency and Q is the quality factor. The noise bandwidth is given by $B = \pi f_c/2Q$. This is greater than the -3-dB bandwidth by the factor $\pi/2$.

A single-pole high-pass filter cascaded with a single-pole low-pass filter is a special case of a band-pass filter having two real poles. Let the pole frequency of the high-pass filter be denoted by f_1 and that of the low-pass filter be denoted by f_2. The center frequency and the quality factor of the band-pass filter are given by $f_c = (f_1 f_2)^{1/2}$ and $Q = f_c/(f_1 + f_2)$. The noise bandwidth is given by $B = \pi f_c/2Q = \pi(f_1 + f_2)/2$. (Note that the frequencies f_1 and f_2 are not the -3-dB frequencies of the filter. If the -3-dB frequencies are denoted by f_a and f_b, where $f_b > f_a$, the quality factor is also given by $Q = f_c/(f_b - f_a)$. Thus an alternate expression for the noise bandwidth is $B = \pi(f_b - f_a)/2$.)

The noise bandwidth of any filter can be measured if a white-noise source and another filter with a known noise bandwidth are available. With both filters driven simultaneously by the white-noise source, the ratio of the noise bandwidths is equal to the square of the ratio of the output voltages. If V_1 is the rms noise output voltage from a filter with the known noise bandwidth B_1 and V_2 is the rms noise output voltage from a filter with the unknown noise bandwidth B_2, it follows that B_2 is given by $B_2 = B_1(V_2/V_1)^2$.

VII. Measuring Noise

Noise is normally measured at an amplifier output where the voltage is the largest and easiest to measure [5], [6], [10]. The output noise is referred to the input by dividing by the gain. In measuring individual devices, a test fixture can be used to hold the gain constant by use of negative feedback [13]. The measuring voltmeter should have a bandwidth that is at least ten times the noise bandwidth of the circuit being measured [5]. If the voltmeter bandwidth is insufficient, a filter with a known noise bandwidth can be used preceding the voltmeter to limit the bandwidth to a known value.

The voltmeter crest factor is the ratio of the peak input voltage to the full-scale rms meter reading at which the internal meter circuits overload. For a sine-wave signal, the minimum voltmeter crest factor is $\sqrt{2}$. For noise measurements, a higher crest factor is required. For Gaussian noise, a crest factor of 3 gives an error less than 1.5%. A crest factor of 4 gives an error less than 0.5%. To minimize errors caused by an inadequate crest factor, measurements should be made on the lower one-third to one-half of the voltmeter scale to avoid overload on the noise peaks.

A true rms voltmeter is preferred over one which responds to the average rectified value of the input voltage but has a scale calibrated to read rms. When the latter type of voltmeter is used to measure noise, the reading will be low. For Gaussian noise, the reading can be corrected by multiplying the measured voltage by 1.13.

Fairly accurate rms noise measurements can be made with an oscilloscope [14]. A filter must be used to limit the noise bandwidth at its input. Although the procedure is subjective, the rms voltage can be estimated by dividing the observed peak-to-peak voltage by the crest factor [5]. One of the advantages of using the oscilloscope is that non-random noise which can affect the measurements can be identified, e.g., a 60-Hz hum signal.

One method is to display the noise simultaneously on both vertical channels of a dual-channel oscilloscope that is set in the dual-sweep mode. The two channels must be identically calibrated and the sweep rate must not be set too high. The vertical offset between the two traces is adjusted until the dark area between them just disappears. The rms

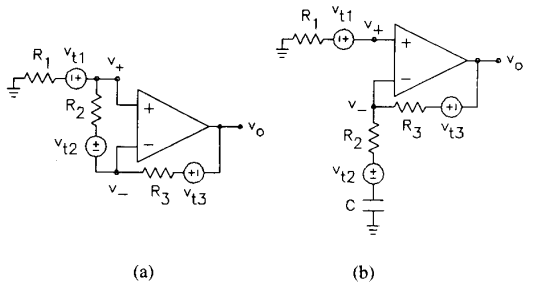


Fig. 4. Circuits used to illustrate addition of noise voltages.

noise voltage is then measured by grounding the two inputs and reading the vertical offset between the traces [15].

VIII. Addition of Noise Voltages

If the models for all noise sources are known, the noise output voltage of a circuit can be calculated by the methods of linear circuit analysis. The output voltage is first calculated as if the instantaneous time-domain value of each source is known. The rms value is then obtained by converting the expression into a root-square sum.

To illustrate this, consider the circuit of Fig. 4(a) consisting of an ideal noiseless operational amplifier (op-amp) and three resistors. Each resistor is modeled by its Thevenin noise model, where the source polarity is arbitrary. Let $R_\Sigma = R_1 + R_2 + R_3$. The instantaneous op-amp input voltages are given by

$$v_+ = v_{t1}(R_2 + R_3)/R_\Sigma + (v_{t2} + v_{t3} + v_o)R_1/R_\Sigma$$

and

$$v_- = (v_{t1} - v_{t2})R_3/R_\Sigma + (v_{t3} + v_o)(R_1 + R_2)/R_\Sigma.$$

The instantaneous output voltage is obtained by setting $v_+ = v_-$ to obtain $v_o = v_{t1} + v_{t2}(R_1 + R_3)/R_2 - v_{t3}$. The rms value of v_o is obtained by converting the expression into a root-square sum by taking the square root of the sum of the squares as follows:

$$\begin{aligned} V_o &= \left[V_{t1}^2 + V_{t2}^2\left(\frac{R_1+R_3}{R_2}\right)^2 + V_{t3}^2\right]^{1/2} \\ &= \left[4kT\left(R_1 + \frac{(R_1+R_3)^2}{R_2} + R_3\right)\Delta f\right]^{1/2} \end{aligned} \quad (9)$$

where the instantaneous voltages have been replaced by the rms voltages. In squaring each term, all negative signs disappear so that the result is independent of the source polarities.

The preceding example illustrates noise calculations when complex impedances are not involved. The circuit of Fig. 4(b) is an example circuit with a complex impedance. The circuit equations are written as if the noise voltages were phasor quantities which are denoted here by bold face letters. Let $Z_1 = R_2 + R_3 + 1/j\omega C$ and $Z_2 = R_2 + 1/j\omega C$, where $\omega = 2\pi f$. The op-amp phasor input voltages are given $\boldsymbol{V}_+ = \boldsymbol{V}_{t1}$ and $\boldsymbol{V}_- = \boldsymbol{V}_{t2}R_3/Z_1 + (\boldsymbol{V}_{t3} + \boldsymbol{V}_o)Z_2/Z_1$. The phasor output voltage $\boldsymbol{V}_o$ is solved for by setting $\boldsymbol{V}_+ = \boldsymbol{V}_-$ to obtain

$$\begin{aligned} \boldsymbol{V}_o = \boldsymbol{V}_{t1}\frac{1 + j\omega(R_2+R_3)C}{1 + j\omega R_2 C} \\ - \boldsymbol{V}_{t2}\frac{j\omega R_3 C}{1 + j\omega R_2 C} - \boldsymbol{V}_{t3}. \end{aligned} \quad (10)$$

This expression is converted into a root-square sum by taking the square root of the sum of the squared magnitudes as follows:

$$\begin{aligned} V_o &= \left[V_{t1}^2\frac{1+\omega^2(R_2+R_3)^2C^2}{1+\omega^2R_2^2C^2} \right. \\ &\quad \left. + V_{t2}^2\frac{\omega^2R_3^2C^2}{1+\omega^2R_2^2C^2} + V_{t3}^2\right]^{1/2} \\ &= \left[4kT\left(R_1\frac{1+\omega^2(R_2+R_3)^2C^2}{1+\omega^2R^2C^2} \right.\right. \\ &\quad \left.\left. + R_2\frac{\omega^2R_3^2C^2}{1+\omega^2R_2^2C^2} + R_3\right)\Delta f\right]^{1/2} \end{aligned} \quad (11)$$

where the phasor voltages have been replaced by rms voltages. This expression is a function of frequency. To evaluate the noise voltage over a band, Δf is replaced by df and the quantity inside the brackets integrated over the band. Alternately, the expression can be converted into a spot noise voltage by dividing both sides by $\sqrt{\Delta f}$.

In the examples presented above, two simplifying assumptions are made. First, it is assumed that the op-amps are noiseless. This is not true for physical op-amps. Second, it is assumed that the noise sources are statistically uncorrelated. This assumption is valid when the noise sources are independent of each other, e.g., when each noise source represents the noise generated by a separate resistor.

IX. The V_n–I_n Amplifier Noise Model

The noise output from any amplifier is a function of the noise generated by the source and the noise generated inside the amplifier. An amplifier noise model can be obtained by reflecting all internal noise sources to the input. In order for the reflected sources to be independent of the source impedance, two noise sources are required—a series voltage source v_n and a shunt current source i_n [16].

Figure 5(a) shows the amplifier noise model, where v_s is the instantaneous source voltage, R_S is the source resistance, and v_{ts} is the instantaneous thermal noise voltage generated by R_S. The instantaneous output voltage is given by

$$v_o = \frac{AR_i}{R_S + R_i}[v_s + (v_{ts} + v_n + i_nR_S)] \quad (12)$$

where A is the voltage gain and R_i is the input resistance. The *equivalent noise input voltage* is the voltage in series with the amplifier input that generates the same noise voltage at the output as all noise sources in the circuit. It is denoted by v_{ni} and is given by the sum of the noise terms in the parentheses in (12).

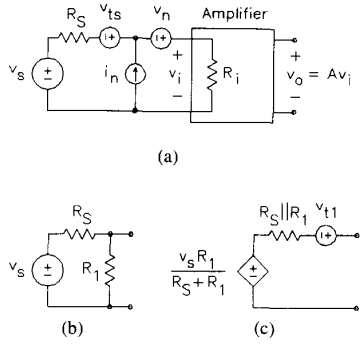


Fig. 5. (a) V_n–I_n amplifier noise model. (b) Source with shunt resistor across output. (c) Thevenin equivalent circuit of source and shunt resistor.

The rms value of v_{ni} is obtained by taking the square root of the time average of

$$v_{ni}^2 = v_{ts}^2 + v_{ts}(v_n + i_n R_S) + v_n^2 + v_n i_n R_S + i_n^2 R_S^2.$$

Because the noise generated by R_S is independent of the noise generated by the amplifier, the average value of the term $v_{ts}(v_n + i_n R_S)$ is zero. However, it cannot be assumed that the average value of $v_n i_n$ is zero. This is because one or more noise sources in the amplifier might contribute to both v_n and i_n. In this case, the correlation coefficient ρ between v_n and i_n must be known. This is defined by

$$\rho = \frac{1}{V_n I_n}\langle v_n i_n \rangle \tag{13}$$

where $\langle v_n i_n \rangle$ represents the time average of $v_n i_n$. The rms value of v_{ni} is then given by

$$V_{ni} = \sqrt{4kTR_S\Delta f + V_n^2 + 2\rho V_n I_n R_S + I_n^2 R_S^2}. \tag{14}$$

The correlation coefficient can take on values in the range $-1 \leq \rho \leq +1$. For the case $\rho = 0$, the sources are said to be *uncorrelated* or *independent*. For R_S very small, $V_{ni} \simeq V_n$ and the correlation coefficient is not important. Similarly, for R_S very large, $V_{ni} \simeq I_n R_S$ and the correlation coefficient is again not important. Unless it can be assumed that $\rho = 0$, the V_n–I_n amplifier noise model can be cumbersome for making noise calculations. For the case $\rho \neq 0$, it is often simpler to use the original circuit with its internal noise sources.

With $v_s = 0$ in (12), the rms noise voltage at the amplifier output is given by

$$V_{no} = \frac{AR_i}{R_S + R_i}\sqrt{4kTR_S\Delta f + V_n^2 + 2\rho V_n I_n R_S + I_n^2 R_S^2}. \tag{15}$$

This equation can be used to solve for V_n and I_n as functions of V_{no} to obtain

$$V_n = \frac{V_{no}}{A}, \qquad \text{for } R_S = 0 \tag{16}$$

$$I_n = \frac{1}{R_S \| R_i}\frac{V_{no}}{A}, \quad \text{for } R_S \text{ large}. \tag{17}$$

These equations suggest methods for measuring V_n and I_n. To measure V_n, V_{no} is measured with the amplifier input terminals shorted and V_n is calculated from (16). To measure I_n, V_{no} is measured with a large value resistor for R_S (ideally $R_S = \infty$) and I_n is calculated from (17). In measuring V_{no}, it is common to use a filter with a known noise bandwidth preceding the voltmeter. The measurements can be converted to spot-noise values by dividing by the square root of the filter noise bandwidth.

X. The Signal-to-Noise Ratio

The decibel *signal-to-noise ratio* (SNR) of the amplifier of Fig. 5(a) is defined by

$$\text{SNR} = 20\log\left[\frac{V_s}{V_{ni}}\right] = 10\log\left[\frac{V_s^2}{4kTR_S\Delta f + V_n^2 + 2\rho V_n I_n R_S + I_n^2 R_S^2}\right]. \tag{18}$$

The source resistance which maximizes the SNR is $R_S = 0$. Although the source resistance is normally fixed, it can be concluded that a series resistor should not be connected between a source and an amplifier if noise performance is a design criterion.

Figure 5(b) shows a source with a shunt resistor connected across its output terminals. To investigate the effect of this resistor on noise, a Thevenin equivalent circuit of the source and shunt resistor is first made. The circuit is shown in Fig. 5(c), where v_{t1} is the instantaneous thermal noise voltage generated by the effective source resistance $R_S \| R_1$. With this circuit connected to the amplifier input in Fig. 5(a), it follows by analogy to (12) that the instantaneous output voltage is given by

$$v_o = \frac{AR_i}{R_S \| R_1 + R_i} \times \left[\frac{R_1}{R_S + R_1}v_s + (v_{t1} + v_n + i_n R_S \| R_1)\right]. \tag{19}$$

The equivalent noise input voltage in series with the amplifier input is given by the sum of the noise terms in the parentheses in this equation.

The source voltage in (19) is multiplied by the factor $R_1/(R_S + R_1)$. To define the instantaneous *equivalent noise input voltage referred to the source*, this term must be factored from the brackets. When this is done, v_o is given by

$$v_o = \frac{AR_i}{R_S \| R_1 + R_i} \times \frac{R_1}{R_S + R_1} \times \left[v_s + \left(1 + \frac{R_S}{R_1}\right)(v_{t1} + v_n + i_n R_S \| R_1)\right]. \tag{20}$$

With the exception of the v_s term, all terms in the brackets in this expression represent the equivalent noise input voltage referred to the source. Let this be denoted by v_{nis}. The rms value is given by

$$V_{nis} = \left[\left(1 + \frac{R_S}{R_1}\right)\left(4kTR_S\Delta f + V_n^2\left[1 + \frac{R_S}{R_1}\right] + 2\rho V_n I_n R_S\right) + I_n^2 R_S^2\right]^{1/2}. \tag{21}$$

The amplifier SNR is given by $\text{SNR} = 20\log(V_s/V_{nis})$. This is maximized when V_{nis} is minimized. The value of R_1 which minimizes this is $R_1 = \infty$. For this value, the SNR expression reduces to the one in (18). When noise is a design criterion, it can be concluded that a resistor should not be connected in parallel with an amplifier input unless the resistor value is large compared to the source resistance.

Both the equivalent noise input voltage v_{ni} and the equivalent noise input voltage referred to the source v_{nis} are defined above. These two voltages are the same if the source is connected directly to the amplifier input terminals. If a coupling network is used between the source and the amplifier, e.g., a bias network, the two voltages are not necessarily the same. In general, to minimize the noise for a particular design, the rms value of v_{nis} should be minimized. This always maximizes the SNR. In the event that $v_{ni} = v_{nis}$, the noise is minimized by minimizing the rms value of v_{ni}.

A bias network consisting of a series element and a parallel (or shunt) element is often required between a source and an amplifier input. From the preceding results, it can be concluded that the series impedance of the bias network should be small compared to R_S and the shunt impedance should be large compared to R_S. For example, a series resistance of $R_S/20$ and a shunt resistance of $20R_S$ can result in a decrease in the SNR by no more than 0.45 dB.

XI. Noise Figure

The decibel *noise figure* (NF) [5], [6] of an amplifier is defined as the difference between its SNR and the SNR if the amplifier were noiseless. It follows from (18) that the noise figure for the amplifier model of Fig. 5(a) is given by

$$\text{NF} = 10\log\left[1 + \frac{V_n^2 + 2\rho V_n I_n R_S + I_n^2 R_S^2}{4kTR_S\Delta f}\right]. \tag{22}$$

A noiseless amplifier has an NF of 0 dB. The value of R_S which minimizes the noise figure is called the *optimum source resistance*. It is given by $R_{S0} = V_n/I_n$. If a signal source has an output resistance R_S that is not equal to the R_{S0} for an amplifier, a resistor should never be connected in series or in parallel with the source to minimize the NF because this decreases the SNR. However, if R_S can be transformed to make $R_S = R_{S0}$, the NF can be decreased and the SNR increased. Adding a transformer between the source and the amplifier is a method of doing this that is discussed in Section XIII.

The NF can be a very misleading specification. If an attempt is made to minimize an amplifier NF by adding resistors either in series or in parallel with the source, the SNR is always decreased. This is referred to as the *noise figure fallacy* [17]. Potential confusion can be avoided if low-noise amplifiers are designed to maximize the SNR. This is accomplished by minimizing the equivalent noise input voltage referred to the source. The low-noise design methods described in this paper are based on this approach.

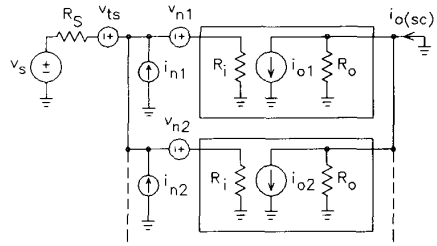


Fig. 6. Circuit used to illustrate noise reduction with parallel devices.

XII. Noise Reduction with Parallel Input Devices

A method which can be used to reduce the noise generated in an amplifier input stage is to realize that stage with several active devices in parallel, e.g., parallel BJT's or parallel FET's [6], [18]. This technique is commonly used in low-noise op-amps. Figure 6 shows a simplified block diagram of an amplifier input stage having N identical devices in parallel. For simplicity, only the first two are shown. The noise source v_{ts} models the instantaneous thermal noise generated by the source resistance R_S. Each amplifier stage is modeled by the V_n–I_n amplifier noise model. The input impedance to each stage is modeled by a resistor. The output circuit is modeled by a Norton equivalent circuit consisting of a parallel current source and resistor. The short-circuit output current from the jth stage can be written $i_{oj} = g_m v_{ij}$, where g_m is the transconductance and v_{ij} is the input voltage for that stage.

The instantaneous short-circuit output current from the circuit can be written

$$\begin{aligned} i_{o(\text{sc})} = g_m \Bigg[& N\frac{\frac{R_i}{N}}{R_S + \frac{R_i}{N}}(v_s + v_{ts}) + N\left(R_S \| \frac{R_i}{N}\right)\sum_{j=1}^{N} i_{\text{nj}} \\ & + \sum_{j=1}^{N}\left(\frac{R_i}{R_i + R_S\|\left(\frac{R_i}{N-1}\right)} v_{nj} \right. \\ & \left. - \frac{R_S\|\left(\frac{R_i}{N-1}\right)}{R_i + R_S\|\left(\frac{R_i}{N-1}\right)} \sum_{\substack{k=1 \\ k\neq j}}^{N} v_{nk}\right)\Bigg]. \end{aligned} \tag{23}$$

To define the equivalent noise input voltage, the term multiplying v_s must be factored from the outer brackets in this equation. All remaining terms with the exception of the v_s term then represent v_{ni}. When this is done and the expression for v_{ni} is converted into a root-square sum, a significant simplification occurs. The final expression for V_{ni} is

$$V_{ni} = \sqrt{4kTR_S\Delta f + \frac{1}{N}V_n^2 + 2\rho V_n I_n R_S + NI_n^2 R_S^2} \tag{24}$$

where ρ is the correlation coefficient between v_n and i_n for any one of the N identical stages.

If $R_S = 0$, (24) reduces to $V_{ni} = V_n/\sqrt{N}$. In this case, the noise can theoretically be reduced to any desired level if N is made large enough. For $R_S \neq 0$, (24) predicts that

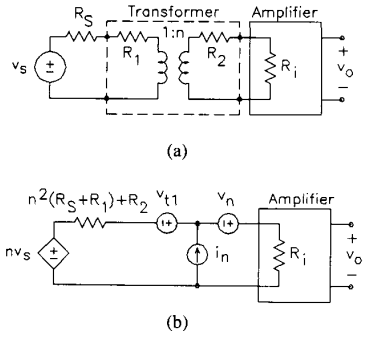


Fig. 7. (a) Signal source coupled to amplifier through ideal transformer. (b) Amplifier with equivalent input circuit.

$V_{ni} \to \infty$ for $N \to 0$ or $N \to \infty$. Thus there is a value of N that minimizes the noise. It is given by

$$N = \frac{V_n}{I_n R_S}. \tag{25}$$

This expression shows that N decreases as R_S increases. It follows that the noise cannot be reduced by paralleling input devices if the source resistance is sufficiently large.

XIII. Noise Reduction with an Input Transformer

A transformer at the input of an amplifier may improve its noise performance. Figure 7(a) shows a signal source connected to an amplifier through a transformer with a turns ratio $1 : n$. Resistors R_1 and R_2, respectively, represent the primary and the secondary winding resistances. Figure 7(b) shows the equivalent circuit seen by the amplifier input with all noise sources shown. The source v_{t1} represents the thermal noise generated by the effective source resistance $n^2(R_S + R_1) + R_2$. By analogy to (12), the instantaneous amplifier output voltage is given by

$$v_o = \frac{AR_i}{n^2(R_S + R_1) + R_2 + R_i} \times \left[nv_s + v_{t1} + v_n + i_n\left(n^2[R_S + R_1] + R_2\right)\right]. \tag{26}$$

The equivalent noise input voltage referred to the source is obtained by factoring the turns ratio from the brackets in (26) and retaining all terms except the v_s term. The expression obtained can be converted into a root-square sum to obtain

$$V_{nis} = \left[4kT\left(R_S + R_1 + \frac{R_2}{n^2}\right)\Delta f + \frac{V_n^2}{n^2} + 2\rho V_n I_n \times \left(R_S + R_1 + \frac{R_2}{n^2}\right) + I_n^2\left(n[R_S + R_1] + \frac{R_2}{n}\right)^2\right]^{1/2} \tag{27}$$

where ρ is the correlation coefficient between v_n and i_n.

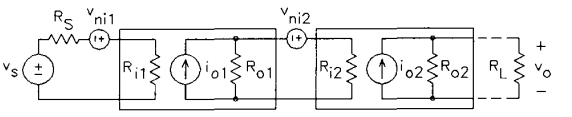


Fig. 8. Diagram of multistage amplifier.

Because the series resistance of a transformer winding is proportional to the number of turns in the winding, it follows that $R_2/R_1 \propto n$. This makes it difficult to specify the value of n which minimizes V_{nis}. In the case that $R_S \gg R_1 + R_2/n^2$, the expression for V_{nis} is given approximately by

$$V_{nis} \simeq \sqrt{4kTR_S\Delta f + \frac{1}{n^2}V_n^2 + 2\rho V_n I_n R_S + I_n^2 n^2 R_S^2}. \tag{28}$$

This is minimized when n is given by

$$n = \sqrt{\frac{V_n}{I_n R_S}}. \tag{29}$$

In this case, the effective source resistance seen by the amplifier is $n^2 R_S = V_n/I_n$. This is the optimum source resistance that minimizes the NF. Thus the NF is minimized and the SNR is maximized simultaneously by the transformer.

The transformer winding resistance can be a significant contributor to the thermal noise at the amplifier input, especially if the source resistance is small. For this reason, a transformer can result in a decreased SNR compared to the case without the transformer [19]. With a BJT input stage, it is shown in Section XVI that the noise can be minimized by biasing the input stage at a particular current. When this is done, a transformer cannot be used to decrease the noise further.

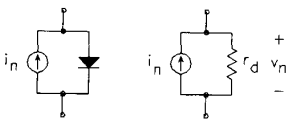
XIV. Noise in Multistage Amplifiers

Multistage amplifiers are commonly analyzed by considering only the noise sources in the input stage. The conditions under which this is valid are discussed in this section. Figure 8 shows a simplified diagram of a multistage amplifier having N stages. For simplicity, only the first two are shown. The instantaneous equivalent noise input voltage for each stage is shown as a series voltage source preceding that stage. The input impedance to each stage is modeled by a resistor. Each output circuit is modeled by a Norton equivalent circuit consisting of a parallel current source and resistor.

The short-circuit output current from the jth stage can be written $i_{oj} = G_{mj}v_{ij(\mathrm{oc})}$, where $v_{ij(\mathrm{oc})}$ is the open-circuit input voltage and G_{mj} is the transconductance gain from the open-circuit input voltage to the short-circuit output current. The latter is given by $G_{mj} = g_{mj}R_{ij}/(R_{o(j-1)} + R_{ij})$, where g_m is the ratio of the short-circuit output current to the actual or loaded input voltage. The open-circuit voltage gain of the jth stage is given by $G_{mj}R_{oj}$.

The overall voltage gain of the circuit can be written

$$K = G_{m1}R_{o1}G_{m2}R_{o2}\cdots G_{mN}R_{oN}\|R_L.$$



(a) (b)

Fig. 9. (a) Noise model of diode. (b) Small-signal noise model of diode.

It is straightforward to show that the output voltage is given by

$$v_o = K\left[v_s + v_{ni1} + \frac{v_{ni2}}{G_{m1}R_{o1}} + \frac{v_{ni3}}{G_{m1}R_{o1}G_{m2}R_{o2}} + \cdots + \frac{v_{niN}}{G_{m1}R_{o1}G_{m2}R_{o2}\cdots G_{m(N-1)}R_{o(N-1)}}\right]. \tag{30}$$

The equivalent noise input voltage v_{ni} is given by the sum of all terms in the brackets in this equation except the v_s term. In the expression for v_{ni}, the equivalent noise input voltage of the second stage is divided by the open-circuit voltage gain of the first stage, that of the third stage is divided by the product of the open-circuit voltage gains of the first and second stages, etc. If the open-circuit voltage gain of the first stage is high enough, the dominant term in the expression for v_{ni} is v_{ni1}. It follows that the noise performance of a multistage amplifier can be analyzed by considering only the noise sources in the input stage if the input stage gain is sufficiently high. This condition is assumed to hold in most of the examples presented in the following.

XV. The Junction-Diode Noise Model

The current in a p-n junction diode consists of two components—the forward diffusion current I_F and the reverse saturation current I_S. The total current is given by $I = I_F - I_S$. The forward diffusion current is a function of the diode voltage V and is given by $I_F = I_S \exp(V/\eta V_T)$, where η is the emission coefficient and V_T is the thermal voltage. (For discrete silicon diodes $\eta \simeq 2$ whereas for integrated circuit diodes $\eta \simeq 1$.) Both I_F and I_S generate uncorrelated shot noise. The total shot noise can be written as a root-square sum of the two shot-noise components and is given by

$$\begin{aligned} I_n &= \sqrt{2q(I_F + I_S)\Delta f} \\ &= \sqrt{2q(I + 2I_S)\Delta f} \\ &\simeq \sqrt{2qI\Delta f} \end{aligned} \tag{31}$$

where the approximation holds for a forward-biased diode for which $I \gg I_S$. Figure 9(a) shows the diode noise model. In Fig. 9(b), the diode is replaced by its small-signal resistance $r_d = \eta V_T/(I + I_S) \simeq \eta V_T/I$. The small-signal open-circuit rms noise voltage across the circuit is given by $V_n = I_n r_d$.

At low-frequencies, the diode exhibits flicker noise. When this is included, the total noise current is given by the root-square sum

$$I_n = \sqrt{2qI\Delta f + \frac{K_f I \Delta f}{f}} \tag{32}$$

where it is assumed that $I \gg I_S$. A plot of I_n versus f for a constant Δf exhibits a slope of -10 dB/*decade* for very low frequencies and a slope of zero for higher frequencies. The two terms under the radical in (32) are equal at the frequency where the noise current is up 3 dB compared to its high-frequency limit. This frequency is called the *flicker-noise corner frequency*. A knowledge of the flicker-noise corner frequency f_f for a diode can be used to calculate the flicker-noise coefficient. It is given by

$$K_f = 2qf_f. \tag{33}$$

Diodes are often used as noise sources in circuits. Specially processed Zener diodes are marketed as solid-state noise diodes. The noise mechanism in these is called *avalanche noise* and it is associated with the diode reverse breakdown current [4]. For a given breakdown current, avalanche noise is much greater than the shot noise in the same current. Avalanche noise diodes have a typical noise density of 0.05 μV *per root hertz* over the frequency range from 10 Hz to 10 MHz [20].

XVI. The BJT Noise Model

The noise analyses of the BJT common-emitter (CE), common-base (CB), and common-collector (CC) amplifiers are given in this section. The load voltage for each amplifier is proportional to the short-circuit output current. This current is calculated for each configuration, and the expression for the equivalent noise input voltage is obtained. The conditions for optimum noise performance are identified.

The principal noise sources in a BJT are thermal noise in the base spreading resistance, shot noise and flicker noise in the base bias current, and shot noise in the collector bias current [1], [4], [21], [22]. The small-signal T-model is used here to calculate the effect of these. Figure 10(a) shows the T-model with the collector node grounded and all noise sources shown. The short-circuit collector output current is labeled $i_{c(sc)}$. The circuit contains two signal sources, one connects to the base (v_1 and R_1) and the other to the emitter (v_2 and R_2). With $v_2 = 0$, the circuit models a CE amplifier. With $v_1 = 0$, it models a CB amplifier.

In the figure, r_x is the base spreading resistance, α is the emitter-to-collector current gain, r_o is the collector-to-emitter resistance, and r_e is the intrinsic emitter resistance. The latter is given by $r_e = \alpha V_T/I_C$, where V_T is the thermal voltage and I_C is the collector bias current. The collector-to-emitter resistance is given by $r_o = (V_{CB} + V_A)/I_C$, where V_{CB} is the collector-to-base bias voltage and V_A is the Early voltage. The collector, emitter, and base bias currents are related by $I_C = \alpha I_E = \beta I_B$, where $\beta = \alpha/(1 - \alpha)$.

The noise sources v_{t1}, v_{tx}, and v_{t2}, respectively, model the instantaneous thermal noise in R_1, r_x, and R_2. The instantaneous shot noise and flicker noise, respectively, in

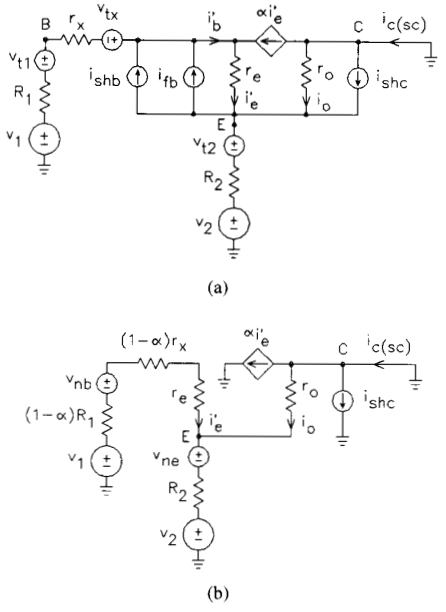


Fig. 10. (a) T-model of BJT with noise sources shown. (b) Equivalent circuit used to solve for $i_{c(sc)}$.

I_B are modeled by i_{shb} and by i_{fb}. The instantaneous shot noise in I_C is modeled by i_{shc}. In the band Δf, the rms values of the noise sources are given by

$$V_{t1} = (4kTR_1\Delta f)^{1/2}$$

$$V_{tx} = (4kTr_x\Delta f)^{1/2}$$

$$V_{t2} = (4kTR_2\Delta f)^{1/2}$$

$$I_{shb} = (2qI_B\Delta f)^{1/2}$$

$$I_{fb} = (K_fI_B\Delta f/f)^{1/2}$$

and

$$I_{shc} = (2qI_C\Delta f)^{1/2}.$$

Figure 10(b) shows an equivalent circuit with Thevenin equivalents made of the noise sources in the base and emitter circuits. Because the left node of the $\alpha i'_e$-controlled source is disconnected from the circuit and connected to ground, the resistors in the base lead must be multiplied by $(1-\alpha)$ in order for the voltage drops across them to be the same. The noise sources v_{nb} and v_{ne} are given by $v_{nb} = v_{t1} + v_{tx} + (i_{shb} + i_{fb})(R_1 + r_x)$ and $v_{ne} = v_{t2} + (i_{shc} - i_{shb} - i_{fb})R_2$. The currents i'_e, i_o, and $i_{c(sc)}$ in this circuit are the same as in the circuit of Fig. 10(a).

The short-circuit output current in Fig. 10(b) is given by $i_{c(sc)} = i_{shc} + \alpha i'_e + i_o$. It will be assumed here that the resistor r_o is large enough so that the current i_o can be neglected in calculating $i_{c(sc)}$. This is an approximation that leads to very little error in practice for the dominant effect of r_o is to set the small-signal collector output resistance.

If i_o is neglected, $i_{c(sc)}$ can be written by inspection from Fig. 10(b) to obtain

$$i_{c(sc)} = i_{shc} + \alpha\frac{v_1 + v_{nb} - v_{ne} - v_2}{(1-\alpha)(R_1 + r_x) + r_e + R_2}. \quad (34)$$

It is convenient to define the BJT transconductance gain G_m by

$$G_m = \frac{\alpha}{(1-\alpha)(R_1 + r_x) + r_e + R_2}. \quad (35)$$

With this definition, (34) can be written

$$i_{c(sc)} = G_m\left[v_1 - v_2 + \left(v_{nb} - v_{ne} + \frac{i_{shc}}{G_m}\right)\right]. \quad (36)$$

The terms in the parentheses in (36) represent the instantaneous equivalent noise input voltage. The expression for v_{ni} can be reduced to

$$v_{ni} = v_{t1} + v_{tx} - v_{t2} + (i_{shb} + i_{fb})(R_1 + r_x + R_2) + i_{shc}\left(\frac{1}{G_m} - R_2\right). \quad (37)$$

This can be converted into a root-square sum over the band Δf to obtain

$$V_{ni} = \left[4kT(R_1 + r_x + R_2)\Delta f + \left(2qI_B\Delta f + \frac{K_fI_B\Delta f}{f}\right)(R_1 + r_x + R_2)^2 + 2\,qI_C\Delta f\left(\frac{R_1 + r_x + R_2}{\beta} + \frac{V_T}{I_C}\right)^2\right]^{1/2}. \quad (38)$$

This expression gives the rms equivalent noise input voltage for both the CE and the CB amplifiers. The SNR for either amplifier is given by SNR $= 20\log(V_i/V_{ni})$, where V_i is the rms value of v_1 for the CE amplifier and the rms value of v_2 for the CB amplifier.

Except at low frequencies, the flicker-noise term in (38) can be neglected. When this is done, V_{ni} can be written

$$V_{ni} = \left[4kT(R_1 + r_x + R_2)\Delta f + 2q\frac{I_C}{\beta}\Delta f(R_1 + r_x + R_2)^2 + 2qI_C\Delta f\left(\frac{R_1 + r_x + R_2}{\beta} + \frac{V_T}{I_C}\right)^2\right]^{1/2}. \quad (39)$$

It can be seen that $V_{ni} \to \infty$ if $I_C \to 0$ or if $I_C \to \infty$. It follows that there is a value of I_C which minimizes V_{ni}. This current is called the *optimum collector bias current* and it is denoted by $I_{C(\text{opt})}$. It is given by

$$I_{C\,(\text{opt})} = \frac{V_T}{R_1 + r_x + R_2} \times \frac{\beta}{\sqrt{1+\beta}}. \quad (40)$$

When the BJT is biased at $I_{C\,(\text{opt})}$, let the equivalent noise input voltage be denoted by $V_{ni\,(\text{min})}$. It is given by

$$V_{ni\,(\text{min})} = \left[4kT(R_1 + r_x + R_2)\Delta f \times \frac{\sqrt{1+\beta}}{\sqrt{1+\beta} - 1}\right]^{1/2}. \quad (41)$$

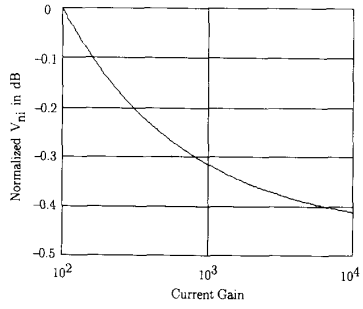


Fig. 11. Plot of decibel change in $V_{ni\,(\min)}$ versus β for BJT.

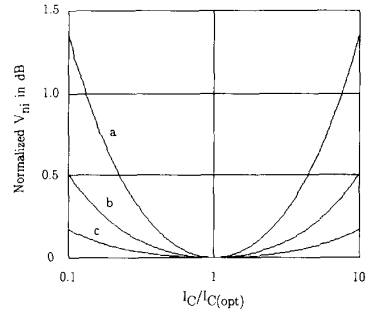


Fig. 12. Plot of $V_{ni}/V_{ni\,(\min)}$ in decibels versus $I_C/I_{C\,(\mathrm{opt})}$ for BJT with a—$\beta = 100$; b—$\beta = 1000$; and c—$\beta = 10\,000$.

For minimum noise, this equation shows that the series resistance in the external base and emitter circuits should be minimized and that the BJT should have a small r_x and a high β.

Although $V_{ni\,(\min)}$ decreases as β increases, the sensitivity is not that great for the range of β for most BJT's. Figure 11 shows a plot of the decibel change in $V_{ni\,(\min)}$ as a function of β for $100 \leq \beta \leq 10\,000$, where the 0-dB reference level corresponds to $\beta = 100$. Most BJT's have a β in the range $100 \leq \beta \leq 1000$. As β increases over this range, $V_{ni\,(\min)}$ decreases by 0.32 dB. Superbeta transistors have a β in the range $1000 \leq \beta \leq 10\,000$ [6]. As β increases over this range, $V_{ni\,(\min)}$ decreases by only 0.096 dB. It can be concluded that only a slight improvement in noise performance can be expected by using higher β BJT's when the device is biased at $I_{C\,(\mathrm{opt})}$.

If $I_C \neq I_{C\,(\mathrm{opt})}$, V_{ni} can be written

$$V_{ni} = V_{ni\,(\min)}\left[1+\frac{0.5\left(I_C/I_{C\,(\mathrm{opt})}+I_{C\,(\mathrm{opt})}/I_C\right)-1}{1+\sqrt{1+\beta}}\right]^{1/2}. \tag{42}$$

Example plots of $V_{ni}/V_{ni\,(\min)}$ versus $I_C/I_{C\,(\mathrm{opt})}$ are given in Fig. 12, where a log scale is used for the horizontal axis. Curve a is for $\beta = 100$, curve b is for $\beta = 1000$, and curve c is for $\beta = 10\,000$. The plots exhibit even symmetry about the vertical line defined by $I_C/I_{C\,(\mathrm{opt})} = 1$. This means, for example, that V_{ni} is the same for $I_C = I_{C\,(\mathrm{opt})}/2$ as for $I_C = 2I_{C\,(\mathrm{opt})}$. In addition, the figure shows that the sensitivity of V_{ni} to changes in I_C decreases as β increases. For example, at $I_C = I_{C\,(\mathrm{opt})}/2$ and $I_C = 2I_{C\,(\mathrm{opt})}$, V_{ni} is greater than $V_{ni\,(\min)}$ by 0.097 dB for $\beta = 100$, by 0.033 dB for $\beta = 1000$, and by 0.010 dB for $\beta = 10\,000$.

Noise specifications for BJT's commonly give measured values for V_n and I_n for the V_n–I_n amplifier noise model. To solve for the theoretical expressions for these, (37) can be written $v_{ni} = v_{t1} - v_{t2} + v_n + i_n(R_1 + r_x + R_2)$, where v_n and i_n are given by $v_n = v_{tx} + i_{shc}V_T/I_C$ and $i_n = i_{shb} + i_{fb} + i_{shc}/\beta$. These expressions can be converted into root-square sums to obtain

$$V_n = \sqrt{4kTr_x\Delta f + 2kT\frac{V_T}{I_C}\Delta f} \tag{43}$$

$$I_n = \sqrt{2qI_B\Delta f + \frac{K_f I_B}{f}\Delta f + \frac{2qI_C}{\beta^2}\Delta f}. \tag{44}$$

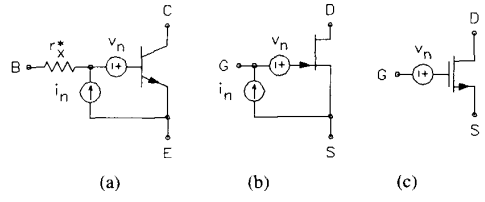


Fig. 13. (a) V_n–I_n noise model for BJT. Asterisk indicates that r_x^* is noiseless, i.e., its noise is included in v_n. (b) Model for JFET. (c) Model for MOSFET.

Because i_{shc} appears in both expressions, the correlation coefficient for v_n and i_n is not zero. If it is assumed that i_{shb}, i_{fb}, and i_{shc} are not correlated, (13) can be used to show that the correlation coefficient for v_n and i_n is given by

$$\rho = \frac{2kT\Delta f}{\beta V_n I_n}. \tag{45}$$

The V_n–I_n BJT noise model is shown in Fig. 13(a). The asterisk indicates that the base spreading resistance r_x^* is considered to be a noiseless resistor.

Equation (44) predicts that a plot of I_n versus frequency would exhibit a slope of -10 dB/decade at low frequencies and a slope of zero at higher frequencies. The *flicker- noise corner frequency* f_f for I_n is the frequency at which I_n is up 3 dB compared to its higher frequency value. This is the frequency for which the center term in the radical in (44) is equal to the sum of the first and last terms. If this frequency is known for a BJT, the flicker-noise coefficient can be solved for. It is given by

$$K_f = 2qf_f\left(1+\frac{1}{\beta}\right). \tag{46}$$

The base spreading resistance r_x is a difficult parameter to measure. This is because r_x is a distributed, variable resistance that is modeled as a lumped-constant resistance. Its value can range from approximately 10 Ω for microwave devices to over several *kilohms* for lower frequency devices [23]. There are several methods for measuring r_x which generally give different values. For this reason, a noise

measurement technique should be used if r_x is to be used in noise calculations [23]. As an example, the LM194 and LM394 are precision matched monolithic n-p-n BJT pairs. These are specified to have a noise equivalent base spreading resistance of 40 Ω [24]. This low value of r_x is accomplished by fabricating each BJT as a number of parallel devices. The design of a low r_x BJT is discussed in [25].

The above analysis shows that the noise performance of the CE amplifier is the same as the CB amplifier. This assumes that the noise generated by the BJT collector load can be neglected. When the load noise is included, this conclusion may no longer be true. To investigate this, let the short-circuit rms noise current generated by the collector load be denoted by $I_{n\ell}$. To account for this noise in (38), the term $I_{n\ell}^2/G_m^2$ must be added inside the brackets, where G_m is given by (35). The effect of $I_{n\ell}$ on the two amplifiers can be compared by comparing the values of G_m for three cases. For the CE amplifier, let $R_1 = R_S$, $R_2 = 0$, and denote G_m by $G_{m\,(\mathrm{CE})}$. For the CB amplifier, let $R_1 = 0$, $R_2 = R_S$, and denote G_m by $G_{m\,(\mathrm{CB})}$. The ratio of $G_{m\,(\mathrm{CE})}$ to $G_{m\,(\mathrm{CB})}$ is given by

$$\frac{G_{m\,(\mathrm{CE})}}{G_{m\,(\mathrm{CB})}} = \frac{(1-\alpha)r_x + r_e + R_S}{(1-\alpha)(R_S + r_x) + r_e}. \tag{47}$$

For $R_S = 0$, the ratio is unity. In this case, the effect of $I_{n\ell}$ on the two amplifiers is the same. For R_S large, the ratio approaches $1/(1-\alpha) = 1+\beta$ so that the effect of $I_{n\ell}$ in the CB amplifier is greater than in the CE amplifier. Therefore, the CE amplifier is the preferred topology for low-noise applications when the source resistance is not low. This conclusion is dependent on the assumed values for R_1 and R_2 in the expression for G_m.

The CC amplifier is often used as a unity-gain buffer between a source and an amplifier. Figure 14 shows the circuit diagram of a CC amplifier with its output connected to the input of a second stage that is modeled with the V_n–I_n amplifier noise model. For simplicity, the bias sources are not shown. The resistor r_x and all BJT noise sources are shown external to the BJT. The source i_{t2} models the thermal noise current in R_2. The voltage across R_i is proportional to the short-circuit current through R_i, i.e., the current i_i evaluated with $R_i = 0$. It is given by

$$\begin{aligned} i_{i\,(\mathrm{sc})} = {} & (G_m/\alpha)[v_1 + v_{t1} + v_{tx} \\ & + (i_{shb} + i_{fb})(R_1 + r_x) + v_n] \\ & - (i_{shb} + i_{fb}) + i_{shc} + i_{t2} + i_n \end{aligned}$$

where G_m is given by (35) with $R_2 = 0$. It follows that the instantaneous equivalent noise input voltage is given by

$$\begin{aligned} v_{ni} = {} & v_{t1} + v_{tx} + v_n + (i_{shb} + i_{fb})(R_1 + r_x - \alpha/G_m) \\ & + (i_{shc} + i_{t2} + i_n)(\alpha/G_m). \end{aligned}$$

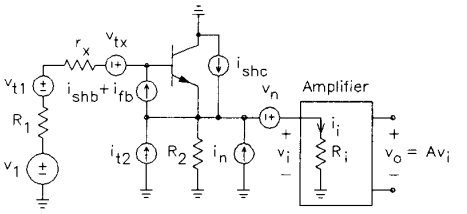


Fig. 14. BJT CC stage connected between signal source and amplifier input.

This can be converted to a root-square sum to obtain

$$\begin{aligned} V_{ni} = \Bigg[& 4kT(R_1+r_x)\Delta f + V_n^2\Delta f + 2\rho V_n I_n \Delta f \\ & \times \left(\frac{R_1+r_x}{1+\beta} + \frac{\alpha V_T}{I_C}\right) + \left(2qI_B\Delta f + \frac{K_f I_B \Delta f}{f}\right)\alpha^2 \\ & \times \left(R_1 + r_x - \frac{V_T}{I_C}\right)^2 + \left(2qI_C\Delta f + \frac{4kT\Delta f}{R_2} + I_n^2\Delta f\right) \\ & \times \left(\frac{R_1+r_x}{1+\beta} + \frac{\alpha V_T}{I_C}\right)^2 \Bigg]^{1/2} \end{aligned} \tag{48}$$

where ρ is the correlation coefficient between v_n and i_n and it is assumed that V_n and I_n are for a bandwidth $\Delta f = 1$ Hz.

It can be seen from (48) that the V_n noise appears directly at the input. The I_n noise is multiplied by $(R_1 + r_x)/(1+\beta) + \alpha V_T/I_C$. If this is less than R_1, the CC amplifier reduces the effect of the I_n noise compared to the case where the source is connected directly to the second stage. The noise voltage generated by the base shot- and flicker-noise currents is independent of the load resistance R_i and can be canceled if $R_1 + r_x - V_T/I_C = 0$. For the case $R_2 = 2kT/qI_C$, the collector shot noise and the thermal-noise current generated by R_2 have equal contributions. For $R_2 \gg 2kT/qI_C = 0.0518/I_C$, the noise generated by R_2 can be neglected.

XVII. Noise in Series-Shunt Feedback Amplifiers

The advantages of negative feedback in amplifier design are well known. This section illustrates the noise analysis of a series-shunt amplifier where the signal source is modeled as a voltage source, e.g., a low output-impedance transducer. The input stage is assumed to be a BJT CE stage. The methods used are applicable to other input stages.

Figure 15(a) shows the simplified diagram of the amplifier with the BJT input stage explicitly shown. The bias sources and networks are omitted for simplicity. This is an example circuit where the BJT is both a CE amplifier and a CB amplifier. It acts as a CE amplifier for the signal source and a CB amplifier for the feedback signal. If the loop gain is sufficiently high, the small-signal voltage gain is approximately the reciprocal of the feedback ratio and is given by $v_o/v_s \simeq 1 + R_F/R_E$.

The circuit in Fig. 15(b) can be used to solve for the equivalent noise input voltage. The figure shows the BJT with its collector connected to signal ground and the circuit seen looking out of the emitter replaced by a Thevenin

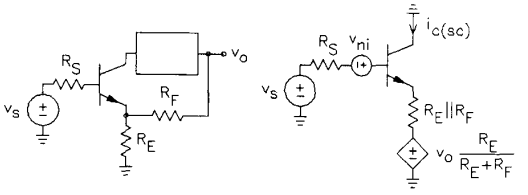


Fig. 15. (a) Series-shunt amplifier. (b) Noise equivalent circuit of input stage.

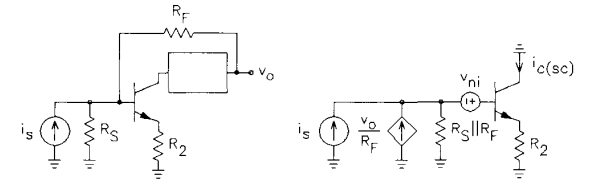


Fig. 16. (a) Shunt–shunt amplifier. (b) Noise equivalent circuit of input stage.

equivalent circuit with respect to v_o. The instantaneous equivalent noise input voltage is modeled by the source v_{ni}. If flicker noise is neglected, the rms value of v_{ni} is obtained from (39) with R_2 replaced with $R_E \| R_F$. It is given by

$$V_{ni} = \left[4kT(R_1 + r_x + R_E \| R_F)\Delta f + 2q\frac{I_C}{\beta}\Delta f(R_1 + r_x + R_E \| R_F)^2 + 2qI_C\Delta f\left(\frac{R_1 + r_x + R_E \| R_F}{\beta} + \frac{V_T}{I_C}\right)^2 \right]^{1/2}. \tag{49}$$

Equations (38) and (40)–(46) also apply with R_2 replaced with $R_E \| R_F$.

For minimum noise, $R_E \| R_F$ should be small compared to $R_1 + r_x$ and the BJT should be biased at $I_{C\,(\mathrm{opt})}$. The resistance $R_E \| R_F$ cannot be zero because the amplifier gain is set by the ratio of R_F to R_E. If the BJT is biased at $I_{C\,(\mathrm{opt})}$ and $R_E \| R_F = R_1 + r_x$, it follows from (41) that the noise is 3 dB greater than for the case where the BJT is biased at $I_{C\,(\mathrm{opt})}$ and $R_E \| R_F = 0$. Note that the value of $I_{C\,(\mathrm{opt})}$ is different for the two cases.

XVIII. Noise in Shunt–Shunt Feedback Amplifiers

This section illustrates the noise analysis of a shunt–shunt amplifier. The signal source is modeled as a current source, e.g., a high output-impedance transducer. The amplifier input stage is assumed to be a BJT CE stage. The methods used are applicable to other stages.

Figure 16(a) shows the simplified diagram of the circuit with the BJT input stage explicitly shown. The bias sources and networks are omitted for simplicity. The signal source is represented by the current source i_s in parallel with the resistor R_S. If the loop gain is sufficiently high, the small-signal transresistance gain is given by $v_o/i_s \simeq -R_F$.

The circuit in Fig. 16(b) can be used to evaluate the input-stage noise performance. The figure shows the BJT with its collector connected to signal ground and the circuit seen looking out of the base replaced by a Norton equivalent circuit with respect to i_s and v_o. The instantaneous equivalent noise input voltage is modeled by the source v_{ni}. The short-circuit collector current $i_{c\,(\mathrm{sc})}$ is given by

$$i_{c\,(\mathrm{sc})} = G_m\left[i_s(R_S \| R_F) + \frac{v_o}{R_F}(R_S \| R_F) + v_{ni}\right] \tag{50}$$

where G_m is given by (35) with R_1 replaced with $R_S \| R_F$.

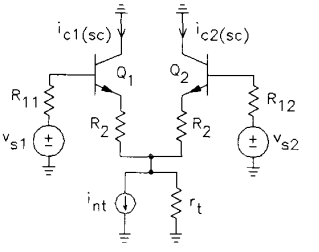


Fig. 17. BJT diff-amp with noise sources.

Because the signal source is a current as opposed to a voltage, the noise equivalent input current i_{ni} in parallel with i_s must be calculated. This is obtained by factoring the coefficient of i_s from (50) and retaining only the term involving v_{ni}. It follows that i_{ni} is given by $i_{ni} = v_{ni}/R_S \| R_F$. When flicker noise is neglected, the rms value of v_{ni} is given by (39) with R_1 replaced with $R_S \| R_F$. It follows that the rms value of i_{ni} is given by

$$I_{ni} = \left[\frac{4kT\Delta f}{R_S \| R_F}\left(1 + \frac{r_x + R_2}{R_S \| R_F}\right) + 2qI_B\Delta f\left(1 + \frac{r_x + R_2}{R_S \| R_F}\right)^2 + 2qI_C\Delta f\left(\frac{1}{\beta} + \frac{1}{R_S \| R_F}\left[\frac{r_x + R_2}{\beta} + \frac{V_T}{I_C}\right]\right)^2\right]^{1/2}. \tag{51}$$

The noise is minimized by making R_2 small and by making R_F large compared to R_S. In addition, the BJT should be biased at $I_{C\,(\mathrm{opt})}$.

XIX. BJT Differential-Amplifier Noise

The differential amplifier (diff-amp) is commonly used as the input stage of op-amps. Figure 17 shows the circuit diagram of a BJT diff-amp. For simplicity, the bias sources are not shown. It is assumed that the BJT's are matched and biased at equal currents. The emitter resistors labeled R_2 are included for completeness. For lowest noise, these should be omitted. The source i_{nt} models the instantaneous noise current generated by the tail current source and the resistor r_t models its output resistance.

For minimum noise output from the diff-amp, the output signal must be proportional to $i_{c1\,(\mathrm{sc})} - i_{c2\,(\mathrm{sc})}$. The subtraction cancels the common-mode noise generated by the tail current i_{nt}. Although a current-mirror active load can be

used to realize the subtraction, the lowest noise performance is obtained with a resistive load. With a resistive load on each collector, a second diff-amp is required to subtract the output signals. The analysis presented here assumes that the circuit output is taken differentially. In addition, it is assumed that r_t is large enough so that it can be approximated by an open circuit. This is equivalent to the assumption of a high common-mode rejection ratio.

The simplest method of analysis is to make use of the results of Section XVI. This is done by solving for an equivalent noise input voltage in series with each BJT base. When solving for the input-noise voltage for one side of the diff-amp, the other side is considered to be noiseless. Let v_{ni1} be the instantaneous equivalent noise input voltage in series with v_{s1} which generates the same noise in $i_{c1\,(sc)}$ as the noise generated by R_{11}, Q_1, and the R_2 in series with the emitter of Q_1. Equation (37) can be used to solve for v_{ni1}. However, the equation must be modified to include the effect of a noiseless resistor in series with the emitter of Q_1. This resistance is $R_2 + r_{ie2}$, where r_{ie2} is the small-signal resistance seen looking into the emitter of Q_2. The latter is given by $r_{ie2} = (1-\alpha)(R_{12} + r_x) + r_e$.

To modify (37), R_2 is replaced with $2R_2 + r_{ie2}$. It follows that v_{ni1} is given by

$$\begin{aligned} v_{ni1} &= v_{t11} + v_{tx1} - v_{t21} + (i_{shb1} + i_{fb1}) \\ &\quad \times (R_{11} + r_x + 2R_2 + r_{ie2}) \\ &\quad + i_{shc1}(1/G_{m1} - 2R_2 - r_{ie2}) \end{aligned}$$

where G_{m1} is given by (35) with R_1 replaced with R_{11} and R_2 replaced with $2R_2 + r_{ie2}$. The components of the collector and emitter currents in Q_1 due to v_{s1} and v_{ni1} are given by

$$i_{c1(sc)} = G_{m1}(v_{s1} + v_{ni1})$$

and

$$i_{e1} = (i_{c1\,(sc)} - i_{shc1})/\alpha + i_{shc1} - i_{shb1} - i_{fb1}.$$

Let v_{ni2} be the instantaneous equivalent noise input voltage in series with v_{s2} which generates the same noise in $i_{c2\,(sc)}$ as the noise generated by R_{12}, Q_2, and the R_2 in series with the emitter of Q_2. By symmetry, it is given by

$$\begin{aligned} v_{ni2} &= v_{t12} + v_{tx2} - v_{t22} + (i_{shb2} + i_{fb2}) \\ &\quad \times (R_{12} + r_x + 2R_2 + r_{ie1}) \\ &\quad + i_{shc2}(1/G_{m2} - 2R_2 - r_{ie1}) \end{aligned}$$

where $r_{ie1} = (1-\alpha)(R_{11} + r_x) + r_e$ is the small-signal resistance seen looking into the emitter of Q_1 and G_{m2} is given by (35) with R_1 replaced with R_{12} and R_2 replaced with $2R_2 + r_{ie1}$. The collector and emitter currents in Q_2 due to v_{s2} and v_{ni2} are given by

$$i_{c2(sc)} = G_{m2}(v_{s2} + v_{ni2})$$

and

$$i_{e2} = (i_{c2\,(sc)} - i_{shc2})/\alpha + i_{shc2} - i_{shb2} - i_{fb2}.$$

By symmetry $G_{m1} = G_{m2} = \alpha/(r_{ie1} + 2R_E + r_{ie2})$, which is denoted by G_m in the following.

The short-circuit collector output current for each side of the diff-amp can be written as the sum of three components—the first is $G_m(v_s + v_{ni})$ for that side of the diff-amp, the second is $-\alpha i_e$ for the other side of the diff-amp, and the third is $\alpha i_{nt}/2$, where it is assumed that i_{nt} divides equally between the emitters of Q_1 and Q_2. (This is strictly true only if $r_{ie1} = r_{ie2}$.) The two output currents are given by

$$\begin{aligned} i_{c1\,(sc)} &= G_m(v_{s1} + v_{ni1} - v_{s2} - v_{ni2}) \\ &\quad + \alpha(i_{shb2} + i_{fb2}) + (1-\alpha)i_{shc2} + \alpha i_{nt}/2 \end{aligned}$$

and

$$\begin{aligned} i_{c2\,(sc)} &= G_m(v_{s2} + v_{ni2} - v_{s1} - v_{ni1}) \\ &\quad + \alpha(i_{shb1} + i_{fb1}) + (1-\alpha)i_{shc1} + \alpha i_{nt}/2. \end{aligned}$$

To define the overall instantaneous equivalent noise input voltage v_{ni}, the difference current $i_{c1\,(sc)} - i_{c2\,(sc)}$ is formed first. The coefficient of $v_{s1} - v_{s2}$ is then factored from the expression and all terms retained except the $v_{s1} - v_{s2}$ term. When the result is converted into a root-square sum, the following expression is obtained:

$$\begin{aligned} V_{ni} = \sqrt{2}\Bigg[& 4kT\left(\frac{R_{11}+R_{12}}{2} + r_x + R_2\right)\Delta f \\ & + \left(2qI_B\Delta f + \frac{K_f I_B \Delta f}{f}\right)\left(\frac{R_{11}+R_{12}}{2} + r_x + R_2\right)^2 \\ & + 2qI_C\Delta f\left(\frac{(R_{11}+R_{12})/2 + r_x + R_2}{\beta} + \frac{V_T}{I_C}\right)^2\Bigg]^{1/2}. \end{aligned} \tag{52}$$

If $R_{11} = R_{12} = R_1$, (52) reduces to $\sqrt{2}$ multiplied by (38). This is 3 dB greater than the equivalent noise input voltage for the CE and CB amplifiers. Above the flicker-noise frequency band, V_{ni} is minimized when each BJT is biased at a collector current given by

$$I_{C\,(opt)} = \frac{V_T}{\frac{R_{11}+R_{12}}{2} + r_x + R_2} \times \frac{\beta}{\sqrt{1+\beta}}. \tag{53}$$

For $R_{11} = R_{12} = R_1$, this expression reduces to (40). The rules for minimizing the diff-amp noise are the same as those for the CE and CB amplifiers.

The LM381 low-noise dual monolithic preamplifier has an input stage that gives the user the option of operating it either as a diff-amp or as a single BJT stage. External leads are provided which can be shorted to remove the second transistor in the diff-amp from the circuit. When this is done, the noise performance is improved by 3 dB [26].

XX. Frequency Response Effects

This section presents two examples which illustrate frequency response effects in noise calculations. The first covers the low-frequency effect of a series coupling capacitor at an amplifier input. The second covers the high-frequency effects of the internal junction and diffusion capacitances of a BJT on the noise performance of a CE amplifier. The methods used in these two examples are applicable in calculating frequency response effects in other circuits.

In general, the objective in a low-noise design is to maximize the signal-to-noise ratio at an amplifier output. This is given by SNR $= 20\log(V_{so}/V_{no})$, where V_{so} is the rms signal output voltage and V_{no} is the rms noise output voltage. Let $V_{so} = AV_s$, where V_s is the rms source voltage and A is the magnitude of the voltage gain, including the gain of an input coupling network. It follows that the SNR can also be written SNR $= 20\log(V_s/V_{nis})$, where $V_{nis} = V_{no}/A$ is the equivalent noise input voltage in series with the source. For a fixed V_s, the SNR is maximized when V_{nis} is minimized. When frequency response effects are considered, the gain A is a function of frequency. The frequency at which A is evaluated should be the frequency of the source. In some cases, this frequency may be different from the frequency at which the noise is evaluated. This is illustrated in the first example below.

Figure 18 shows an amplifier with an input coupling network consisting of a series capacitor C_1 and a shunt resistor R_1. The V_n–I_n amplifier noise model is used for the amplifier. The thermal noise sources for the resistors are shown. To simplify the analysis, the correlation between v_n and i_n will be neglected and it will be assumed that $R_i \gg R_1$. To calculate the amplifier input voltage, phasor notation is used. By superposition, the input voltage is given by

$$\boldsymbol{V}_i = \left(\frac{\boldsymbol{V}_s + \boldsymbol{V}_{ts}}{R_S + 1/j\omega C_1} + \boldsymbol{I}_{t1} + \boldsymbol{I}_n\right) \times \left(R_S + \frac{1}{j\omega C_1}\right)\|R_1 + \boldsymbol{V}_n. \tag{54}$$

To calculate the equivalent noise input voltage referred to the source, the expression for $\boldsymbol{V}_i/\boldsymbol{V}_s$ must be factored from this equation and all terms retained except the $\boldsymbol{V}_s$ term. The expression for $\boldsymbol{V}_i/\boldsymbol{V}_s$ must be evaluated at the source frequency, not the frequency of the noise. In circuits where a series input coupling capacitor is used, the capacitor is usually chosen to be large enough so that it can be considered to be a short circuit at the source frequency (or band of frequencies). In this case, $\boldsymbol{V}_i/\boldsymbol{V}_s = R_1/(R_S+R_1)$. When this is factored from (54), the rms equivalent noise input voltage in series with the source can be solved for to obtain

$$V_{nis} = \left[4kTR_S\Delta f\frac{\omega^2(R_S+R_1)^2C_1^2}{1+\omega^2(R_S+R_1)^2C_1^2} + \left(1+\frac{R_S}{R_1}\right)^2 V_n^2\Delta f + \left(\frac{4kT\Delta f}{R_1} + I_n^2\Delta f\right) \times (R_S+R_1)^2\frac{1+\omega^2R_S^2C_1^2}{1+\omega^2(R_S+R_1)^2C_1^2}\right]^{1/2} \tag{55}$$

where it is assumed that V_n and I_n are for a bandwidth $\Delta f = 1$ Hz. It can be seen that the thermal noise generated by R_S is multiplied by the square magnitude of a high-pass transfer function which approaches 0 as $\omega \to 0$. The V_n noise is independent of frequency. Both the thermal noise generated by R_1 and the I_n amplifier noise are multiplied by the square magnitude of a low-pass shelving transfer function. It can be concluded that C_1 causes the R_S noise to decrease and the R_1 and I_n noise to increase but remain finite as $\omega \to 0$. The total noise voltage in any band can be obtained by replacing Δf with df and integrating the expression inside the brackets over that band.

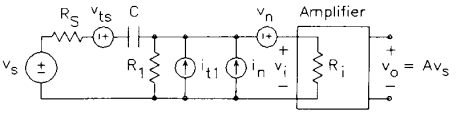


Fig. 18. Circuit used to illustrate effect of coupling capacitor on low-frequency noise.

To illustrate the problems that occur if the incorrect expression for $\boldsymbol{V}_i/\boldsymbol{V}_s$ is factored from the equation for $\boldsymbol{V}_i$, let $\boldsymbol{V}_i/\boldsymbol{V}_s = R_1/(R_S + R_1 + 1/j\omega C_1)$. This is the general frequency-dependent expression for the gain. When it is factored from the expression for $\boldsymbol{V}_i$, the following expression for V_{nis} is obtained:

$$V_{nis} = \left[4kTR_S\Delta f + \left(4kTR_1\Delta f + V_n^2\Delta f + I_n^2\Delta f R_1^2\right)\frac{1+\omega^2R_S^2C_1^2}{\omega^2R_1^2C_1^2}\right]^{1/2}. \tag{56}$$

This expression predicts that the thermal noise generated by R_S is independent of frequency even though there is a series coupling capacitor between the source and amplifier. The thermal noise generated by R_1 and the V_n and I_n amplifier noise are multiplied by the reciprocal of the square magnitude of a high-pass transfer function which approaches ∞ as $\omega \to 0$. These observations certainly do not agree with intuition. The problem is caused by factoring the incorrect expression for $\boldsymbol{V}_i/\boldsymbol{V}_s$ from the equation for $\boldsymbol{V}_i$.

The circuit in Fig. 19 is used for the second example of frequency-response effects. The figure shows the circuit diagram of a BJT CE amplifier in which the base spreading resistance r_x, the collector-to-emitter resistance r_o, the base-to-emitter diffusion capacitance c_π, the collector-to-base depletion capacitance c_μ, and the BJT noise sources are modeled as elements external to the transistor. For simplicity, the bias sources are not shown. The base input resistance is given by $r_\pi = (1+\beta)r_e$. In writing the circuit equations, phasor notation is used. The collector and base currents can be written

$$\boldsymbol{I}_{c\,(\mathrm{sc})} = \beta\boldsymbol{I}_b' - \boldsymbol{I}_{shc} + j\omega c_\mu\boldsymbol{V}_b' \simeq \beta\boldsymbol{I}_b' - \boldsymbol{I}_{shc}$$

and $\boldsymbol{I}_b' = \boldsymbol{V}_b'/r_\pi$ where $\boldsymbol{V}_b'$ is given by

$$\boldsymbol{V}_b' = \left(\frac{\boldsymbol{V}_s + \boldsymbol{V}_{ts} + \boldsymbol{V}_{tx}}{R_S + r_x} + \boldsymbol{I}_{shb} + \boldsymbol{I}_{fb}\right) \times [(R_S + r_x)\|r_\pi]\|\left[\frac{1}{j\omega(c_\pi + c_\mu)}\right]. \tag{57}$$

These equations can be solved for $\boldsymbol{I}_{c\,(\mathrm{sc})}$ to obtain

$$\boldsymbol{I}_{c\,(\mathrm{sc})} = \frac{\beta}{r_\pi}\left[\frac{\boldsymbol{V}_s + \boldsymbol{V}_{ts} + \boldsymbol{V}_{tx}}{R_S + r_x} + \boldsymbol{I}_{shb} + \boldsymbol{I}_{fb}\right] \times \frac{(R_S + r_x)\|r_\pi}{1 + j\omega[(R_S + r_x)\|r_\pi](c_\pi + c_\mu)} - \boldsymbol{I}_{shc}. \tag{58}$$

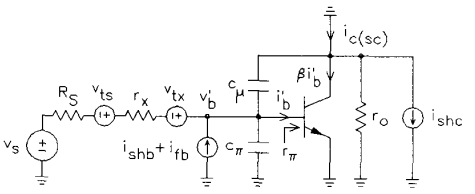


Fig. 19. BJT CE amplifier used to illustrate high-frequency noise calculations.

To calculate the equivalent noise input voltage referred to the source, the coefficient of $\boldsymbol{V}_s$ (evaluated at the frequency of $\boldsymbol{V}_s$) must be factored from (58) and all terms retained except for the $\boldsymbol{V}_s$ term. It will be assumed here that the frequency of the source is equal to the frequency at which the noise is calculated. In this case, the rms noise equivalent input voltage can be written

$$V_{nis} = \left[4kT(R_S + r_x)\Delta f + \left(2qI_B\Delta f + \frac{K_f I_B \Delta f}{f}\right) \times (R_S + r_x)^2 + 2qI_C\Delta f\left(\frac{R_S + r_x}{\beta} + \frac{V_T}{I_C}\right)^2 \times (1 + \omega^2\tau^2)\right]^{1/2} \quad (59)$$

where the time constant τ is given by

$$\tau = [(R_S + r_x)\|r_\pi](c_\pi + c_\mu).$$

It can be seen from this expression that the noise component due to the collector shot noise increases at a rate of 20 dB/dec above the frequency defined by $\omega = 1/\tau$. Thus the signal-to-noise ratio given by SNR $= 20\log(V_s/V_{nis})$ decreases as frequency is increased above that frequency. In reality, the high-frequency noise output from the circuit approaches a constant whereas the signal approaches zero as frequency is increased. Because (59) is derived under the assumption that the frequency at which the noise is evaluated is equal to the source frequency, the equation cannot be used to calculate the noise at a frequency different from that of the source.

XXI. The FET Noise Model

The noise models for the junction FET (JFET) and the metal–oxide–semiconductor FET (MOSFET) are given in this section. The principal noise sources in the FET are thermal noise and flicker noise generated in the channel [1], [4], [27]. For the JFET, this assumes that the gate current is zero. Otherwise, shot noise in the gate current must be included. Flicker noise in a MOSFET is usually larger than in a JFET because the MOSFET is a surface device in which the fluctuating occupancy of traps in the oxide modulates the conducting surface channel all along the channel [1]. The relations between the flicker noise in a MOSFET and its geometry and bias conditions depend on the fabrication process [28]. In most cases, the flicker noise, when referred to the input, is independent of the bias voltage and current and is inversely proportional to the product of the active gate area and the gate oxide capacitance per unit area [4]. Considerations for the design of low-frequency low-noise MOSFET amplifiers are discussed in [29]. Comparisons of bipolar versus CMOS devices for low-noise monolithic amplifier designs are given in [30].

Because the JFET has less flicker noise, it is usually preferred over the MOSFET in low-noise applications at low frequencies. Compared to the silicon JFET, the gallium-arsenide (GaAs) JFET is potentially lower in noise [20]. However, the GaAs JFET can exhibit very high flicker noise, making this device useful only for high frequencies. Because the noise models for the JFET and the MOSFET are essentially the same, the analyses presented in this section apply to both.

It is assumed that the FET is biased in the saturation region. The drain current is given by

$$i_D = K(1 + \lambda v_{DS})(v_{GS} - V_{TO})^2$$

where v_{GS} is the gate-to-source voltage, v_{DS} is the drain-to-source voltage, K is the transconductance parameter, λ is the channel-length-modulation factor, and V_{TO} is the threshold voltage. For the JFET, the transconductance parameter is given by $K = I_{DSS}/V_{TO}^2$, where I_{DSS} is the drain-to-source saturation current and V_{TO} is also called the pinchoff voltage. For the MOSFET, K is given by $K = \mu_o C_{\text{ox}} W/2L$, where μ_o is the average carrier mobility in the channel (denoted by μ_n for the n-type channel and μ_p for the p-type channel), C_{ox} is the gate oxide capacitance per unit area, W is the effective channel width, and L is the effective channel length [31].

Figure 20(a) shows the FET T-model with the drain node grounded and all noise sources shown. For the MOSFET, it is assumed that the small-signal bulk-to-source voltage is zero so that the bulk lead can be omitted from the model. The short-circuit drain output current is labeled $i_{d\,(\text{sc})}$. There are two signal sources in the circuit, one connects to the gate (v_1 and R_1) and the other to the source (v_2 and R_2). With $v_2 = 0$, the circuit models a CS amplifier. With $v_1 = 0$, it models a CG amplifier. The small-signal transconductance is given by

$$g_m = 2[K(1 + \lambda V_{DS})I_D]^{1/2} \simeq 2(KI_D)^{1/2}$$

where I_D is the drain bias current, V_{DS} is the drain-to-source bias voltage, and the approximation assumes that $\lambda V_{DS} \ll 1$. The drain-to-source resistor r_o is given by $r_o = (V_{DS} + 1/\lambda)/I_D$.

The sources v_{t1} and v_{t2}, respectively, represent the instantaneous thermal noise generated by R_1 and R_2. The rms values are $V_{t1} = (4kTR_1\Delta f)^{1/2}$ and $V_{t2} = (4kTR_2\Delta f)^{1/2}$. The source i_{shg} represents the instantaneous shot noise in the JFET gate current. The rms value is given by $I_{shg} = (2qI_G\Delta f)^{1/2}$, where I_G is the gate bias current. This source is omitted in the MOSFET model. In the properly biased JFET, I_G consists of the saturation current of the reverse-biased gate-to-channel junction. In most applications, this is small enough so that it can be neglected.

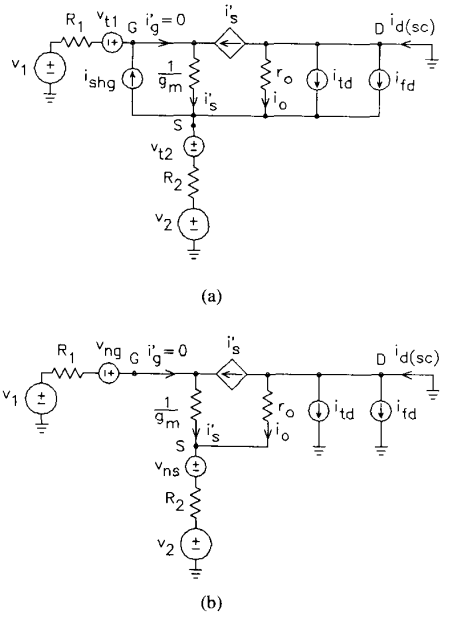


Fig. 20. (a) Noise equivalent circuit of FET. (b) Circuit used to solve for $i_{d\,(sc)}$.

The sources i_{td} and i_{fd}, respectively, represent the instantaneous thermal noise and flicker noise generated in the channel. For both the MOSFET and the JFET, the rms value of i_{td} is given by $I_{td} = [4kT(2g_m/3)\Delta f]^{1/2}$. For the MOSFET, the rms value of i_{fd} is given by $I_{fd} = (K_f I_D \Delta f / f L^2 C_{ox})^{1/2}$, where a typical value for the flicker noise coefficient is $K_f = 10^{-28}$ F · A [31]. For the JFET, the rms value of i_{fd} is given by $I_{fd} = (K_f I_D \Delta f / f)^{1/2}$. The only difference in the equations for I_{fd} for the two devices is the absence of the L^2 and C_{ox} terms in the JFET equation. It follows from the equation for I_{td} that the rms thermal-noise current generated in the channel is the same as the short-circuit thermal-noise current generated by a resistor of value $3/2g_m$.

Figure 20(b) shows an equivalent circuit with Thevenin equivalents made of the noise sources in the external gate and source circuits. The noise sources v_{ng} and v_{ns} are given by $v_{ng} = v_{t1} + i_{shg}R_1$ and $v_{ns} = v_{t2} + (i_{td} + i_{fd} - i_{shg})R_2$. The short-circuit drain current is given by $i_{d\,(sc)} = i_{td} + i_{fd} + i'_s + i_o$. To simplify the calculation of $i_{d\,(sc)}$, it will be assumed that r_o is large enough so that the current i_o can be neglected. This approximation leads to little error in practice because the dominant effect of r_o is to set the small-signal drain output resistance. It follows from Fig. 20(b) that $i_{d\,(sc)}$ is given by

$$i_{d\,(sc)} = i_{td} + i_{fd} + \frac{v_1 + v_{ng} - v_{ns} - v_2}{1/g_m + R_2}. \tag{60}$$

Let the transconductance gain G_m for the FET be defined by

$$G_m = \frac{1}{1/g_m + R_2}. \tag{61}$$

It follows that (60) can be written

$$i_{d\,(sc)} = G_m\left[v_1 - v_2 + \left(v_{ng} - v_{ns} + \frac{i_{td} + i_{fd}}{G_m}\right)\right]. \tag{62}$$

The instantaneous equivalent noise input voltage v_{ni} is given by the terms in the parentheses in this equation. The expression can be reduced to

$$v_{ni} = v_{t1} - v_{t2} + i_{shg}(R_1 + R_2) + (i_{td} + i_{fd})\left(\frac{1}{G_m} - R_2\right). \tag{63}$$

This equation can be converted into a root-square sum over the band Δf to obtain

$$V_{ni} = \left[4kT(R_1 + R_2)\Delta f + 2qI_G(R_1 + R_2)^2\Delta f + \frac{4kT}{3\sqrt{KI_D}}\Delta f + \frac{K_f}{4KfL^2C_{ox}}\Delta f\right]^{1/2} \tag{64}$$

where $I_G = 0$ for the MOSFET and the L^2 and C_{ox} terms are omitted for the JFET.

For minimum noise, it can be concluded from (64) that the series resistance in the external gate and source circuits should be minimized and the FET should have a high transconductance parameter K and a low flicker-noise coefficient K_f. It can be seen that the channel thermal noise decreases as the drain bias current increases. If all noise except the channel thermal noise is neglected, (64) predicts that $V_{ni} \propto I_D^{-1/4}$. This decreases by 1.5 dB each time I_D is doubled.

The JFET gate current is commonly assumed to be zero when the gate-to-channel junction is reverse-biased. For a high source impedance, the effect of the gate current on the noise might not be negligible. In the design of low-noise JFET circuits, particular attention must be paid to the variation of the gate current with drain-to-gate voltage. In general, the gate current increases with drain-to-gate voltage. Some devices exhibit a threshold effect such that the gate current increases rapidly when the drain-to-gate voltage exceeds some value. The drain-to-gate voltage at which this occurs is called the I_G *breakpoint*. It is typically in the range of 8 to 40 V, depending on the particular device [32].

For low-noise applications, the FET should have a high transconductance parameter. For the JFET, this requires a large drain-to-source saturation current and a small threshold or pinchoff voltage. As an example, the CD860 is a dual-matched n-channel JFET pair that is specified as an ultra-low-noise device having the typical parameters $I_{DSS} = 100$ mA, $V_{TO} = -1.5$ V, and $K = 4.4 \times 10^{-2}$ A/V^2. In contrast, the 2N5457 is a general-purpose n-channel JFET having the typical parameters $I_{DSS} = 3$ mA, $V_{TO} = -3$ V, and $K = 3.3 \times 10^{-4}$ A/V^2.

Noise specifications for FET's usually give measured values for V_n and I_n for the V_n–I_n amplifier noise model. To obtain theoretical expressions for these, (63) can be written

$$v_{ni} = v_{t1} - v_{t2} + v_n + i_n(R_1 + R_2)$$

where $v_n = (i_{td} + i_{fd})/g_m$ and $i_n = i_{shg}$. The rms values for v_n and i_n are given by

$$V_n = \sqrt{\frac{4kT}{3\sqrt{KI_D}}\Delta f + \frac{K_f}{4KfL^2C_{ox}}\Delta f} \quad (65)$$

$$I_n = \sqrt{2qI_G\Delta f} \quad (66)$$

where $I_n = 0$ for the MOSFET and the L^2 and C_{ox} terms are omitted for the JFET. It is common to assume that i_{shg} is independent of both i_{td} and i_{fd}. Thus the correlation coefficient between v_n and i_n is zero. Figure 13(b) shows the V_n–I_n noise model for the JFET. Figure 13(c) shows the model for MOSFET. The latter model is valid only when the MOSFET small-signal bulk-to-source voltage is zero.

Measured V_n data for typical NMOS and PMOS devices are given in [31] and [32]. The devices described were fabricated with a 6-μm, silicon-gate, p-well CMOS process. The oxide thickness was 750 Å and the drain current for all measurements was 45 μA. For the NMOS devices, the flicker noise was found to be dominant below 10 kHz. For the PMOS devices, it was found to be dominant below 1 kHz. At 100 Hz, a 100 μm/5 μm NMOS device was found to exhibit a noise voltage of 680 nV per root hertz while a corresponding PMOS device exhibited 120 nV per root hertz. Thus the PMOS device noise was approximately 5 times less than the NMOS device noise.

It can be seen from (65) that a plot of V_n versus frequency would exhibit a slope of -10 dB/decade at low frequencies and a slope of zero at higher frequencies. The *flicker-noise corner frequency* f_f for V_n is defined as the frequency at which V_n is up 3 dB compared to its higher frequency value. This is the frequency for which the two terms in the brackets in (65) are equal. A knowledge of f_f for a FET can be used to calculate the flicker-noise coefficient K_f. It is given by

$$K_f = \frac{16}{3}kTf_fL^2C_{ox}\sqrt{\frac{K}{I_D}} \quad (67)$$

where the L^2 and C_{ox} terms are omitted for the JFET.

XXII. Examples of FET Noise Calculations

Circuit diagrams for a JFET diff-amp and a MOSFET diff-amp can be obtained by replacing the BJT's in Fig. 17 with either JFET's or MOSFET's. The bias sources are not shown in the figure. The source i_{nt} models the tail supply noise current and r_t models its small-signal resistance. The two resistors labeled R_2 are included for completeness. For minimum noise, these should be omitted. Let the output from the diff-amp be taken differentially so that the common-mode noise generated by the tail current source is canceled. The equivalent noise input voltage is given by

$$V_{ni} = \sqrt{2}\left[4kT\left(\frac{R_{11}+R_{12}}{2}+R_2\right)\Delta f + 2qI_G\Delta f\left(\frac{R_{11}+R_{12}}{2}+R_2\right)^2 + \frac{4kT\Delta f}{3\sqrt{KI_D}} + \frac{K_f\Delta f}{4KfL^2C_{ox}}\right]^{1/2} \quad (68)$$

where $I_G = 0$ in the case of the MOSFET and the L^2 and C_{ox} terms are omitted for the JFET. For the case that $R_{11} = R_{12} = R_1$, the expression reduces to $\sqrt{2}$ multiplied by (64). This is 3 dB greater than the equivalent noise input voltage for the CS and CG amplifiers. The rules for minimizing the FET diff-amp noise are the same as those for the CS and CG amplifiers.

In the following, the application of the MOSFET noise model at low frequencies is illustrated for four example circuits. Each MOSFET is modeled by the circuit of Fig. 13(c). It is assumed that the frequency is low enough so that the dominant component of the noise is flicker noise. In this case, the thermal noise term in (65) for V_n is neglected. It is straightforward to modify the results for the higher frequency case where the dominant component of the noise is thermal noise or for the more general case where both thermal noise and flicker noise are included.

The circuits are shown in Fig. 21. The analysis assumes that each transistor is operated in the saturation region and that the noise sources are uncorrelated. Because the MOSFET exhibits no current noise, the output resistance of the signal source is omitted with no loss in generality. In the circuits of Fig. 21(a) and (b), the bulk lead of M2 is connected to a signal ground rather than to the source lead of M2. This might seem to make the noise model of Fig. 13(c) not applicable because the model is derived under the assumption that the small-signal bulk-to-source voltage is zero. However, the noise model is valid when the output from the circuit is taken from the MOSFET source, which is the case for M2 in Fig. 21(a) and (b). This is because the equivalent-noise input voltage is solved for by connecting the output node to signal ground and solving for the short-circuit output current. For this condition, the small-signal bulk-to-source voltage is zero.

Figure 21(a) shows a single-channel NMOS enhancement-mode CS amplifier with an active NMOS enhancement-mode load. It is assumed that the two MOSFET's have matched model parameters, and are biased at the same current. With $v_o = 0$, the small-signal short-circuit output current can be written

$$i_{o\,(sc)} = g_{m1}(v_s + v_{n1}) - g_{m2}v_{n2} = g_{m1}(v_s + v_{ni})$$

where v_{ni} is the instantaneous equivalent noise input voltage given by

$$v_{ni} = v_{n1} - (g_{m2}/g_{m1})v_{n2}.$$

The rms value of v_{ni} is

$$V_{ni} = [V_{n1}^2 + (g_{m2}/g_{m1})^2V_{n2}^2]^{1/2}.$$

When the low-frequency approximation is used for V_n in (65), the expression for V_{ni} can be reduced to

$$V_{ni} = \left[\frac{K_f\Delta f}{2\mu_nC_{ox}^2W_1L_1f}\left(1+\left[\frac{L_1}{L_2}\right]^2\right)\right]^{1/2}. \quad (69)$$

The noise can be reduced by increasing W_1 and L_2 and by making $L_1 = L_2$. The noise is independent of W_2.

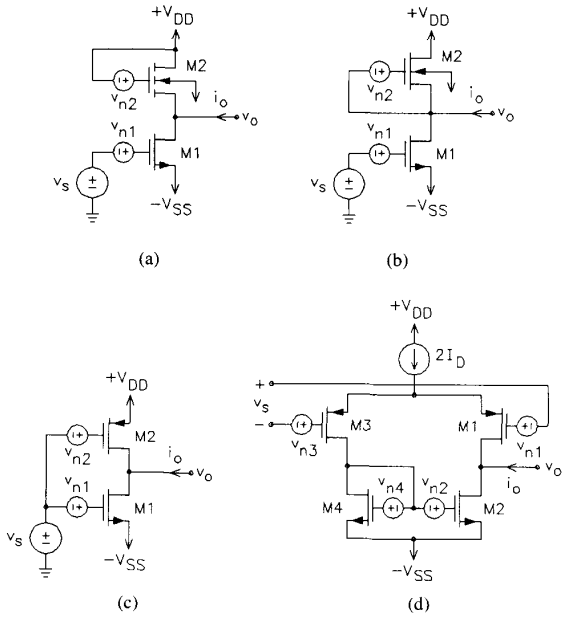


Fig. 21. MOSFET circuits for example noise calculations.

Figure 21(b) shows a single-channel NMOS enhancement-mode CS amplifier with an active NMOS depletion-mode load. It is assumed that the two MOSFET's are biased at the same current. With $v_o = 0$, the expression for $i_{o\,(\mathrm{sc})}$ is the same as for the circuit of Fig. 21(a). Therefore, the expression for v_{ni} is the same. However, the two MOSFET's cannot be assumed to have the same flicker-noise coefficient. The low-frequency expression for V_{ni} is

$$V_{ni} = \left[\frac{K_{f1}\Delta f}{2\mu_n C_{\mathrm{ox}}^2 W_1 L_1 f}\left(1 + \frac{K_{f2}}{K_{f1}}\left[\frac{L_1}{L_2}\right]^2\right)\right]^{1/2}. \quad (70)$$

The noise can be reduced by increasing W_1 and L_2 and by making $L_1 = L_2[K_{f1}/K_{f2}]^{1/2}$. The noise is independent of W_2.

Figure 21(c) shows a push–pull complementary MOSFET (CMOS) amplifier. It is assumed that the two MOSFET's are biased at the same current. With $v_o = 0$, the small-signal short-circuit output current is given by

$$\begin{aligned} i_{o\,(\mathrm{sc})} &= g_{m1}(v_s + v_{n1}) + g_{m2}(v_s + v_{n2}) \\ &= (g_{m1} + g_{m2})(v_s + v_{ni}) \end{aligned}$$

where v_{ni} is the instantaneous equivalent noise input voltage given by

$$v_{ni} = (g_{m1}v_{n1} + g_{m2}v_{n2})/(g_{m1} + g_{m2}).$$

The rms value of v_{ni} is

$$V_{ni} = [g_{m1}^2 V_{n1}^2 + g_{m2}^2 V_{n2}^2]^{1/2}/(g_{m1} + g_{m2}).$$

In order for the quiescent output voltage to be midway between the rail voltages, the circuit is commonly designed with $g_{m1} = g_{m2}$. When this is true and the low-frequency approximation is used for V_n in (65), V_{ni} can be written

$$V_{ni} = \frac{1}{2}\left[\frac{K_{f1}\Delta f}{2\mu_n C_{\mathrm{ox}}^2 W_1 L_1 f} + \frac{K_{f2}\Delta f}{2\mu_p C_{\mathrm{ox}}^2 W_2 L_2 f}\right]^{1/2}. \quad (71)$$

The noise can be decreased by increasing the size of both transistors. For $g_{m1} \neq g_{m2}$, a technique for further reducing V_{ni} is to increase L for the MOSFET for which K_f/μ_o is the largest [29].

Figure 21(d) shows a diff-amp with a current-mirror active load. It is assumed that M1 and M3 have matched model parameters and similarly for M2 and M4. In addition, it is assumed that all four transistors are biased at the same current so that $g_{m1} = g_{m3}$ and $g_{m2} = g_{m4}$. Because the noise generated by the tail source is a common-mode signal, it is canceled at the output by the current-mirror load and is not modeled in the circuit. The differential input voltage is given by $v_{id} = v_s + v_{n1} - v_{n3}$. The component of the small-signal short-circuit output current due to v_{id} is $i_{o\,(\mathrm{sc})} = g_{m1}v_{id}$. To solve for the component of $i_{o\,(\mathrm{sc})}$ due to v_{n2} and v_{n4}, the sources v_s, v_{n1}, and v_{n3} are set to zero. This forces M4 to have zero drain signal current. Thus the gate of M4 is a signal ground and $i_{o\,(\mathrm{sc})} = g_{m2}(v_{n2} - v_{n4})$. The total small-signal short-circuit output current is given by

$$\begin{aligned} i_{o\,(\mathrm{sc})} &= g_{m1}(v_s + v_{n1} - v_{n3}) + g_{m2}(v_{n2} - v_{n4}) \\ &= g_{m1}(v_s + v_{\mathrm{ni}}) \end{aligned}$$

where v_{ni} is the instantaneous equivalent noise input voltage given by

$$v_{ni} = v_{n1} - v_{n3} + (g_{m2}/g_{m1})(v_{n2} - v_{n4}).$$

When the low-frequency approximation is used for V_n in (65), V_{ni} can be written

$$V_{n1} = \sqrt{2}\left[\frac{K_{f1}\Delta f}{2\mu_p C_{\mathrm{ox}}^2 W_1 L_1 f}\left(1 + \frac{K_{f2}}{K_{f1}}\left[\frac{L_1}{L_2}\right]^2\right)\right]^{1/2}. \quad (72)$$

The noise can be reduced by increasing W_1 and L_2 and by making $L_1 = L_2[K_{f1}/K_{f2}]^{1/2}$. The expression is independent of W_2.

Experimental measurements on two diff-amp circuits, as shown in Fig. 21(d), are presented in [29]. The bias current I_D was 5 μA and the bandwidth was limited to 20 Hz–20 kHz. The first circuit had the parameters $W_1 = W_3 = 500\mu$m, $L_1 = L_3 = 5$ μm, $W_2 = W_4 = 100$ μm, and $L_2 = L_4 = 4$ μm. The measured value of V_{ni} was 38 μV. The second circuit had the parameters $W_1 = W_3 = 500$ μm, $L_1 = L_3 = 5$ μm, $W_2 = W_4 = 50$ μm, and $L_2 = L_4 = 44$ μm. The measured value of V_{ni} was 7.5 μV. Thus a five times noise reduction (14 dB) was obtained by increasing the length of the n-channel MOSFET's from 4 to 44 μm. The voltage gain of each circuit was 44 dB.

A CMOS amplifier can be obtained from the circuit of Fig. 21(c) by connecting the gate of M2 to a dc bias source rather than to the signal source. The short-circuit output

current is given by

$$i_{o\,(\mathrm{sc})} = g_{m1}(v_s + v_{n1}) + g_{m2}v_{n2}$$
$$= g_{m1}(v_s + v_{ni})$$

where v_{ni} is the instantaneous equivalent noise input voltage given by $v_{ni} = v_{n1} + (g_{m2}/g_{m1})v_{n2}$. The rms value of v_{ni} is given by (72) divided by $\sqrt{2}$. Thus the CMOS amplifier has an equivalent input noise voltage that is 3 dB less than the CMOS diff-amp of Fig. 21(d).

XXIII. Comparison of the BJT and the FET

An example numerical comparison of the noise performance of the BJT and the FET is presented in this section. Because typical numerical values of device parameters must be assumed, the conclusions may not be applicable to specific devices. However, the example serves to illustrate the differences, in general, between the BJT and the FET. Because flicker noise is so device-dependent, it is neglected. Therefore, the calculations are valid only in the frequency band where flicker noise is negligible. For the BJT, it is assumed that $r_x = 40\ \Omega$ and $\beta = 500$. For the FET, it is assumed that $K = 5 \times 10^{-4}$ A/V^2, $\lambda = 0$, and $V_{TO} = -2$ V. Because V_{TO} is negative, the FET can be considered to be either a JFET or a depletion-mode MOSFET. In the case of a JFET, the drain-to-source saturation current has the value $I_{DSS} = KV_{TO}^2 = 2$ mA.

The equivalent noise input voltage is calculated for each device as a function of the total resistance of the input loop. For the BJT, the noise is calculated both for a constant collector bias current and for the optimum collector bias current $I_{C\,(\mathrm{opt})}$. For the FET, the noise is calculated for a constant drain bias current. For the constant current cases, it is assumed that both the BJT and the FET are biased at 1 mA so that the devices are compared at the same power dissipation. (This assumes the same bias voltage across each device.)

In (39) and (41), let $R_\Sigma = (R_1 + R_2)$. This is the total resistance of the input loop, i.e., the effective source resistance seen by the device. For $I_C = 1$ mA, the BJT noise voltage for $\Delta f = 1$ Hz is calculated from (39) to obtain

$$V_{ni} = 3.58 \times 10^{-14}\left[1.30 \times 10^{7}(R_\Sigma + 40) + 500(R_\Sigma + 40)^2 + (R_\Sigma + 13\,000)^2\right]^{1/2}\ \mathrm{V}/\sqrt{\mathrm{Hz}}. \quad (73)$$

For $I_C = I_{C\,(\mathrm{opt})}$, the BJT noise voltage for $\Delta f = 1$ Hz is calculated from (41) to obtain

$$V_{ni\,(\min)} = 1.32 \times 10^{-10}\sqrt{R_\Sigma + 40} \qquad \mathrm{V}/\sqrt{\mathrm{Hz}}. \quad (74)$$

For $I_D = 1$ mA, the FET noise voltage for $\Delta f = 1$ Hz is calculated from (64) with $I_G = 0$ to obtain

$$V_{ni} = 1.29 \times 10^{-10}\sqrt{R_\Sigma + 471} \qquad \mathrm{V}/\sqrt{\mathrm{Hz}}. \quad (75)$$

Figure 22 shows the plots of V_{ni} versus R_Σ for the three cases. Curve a is a plot of (73). Curve b is a plot of (74). Curve c is a plot of (75). For R_Σ small, the two BJT cases

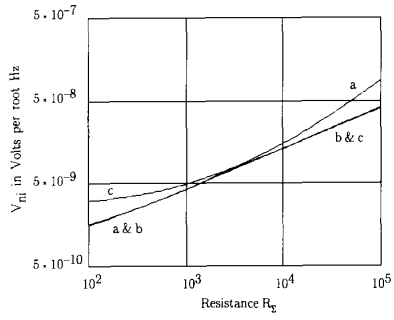


Fig. 22. Plots of V_{ni} versus R_Σ for a—example BJT biased at constant I_C; b—example BJT biased at $I_{C\,(\mathrm{opt})}$; and c— example JFET biased at constant I_D.

give the lowest noise. Although the curves almost coincide, the noise is slightly lower for the BJT biased at $I_{C\,(\mathrm{opt})}$. For R_Σ large, the FET and the BJT biased at $I_{C\,(\mathrm{opt})}$ give the lowest noise. Although the curves almost coincide, the FET noise is slightly lower than the BJT noise. For R_Σ in the 3- to 4-kΩ range, the FET and the BJT biased at $I_C = 1$ mA give approximately the same noise, while the BJT biased at $I_{C\,(\mathrm{opt})}$ gives slightly lower noise.

For the numerical examples, it can be concluded that the BJT gives better noise performance for low R_Σ. For large R_Σ, the BJT and FET give approximately the same noise performance provided that the BJT is biased at $I_{C\,(\mathrm{opt})}$. For large R_Σ, $I_{C\,(\mathrm{opt})}$ for the BJT can become very small. A very small bias current is a disadvantage when the amplifier slew rate, e.g., an op-amp, is a design consideration. For this reason, the FET may be preferable when the source resistance is high.

The above conclusions neglect flicker-noise effects. Flicker noise is so device-dependent that it is difficult to make general conclusions. However, the FET usually exhibits more flicker noise at low frequencies than the BJT. In JFET's not selected for low flicker noise, the flicker-noise corner frequency for V_n can be as high as several kilohertz [20]. In MOSFET's, it can be even higher [4].

A consideration in the noise comparisons of the CE BJT and CS FET amplifiers is the difference in input bias currents. To prevent the BJT base bias current from flowing through the signal source, either a coupling capacitor or an offset current source is required. The value of a coupling capacitor may be large if it is chosen to minimize the noise. Because there is no such thing as a noiseless current source, an offset current source can increase the noise. The zero FET gate current can eliminate the need for the capacitor and offset current source.

XXIV. Operational-Amplifier Noise

Different noise models have been used by manufacturers in specifying op-amp noise performance [5]. All are variations of the V_n–I_n amplifier noise model. When using data specified by a manufacturer, the op-amp user must be certain that he or she understands which model the data applies to. The simplest model is given in Fig. 23. This is

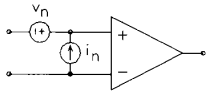


Fig. 23. Op-amp noise model.

the same model used in [18] and [26]. The noise source v_n can be placed in series with either input. In general, the two noise sources in the model are correlated. Two examples are presented here which illustrate the use of the model in evaluating op-amp noise performance.

Specifications for V_n and I_n for an op-amp are made for a bandwidth $\Delta f = 1$ Hz. The Op-27 is a low-noise op-amp having a BJT diff-amp input stage. Each BJT in the diff-amp consists of two BJT's connected in parallel [18]. This effectively halves r_x for each side of the diff-amp. Typical numerical values are 3 to 6 nV per root hertz for V_n, 0.4 to 4 pA per root hertz for I_n, 2 to 3 Hz for the V_n flicker-noise corner frequency, and 100 to 200 Hz for the I_n flicker-noise corner frequency. The TL071 is a low-noise op-amp having a JFET diff-amp input stage and BJT's in the following stages. Typical numerical values are 18 nV per root hertz for V_n, 0.01 pA per root hertz for I_n, and 200 Hz for the flicker-noise corner frequency for V_n.

Figure 24(a) shows a noninverting amplifier with all noise sources shown. The signal source is modeled as a voltage source, e.g., a low-output-impedance transducer. The voltage gain is given by $v_o/v_s = 1 + R_F/R_1$. Let $R_\Sigma = R_1 + R_F$. By superposition, the instantaneous op-amp input voltages are given by

$$v_+ = v_s + v_{ts} + v_n + i_{n1}R_S$$

and

$$v_- = (v_o + v_{tf})R_1/R_\Sigma + v_{t1}R_F/R_\Sigma - i_{n2}R_1\|R_F.$$

The instantaneous output voltage is obtained by setting $v_+ = v_-$ to obtain

$$v_o = \left(1 + \frac{R_F}{R_1}\right)\left[v_s + v_{ts} + v_n + i_n(R_S + R_1\|R_F) - \frac{v_{tf}R_1 + v_{t1}R_F}{R_1 + R_F}\right]. \tag{76}$$

With the exception of the v_s term, the terms in the brackets represent v_{ni}. These can be converted into a root-square sum over the band Δf to obtain

$$V_{ni} = \left[4kT(R_S + R_1\|R_F)\Delta f + V_n^2\Delta f + 2\rho V_n I_n(R_S + R_1\|R_F)\Delta f + I_n^2(R_S + R_1\|R_F)^2\Delta f\right]^{1/2} \tag{77}$$

where ρ is the correlation coefficient between v_n and i_n and it is assumed that V_n and I_n are for $\Delta f = 1$ Hz. For minimum noise, $R_1\|R_F$ should be small compared to R_S.

Figure 24(b) shows an inverting amplifier with all noise sources shown. The signal source is modeled as a current source, e.g., a high-output-impedance transducer. The

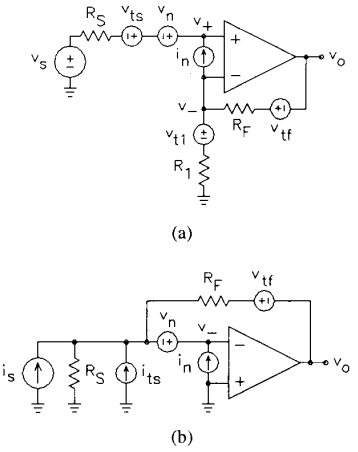


Fig. 24. (a) Noninverting op-amp amplifier. (b) Inverting op-amp amplifier.

transresistance gain is given by $v_o/i_s = -R_F$. The instantaneous voltage at the op-amp input is given by

$$v_- = v_n + (i_s + i_{ts} + i_n)R_S\|R_F + (v_{tf} + v_o)R_S/(R_S + R_F).$$

The instantaneous output voltage is obtained by setting $v_- = 0$ to obtain

$$v_o = -R_F\left[i_s + i_{ts} + \frac{v_{tf}}{R_F} + v_n\left(\frac{1}{R_S} + \frac{1}{R_F}\right) + i_n\right]. \tag{78}$$

With the exception of the i_s term, the terms in the brackets represent the equivalent noise input current i_{ni}. These terms can be converted into a root-square sum over the band Δf to obtain

$$I_{ni} = \left[4kT\left(\frac{1}{R_S} + \frac{1}{R_F}\right)\Delta f + V_n^2\left(\frac{1}{R_S} + \frac{1}{R_F}\right)^2\Delta f + 2\rho V_n I_n\left(\frac{1}{R_S} + \frac{1}{R_F}\right)\Delta f + I_n^2\Delta f\right]^{1/2} \tag{79}$$

where it is assumed that V_n and I_n are for $\Delta f = 1$ Hz and ρ is the correlation coefficient between v_n and i_n. For minimum noise, R_F should be large compared to R_S.

XXV. Design Example

The example design of a low-noise feedback amplifier having a voltage gain of 50 (34 dB) is presented in this section. The circuit is typical of a low-noise microphone preamplifier. The theoretically predicted noise performance of the circuit is compared to that predicted by a SPICE simulation. The noise models used by SPICE are described in [34].

Figure 25 shows the circuit diagram. The amplifier has a diff-amp input stage followed by a second diff-amp which cancels the common-mode noise generated by the tail source. This topology is commonly used in low-noise monolithic op-amps [18]. Resistors R_{C1} and R_{C2} together

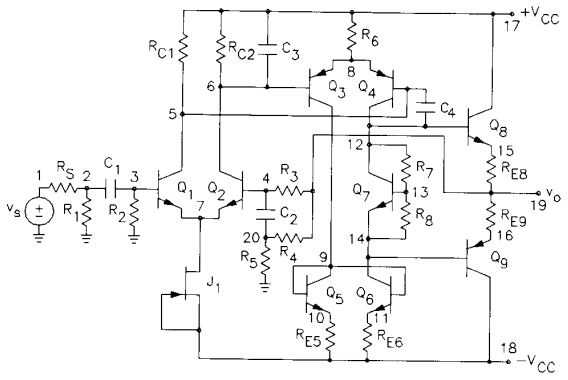


Fig. 25. Circuit diagram for design example with SPICE nodes numbered.

form what is called a *quiet load* on the input diff-amp. A resistor is called a quiet load because it generates less noise than would be generated by an active load [20]. Active loads generate more noise because they amplify their own internal noise [4].

The signal source is assumed to have the resistance $R_S = 200\ \Omega$. This is a typical output resistance for a microphone. For minimum noise, $R_1 \| R_2$ must be large compared to R_S. With $R_1 = R_2 = 40\ \text{k}\Omega$, $R_1 \| R_2 = 20\ \text{k}\Omega$ which is 100 times R_S. The effective midband source resistance is $R_S \| R_1 \| R_2 = 198\ \Omega$. The feedback network consists of R_3, R_4, R_5, and C_2. The midband voltage gain specification requires $1 + (R_3 \| R_4)/R_5 = 50$, where it is assumed that the loop gain is large. For minimum dc offset at the output, $R_2 = R_3$ is required. For the midband resistance seen by each diff-amp input to be the same, $R_S \| R_1 \| R_2 = R_3 \| R_4 \| R_5$ is required. The values $R_3 = 40\ \text{k}\Omega$, $R_4 = 13.2\ \text{k}\Omega$, and $R_5 = 202\ \Omega$ satisfy these conditions.

The outputs from the input diff-amp (Q_1 and Q_2) are connected to the input of a second diff-amp (Q_3 and Q_4) which cancels the common-mode noise generated by $J1$. The second diff-amp has an active current-mirror load (Q_5 and Q_6) which drives the complementary common-collector output stage (Q_8 and Q_9). The base bias voltage for the output stage is provided by a V_{BE} multiplier voltage reference (Q_7). The resistors in the circuit are calculated to bias Q_3 through Q_6 at 1 mA each, Q_7 at 0.75 mA, and Q_8 and Q_9 at 2 mA each.

Capacitor C_1 prevents the base bias current in Q_1 from flowing in the source. Capacitor C_2 gives 100% dc feedback for bias stability. To minimize their effect on noise, these capacitors must be large enough so that each is a signal short circuit in the transfer function for the impedance seen looking out of the bases of Q_1 and Q_2 at audio frequencies. To meet this condition, C_1 and C_2 are calculated so that the zero frequency in each impedance transfer function is 20 Hz. This requires $(R_S \| R_1)C_1 = (R_4 \| R_5)C_2 = 1/40\pi$. The values $C_1 = C_2 = 40\ \mu\text{F}$ satisfy this condition. The lower -3-dB cutoff frequency is set by the zero in the voltage gain transfer function of the feedback network. The lower cutoff frequency is given by

$$f_\ell = (R_4 + R_5)/[2\pi R_5(R_3 + R_4)C_2] = 5\ \text{Hz}.$$

Capacitors C_3 and C_4 frequency compensate the two forward paths in the amplifier and set the gain–bandwidth product. It can be shown that the two capacitors must have the same value and that the gain–bandwidth product is given approximately by $f_x = I_T/4\pi C V_T$, where I_T is the diff-amp tail current and $C = C_3 = C_4$. The upper -3-dB cutoff frequency is given by $f_u = f_x/A$, where A is the magnitude of the voltage gain with feedback. The value of C used in the example is 120 pF. This gives the amplifier an upper cutoff frequency of approximately 1 MHz. The relationships between gain–bandwidth product and upper cutoff frequency of op-amp circuits are discussed in [35].

For Q_1 and Q_2, it is assumed that $r_x = 40\ \Omega$, $\beta = 500$, $V_T = 0.0259$ V, and $T = 300$ K. For the effective source resistance of 198 Ω, the value of $I_{C\,(\text{opt})}$ calculated from (40) is $I_{C\,(\text{opt})} = 2.92$ mA. Equation (42) predicts a decrease in V_{ni} of 0.23 dB if a collector current of 1 mA is used instead of the optimum value. This is the bias current chosen for the example. The current is set by the JFET parameters $V_{TO} = -2$ V and $K = 5 \times 10^{-4}$ A/V^2. The equivalent noise input voltage is calculated by multiplying the value calculated from (42) by $\sqrt{2}$ to obtain $V_{ni} = 2.95 \times 10^{-9}$ V, where it is assumed that $\Delta f = 1$ Hz. This is the V_{ni} in series with either BJT base. To transform V_{ni} into the equivalent noise input voltage referred to the source, it is multiplied by $(1 + R_S/R_1 \| R_2)$ to obtain $V_{nis} = 2.98 \times 10^{-9}$ V per root hertz.

For completeness, the SPICE code used for analysis is given below. The code gives the numerical values of all elements and model parameters used. Although the model parameters used for the JFET and the BJT's are representative, they do not represent the parameters for any specific device. The value for the forward current gain BF is chosen to give Q_1 and Q_2 a β of 500 for the assumed Early voltage $VA = 100$ V. To illustrate the calculation of flicker noise, it is assumed that the flicker-noise corner frequency for I_n has the value $f_f = 150$ Hz. The value of the flicker-noise coefficient is calculated from (46) to obtain $K_f = 4.81 \times 10^{-17}$.

The SPICE code is as follows: LOW-NOISE AMPLIFIER DESIGN EXAMPLE; VPLUS 17 0 DC 15; VMINUS 18 0 DC −15; VS 1 0 AC 1V; RS 1 2 200; R1 0 2 40K; R2 0 3 40K; R3 4 19 40K; R4 19 20 13.2K; R5 0 20 202; R6 8 17 1.5K; R7 12 13 4.4K; R8 13 14 2.6K; RC1 5 17 1.51K; RC2 6 17 1.51K; RE5 10 18 1.5K; RE6 11 18 1.5K; RE8 15 19 100; RE9 16 19 100; C1 2 3 40U; C2 4 20 40U; C3 6 17 270P; C4 5 12 270P; J1 7 7 18 JMOD; Q1 5 3 7 NMOD; Q2 6 4 7 NMOD; Q3 9 6 8 PMOD; Q4 12 5 8 NMOD; Q5 9 9 10 NMOD; Q6 14 9 11 NMOD; Q7 12 13 14 NMOD; Q8 17 12 15 NMOD; Q9 18 14 16 PMOD; .MODEL JMOD NJF (VTO=−2, BETA=5E−4); .MODEL NMOD NPN IS=12.6F BF=448 RB=40 VA=100 TF=240P CJC=6.7P KF=4.81E−17; .MODEL PMOD PNP IS=12.6F BF=448 RB=40 VA=100 TF=240P CJC=6.7P KF=4.81E−17;

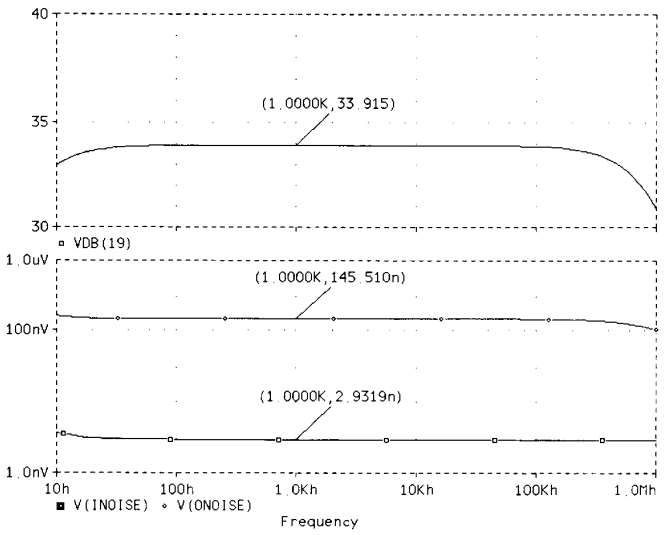


Fig. 26. Gain, input noise, and output noise of example amplifier calculated by SPICE.

.OP; .AC DEC 20 10 1MEG; .NOISE V(19) VS; .PROBE; .END.

Figure 26 shows the results of the SPICE simulation. The upper plot shows the amplifier gain in decibels versus frequency. The gain at 1 kHz is labeled 33.9 dB. The lower plot shows the equivalent noise input voltage referred to the source and the output noise, where the values are calculated for a bandwidth $\Delta f = 1$ Hz. At 1 kHz, the equivalent input noise referred to the source is 2.93 nV. This is greater than the theoretically predicted value by less than 2%. The low frequency rise in the noise due to flicker noise can be seen in the figure. The frequency below which the flicker noise begins to rise is lower than the flicker-noise corner frequency of 150 Hz. This is because the noise sources in the circuit other than I_n noise raise the midband noise level to effectively lower the frequency at which flicker noise appears to rise. SPICE calculates the equivalent noise input voltage referred to the source at any frequency by dividing the output noise by the gain at that frequency. If the source frequency is not equal to the frequency at which the noise is calculated, this can cause V_{nis} to rise artificially at the low and high frequencies. These effects are discussed in Section XX.

XXVI. Concluding Remarks

In a paper of this nature, it would be difficult to give a detailed discussion of all aspects of low-noise design. The topics covered have been chosen to emphasize the fundamentals rather than specific applications. These fundamentals are applicable to both discrete circuit design and integrated circuit design. The paper has been written with two primary objectives. The first is to present a comprehensive treatment of the methods of characterizing and analyzing the noise performance of circuits. The second is to give a description of the noise models of active devices and to show how these models can be used to predict the performance of the devices. Some areas of great importance that are not covered are power supply noise and the effect of grounding and shielding on noise. A comprehensive coverage of grounding, shielding, and methods of decoupling power supply noise are covered in [5].

An extensive literature has been published in the area of noise that dates back as far as the discovery of electrical fluctuations. It would be impossible to reference all of the authors who have written on this topic. The references cited are primarily those which the author has found useful in applications to low-noise circuit design. In addition, several background survey papers are referenced which cover some of the basic theory and give extensive references. An excellent general reference on noise is [36]. This volume contains reprints of 22 papers and several extensive bibliographies.

Acknowledgment

The author wishes to thank Dr. T. E. Brewer and the reviewers for their helpful comments and suggestions.

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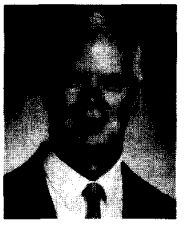

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Prolog to

Fundamentals of Low-Noise Analog Circuit Design

A tutorial introduction to the paper by Leach

Although rapid advances have been made in solid-state devices in the past 40 years, noise in electronic circuits is omnipresent and inevitable. This is because the noise that arises in an electronic device is generated by the basic mechanisms which are responsible for the conduction of current through it. The design of low-noise circuits can be a frustrating experience for circuit designers if the fundamental noise models of devices are not understood. The purpose of this review paper is to describe these models and to show how they are used to calculate noise performance of analog circuits.

The paper begins with a basic definition and overview of the types of electronic noise. Thermal noise is generated when thermal energy causes electrons to move randomly in a resistive material. Shot noise is generated by the random diffusion of holes and electrons through a potential barrier in a semiconductor and by the random recombination of holes and electrons. Flicker noise is caused by the imperfect contact between two conducting materials causing the conductivity to fluctuate in the presence of a direct current. Burst noise is caused by the presence of a metallic impurity in a p-n junction. Basic circuit models for noise sources are described and theoretical expressions for the rms noise voltages and currents are given.

Electrical filters are commonly used to limit the bandwidth of noise in noise measurements. The paper describes the effects of such a filter. The noise bandwidth of a filter is defined and methods for calculating it are described. The noise bandwidths of several commonly used filter topologies are given. In addition, some of the practical aspects of measuring noise are described. These include voltmeter bandwidth and crest factor considerations, correction of noise measurements made with average responding voltmeters, and use of an oscilloscope to measure noise.

The paper illustrates methods for calculating the rms value of the sum of noise voltages and currents. The V_n–I_n amplifier noise model is described. This model is used to define signal-to-noise ratio and to derive conditions under which the noise performance of an amplifier is not degraded by an input coupling network. Two methods for reducing the noise generated by the input stage of an amplifier are described. These are the use of parallel input devices and the use of an input transformer. It is shown that noise in multistage amplifiers is principally determined by the noise generated in the input stage.

The paper covers in detail the noise models of active solid-state devices. These include the junction diode, the bipolar junction transistor (BJT), and the field-effect transistor (FET). Both the junction FET (JFET) and the metal–oxide–semiconductor FET (MOSFET) are covered. Notations and conventions closely correspond to those used in SPICE. For the BJT and the FET, noise is analyzed by calculating the equivalent noise voltage in series with the device input which generates the same noise at its output. Conditions for minimum noise in each device are identified. It is shown that an optimum BJT bias current exists for which the noise is minimized, and the sensitivity of the noise to changes in bias current is analyzed. The V_n–I_n amplifier noise model is derived for both the BJT and the FET.

Additional topics which are covered in the paper include noise in feedback amplifiers, differential-amplifier noise, frequency-response effects, and noise models for operational amplifiers. Example calculations are presented for MOSFET circuits which demonstrate the dependence of noise on device geometry. A comparison of the noise performance of the BJT and the FET is given that illustrates how one device can give less noise than the other. The paper concludes with a design example which illustrates low-noise analysis and design procedures. A SPICE simulation is included which illustrates the use of SPICE for noise calculations.

The paper should be of special interest to solid-state analog circuit designers, researchers in the solid-state circuits area, materials scientists, and physicists. In addition, it should be of general interest to those interested in the fundamentals of noise in analog circuits and its measurement.

—George Likouezos

0018–9219/94$04.00 © 1994 IEEE