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Fuse-Based Short-Circuit Protection of Converter Controlled Low-Voltage DC Grids

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Fuse Based Short-Circuit Protection of Converter Controlled Low Voltage DC Grids

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***Abstract*—Low Voltage DC microgrids emerge as a viable alternative to AC microgrids. A large research interest is noted towards fast and selective protection of DC grids, typically focusing on hybrid or full solid state solutions. In this paper, the use of fuses as short-circuit protection in Low Voltage DC microgrids is evaluated. The main advantage of fuses is that they are simple, cheap, standardized and have low steady state losses. A theoretical basis is formed to model DC short-circuit currents in grids with a limited short-circuit availability. The outcomes are applied to evaluate the possibilities of fuse protection in LVDC grids. It was found that fuses are an effective means of protection, although the required amount of capacitance at the output of the voltage balancing converter can be high, which impacts the total system cost. A fuse based protection strategy is presented that highlights the need for additional capacitance to clear faults compared to the necessary capacitance for system stability. An experimental setup was built to validate the claims.**

I. Introduction

Since several years, there is a wide and growing research interest in Low Voltage DC (LVDC) microgrids. The use of DC is preferred over AC because of the higher power transmission capability and higher efficiency [1]. Furthermore, DC networks show a high compatibility with PV generation, consumption of DC loads and DC battery and fuel cell storage systems [2].

However, the need for fast and selective protection is often referred to as one of the remaining challenges for LVDC grids to break through [3]. An overview of the current state-of-the-art in LVDC protection can be found in [4], [5]. In literature, an assessment and correct application guidelines for fuse based protection is missing. The use of fuses has not been investigated thoroughly for LVDC applications since they are considered as back-up protection [4] or not actively controllable and thus not suitable for future grids [5]. However, in this paper, it will be shown that fuses are a viable alternative for protection of radial LVDC systems and can bridge the gap in protection methods until the development of new solid state circuit breakers is well established. Compared to solid state protection, fuses are less costly and have lower steady state losses.

In [6], fuses are considered as a viable alternative to DC circuit breakers (CBs), although it is highlighted that faults with large time constants (>6 ms) decrease the ability of the fuse to interrupt the current and quench the arc. This issue is also described in technical documents of several manufacturers [7], [8], [9], [10]. However, it is also mentioned that these large time constants are typically found when armatures or field windings of motors need to be protected, which have a very high inductance. However, in LVDC grids, the inductance of cables and connectors is relatively small compared to high inductive motor windings. The authors of [11] focused on developing a model to correctly estimate the arcing time of a specific fuse under DC conditions. Ideal DC sources were considered and the capacitive discharge that characterizes power electronics controlled LVDC systems was thus not taken into account. In [12], the use of fuses is analyzed for 24V systems that are converter controlled. Guidelines are given regarding the minimal capacitance for fuse tripping and voltage dip mitigation. In [1], the authors state that the converters in a microgrid need to be designed with a higher power capacity than the loads would require, such that the steady state fault current is large enough to trip the fuse. In this paper, it will be shown that it is not necessary to overdimension the entire converter. Only the converter output capacitance might need to be increased to provide sufficient short-circuit (SC) current. Besides SC protection, fuses also need to offer protection against indirect contact in TN-S earthed LVDC systems [13].

In [14], meshed LVDC grids are considered. This grid type presents higher current transfer possibilities compared to radial grids. However, power flow controllers are required to avoid that a cable gets overloaded. Furthermore, it is highlighted that selective short-circuit protection is one of the main challenges for meshed LVDC grids [15]. Fuses are used as back-up protection in [16]. However, they do not seem a viable alternative for selective protection in meshed ring type grids since current directionality measurements and typically communication are required to isolate the faulty cable [17]. In [18], a differential current protection methodology for a ring type LVDC microgrid is presented. The authors highlight that fault localization based on current intensity or its derivative cannot accurately distinguish the faulted line in ring type DC microgrids.

The purpose of this paper is to develop a fuse based short-circuit protection strategy for radial LVDC microgrids. The central research question can be formulated as: To what extent can fuses be used in LVDC grids for SC protection and how does this impact the design of the installation as a whole?

Section II is dedicated to modeling of SCs with emphasis on the source behaviour during faults. Furthermore, transient

currents in DC are reviewed. Section III provides methods for fuse selection and indicates how the electrical installation needs to be dimensioned for selectivity and limited voltage dip. In section IV, a case study where fuse protection is considered, is discussed and experimental results are presented. Section V concludes this paper.

II. Modeling short-circuit currents in LVDC grids

In AC, several IEC [19] or IEEE [20] standards can be followed to dimension the protection equipment of the installation. The influence of capacitors is typically neglected as the contribution to the fault current is very momentary and dies out before the breakers or fuses clear [20]. In DC systems, IEC 61660-1 presents a (manual) calculation method for SC currents in DC auxiliary installations [21]. The need for a modification of this standard has been expressed in [22], because only diode rectifier converters are included. Furthermore, batteries are always assumed to be directly connected to the DC grid, which further limits the applicability of the standard. Modeling includes that assumptions need to be made to simplify the system under study, which will be the subject of this section. First, sources and cables are discussed. In contrast to IEC 61660-1, the focus of the considered sources is on power electronics converters. It will be shown that in this case, the fault current is mainly determined by the output capacitance. Then, the transient current step response in DC grids with limited initial energy is reviewed.

A. Source

The focus of this paper is on LVDC grids that are stabilized by power electronics converters, here referred to as Voltage Balancing Converters (VBCs). Direct connection of batteries is thus not considered as the fault behaviour will be different and determined by the battery state of charge [23].

During steady state, the VBC can be represented as a voltage source. The voltage loop controller will keep the voltage stable and within boundaries. A balance exists between the current going to the loads and the current from the VBC. However, when a SC fault occurs, a large fault current will flow that will discharge the VBC output capacitor. Indeed, the unbalance between the VBC current i_{VBC} and the short-circuit current i_{SC} leads to a very rapid decrease of the capacitor voltage v_C as the short-circuit current is mainly drawn from the capacitor. Assuming that the voltage controller reacts when the fault is still present, it will try to counteract this voltage decrease by increasing the reference value of the current controller. The actual increase will depend on the measured voltage dip and the controller parameters. However, even if the VBC delivers its maximum current, which is defined by the physical limitations of the converter, i_{VBC} will still be considerably lower than i_{SC}. Therefore, it is neglected to describe the source behavior during the fault:

$$i_{SC} = i_C + i_{VBC} \approx i_C \tag{1}$$

As long as the fault is present, the VBC can thus be represented by the output capacitor in series with the Equivalent Series Resistance (ESR). For higher accuracy, the Equivalent Series Inductance (ESL) can be included as well, but this value is not always given in the datasheet. When the fault is cleared, the voltage will start to increase again. The time it takes to fully recover to the nominal voltage, will depend on the depth of discharge, the maximum VBC current and the capacitance. During the recovery time, the VBC can be represented as a current source in parallel with a capacitor. An overview of the different VBC models is given in Fig. 1.

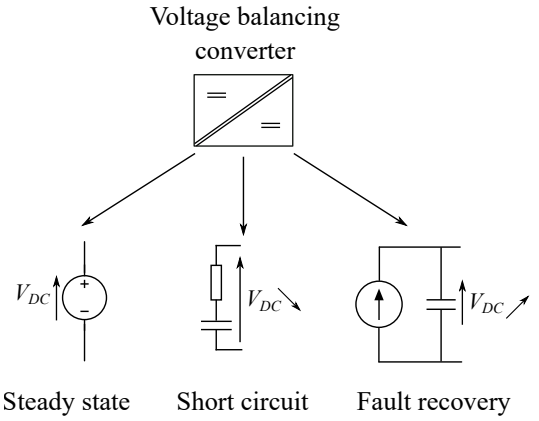

Fig. 1: The equivalent model of the VBC depends on the circuit conditions.

The speed of the voltage controller, and thus of the recovery, is physically limited by the maximum VBC current, the switching frequency (f_s) and the speed of the inner current loop of the VBC. As a rule of thumb, the current controller is tuned to regulate the current within 10 switching cycles or more, which means that the highest bandwidth is around one tenth of f_s [24]. The voltage controller follows a similar philosophy and cannot be faster than one tenth of the current controller bandwidth. When, for example, a VBC operates at f_s = 50 kHz, the current and voltage controller bandwidth are assumed to be 5 kHz and 500 Hz.

Note that the switching frequency of the VBC is also dependent on the voltage level, power level and the transistor technology. Higher frequencies are beneficial to increase the converter power density. However, the maximum temperature increase of the transistor imposes an upper limit on the switching frequency due to the switching losses [24]. In [25], IGBTs are used for a 900 V, 4.8 kW prototype switching at 20 kHz. In [26], Si MOSFETs are operated between 30...70 kHz in a 2 kW, 600 V VBC. Also wide bandgap components such as SiC MOSFETs are possible candidates. The reduced switching time allows to increase the switching frequency considerably. SiC MOSFETs are used at a switching frequency of 200 kHz in a 6 kW VBC prototype in [27].

B. Cable

In DC steady state conditions, the voltage drop across a cable is determined solely by the cable resistance. For transient phenomena, such as short-circuits, the cable inductance will limit the di/dt of the currents and should therefore be taken into account for the modeling. The cable capacitance will form

a resonant network with the inductance and can be taken into account when very detailed calculations are aimed at. However, the capacitance is usually not found in manufacturer datasheets of low voltage cables. In the remainder of this paper, the cable capacitance will be neglected.

C. Short-circuit calculations

In this subsection, the prospective short circuit current of sources with limited initial energy, stored in the capacitors, is reviewed. In comparison, traditional AC systems have a high amount of rotating inertia available from the synchronous generators. However, also in AC, concerns have been expressed regarding the impact on grid stability [28] and protection [29] due to the increasing amount of converter interfaced generators.

'Prospective' means that the current is calculated without the influence of protection devices. The protection equipment's resistance will reduce the amplitude of the fault current. This section provides a short review on the current step response in first and second order circuits. It is included as the results are a necessary basis for section III, where they are used to verify if fuses will operate or not.

1) RC model: The governing differential equation of a capacitor with initial voltage V_0 that discharges on a purely resistive load R, can be found by applying Kirchoff's Voltage Law (KVL):

$$-\frac{1}{C}\int i(t)dt = R \cdot i(t) \tag{2}$$

This is a first order system with an exponentially decaying current, given by:

$$i(t) = \frac{V_0}{R}e^{-t/\tau} \tag{3}$$

with time constant $\tau = RC$.

2) RLC model: The dynamic behaviour of a capacitor discharge on a resistive-inductive load is again determined by applying KVL:

$$-\frac{1}{C}\int i(t)dt = R \cdot i(t) + L\frac{di(t)}{dt} \tag{4}$$

The step response of this second order differential equation depends on the component parameters. Three cases can be considered, of which two have practical relevance. Firstly, if $R^2 < \frac{4L}{C}$, the response is underdamped (UD) and the current is given by:

$$i_{UD}(t) = \frac{V}{\omega_1 L}e^{\frac{-R}{2L}t}\sin(\omega_1 t) \tag{5}$$

where V is the initial capacitor voltage and ω_1 the damped natural frequency of the system:

$$\omega_1 = \sqrt{\frac{1}{LC} - (\frac{R}{2L})^2} \tag{6}$$

Secondly, when $R^2 = \frac{4L}{C}$, the system is critically damped (CD). However, it is unlikely that this criterion is exactly met and the analysis is therefore omitted.

Thirdly, when $R^2 > \frac{4L}{C}$, the system has an overdamped (OD) response, given by:

$$i_{OD}(t) = \frac{V}{\omega_1 L}e^{\frac{-R}{2L}t}\sinh(\omega_1 t) \tag{7}$$

In this equation, V and ω_1 are again, respectively, the initial capacitor voltage and the damped natural frequency. However, ω_1 is now expressed as:

$$\omega_1 = \sqrt{(\frac{R}{2L})^2 - \frac{1}{LC}} \tag{8}$$

Note that the focus is put on circuits with a low initial energy, stored in the capacitor. In other works, typically an ideal voltage source is assumed and the focus is on applications with very high inductance (e.g. motors) that limit the rise time of the current. Those circuits are typically modeled as a constant voltage source (strong DC grid, e.g. battery powered) with an RL load, and the behaviour is thus very different.

III. Fuses as short-circuit protection

A fuse is characterized by several parameters that can be found in the datasheet and that allow a correct selection for a specific application. An overview of these parameters can be found in [30]. In this section, the use of fuses as short-circuit protection in the context of LVDC is treated, focusing on the available I^2t, the peak current in DC grids, selectivity and the voltage dip.

A. System I^2t value

The I^2t value or joule integral of a fuse expresses the amount of heat energy that is transmitted to the system when a SC occurs, before the fuse opens. It depends on the physical construction such as the material and dimensions of the fuse element. Note that the unit is A^2s and not joules, so strictly speaking this is not an energy value [30]. Two I^2t values are typically defined: The pre-arcing (or melting) I^2t defines the required amount of A^2s to start the melting of the fuse. The total I^2t defines the total amount of A^2s that is transmitted after the arcing has stopped and the fuse is completely open.

The fuse I^2t value can be found in the datasheet. For a fuse to blow as a consequence of a SC, sufficient energy needs to be available. The time integral of the current that is provided by the system needs to be larger than the fuse I^2t value:

$$I^2t_{system} > I^2t_{fuse} \tag{9}$$

where I^2t_{system} is defined as:

$$I^2t_{system} = \int_{t=0}^{t=\infty} i^2(t)dt \tag{10}$$

To verify whether enough energy is available to blow the fuse, the system I^2t thus needs to be calculated. The calculation of the above integral is dependent on the system model and the system parameters. The capacitors are considered to be charged to the DC grid voltage level V.

In case of an RC circuit, or when the circuit inductance is neglected, the system I^2t value can be calculated to be:

$$I^2t_{system,RC} = \frac{CV^2}{2R} \tag{11}$$

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In essence, the system I^2t value is this given by the energy in the capacitor, divided by the total resistance of the circuit.

When the inductance is taken into account, the expression for the I^2t value of the system becomes more complicated, and differs for the UD and OD case.

$$\begin{aligned} I^2t_{system,UD} &= \frac{V^2}{\omega_1^2 L^2} \cdot \left(\frac{L}{2R} - \frac{R/L}{2((R/L)^2) + 4\omega_1^2}\right) \\ &= \frac{CV^2}{2R} \end{aligned} \tag{12}$$

$$I^2t_{system,OD} = \frac{2LV^2}{R^3 - 4RL^2\omega_1^2} = \frac{CV^2}{2R} \tag{13}$$

Despite the different waveform of the current in the three cases, the system I^2t value is identical, since the initial amount of energy is equal and assumed to be stored in the capacitor. This is interesting from a practical point of view, as the system I^2t value can correctly be estimated without prior knowledge of the inductance. The energy that is required for the fuse to melt is extracted from the electrical circuit. The practical relevance of I^2t_{system} is that it will express whether there is sufficient energy available to blow the fuse or not.

However, care should be taken when interpreting this result as no time aspect is taken into account. The upper limit of the integral was set to infinity from a theoretical perspective to obtain the total I^2t_{system} value. From a practical point-of-view, the current will approximately reach zero after 5τ. It was highlighted in section II that the time constant differs for RC and RLC circuits. The prospective short-circuit transient will decay the fastest for the RC case and the fuse I^2t value will thus be reached faster as well. For more inductive circuits, the time constant is higher and the transient thus takes longer. This also means that the heat that is required to blow the fuse is generated over a longer interval and the total clearance time will be longer. This is also shown in Fig. 2, where the primitive functions of the different integrals evaluated over 0 to t (Eqns. (14) - (16)), are plotted, for V = 380 V, C = 100 μH, R = 0.01 Ω and increasing L. It can be seen that for a fuse with a given I^2t rating, the fuse will always blow fastest when L = 0. When L increases, the time to reach the required I^2t does too.

$$\int_0^t i_{RC}^2(t)dt = -\frac{CV^2}{2R}(e^{-2t/(RC)} - 1) \tag{14}$$

$$\begin{aligned} \int_0^t i_{UD}^2(t)dt = \frac{CV^2}{2R} - \Big(\frac{V^2}{\omega_1^2 L^2}\Big(\big(e^{-Rt/L}(2\omega_1 \sin(2\omega_1 t) \\ - \frac{(R/L)\cos(2\omega_1 t)}{2((R/L)^2 + 4\omega_1^2)} + \frac{L}{2R}e^{-Rt/L}\big)\Big)\Big) \end{aligned} \tag{15}$$

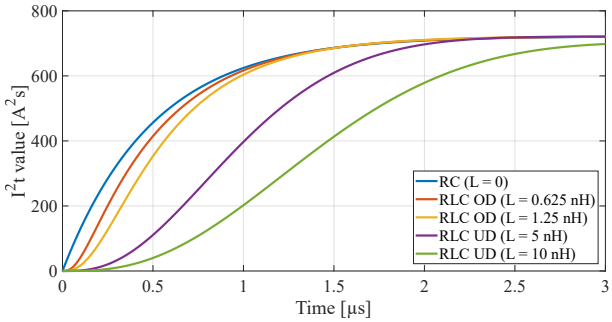

Fig. 2: Developed I^2t as a function of time for V = 380 V, C = 100 μF, R = 0.01 Ω and increasing L.

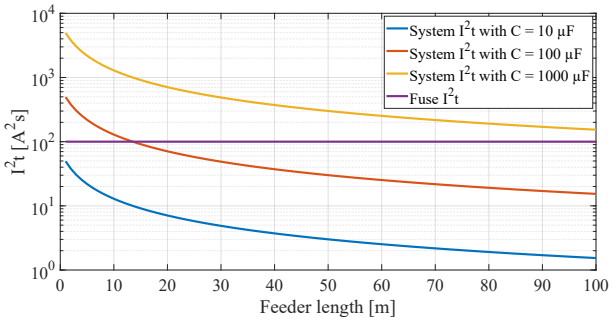

Fig. 3: Comparison of system and fuse I^2t for a 4 mm^2 feeder for different capacitance values.

$$\begin{aligned} \int_0^t i_{OD}^2(t)dt = \frac{CV^2}{2R} - (LR^2(V^2(e^{-2\omega_1 t} + e^{2\omega_1 t})/4 \\ - V^2/2) + 2L^3V^2\omega_1^2 - L^2RV^2\omega_1 \\ (e^{-2\omega_1 t} - e^{2\omega_1 t})/2) \\ \cdot \frac{1}{L^2\omega_1^2 e^{Rt/L}(R^3 - 4L^2R\omega_1^2))} \end{aligned} \tag{16}$$

Equations (11)-(13) are applied to a feeder with increasing length that is fed from a VBC with different output capacitance (C = 10, 100 or 1000 μF). A feeder with a cross section of 4 mm^2 is considered, of which the resistance and inductance are given by the manufacturer as 0.0046 Ω/m and 0.285 μH/m. The capacitance in the grid is constant per case but the resistance and inductance increase linearly with the length. The results are plotted in Fig. 3. The violet horizontal line represents the I^2t_{fuse} and was set to 100, as an example. It can be seen that, when the output capacitance C = 10 μF, there is not sufficient energy available to blow the fuse in case of a SC. When C = 100 μF, the fuse will blow when the cable length does not exceed 13 m. For C = 1000 μF, the cable length can be 100 m or more and the fuse will still operate.

For a given cable, the minimal output capacitance of the VBC C_{VBC} can be calculated by combining Eqns. (9) and (11):

$$C_{VBC} > \frac{I^2t_{fuse}V^2}{2R} \tag{17}$$

In which R is the total resistance of the line.

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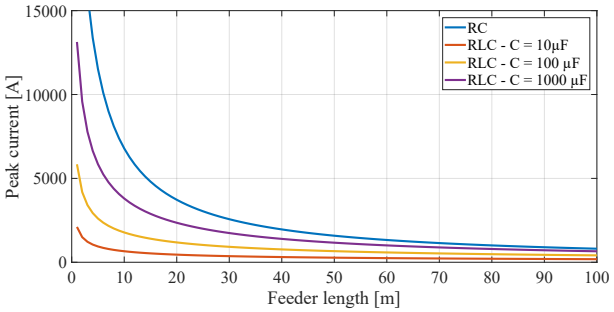

Fig. 4: Comparison of the peak current for increasing feeder length and different capacitance values.

B. Peak current

The interruption rating (IR) is the maximum current that a fuse can safely interrupt, without being damaged. In an application, the maximum fault current that can occur in the system should not exceed the selected fuse interruption rating.

The peak current thus needs to be calculated for correct fuse selection. The peak current depends on the system parameters. In case of an RC circuit, the peak current is given by:

$$I_{peak,RC} = \frac{V}{R} \tag{18}$$

and occurs at time t = 0 (immediately after the fault).

In case of an underdamped RLC circuit, the peak current can be found by differentiating Eqn. (5) and equate the result to zero. It is given by:

$$I_{peak,UD} = \frac{V}{\omega_1 L} e^{(\frac{-R}{2\omega_1 L}) \arctan(\frac{2\omega_1 L}{R})} \cdot \sin(\arctan(\frac{2\omega_1 L}{R})) \tag{19}$$

and occurs at time t = $\frac{1}{\omega_1} \arctan(\frac{2\omega_1 L}{R})$

In case of an overdamped RLC circuit, the peak current is given by:

$$I_{peak,OD} = \frac{V}{\omega_1 L} e^{(\frac{-R}{4\omega_1 L} \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L}))} \cdot \sinh(0.5 \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L})) \tag{20}$$

and occurs at time t = $\frac{1}{2\omega_1} \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L})$

The latter can however be approximated by: $I_{peak,OD} \approxeq \frac{V}{2\omega_1 L}$, when only the dominant time constant is considered.

The above expressions were again evaluated for a 4 mm^2 feeder with increasing length and different C_{VBC}. The results are plotted in Fig. 4. The upper blue line represents the prospective peak current for the RC model, where the cable inductance is neglected. In this case, the capacitance does not influence the peak current as it is only dependent on the voltage level and the circuit resistance. In contrast, when the line inductance is included, the prospective peak current is always lower. For the same inductance, a higher capacitance value increases the prospective peak current. For C = 10 or 100 μF, the considered system is always UD. For C = 1000 μF, the system transitions from UD to OD around l = 50 m.

C. Selectivity and sympathetic tripping

Protection selectivity is defined by [31] as *"Total selectivity: Overcurrent selectivity where, in the presence of two protection devices against overcurrent in series, the loadside protection device carries out the protection without making the other device trip."*

In radial grids, providing selectivity is straightforward using fuses. Referring to Fig. 5a, a small LVDC network is shown where one VBC feeds two Load Converters (LC1 and LC2). The output capacitance of the VBC is denoted by C_{VBC} and the input capacitance of the load converters by C_1 and C_2. Firstly, if a fault occurs in the connecting cable, F_{VBC} needs to operate while F_1 and F_2 may not blow. To assure that the system completely turns off, it is assumed that both LCs have an under-voltage protection that automatically shuts down the LC in case the supply from the VBC is down. Secondly, when a fault occurs after the terminals of LC1, e.g. due to a capacitor short-circuit, fuse F_{VBC} is in series with F_1 in the fault path. The necessary condition for selectivity is that the melting I^{2}t of F_{VBC} is higher than the total I^{2}t of F_1:

$$I^2t_{melt,F_{VBC}} > I^2t_{total,F1} \tag{21}$$

However, as is apparent from Fig. 5a, not only the VBC but also LC2 will contribute to the total fault current, assuming that the under-voltage protection did not react that quickly. If the fault current coming from the discharge of C_2 is too large, F_2 will also blow. This phenomenon is known as sympathetic tripping. To avoid this, the input capacitance of LC2 should be small enough. The worst case scenario is when a fault occurs just before the terminals of the LCs. The input capacitance of the load converters will discharge upon this fault. The only limiting resistance is $R_{ESR,C2}$, the ESR of the input capacitor. From Eqn. (11), the maximum input capacitance of LC2 can be calculated:

$$C_{input,2} < \frac{2 \cdot I^2t_{melt,F2} \cdot R_{ESR,C2}}{V^2} \tag{22}$$

The same reasoning can be applied to LC1. Note that the required input capacitance of LC1 and LC2 is also dependent on the converter parameters, such as the used switching frequency. From the required capacitance and the converter power, the fuse current rating can be selected. Multiple I^{2}t ratings exist for fuses with the same current rating and an appropriate one should be selected according to Eqn. 22. When a suitable combination cannot be found, selectivity is not completely guaranteed. Faults near the end of the cable may result in sympathetic tripping of the input fuse.

The presented case is a radial grid that is fed from one specific converter. Similarly, the same reasoning can be applied to a grid that is fed from multiple sources. In Fig. 5b, the grid is fed from the two VBCs that share the total output power based on their droop function and are physically connected to the same bus. When a fault occurs in the cabling, both fuses ($F_{VBC,1}$ and $F_{VBC,2}$) should operate. This means that sufficient capacitance is required at the terminals of both VBCs.

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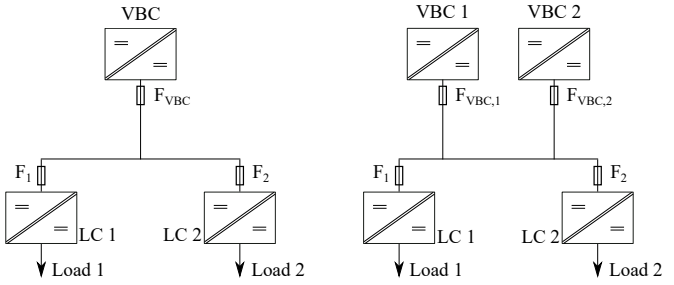

(a) LVDC network balanced by a VBC supplying two loads via a cable.

(b) LVDC network with two VBCs.

Fig. 5: Single line diagrams.

In general, all sources will contribute to the total fault current. The amount by which will depend on the impedance from each source to the fault. However, when designing a system with multiple sources one needs to keep in mind that not all sources might continuously be available. Assume again a system that is fed from two converters. The grid can be controlled by each one of them separately or by both converters together. When only one of them is active, the other is assumed to be disconnected from the grid, such that the capacitance does not contribute to the short-circuit current. The available short-circuit current is then lower than when both converters are active. This also means that the problem of multiple converters can be split up by assuring that the available amount of energy is sufficiently high for each converter separately.

In conclusion, providing selectivity using fuses is straightforward in radial grids by comparing the total and melting I^2t values. For VBCs, there is a lower limit to the amount of output capacitance that needs to be installed. The capacitance of the VBC needs to be sufficiently large to blow the fuse that protects the cable and the fuses at the input of the load converters. In contrast, the fuses that are placed at the loads are not allowed to blow when a fault occurs in the cable or in another load. To prevent this sympathetic tripping, there is an upper limit to the input capacitance of the loads.

D. System voltage dip

As a consequence of the SC, a voltage dip will be observed in the network. Based on an energy balance, this dip can be characterized by the following equation:

$$\frac{CV_1^2}{2} = (R_F + R_{fuse})I^2 t_{fuse,total} + \frac{CV_2^2}{2} \qquad (23)$$

In which V_1 is the voltage before the fault occurs and V_2 is the voltage after the fault is cleared. R_F is the total fault resistance (cables and capacitor ESR), R_{fuse} is the resistance of the fuse and C is the capacitance in the network. Eqn. (23) can be used to characterize the prospective voltage dip in every point of the network, based on the distance from the VBC and the fault parameters. However, it will be difficult to obtain accurate results as the resistance of the fuse is not a constant parameter during the fault transient and is also not given in the fuse datasheet. Alternatively, Eqns. (14)-(16) can be used, but the same limitations apply.

Nevertheless, general trends can be derived. A higher voltage dip is expected for fuses with higher I^2t ratings and faults with higher fault resistance, for example more to the end of a cable. Furthermore, the voltage dip can be limited by installing more capacitance. The minimal required amount of capacitance for fuse tripping was already discussed under section III-A. When an extra boundary condition is set to the max allowed voltage dip, Eqn. (23) can be used as a guideline for selecting the required capacitance. Lastly, the DC voltage level also plays an important role. Networks with higher voltages will experience lower voltage drops, as the amount of stored energy increases with the square of the voltage.

E. Protection methodology

The developed methodology is summarized as a flowchart in Fig. 6. At first, the system needs to be specified in terms of the chosen cable, VBCs, LCs, fuse and allowed voltage dip ΔV. The current rating of the fuse will depend on the current carrying capacity of the cable [30]. A certain overcurrent is typically allowed for a limited amount of time to increase the cable utilization [32]. Then, the minimal required capacitance C_{min} can be calculated from Eqns. (9) and (11), to ensure that sufficient I^2t is available to blow the fuse. When C_{VBC} is too low, extra capacitance is required or a fuse with lower I^2t rating should be selected. In principle, also the cable cross section can be increased. A cost analysis can indicate the preferred option. Next, the dominant time constant of the circuit needs to be verified to the specifications of the fuse manufacturer. The time constant needs to be sufficiently low, e.g. below 1 ms. If this is not the case, C_{VBC} or the cable section can be increased to meet the requirements. Subsequently, the peak current needs to be calculated using Eqns. (18) - (20) or via numerical simulation and compared to the IR of the fuse. Then, the minimal SC current needs to be calculated. It needs to be verified that this current is still sufficiently high, e.g. a factor of 10 compared to the fuse rating. When this is not the case, the cross section needs to be increased such that a higher minimal fault current will flow. Then, the prospective voltage dip ΔV needs to be calculated using Eqn. (23) and compared to the allowed dip ΔV_{max}. In case this condition is not met, increasing C_{VBC} is the easiest way of reducing this dip although increasing the cross section is also an effective option. Finally, it needs to be verified whether multiple loads are connected to the feeder. Selectivity can be guaranteed by calculating the maximum input capacitance based on Eqn. (22).

When the protection of a system is designed, care must be taken as the actual impedance between the source and the fault is never perfectly known. A conservative approach during the design stage is recommended. This can be achieved by estimating the cable resistance at the worst case operating temperature and by providing sufficient margin between the calculated and the installed capacitance at the VBC.

To conclude this section, an overview of important formulas is given in Table I.

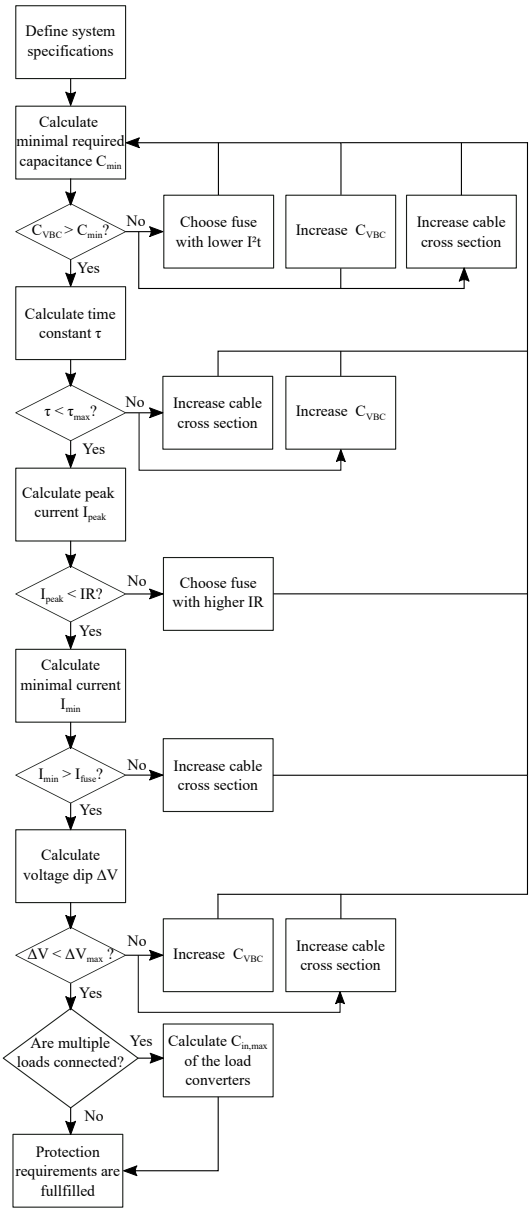

Fig. 6: Fuse based protection flowchart of LVDC systems.

TABLE I: Overview of relevant formulas for prospective DC short circuit calculations.

	RC	RLC UD	RLC OD
τ_1	RC	$\frac{2L}{R}$	$\frac{2L}{2\omega_1 L - R}$
τ_2	/	/	$\frac{-2L}{2\omega_1 L + R}$
ω_1	/	$\sqrt{\frac{1}{LC} - (\frac{R}{2L})^2}$	$\sqrt{(\frac{R}{2L})^2 - \frac{1}{LC}}$
I_{peak}	$\frac{V}{R}$	$\frac{V}{\omega_1 L} e^{(\frac{-R}{2\omega_1 L})} \arctan(\frac{2\omega_1 L}{R})$ $\sin(\arctan(\frac{2\omega_1 L}{R}))$	$\frac{V}{\omega_1 L} e^{(\frac{-R}{4\omega_1 L} \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L}))}$ $\sinh(0.5 \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L}))$
t_{peak}	0	$\frac{1}{\omega_1} \arctan(\frac{2\omega_1 L}{R})$	$\frac{1}{2\omega_1} \ln(\frac{R+2\omega_1 L}{R-2\omega_1 L})$
I^2t	$\frac{CV^2}{2R}$	$\frac{CV^2}{2R}$	$\frac{CV^2}{2R}$

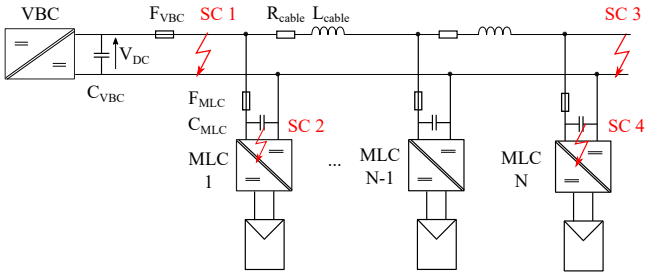

Fig. 7: A BIPV feeder balanced by a VBC and N MLCs connected in parallel.

TABLE II: Overview of system parameters.

Feeder			
A	L	R_{cable}	L_{cable}
6 mm^2	30 m	0.00308 Ω/m	0.294 $\mu H/m$
VBC ([34])			
V_{DC}	C_{VBC}	R_{VBC}	
380 V	220 μF	1.2057 Ω	
	20 μF	0.0127 Ω	
MLC ([35])			
N	P_{out}	C_{MLC}	R_{MLC}
20	300 W	2 μF	0.07955 Ω

IV. Case Study and Experimental Results: BIPV Feeder

In this section, the derived methodology will be applied to the case of a LVDC backbone feeder with multiple Module-Level Converters (MLCs) and experimentally validated.

A. Case study

The system of interest is shown in Fig. 7 and a summary of the system parameters is presented in Table II. Building Integrated PhotoVoltaics (BIPV) is an application where the use of LVDC offers several advantages such as a lower amount of components and a higher reliability [33].

The network voltage V_{DC} is controlled by the VBC, with output capacitance C_{VBC} and a fuse F_{VBC}. The parameters of the VBC are based on the experimental prototype discussed in [34]. The feeder resistance and inductance are represented by R_{cable} and L_{cable}. The cable cross section A was selected to be 6 mm^2 based on the total current that flows through it. The feeder is connected to N MLCs that each have an output capacitance C_{MLC} and a fuse F_{MLC}, also based on the parameters of an experimental MLC prototype [35].

In Fig. 7, four SCs at different locations are shown. SC 1 is a fault right after the converter terminals and needs to be cleared by fuse F_{VBC}. The fuses of the MLCs, F_{MLC}, are not allowed to blow. It is the highest possible fault current that F_{VBC} will experience and will thus determine the interruption rating of F_{VBC}. SC 2 is a fault in the MLC closest to the VBC. To have selective protection, only the fuse in the faulty MLC must operate without affecting F_{VBC} and F_{MLC} of the nearby MLCs. Moreover, this is the highest fault current that the MLC will experience and thus defines the IR of F_{MLC}. SC 3 is a fault at the end of the feeder and will be the lowest

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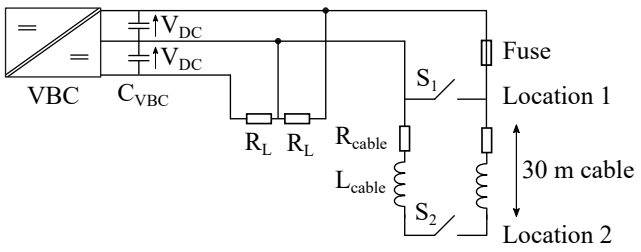

Fig. 8: Schematic overview of experimental set-up 1.

fault current that F_{VBC} needs to interrupt. SC 4 is a SC in the last MLC and will lead to the largest voltage dip. The distance from the VBC to the first MLC is 10 m and then an MLC is placed every 1 m.

The SC protection is calculated according to the flowchart of Fig. 6, supported by numerical PLECS simulation results. A Littlefuse KLKD 20 A fuse with an IR of 50 kA and a total I^2t of 1151.185 A^2s was selected for F_{VBC}. A maximum voltage dip of 50 V is allowed in the system when a MLC fails.

The minimal required capacitance was calculated to be 1182.7 μF. This is about five times more than the available amount, which means that extra capacitance needs to be installed. Three extra KEMET ALS30A471KE500 500 V, 470 μF capacitors with an ESR of 0.194 Ω and a high volume cost of approximately 18 EUR per piece, can be used.

Then, the time constant of the system is calculated for a fault with the highest inductance, thus at the end of the line. The system is underdamped and has a time constant below 0.2 ms, which is sufficiently low and no re-rating should be applied [36].

The peak current, directly after the VBC terminals, was found to be 36.057 kA. This is below the fuse IR of 50 kA, so no other fuse needs to be selected.

The minimal current, at the end of the feeder, is found to be 1197 A. This is sufficiently high, as it falls in the short-circuit zone of the fuse, where adiabatic heating occurs.

Finally, selectivity and the voltage dip need to be checked. When one MLC fails, the maximum allowed voltage dip is 50 V. The maximum output current of the MLC is approx. 0.8 A, which means that a fuse of, e.g. 2 A can be used. The peak current was found to be 3.142 kA. The chosen fuse is a 2 A Bel Fuse 0ADAP2000 with an I^2t of 1.28 A^2s and an IR of 10 kA. From the simulation, it was found that a voltage dip of only 3 V occurs, measured at the last MLC. To make sure that no sympathtic tripping occurs, the maximum input capacitance of the MLC needs to be calculated using Eqn. (22) and was found to be 1.4 μF. This is lower than the actually installed value of 2 μF. To keep the input capacitor at its current value, a fuse with higher I^2t rating needs to be chosen. To this end, a Schurter 1000 V, 2 A ASO fuse was selected with an IR of 20 kA and an I^2t of 4.755 A^2s. Then, the maximum capacitance is 5.2 μF, which is sufficiently high to avoid sympathetic tripping.

B. Experimental results

1) Setup 1: In order to test the performance of fuses in LVDC applications and to validate the hypotheses of sections II and III, an experimental setup was built. A schematic overview of the setup is shown in Fig. 8. The used VBC was presented in [34]. Extra capacitance was added and faults can be made by closing a relay, on two different locations. Location 1 is at the beginning of a 30 m, 6 mm^2 cable. Location 2 is at the end of the 30 m cable and thus means that the fault resistance and inductance is higher. The used VBC is in essence a bipolar converter but the faults are made from the positive pole to the 0 V pole. The VBC also feeds load R_L = 336 Ω, in bipolar configuration.

An overview of the measurement results is given in Table III. Fig. 9 plots the measured voltage dip as a function of the I^2t rating of the fuse. As expected from Eqn. 23, higher I^2t ratings lead to a larger voltage dip and this trend is clearly visible. Moreover, also from Eqn. 23, it is expected that faults with higher fault resistance will lead to a higher voltage decrease as more energy is dissipated during the fault clearance time. Also this hypothesis is confirmed by looking at faults that occur immediately after the VBC and faults that occur at the end of a 30 m cable. The resulting voltage dip is always higher at the end of the feeder. Thirdly, the measurements were done for two capacitance values at the output of the VBC. Increasing the capacitance leads to more energy in the network, which decreases the voltage dip.

In Fig. 10, the required clearance time (Δt) is plotted as a function of the I^2t rating of the fuse. Increasing the capacitance makes the fuse trip faster as more short-circuit current is available, which heats up the fuse more rapidly. Similarly, when the fault resistance is lower, the fuse operates faster. Furthermore, it can be seen that the fuses operate fast enough to ensure protection against indirect touch voltage, for which the fault needs to be cleared within approximately 400 ms [13].

In Fig. 11, the measured voltage profiles before, during and after the clearance of fault are plotted. A moving average low pass filter with a span of five was used to filter out the measurement noise. Before the fault, the voltage is stable around 380V. When the fault occurs, a momentary voltage dip is visible due to the large fault current that discharges the capacitor. The discharge stops when the fuse clears the fault. Afterwards, the voltage increases again due to the reaction of the voltage controller, increasing the charge current. Also note that the charging occurs faster (steeper slope) when the voltage dip is larger. For test 17, 18, 22, 23, 24, it can be noticed that the voltage does not increase, as the VBC went into a protection mode, since the voltage has dropped below 300 V.

2) Setup 2: A second experimental setup was built to investigate the performance of fuses in networks with multiple sources, as shown in Fig. 5b. The schematic overview of the setup is displayed in Fig. 12. Two Delta Elektronika SM660-AR11 sources (VBC 1 and VBC 2) are present in the system and regulate the voltage at 380 V. As the internal capacitance of the sources is not known, C_1 and C_2 were added as extra VBC capacitance of 220 μF. The VBCs are connected through a 6 mm^2 cable of 27 m long. Two loads $R_{L,1}$ and $R_{L,2}$ are each connected via a 6 m long, 2.5 mm^2 cable. Six fuses (F_1 to F_6) are installed. The ampacity of the fuses at the output

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TABLE III: Experimental results from fuse tests - Set-up 1.

Test	C_{VBC}	Fault	Fuse				Measurement		
	(μF)		Type	I (A)	I²t (A²s)	IR (kA)	ΔV (V)	I peak (A)	Δt (μs)
1	780	1	0ADA	2	1.28	10	36	2333	24
2	780	1	0ADA	4	15.5	10	68	4250	112
3	780	1	0ADA	6	41.76	10	100	3000	64
4	780	1	0ADA	8	76.8	10	140	3000	360
5	780	1	0ADA	10	101.4	10	156	3083	720
6	780	1	ADEP9200RE	20	120	20	228	3500	600
7	780	2	0ADA	2	1.28	10	44	1500	52
8	780	2	0ADA	4	15.5	10	84	1500	128
9	780	2	0ADA	6	41.76	10	148	1583	760
10	780	2	0ADA	8	76.8	10	228	1416	560
11	780	2	0ADA	10	101.4	10	268	1583	560
12	780	2	ADEP9200RE	20	120	20	260	1250	600
13	1140	1	0ADA	2	1.28	10	24	6042	20
14	1140	1	0ADA	4	15.5	10	40	3250	40
15	1140	1	0ADA	6	41.76	10	64	2667	55
16	1140	1	0ADA	8	76.8	10	88	4625	80
17	1140	1	0ADA	10	101.4	10	96	2625	80
18	1140	2	ADEP9200RE	20	120	20	168	3792	65
19	1140	2	0ADA	2	1.28	10	28	4208	50
20	1140	2	0ADA	4	15.5	10	52	4666	120
21	1140	2	0ADA	6	41.76	10	92	2875	180
22	1140	2	0ADA	8	76.8	10	140	2333	220
23	1140	2	0ADA	10	101.4	10	148	3958	240
24	1140	2	ADEP9200RE	20	120	20	200	4292	280

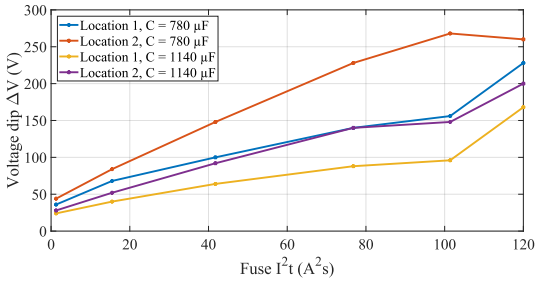


Fig. 9: Measured voltage dip as a function of the fuse I^2t value for two different capacitance values and two fault locations.

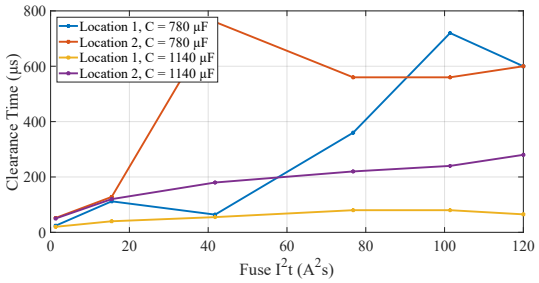
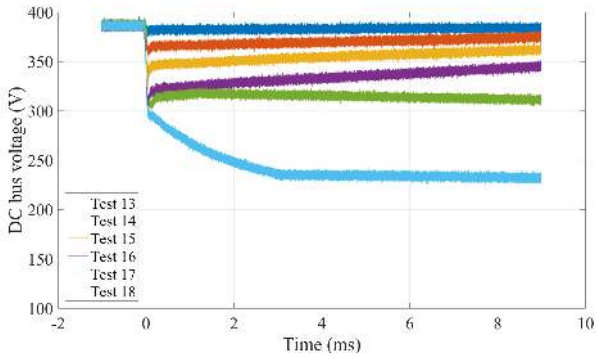


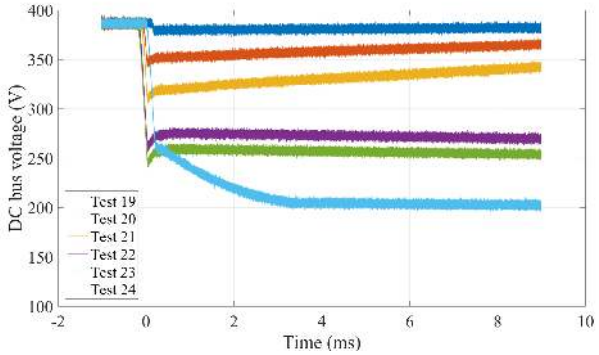
Fig. 10: Measured clearance time in µs as a function of the fuse I^2t value for two different capacitance values and two fault locations.

of the VBCs is 20 A, at the connection cable 6 A, and 2 A towards the load resistors. Faults can again be made by closing a relay on location 1 or 2.

Four tests were accomplished and the results are displayed in Table IV. The voltage dip and peak current at VBC 1 and



(a) Location 1, C = 1140 μF.



(b) Location 2, C = 1140 μF.

Fig. 11: Measured voltage profile before, during and after the fault.

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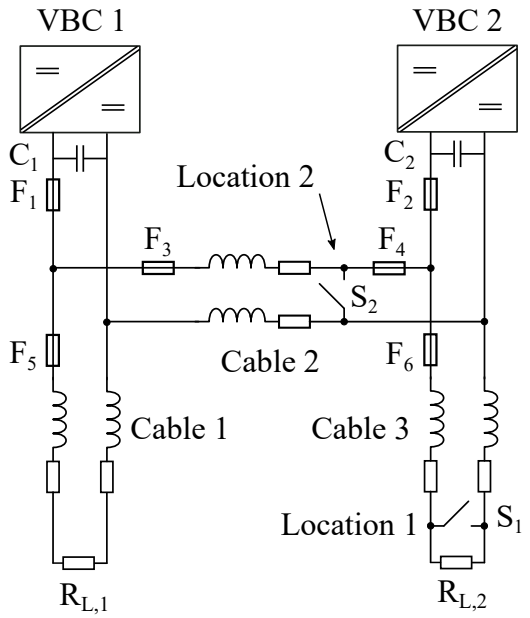
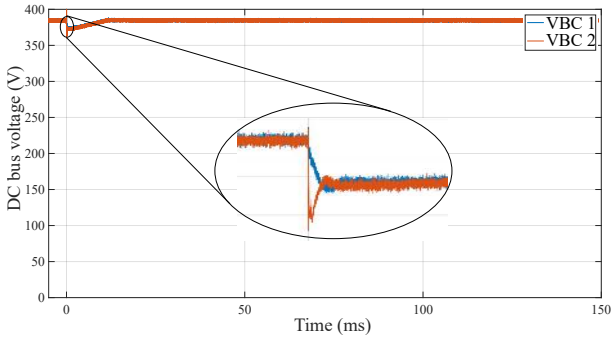
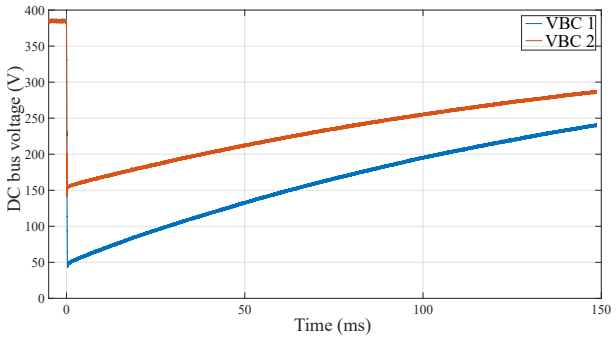


Fig. 12: Schematic overview of experimental set-up 2.



(a) Test 25.



(b) Test 28.

Fig. 13: Measured voltage at the VBC terminals before, during and after the fault.

VBC 2 are measured and respectively denoted as ΔV_1, ΔV_2, $I_{peak,1}$ and $I_{peak,2}$. To avoid confusion, the numbering of the tests was continued. Test 25 is a SC fault on location 1 in Fig. 12 when both VBCs are operational. As the fault is closer to VBC 2, it is expected that VBC 2 will contribute more to the fault current. This hypothesis was confirmed and the measured voltage dip at VBC 2 (ΔV_2) is more than twice as large as ΔV_1. The peak current from VBC 2 ($I_{peak,2}$) is about 30 times larger than $I_{peak,1}$. Note that selectivity was achieved as only F_6 tripped and the other fuses remained operational. The voltage measurement is displayed in Fig. 13a.

As discussed in section III, not necessarily all VBCs are available in the network. The amount of installed capacitance per VBC should thus be sufficiently high to trip all faults. This was tested by disconnecting first VBC 2 from the network such that only VBC 1 contributes to the fault current (test 26) and subsequently the opposite situation where only VBC 2 is connected to the network (test 27) is evaluated. From Table IV, it can be seen that selectivity was achieved for both tests. The voltage dip and peak current are again different due to the extra impedance of cable 2.

Furthermore, SC faults in the connection cable between both VBCs (cable 2) can occur. This fault situation is verified in test 28 by closing a relay on location 2. The resulting voltage dips at VBC 1 and 2 are shown in Fig. 13b. Selectivity is again demonstrated as only F_3 and F_4 have tripped. Note, however, that the voltage dip is more severe as compared to test 25. This is a consequence of the larger I^2t value of the fuses that are used to protect cable 2.

C. Discussion

Fuses have a proven track record as protection devices in electrical installations and their datasheet parameters are derived in accordance to standards such as IEC60127 and IEC60269. They have the advantage of being simple and cheap. Furthermore, they have high interruption ratings in relatively small packages and can therefore be easily integrated in PCBs of power electronic converters. Their major disadvantage is that physical replacement of the fuse cartridge is required after operation.

In [4], fuses are considered as an unreliable protection method as they only trip the faulted pole, and should thus only be considered as back-up protection for the main circuit breaker. Firstly, it is not necessarily undesirable that only one pole gets isolated. For a bipolar LVDC system, this can increase the reliability as the unaffected pole can remain operational and bipolar devices could use the remaining voltage to safely shut down the application or continue to operate under reduced power. Secondly, a strong research interest is visible for the development hybrid or solid state circuit breakers [4], [37], [38]. Their main advantage is that they will interrupt faults in a time span of several μs, leading to a minimal impact on the network in terms of voltage dip and energy dissipation in the lines and components. However, for LVDC grids to break through, the protection units do not only need to be available but consensus is required on standard test methods and parameters that allow an easy and fair comparison between different manufacturers. No such standards are available yet for hybrid or solid state circuit breakers.

Fuses and purely mechanical breakers thus have a strong advantage here as their use as safety elements is already strongly standardized, also for DC interruption. Although it is expected that hybrid and solid state CBs will be an essential

TABLE IV: Experimental results from fuse tests - Set-up 2.

Test	C_{VBC}	Fault	Tripped fuses				Measurement			
	(μF)		Type	I (A)	I²t (A²s)	IR (kA)	ΔV_1 (V)	ΔV_2 (V)	$I_{peak,1}$ (A)	$I_{peak,2}$ (A)
25	220	1	F6	2	1.28	10	9.6	19.9	263.3	8270.0
26	220	1	F6	2	1.28	10	49.9	NA	980.1	NA
27	220	1	F6	2	1.28	10	NA	30.1	NA	6159.1
28	220	2	F3, F4	6	41.76	10	337.2	238.4	2172.2	25132.0

part of future LVDC grids, fuses are a viable option to bridge the gap and help in the roll-out of LVDC systems, although they put constraints on the capacitance.

Although fuse datasheets typically only show the time-current curves up to 1 or 10 ms (as prescribed by the standard), it was shown that fuses are able to operate much faster than this. They are able to clear faults within the 100..1000 μs range but need sufficient capacitance to provide the necessary high fault current and limit the resulting voltage dip. This extra capacitance also means a higher total system cost and lower power density of the VBC and can be used as an argument for further development of solid state CBs.

Another important aspect to take into consideration is the thermal stress on the converter components due to the large short-circuit currents. Fig. 14 shows a typical half bridge configuration with current measurement through the inductor L and two possible fault locations. This topology can be used as step-up or step-down converter, depending on the application. For SC 1 and SC 2, the capacitor which is closest to the SC will discharge into the fault. The internal temperature of the capacitor will increase as a consequence of the power dissipation in the ESR. As temperature is a critical stressor for most capacitor technologies, the discharge will lead to a reduction of its useful lifetime [39]. When the temperature increases beyond the maximum allowed temperature, an immediate failure might occur.

For SC 1, inductor L and the current measurement are present in between the transisors and the SC. The inductor will limit the current surge and, depending on the speed of the control system, the microcontroller can turn off both transistors before a failure occurs. The fault is not fed by C2, as the inductor current will circulate through diode D2.

For SC 2, the consequences for the converter can be more damaging. The current through L will again increase due to the SC. When the microcontroller turns off both transistors, the inductor current will keep flowing through D1, thus feeding the fault. Due to the losses in the diode, the junction temperature will rise. This can again lead to a catastrophic failure when the component specifications are violated. A possible solution to protect the transistor/diode is the inclusion of a series fuse as proposed in [8], [9], [10], [40]. The impact on the converter components is thus dependent on the used topology and the location of the fault and should be investigated on a per case basis.

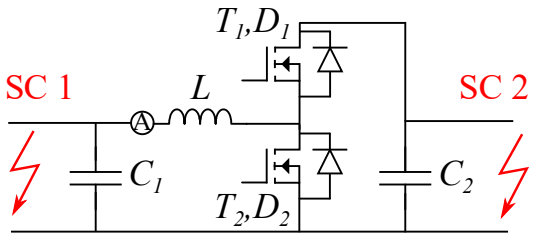


Fig. 14: Typical half bridge structure with SC faults at the input or output terminal.

V. Conclusions

In this paper, the use of fuses as SC protection in radial LVDC grids has been discussed. The problem of converter dominated grids with a limited and relatively low amount of energy stored in the VBC capacitance, which leads to a rapid decay in the SC current, has been presented. An analytical framework to calculate the peak current and minimal capacitance for correct fuse operation was developed by introducing the system I²t value. Selectivity can be achieved by putting a limit on the minimal amount of capacitance for VBCs and a maximal amount on the LCs. The voltage dip that results from the SC will be lower when the fuse I²t rating is lower, when the fault resistance is lower or when more capacitance is present in the grid. The above conclusions were validated by experimental results. As electrostatic energy stored in the capacitors is essential to trip the fuse in fault conditions, adopting a fuse-based protection strategy may require to upgrade the amount of capacitance in the network.

Compared to the state-of-the-art, this paper has clearly indicated the real limitations and trade-offs of using fuses in LVDC grids and provided a fuse based protection methodology. Furthermore, the role of fuses as an enabling element in the industrial development and adoption of LVDC grids was discussed.

VI. Acknowledgements

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