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Fusion bonding of rough surfaces with polishing technique for silicon micromachining

C. Gui, H. Albers, J.G.E. Gardeniers, M. Elwenspoek, P.V. Lambeck

Abstract Surface roughness is one of the crucial factors in silicon fusion bonding. Due to the enhanced surface roughness, it is almost impossible to bond wafers after KOH etching. This also applies when wafers are heavily doped, have a thick LPCVD silicon nitride layer on top or have a LPCVD polysilicon layer of poor quality. It has been demonstrated that these wafers bond spontaneously after a very brief chemical mechanical polishing step. An adhesion parameter, that comprises of both the mechanical and chemical properties of the surface, is introduced when discussing the influence of surface roughness on the bondability. Fusion bonding, combined with a polishing technique, will broaden the applications of bonding techniques in silicon micromachining.

1 Introduction

Silicon fusion bonding (SFB) is the joining of two silicon wafers without the use of any intermediate adhesives at room temperature (RT) in an ambient atmosphere, followed by a high temperature annealing step. This technology has been used broadly in the fabrication of silicon-on-insulator (SOI), silicon power devices, sensors and actuators (S&A), as well as micro electromechanical systems, see e.g. Petersen et al. (1988), Barth (1990) and Gösele et al. (1995).

It is widely believed that both the macroscopic surface flatness and the microscopic surface roughness are crucial for successful wafer bonding. Commercially available well-polished silicon wafers, with or without a buried oxide layer or well grown epitaxial layers, having a flatness variation of several µm and a micro roughness not exceeding several Å, can be easily bonded at RT in a clean room environment, as has been done in the SOI community, Maszara et al. (1991). The deformation of wafers during SFB is shown graphically in Fig. 1. However, after some processing steps, RT bonding is not so straight forward. For instance, SFB is sometimes very difficult after very heavy boron diffusion, Bäcklund et al. (1990) and Schmidt (1994). Silicon wafers after KOH etching, LPCVD polysilicon deposition and thick LPCVD $Si_{3+x}N_4$ deposition, are not directly bondable. The enhancement of the surface micro roughness due to these processes is believed to be the main obstacle for RT bonding.

Chemical mechanical polishing (CMP) plays an important role in SFB in two ways: by preparing very flat and smooth surfaces for successful RT bonding, and by mechanically thinning one side of the bonded wafer pair to the desired thickness. While the latter is one of the key techniques in the fabrication of SOI wafers and silicon power devices, Haisma et al. (1989) and Blackstone (1995), the former, however, is a crucial and very critical process step for the fabrication of S&A devices, where bonding between a large range of materials and bonding of silicon wafers with micro mechanical structures are of interest. In fact, CMP is the only technique that, so far, can offer such a rigid surface smoothness for SFB.

Previously, Haisma et al. have demonstrated that wafer bonding can be applied to various types of materials and material combinations by using dedicated optical polishing techniques, Haisma et al. (1994). They concluded that the polishing step is the most important in the process of preparing materials for wafer bonding. And CMP seems to be the sole polishing process in preparing semiconductor materials for wafer bonding.

The object of this research is to implement CMP as an *on-site* process for fusion bonding of silicon and silicon related materials, such as silicon dioxide, silicon nitride, and polysilicon, which may offer more freedom for the applications of bonding technology in the fabrication of S&A devices. Specifically, we show that silicon wafers after KOH etching, very heavy boron diffusion, LPCVD silicon rich nitride ($Si_{3+x}N_4$) deposition and LPCVD polysilicon deposition, can be bonded after being shortly polished with a CMP machine.

Based on the surface contact mechanics, we use an adhesion parameter which includes both the mechanical properties, such as surface roughness, surface elastic constant, and chemical properties, such as surface energy, to evaluate the bondability of a certain wafer surface.

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C. Gui, H. Albers, J.G.E. Gardeniers, M. Elwenspoek, P.V. Lambeck
MESA Research Institute, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands,

Correspondence to: C. Gui

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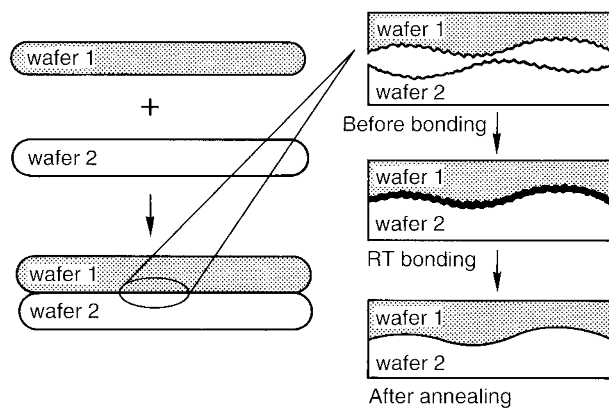

Fig. 1. Silicon fusion bonding process showing the deformation of silicon wafers

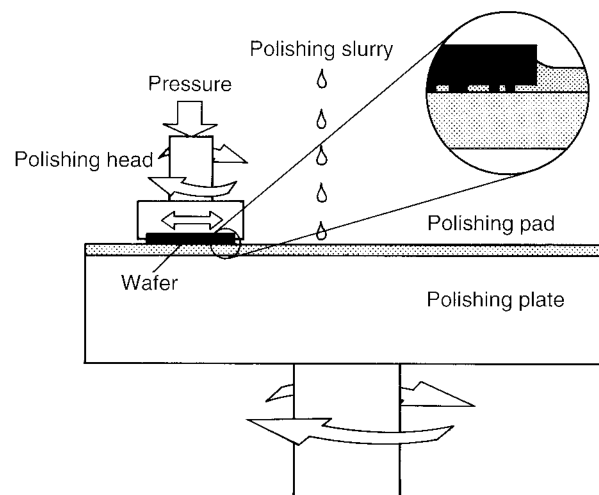

Fig. 2. Schematic drawing of the CMP set-up

2 Experiments

2.1 Sample preparation

One side polished, 380 μm thick 3 inch (100) silicon wafers were used in the following experiments. After standard wafer cleaning (dipping in fuming nitric acid and 70% hot nitric acid, plus rinsing in deionized (DI) water), the wafers underwent either KOH etching, or very heavy boron diffusion, or LPCVD $Si_{3+x}N_4$, or LPCVD polysilicon deposition. % KOH solution at 75 °C for 10 minutes. The etch rate of the KOH solution was about 1 μm/min. Boron doping was carried out in a solid source dotation system at 1100 °C for 3 hours. The boron oxide was then removed from the wafers by BHF etching for 1 hour. The surface boron concentration was about 3×10^{20} cm^{-3}, and the doping depth was about 2.5 μm. The LPCVD $Si_{3+x}N_4$ layer was grown on the silicon wafers from a gas mixture of SiH_2Cl_2 (70 sccm) NH_3 (18 sccm), in 200 mTorr at 850 °C. The thickness of the LPCVD $Si_{3+x}N_4$ layer was about 430 nm. The LPCVD polysilicon layer was deposited from SiH_4 at 250 mTorr and 590 °C. The inner stress of the LPCVD polysilicon layer was released with an annealing step.

In order to evaluate the effects of CMP, some of the wafers underwent SFB directly after the preparation, while others were first polished and then bonded together.

2.2 Polishing

The CMP process was done by using an E460 CMP machine, which has a single polishing head. A schematic drawing of the CMP set up is shown in Fig. 2. The polishing pad is put on top of the polishing plate, the temperature of which can be adjusted from 0° to 80 °C. The wafer is held opposite the polishing pad by a chuck that is mounted onto the polishing head. During polishing, the wafer is pressed onto the polishing pad with adjustable pressure. Both the head and plate rotate and the head sweeps on the pad. At the same time, the slurry is introduced onto the pad. The wafer surface is undergoing both mechanical wearing and chemical etching simultaneously. The protrusions of different height on the wafer will experience different pressures and subsequently different wearing and etching. This difference in the removal rate will lead to smoothening of the surface.

The CMP process was specially optimized for single crystalline silicon polishing in terms of the removal rate and the surface smoothness, Gui (1996). The polishing slurry was Nalco 2350 which was diluted in DI water at a ratio of 1 to 30. The pH value of the slurry was about 11. The working pressure and the plate temperature of CMP were 1 bar and 25 °C, respectively. The polishing pad was UR 100, which is very soft and specially made for silicon final polishing. The silicon removal rate of CMP was about 30 nm/min.

The same process was applied for the polishing of a LPCVD $Si_{3+x}N_4$ layer. A removal rate of about 2.5 nm/min. was found, which is 12 times lower than the silicon removal rate, while the LPCVD $Si_{3+x}N_4$ layer surface quality after polishing was comparable to that of silicon wafers after polishing.

Compared with single crystalline silicon, a LPCVD polysilicon layer is removed more easily both mechanically and chemically in the CMP process. Another slurry LS 10, which has a lower pH value and consists of smaller particles than Nalco 2350, was used in polysilicon polishing, while the polishing pad remained the same. The resulting removal rate is about 20 to 30 nm/min., and a mirror like smooth surface was obtained.

It was observed that after CMP the polished surface is covered with large amounts of particles and is also contaminated by sodium-containing chemicals from the slurry. The polishing particles are typically 30 to 50 nm in diameter. The remaining particles on the wafer surface are, of course, disastrous for bonding. The post CMP cleaning process is first brushing the wafer surface with DI water, followed by a RCA $[H_2SO_4(1) + H_2O(5) + 30\%\ H_2O_2(1)]$ clean. The former step is applied to remove the polishing particles, while the latter one is used to remove the sodium contamination.

2.3 Bonding

The SFB experiments were carried out in a class 100 clean room environment at RT and standard atmosphere. Before bonding,

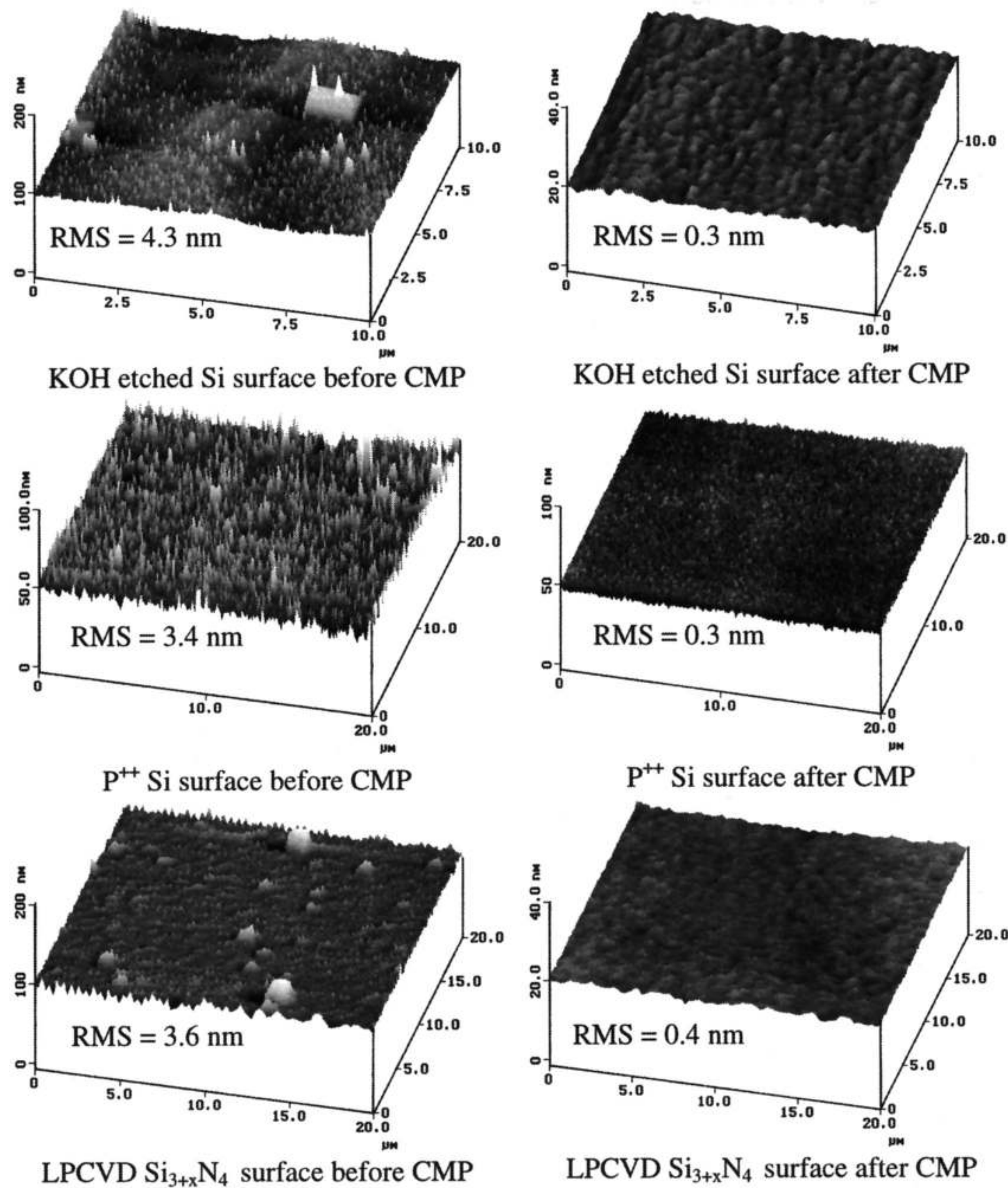

Fig. 3. AFM images of different wafer surfaces before and after CMP

all wafers were treated with RCA cleaning at 80 °C for 20 minutes, followed by a standard wafer cleaning. After spin drying, the wafers were immediately brought together for RT bonding in a self-made bonding set up, which has an IR camera that enables one to monitor the RT bonding process. Slight pressure was necessary for the first point of contact for the most successful RT bonding, and in that case the contact wave propagated over the whole wafer immediately. Once the wafer pairs were successfully bonded at RT, they were annealed for 2 hours at 1000 °C in N_2. The bond strength after annealing was measured using the crack propagation method, W. P. Maszara et al. (1988). The particles and voids captured between the wafer pair were detected by using the IR camera.

3
Results

The surface roughness of the wafers measured with atomic force microscopy (AFM) are presented in Fig. 3. For all investigated materials the root mean square (RMS) roughness after polishing was typically 3 to 4 Å. This is about one order of magnitude lower than that before CMP, no matter what kind of surface topography they have before CMP.

The cross sections of the LPCVD polysilicon surface before and after CMP have been measured with transition electron microscopy (TEM), which reveals the surface topography in nano scale. LPCVD polysilicon surface before polishing (Fig. 4a) is significantly rougher than that after polishing (Fig. 4b).

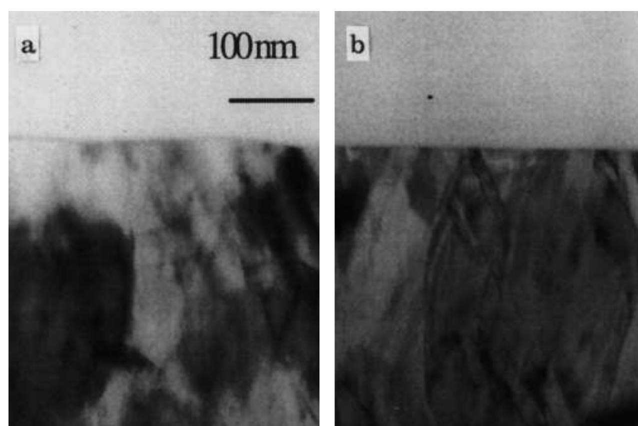

Fig. 4. TEM images showing polysilicon surface topography before **a** and after **b** CMP

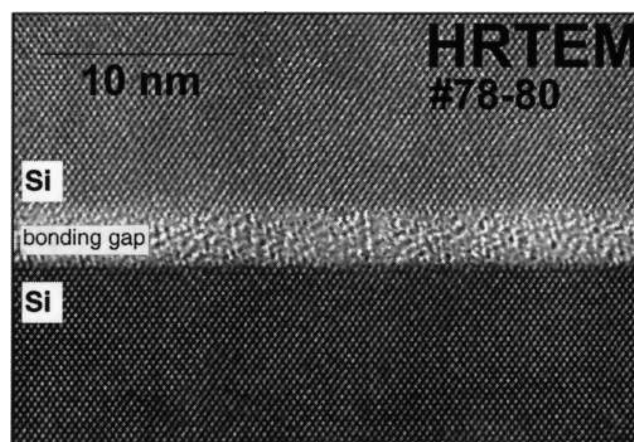

Fig. 5. High resolution TEM image showing the bond interface between Si and Si after KOH etching and polishing

Table 1. SFB of silicon wafers with different surface conditions

Surface conditions of bonding wafer pair	Bondability without CMP	Bondability with CMP
KOH etched Si to KOH etched Si	—	++
$^{++}$ Si to P^{++} Si	0	++
LPCVD $Si_{3+x}N_4$ to P^{++} Si	—	+
LPCVD PolySi to SiO_2	—	++

Note '—' impossible, '0' difficult, '+' possible with slight pressure, '++' spontaneously after first contact

The SFB results are summarized in Table 1. The RT bond strength for all successfully bonded wafer pairs was measured to be between 50 mJ/m^2 and 200 mJ/m^2. The contact wave propagation speed of a typical spontaneous silicon to silicon RT bonding was about 3.0 cm/sec.

The bonding interfaces of KOH etched silicon to KOH etched silicon, LPCVD $Si_{3+x}N_4$ to P^{++} silicon and LPCVD polysilicon to thermal silicon oxide, have been examined using TEM. In all three cases, a uniform and closed interface was observed which shows the two materials have been completely combined together through the bonding and fusion process. High resolution TEM reveals a uniform amorphous layer of 28 Å thick at the bonding interface between two KOH etched silicon (100) wafers after a brief polishing (Fig. 5). This shows that the binding of two silicon wafers was via the two native oxide layers on the wafers.

At the bonding interface of LPCVD $Si_{3+x}N_4$ to P^{++} silicon, an intermediate layer of about 9 nm thick was observed (Fig. 6). This layer is amorphous and is significantly different from the LPCVD $Si_{3+x}N_4$ layer. This layer is so thick that it cannot be a pure native oxide layer. Auger analysis has revealed that there is a clear oxygen peak in this intermediate layer, which indicates the diffusion of oxygen and the formation of $Si_xO_yN_z$ diffusion zone.

The bonding interface of LPCVD polysilicon to thermal silicon oxide is very uniform (Fig. 7). This interface is even smoother than the deposition interface between LPCVD polysilicon and the thermal oxide. We believe that the bonding mechanism between the polysilicon and silicon dioxide is the

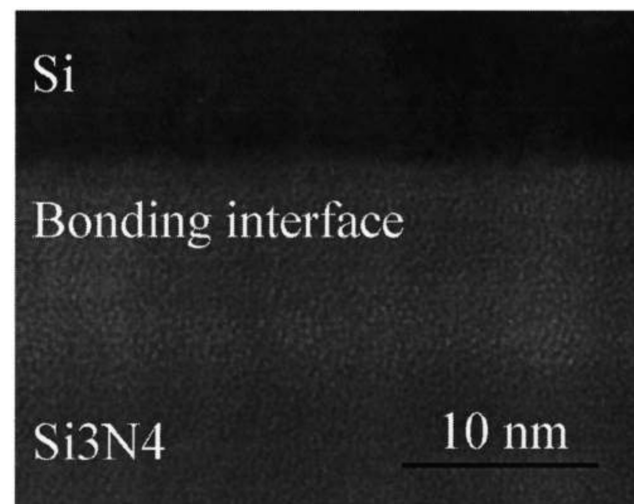

Fig. 6. TEM image showing the bonding interface of silicon and silicon nitride

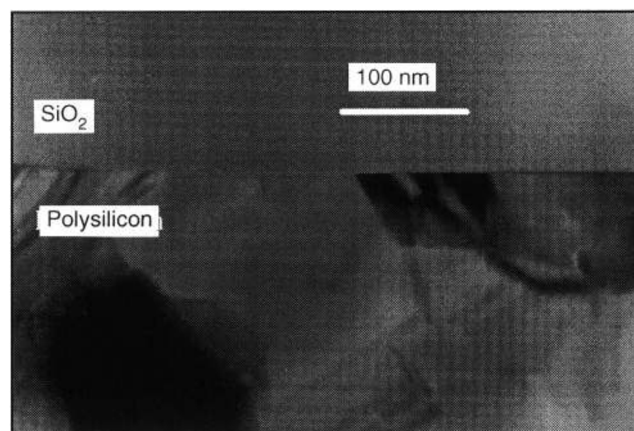

Fig. 7. TEM image showing the bonding interface between polysilicon and SiO_2

same as that between single crystalline silicon and silicon dioxide. The adhesion force between the thin water layer of several nm thick on both polysilicon and silicon dioxide layer is the dominant binding force during RT bonding. After annealing at elevated temperatures, siloxane bonds (Si–O–Si) take place under the release of water.

4 Applications

SFB together with CMP technology offers many new possibilities for silicon micromachining. Bonding of silicon wafers having a rough surface due to previous process steps or having on top deposited layers of poor surface quality is not a problem anymore with this *on-site* polishing technique. Here we show two of these applications: Silicon on Nitride (SON) wafers, and Si–SiO_2–PolySi–SiO_2–Si (SISI) wafers.

4.1 SON wafers

Previously bonding between silicon and silicon nitride has been reported by several authors. However, only nitride layers thinner than 100 to 200 nm were involved in those bonding experiments, e.g. Harendt et al. (1992) and Bang et al. (1993). Using the polishing technique, we have successfully fabricated SON sandwich wafers with 1 μm thick silicon nitride in between. These SON sandwich wafers have been used in fabricating infrared bolometers where a silicon nitride layer is used as a membrane and provides thermal isolation, Sánchez et al. (1996). The SON fabrication process started with growing low stress LPCVD $Si_{3+x}N_4$ on top of one silicon wafer. This wafer is subsequently polished and fusion bonded to a second P^{++} doped and polished silicon wafer. Finally, the wafer pair is thinned from the backside of the P^{++} doped silicon wafer by KOH etching. The back-etching stops on the P^{++} doped silicon and a polishing step is applied to smooth the top silicon layer surface. The cross section of a resulting SON wafer is shown in Fig. 8.

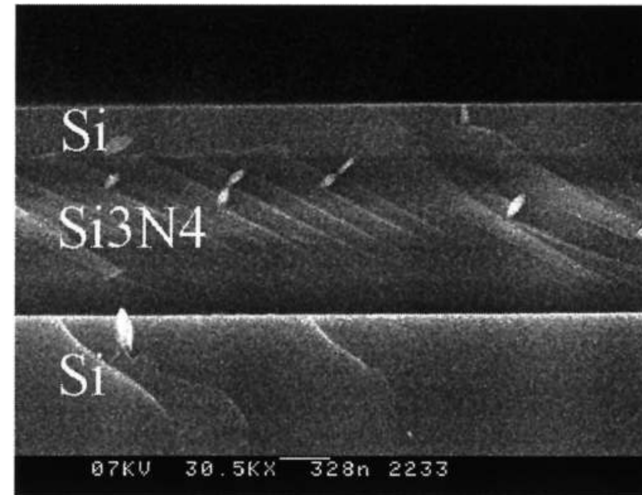

Fig. 8. SEM photo showing the bond interface between boron doped Si and LPCVD $Si_{3+x}N_4$. The top silicon layer is about 400 nm thick. The LPCVD $Si_{3+x}N_4$ layer is about 1 μm thick

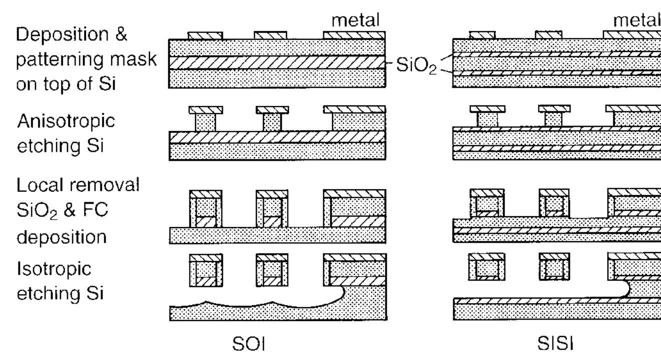

Fig. 9. Processes of fabricating micromechanical structures on SOI (left) and SISI (right) sandwich wafers using the black silicon method of the reactive ion etching technique, De Boer et al. (1995)

4.2 SISI sandwich wafers

In silicon micromachining, there is a tendency to fabricate micromechanical structures from SOI and SISI sandwich wafers, De Boer et al. (1995). The processes of fabricating micromechanical structures on SOI and SISI sandwich wafers
using the black silicon method of the reactive ion etching technique is shown in Fig. 9. Compared to SOI wafers, SISI wafers have many advantages. First, the upper silicon dioxide layer can be made very thin to ensure a very low built-in stress in the top silicon layer, while the lower thermal oxide can be grown thick enough to obtain satisfactory electric isolation. Secondly, the middle LPCVD polysilicon layer is used as the sacrificial layer, and after releasing the top silicon structures, a flat bottom surface can be achieved, which offers good dynamic properties of the moving structures.

Fabricating SISI wafers is comparable to the process of making SOI wafers. The process begins by growing a thin thermal oxide layer and then a LPCVD polysilicon layer on the device wafer. The divice wafer is then polished and fusion bonded to another oxidized wafer, or handle wafer. After annealing, the bonded wafer pair is thinned and smoothed from the backside of the device wafer to the desired thickness. An example of a cross section of a SISI wafer is shown in Fig. 10.

5 Discussion

From the AFM and TEM images (Fig. 3 and 4), we conclude that in all cases large surface roughness of the wafers before CMP is most probably responsible for the poor bondability of these wafers. CMP is an ideal technique to smooth the rough surfaces before bonding.

RMS roughness is frequently used to characterize the bondability of a silicon wafer surface. This method, however, is limited by the fact that the RMS value is strongly dependent on the scan length or area. Recently Bergh et al. (1995) and Roberds et al. (1995) have improved the evaluation of the wafer bonding ability in terms of surface roughness by introducing the power spectrum which comprises of both the amplitude and the spatial frequency information of the surface distortions. Only empirical models were obtained. Furthermore some questions still remain unclear. For instance,

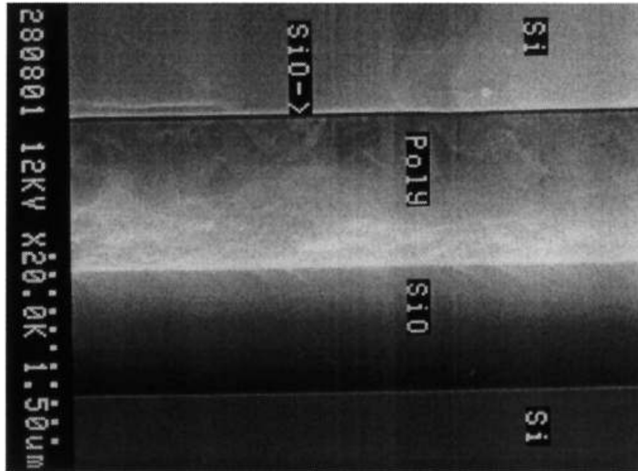

Fig. 10. SEM image showing the cross section of a SISI sandwich wafer. The top silicon layer is 25 μm thick. The LPCVD polysilicon layer is 1.5 μm thick. The upper and lower silicon dioxide layers are 50 nm and 1 μm thick respectively. The interface between the LPCVD polysilicon and the lower silicon dioxide layer is the bond interface

it cannot be explained by using the power spectrum analysis why a 'soft' material, e.g. SiO_2, is bonded more easily than a 'hard' material, e.g. $Si_{3+x}N_y$, even though both of them have the same surface roughness; or why hydrophobic bonding seems to be more sensitive to the surface micro roughness than hydrophilic bonding. These questions can be answered however, if, together with the surface topography, the material elastic properties and the surface energy are taken into account in evaluating wafer bondability.

Here, we consider the elastic contact between a nominally flat, rough surface and a nominally flat, perfectly smooth surface. The roughness of the nominally flat, rough surface is assumed to be a random series of asperities, which have spherical caps of the same constant radius β, with a Gaussian height distribution:

$$\phi(z) = \frac{1}{(2\pi)^{1/2}} \exp\left\{-\frac{z^2}{2\sigma^2}\right\} \tag{1}$$

where $\phi(z)\,dz$ is the probability that an asperity has a height between z and $z+dz$ above the plane defined by the mean asperity height, σ is the standard deviation of the distribution of asperity heights.

The adhesion parameter $1/\Delta_c$, which is defined as the ratio of the standard deviation of the distribution of asperity heights to the extension which an asperity can sustain before the adhesion breaks, can be derived as, Fuller and Tabor (1975):

$$\frac{1}{\Delta_c} = 0.513\,\frac{\sigma}{\beta^{1/3}}\left\{\frac{K}{\Delta\gamma}\right\}^{2/3} \tag{2}$$

where β is the radius of curvature of the spherical asperity, $\Delta\gamma$ is the surface energy between the two contacted surfaces, and K is the elastic constant defined by the Poisson ratio and the Young's modules of the two materials:

$$K = \frac{4}{3}\left\{\frac{1-\nu_1^2}{E_1} + \frac{1-\nu_2^2}{E_2}\right\}^{-1} \tag{3}$$

Table 2. The adhesion parameters of different rough surfaces bonded to a perfectly smooth flat silicon wafer

Surface conditions	$1/\Delta_c$ before CMP	$1/\Delta_c$ after CMP
KOH etched silicon	10.0 ~ 14.6	0.23 ~ 0.34
P^{++} doped silicon	5.5 ~ 8.0	0.35 ~ 0.51
LPCVD $Si_{3+x}N_4$	3.9 ~ 5.7	0.26 ~ 0.38

Figure 6 of Fuller and Tabor (1975) presents the relation between the relative pull-off force of the contacted interface and the adhesion parameter. The relative pull-off force needed to separate the interface decreases by increasing the adhesion parameter. Once $1/\Delta_c > 3$, no force is needed to separate the interface.

The calculated adhesion parameters of wafers having different surface conditions, which are assumed to be bonded to a nominally flat, perfectly smooth silicon wafer, are summarized in Table 2. The adhesion parameters decrease from higher than 3 to well below it, which means that the unbondable wafers become bondable. Note that the bondability in Table 1 corresponds reasonably well with the adhesion parameter in Table 2, which demonstrates the predictive power of the adhesion parameter.

6 Conclusion

CMP has been shown to be a very promising *on-site* technique for SFB, which grants more freedom in application of SFB in silicon micromachining. KOH etched Si wafer surface, P^{++} Si wafer surface, LPCVD $Si_{3+x}N_4$ and LPCVD polysilicon layers, which were believed to be not spontaneously bondable, have been successfully bonded after CMP. The enhanced surface roughness was found to be responsible for the poor bondability of the above mentioned surfaces before polishing. As long as surface roughness is the main concern, more silicon related materials, such as PECVD SiO_2, PECVD Si_xN_y, sputtered silicon and polysilicon and so on, can be made fusion bondable after a polishing step. Based on surface contact mechanics, an adhesion parameter, which includes both the mechanical and chemical properties of the surface, was introduced to evaluate the bondability of wafers. This parameters gives a reasonably good prediction of the bondability.

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