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G4-FET modeling for circuit simulation by adaptive neuro-fuzzy training systems

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Abstract: G4-FET has attracted attention as an emerging device for the future generations of semiconductor industry. This paper is intended to propose a model representing the characteristics of G4-FET device in order to perform circuit simulations. The modeling approach is established upon the neuro-fuzzy technique whose main strength is that they are universal approximators with the ability to solicit interpretable IF-THEN rules. The accuracy of the proposed model is verified by HSPICE circuit simulations.

Keywords: G4-FET, adaptive neuro-fuzzy training systems, semiconductor industry, circuit simulation, HSPICE model

Classification: Electron devices, circuits, and systems

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1 Introduction

To increase the current drivability and reduce short-channel effects, the international technology road map (ITRS) depicts switching from bulk to multiple-gate SOI devices [1]. Among multiple-gate devices, four-gate transistor (G4-FET) has become a promising candidate for the circuit design because of its maximum functional flexibility, high intrinsic DC gain, low-noise operation and radiation hardness [1]. In G4-FETs if we drive all gates, we have the opportunity to build multiple-input circuits with much reduced transistor count compared to their CMOS counterparts. For instance, it is possible to create a digital non-majority voting circuit with only one G4-FET and a load device [2].

Various publications like [3, 4] introduced analytical models for this structure. In [4], a simple model that links the drain–current to the terminal voltages is introduced for only a specific mode in which majority carriers flow in the volume of the silicon film far from the silicon/oxide interfaces.

Analytical models in all operating modes for such devices are required to be utilized in circuit simulation and design tools. Here, we propose a technique to include G4-FET devices in HSPICE netlist making use of adaptive neuro-fuzzy training systems. Our intention is to provide a framework to facilitate the simulation of G4-FET based circuits.

2 Device simulations

The structure of an N-channel G4-FET device is demonstrated in Fig. 1 (a). It is a majority carrier, buried channel, accumulation mode device. It has two vertical MOS gates and has two lateral JFET gates that make up PN junctions with the channel region [5]. To control the conduction path, we can apply a suitable bias to each of the four gates. For an N-type device, by applying a negative voltage to the top gate, the channel region below this gate could be depleted. Similarly, negative voltages applied to either of the JFET gates broaden (narrow) the PN-junction depletion region (channel region) [6]. By combining MOS and JFET effects in the G4-FET, the three possible current components are modulated as follow: the front interface accumulation current chiefly controlled by the front-gate, the back interface accumulation current mainly controlled by the back gate and the volume

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current whose cross-sectional dimensions are regulated by the depletion of all the gates [5]. It is important to note that the N-type structure is equivalent to that of a P-channel inversion mode SOI MOSFET with two body contacts on each side of the channel [7]. Therefore, the G4-FET can be fabricated with typical SOI CMOS process [7].

To simulate the device, the Sentaurus device simulator tool [8] was used. The density gradient transport model is used for transport which solves the quantum potential equations self-consistently with the Poisson and carrier continuity equations [8]. Fig. 1 (b) and (c) show the I-V and C-V characteristics, respectively, when both V_{Jgate} voltages are equal to -3.3 V.

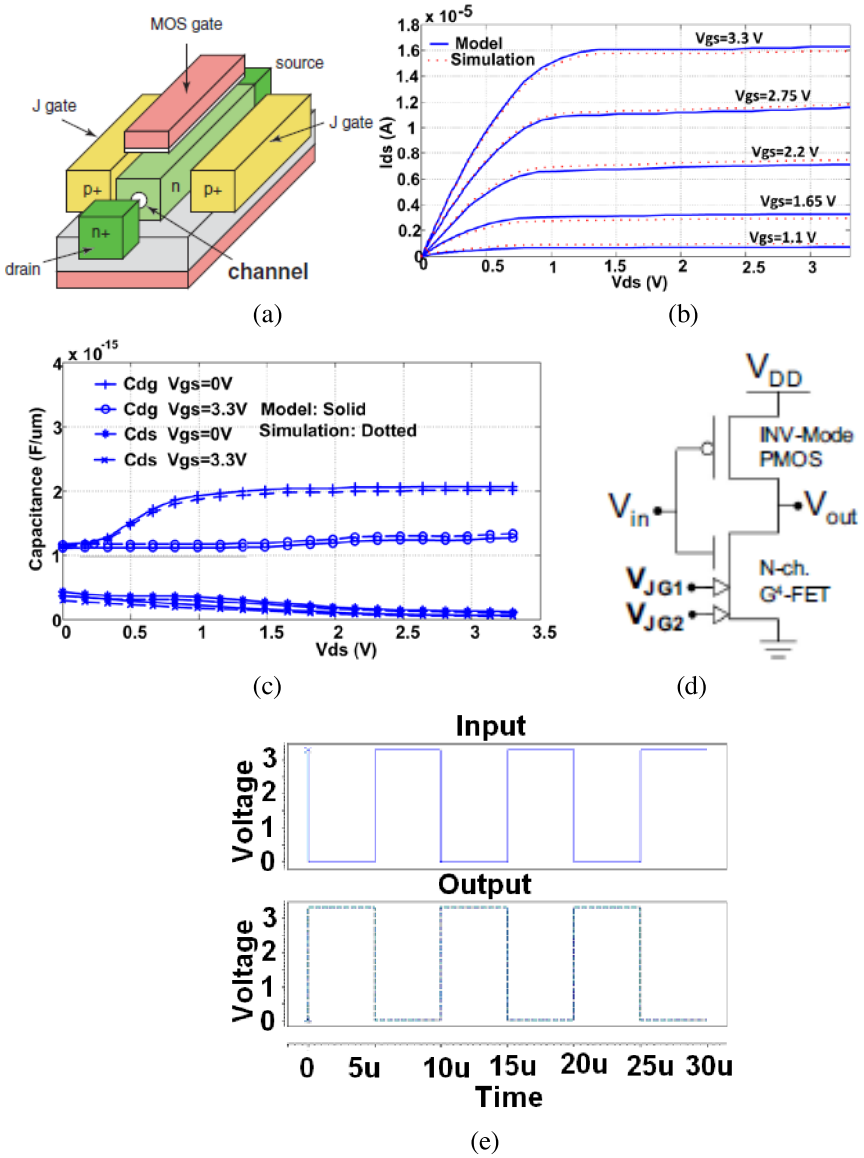

Fig. 1. (a) N-type G4-FET, (b) I-V and (c) C-V characteristics when V_{Jgate}s are equal to -3.3 V, (d) an inverter using G4-FET (e) Input and Output signals of Inverter (channel length, silicon thickness, and buried oxide thickness are 1.2 μm, 20 nm, and 100 nm, respectively).

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3 Adaptive neuro-fuzzy training system

ANFIS is an adaptive network which combines the application of neural network and fuzzy logic. One of the major applications of ANFIS is modeling of nonlinear systems and functions. For this purpose in the fuzzy section, only the zeroth-order or first order Sugeno inference system or the Tsukamoto inference system can be used [9].

For simplicity, we assume that the fuzzy inference system has two inputs (x, y) and one output (f). For a first-order Sugeno fuzzy model, a typical rule set with fuzzy-based IF-THEN rules can be expressed as:
Rule 1: If x is A_1 and y is B_1, then

$$f_1 = p_1 x + q_1 y + r_1 \tag{1}$$

Rule 2: If x is A_2 and y is B_2, then

$$f_2 = p_2 x + q_2 y + r_2 \tag{2}$$

Here p_i, q_i, and r_i are linear output parameters where $i = 1, 2$.

The reasoning mechanism for this sugeno model is shown in Fig. 2 (a). The corresponding equivalent ANFIS architecture is also shown in Fig. 2 (b).

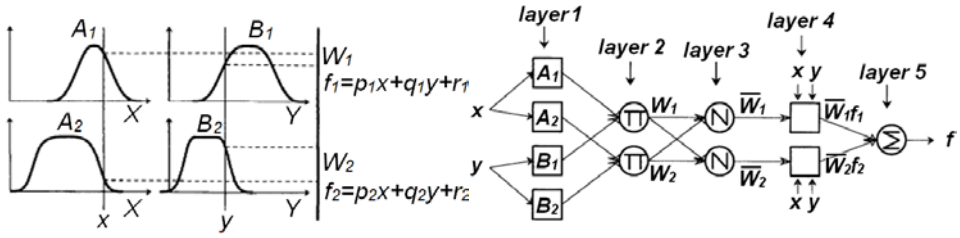

Fig. 2. (a) Inference method of sugeno model, (b) ANFIS architecture based on sugeno.

It should be noted that the circle indicates a fixed node, whereas the square indicates an adaptive node. A description of the layers in the network is summarized as follows:

Layer 1: Every node in this layer is an adaptive node with a node output defined by

$$O_{1,i} = \mu_{Ai}(x), \ i = 1, 2, \ldots, \tag{3}$$

$$O_{1,i} = \mu_{Bi-2}(y), \ i = 3, 4, \ldots, \tag{4}$$

where i is the membership grade of a fuzzy set (A_1, A_2, B_1, B_2) and $O_{1,i}$ is the output of the node i in Layer 1. The membership function that has been used in this study is the Gaussian function given by

$$\mu_A(x) = \exp\left(\frac{-0.5(x-c)^2}{\sigma^2}\right) \tag{5}$$

where c and σ are referred to as premise parameters.

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Layer 2: Each node in this layer is a fixed node and calculates the firing strength of a rule via multiplication. The outputs are given by

$$O_{2,i} = w_i = \mu_{Ai}(x).\ \mu_{Bi}(y),\ \ i = 1, 2. \tag{6}$$

In general, any other T-norm operator performing fuzzy AND method can be used as the node function in this layer.

Layer 3: Every node in this layer is also fixed and performs a normalization of the firing strength from the previous layer. The outputs of this layer are called normalized firing strengths and are given by

$$O_{3,i} = \overline{w_i} = \frac{w_i}{w_1 + w_2}, i = 1, 2 \tag{7}$$

where $O_{3,i}$ denotes the Layer 3 output.

Layer 4: In this layer, all nodes are adaptive, and the output of a node is the product of the normalized firing strength and a first-order polynomial given by

$$O_{4,i} = \overline{w_i} f_i = \overline{w_i}(p_i x + q_i y + r_i),\ \ i = 1, 2, \tag{8}$$

where w_i is the output of Layer 3, and (p_i, q_i, r_i) is the parameter set. Parameters in this layer are referred to as the consequent parameters.

Layer 5: The single node in this layer is a fixed node and computes the overall output as the summation of all incoming signals

$$O_{5,i} = \sum_i \overline{w_i} f_i = \frac{\sum_i w_i f_i}{\sum_i w_i},\ \ i = 1, 2, \tag{9}$$

where $O_{5,i}$ denotes the Layer 5 output.

A hybrid learning algorithm is used for ANFIS training, and it consists of two stages: forward pass and backward pass. In the forward pass, the consequent parameters are identified by the least squares estimation, and in the backward pass, the premise parameters are updated by the gradient descent. Further details about ANFIS and these learning algorithms can be found in [9].

In this paper, we used ANFIS for modeling of G4-FET device. For this purpose, we assumed terminal voltages, W, and L as input parameters while I_D and capacitances among different terminals have been assumed as output parameters for this device. The minimum and maximum data ranges used to develop the ANFIS model are shown in Table I (a).

4 Simulation results and discussion

4.1 ANFIS Modeling

For modeling of G4-FET, we obtained more than 2500 data for each output parameter from device simulator and then we used about 80% of these data for training of ANFIS and remaining were used for testing of trained ANFIS structure. Also, we implemented different structures for ANFIS and in each case we measured the train and test error of ANFIS structures. Different

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ANFIS structures and relative errors are shown in Table I (b). The selected ANFIS structure for modeling of G4-FET device is shown in Table I (c). In fact, by increasing the number of membership functions and rules, we can decrease the errors but the system will be much complicated and less efficient. Fig. 1 (b) and (c) demonstrate high accuracy for our modeling approach.

After Modeling of G4-FET with ANFIS structure, we can use it in HSPICE. To the best of our knowledge, no SPICE models such as BSIMs have been developed for this kind of device. In fact, we can use the ANFIS as a neuro-fuzzy behavioral model in a circuit simulator after translating the ANFIS equations into an appropriate syntax. The main elements contributing to the nonlinear behavior of the G4FET device are the drain current I_D and capacitances among different terminals which are the functions of the V_{GS}, V_{JG1S}, V_{JG2S}, V_{DS}, W and L parameters. V_{GS}, V_{JG1S}, V_{JG2S}, V_{DS}, and I_D are respectively, the gate source voltage, junction-gate source voltages, drain source voltage, and drain current. Besides, L and W are channel length and width of G4-FET device, respectively. Therefore, in HSPICE implementation, the G4-FET may be considered as a voltage-controlled current source with nonlinear capacitances among different terminals.

4.2 Circuit Modeling

After optimizing the proposed ANFIS structure, all parameters of Gaussian input membership functions and linear output parameters are obtained. The firing strength of each rule can be calculated via multiplication of the

Table I. (a) Data ranges used for ANFIS structure, (b) Different ANFIS structures and relative errors, (c) Specifications of proposed ANFIS structure.

(a)

Range	V_{GS1}	V_{GS2}	V_{GS3}	V_{DS}	W	L
Min	0	-3.3 V	-3.3 V	0	100 nm	1.2 um
Max	3.3 V	0	0	3.3 V	500 nm	3.4 um

(b)

MF (in1)	MF (in2)	MF (in3)	MF (in4)	MF (in5)	MF (in6)	No. of Rules	Train Error	Test Error
3	2	2	4	2	2	192	3.24E-07	4.18E-07
3	3	3	2	2	2	216	2.78E-07	3.39E-07
2	3	3	3	2	2	216	1.16E-07	1.41E-07
4	3	3	2	2	2	288	2.87E-07	3.78E-07
3	3	3	3	2	2	324	1.07E-07	1.43E-07
3	3	3	4	2	2	432	7.38E-08	1.19E-07

(c)

Type	Sugeno
Input/Output	6/10
No. of input membership functions	2 for input1,5,6 and 3 for other inputs
No. of output membership functions	216
Input membership function type	Gaussian
Output membership function type	Linear
No. of fuzzy rules	216
No. of linear parameters	1080
No. of nonlinear parameters	30
No. of epochs	50

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Gaussian input membership functions (fuzzy AND), and the final outputs of the model are calculated as the summation of the contribution from each rule. We implemented these equations in HSPICE netlist [10]. For testing G4-FET operation, we simulated an inverter by using G4-FET and a conventional PMOS transistor as shown in Fig. 1 (d). In this structure, we connected both junction gates to ground and by applying a pulse to input, we could see operation of inverter. The transient simulation results presented in Fig. 1 (e) verify the functionality of our model. So, we can use this model for simulating more complex G4FET-based circuits. We also measured the CPU time for the ANFIS model by using MATLAB. For 50 simulation points, the CPU time for ANFIS model is 250 s. The ANFIS model is much faster than device simulator which it takes more than 14200 s to simulate 50 points.

5 Conclusion

In this paper, we presented a method to model the characteristics of G4-FET transistors. We performed extensive simulations on G4-FET device to extract sufficient data to train an adaptive neuro-fuzzy system. We took advantage of ANFIS whose major application is modeling nonlinear systems and functions. Having trained the system, we obtained the SPICE netlist of the G4-FET device. The extracted SPICE netlist was used in the netlist of an Inverter gate to verify the functionality of the device. The simulations revealed that the operation of a circuit based on our proposed model for G4-FET device is correct. Thus, the proposed method is applicable for simulating the G4-FET based circuits. Also, the CPU time will be improved by using ANFIS modeling.

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