HOKKAIDO UNIVERSITY

Title	GaAs nanowire growth on polycrystalline silicon thin films using selective-area MOVPE
Author(s)	Ikejiri, Keitaro; Ishizaka, Fumiya; Tomioka, Katsuhiro; Fukui, Takashi
Citation	Nanotechnology, 24(11), 115304 https://doi.org/10.1088/0957-4484/24/11/115304
Issue Date	2013-03-22
Doc URL	http://hdl.handle.net/2115/55281
Rights	This is an author-created, un-copyedited version of an article accepted for publication in Nanotechnology. IOP Publishing Ltd is not responsible for any errors or omissions in this version of the manuscript or any version derived from it. The definitive publisher authenticated version is available online at 10.1088/0957-4484/24/11/115304.
Type	article (author version)
File Information	Revised Manuscript.pdf

GaAs Nanowire Growth on Polycrystalline Silicon Thin Films Using Selective-area MOVPE

Keitaro Ikejiri[†, a)], Fumiya Ishizaka[†, b)], Katsuhiro Tomioka[†, ‡], and Takashi Fukui[†]

[†]Graduate School of Information Science and Technology and Research Center for Integrated Quantum Electronics, Hokkaido University, North 13, West 8, Sapporo, 060-8628, Japan

[‡]Japan Science and Technology Agency–PRESTO, Kawaguchi 332-0012, Japan

a) Email: ikejiri@rciqe.hokudai.ac.jp

b) Email: ishizaka@rciqe.hokudai.ac.jp

ABSTRACT

The growth mechanism of GaAs nanowires (NWs) grown on polycrystalline silicon (poly-Si) thin films using selective-area metalorganic vapor-phase epitaxy was investigated. Wire structures were selectively grown in the mask openings on a poly-Si substrate. The appearance ratio of wire structures strongly depended on the growth conditions and deposition temperature

of the poly-Si substrate. Evaluation of the grown shapes and growth characteristics revealed that GaAs NWs grown on a poly-Si substrate have the same growth mechanism as conventional GaAs NWs grown on a single-crystalline GaAs or Si substrate. Experiments showed that the wire structure yield can be improved by increasing the Si grain size and/or increasing the Si deposition temperature. The growth model proposed for understanding NW growth on poly-Si is based on the mask opening size, the Si grain size, and the growth conditions. The ability to control the growth mode is promising for the formation of nanowires with complex structures on poly-Si thin layers.

1. Introduction

Semiconductor nanowires (NWs), which have diameters on the nanometer scale, can be produced by using a crystal growth technique and can potentially be fabricated with various kinds of structures such as radial (core-shell) [1–3], axial [4,5], hetero, and quantum dot [6–8]. Such NW structures could be used in nanoscale devices including light-emitting diodes (LEDs) [9–11], lasers [12], photodetectors [13], field effect transistors [1,9], and photovoltaic devices [14]. Core-shell NWs are a promising candidate for high-efficiency LEDs because these types of heterostructures have large surface areas with diameters on the nanometer scale and can potentially have a junction area more than ten times that of conventional planar LEDs.

We have grown III–V compound semiconductor NWs by using selective-area metal organic vapor-phase epitaxy (SA-MOVPE) [1–3,5,11,14–19]. With this method, III–V NWs with precise positioning and vertical alignment have been grown on not only III–V substrates but also Si ones regardless of any mismatch in the lattice constant [15,16]. The elastic relaxation of a strained layer occurs near the interface because the crystal growth area is limited to only the small openings in an amorphous mask. This is greatly advantageous for selecting both NW and substrate materials. For example, NWs can be formed on lattice mismatched substrates such as GaAs/Si [16] and InAs/Si [15]. We previously grew AlGaAs/GaAs core-multi-shell NW LEDs on Si [11].

Scarce resources such as Ga and In must be used efficiently, and conventional LEDs contain a large amount of such high-cost rare materials in their substrates. In contrast, NW LEDs can be grown on a low-cost Si substrate. Further progress in developing low-cost LEDs is expected to follow the emergence of glass-based poly-crystalline silicon (poly-Si) thin-film substrates for NW optical devices owing to their lower production cost and greater scalability than conventional LED structures formed on compound semiconductor substrates. Poly-Si substrates are formed using mature processes that have been used to form glass-based flat-panel displays, and they have good compatibility with high-volume manufacturing processes.

NWs have been synthesized by vapor–liquid–solid growth on a non-single crystalline surface

such as InP nano-needles on microcrystalline silicon surfaces [20,21], Si NWs have been grown

on amorphous Si substrates by host- mediated catalyst growth [22], and InP NWs have been

grown on oxidized silicon substrates by laser-assisted catalytic growth [23]. However, there

have been no detailed reports on the growth mechanism of NWs grown on microcrystalline or

non-crystalline surfaces from the crystal growth point of view. To be able to grow a nanowire

device on poly-Si we need to understand the mechanism of selective area growth of nanowires

on a polycrystalline surface. We can then fabricate an appropriate NW structure for the device

application, especially LEDs. Here, we demonstrate the growth of GaAs NWs on poly-Si by

SA-MOVPE and clarify the correlation between the growth morphology, the growth conditions,

and the crystallinity of the underlying poly-Si.

2. Experimental procedure

A 50-nm-thick poly-Si thin film was used as the substrate. It was deposited on a 300-nm-thick

SiO_2-coated Si (001) wafer using RF sputtering. The SiO_2-coated Si (001) wafer corresponds to

an equivalent glass substrate. The SiO_2/Si wafer temperature (T_S) during poly-Si deposition

ranged from room temperature (RT) to 600°C. Next, a 20-nm-thick SiO_2 layer was formed on

the poly-Si substrate as a mask by thermal oxidation at 900°C. It was then partially removed

using electron beam lithography and wet chemical etching to form periodic mask openings as a

template for selective-area growth. A grown substrate is schematically illustrated in Fig. 1 (a).

The diameter, d_0, of the openings varied from 60 to 200 nm, and the opening pitch, a, of the mask was 500 nm. Finally, these substrates were degreased in organic solvents in an ultrasonic bath and slightly etched with buffered HF (BHF) solution to remove the native oxide that had formed on the openings during processing.

Next, GaAs growth was carried out using a horizontal low-pressure MOVPE system. The total flow rate of the gases was maintained at 5.75 standard liters per minute. The working pressure was 0.1 atm, and the source materials were trimethylgallium (TMG) and arsine (AsH$_3$). The growth time was 30 minutes. The partial pressures of the TMG and AsH$_3$ were 2.5×10^{-6} and 5.0×10^{-4} atm, respectively, which are typical conditions for growing GaAs nanowires on Si (111) substrates [16]. Prior to growth, thermal cleaning in an H$_2$ ambient was carried out at 900°C to remove the native oxide on the mask openings. The growth temperature (T$_G$) was 650, 700, or 760°C. The grown structures were characterized by scanning electron microscopy (SEM) and transmission electron microscopy (TEM).

3. Results and discussion

3.1 Growth morphologies of GaAs on poly-Si thin films

For the selective-area MOVPE, we used partially opened amorphous thin films as mask templates. We previously grew GaAs NWs on GaAs (111)B [17,19] and Si (111) [16] substrates

that were well controlled in terms of size and position. The growth mechanism was faceting growth without any catalyst [19].

An SEM image of GaAs grown at 700°C on poly-Si is shown in Fig. 1 (b). The underlying poly-Si substrate had been deposited at 600°C. GaAs NWs with a hexagonal pillar shape were partly obtained on poly-Si thin films (Fig. 1(c)). GaAs NWs have six-fold {−110} hexagonal sidewalls and grow in the <111>B direction [16,17,19]. Therefore, the hexagonal sidewalls of the nanowires on the poly-Si thin films were considered to have six-fold {−110} oriented facets and to have grown in the <111>B direction. This growth in an inclined direction probably reflects the orientations of the poly-Si grains in the mask openings.

Hillock structures that were polycrystalline islands of GaAs (Fig. 1(d)) and no growth openings (Fig. 1(e)) were also observed. SEM analysis revealed no thermal deformations or heat shrinking of the SiO_2 template during growth. The appearance ratio for the three types of growth morphologies (wire, hillock, and no growth) as a function of the diameter of the openings (d_0) are shown in Fig. 2. The highest appearance ratio for NW structures was at an opening diameter of 100 nm. The appearance ratio for hillock structures increased with the opening diameter. The appearance ratio for no growth was higher for a smaller d_0. These results indicate that the appearance ratio strongly depends on d_0. The model we propose to explain the dependency of the growth morphology on d_0 is as follows. When d_0 is small, an initial nucleus of GaAs on Si is

difficult to form because there is insufficient area for forming a stable nucleus on a Si grain in a

mask opening. This is why the occurrence probabilities for both wire and hillock structures were

low when d_0 was 100 nm or less. When d_0 was around 100 nm, NWs were more likely to grow

because the openings were more likely to have only one Si grain, meaning that the growth was

equivalent to that on a single-crystalline Si surface. When d_0 was larger, hillock structures,

which originated from irregular growth on the grain boundary, were more likely to grow

because the openings were more likely to have several Si grains. Under such conditions,

nucleations occurred for more than one grain in a mask opening simultaneously. The resulting

crystal nuclei interfered with each other, causing irregular polycrystalline structures to form.

To obtain more information about the formation of wire structures on poly-Si, we analyzed

GaAs wire and poly-Si interface by TEM with the electron beam parallel to the (1−10) side

facet of the NWs. Figure 3 shows TEM results of GaAs NWs grown at 700°C on a poly-Si

substrate that had been deposited at 600°C. Figure 3 (a) shows a TEM image of a whole NW

that indicates that there was lateral overgrowth of GaAs onto the SiO_2 masked area near the base

of the grown crystal. However, the nanowires had a constant width (no tapering). Figures 3 (b)

and (c) show high-resolution TEM images of the top and bottom part of the NWs showing that

the nanowires grew in the [111] direction. Analysis of the selected area diffraction pattern

revealed that the bright and dark contrast corresponding to the radial direction of the NWs was due to rotational twins of the zincblende lattice in the NWs.

The results of our structural analysis clearly indicate that the GaAs NWs that formed on the poly-Si substrate had a growth mode similar to that of GaAs NWs that form on single-crystalline GaAs [18] and Si [16]. Moreover, the current NWs were inclined 6° with respect to the perpendicular direction of the substrate. This angle agrees well with the tilted angle of the crystal axis of the Si grain at the base region of the NWs (marked by the solid line in Fig. 3 (f)]. This indicates that there is a heteroepitaxial relationship between a GaAs NW and a Si grain located at the base of the NW. Furthermore, when the mask openings are mostly occupied by a single crystal grain, as shown in Fig. 3 (f), NW growth proceeds via lateral overgrowth of GaAs onto other Si grains near the base of the grown crystal. These analysis results strongly support the model of crystal growth described earlier in this section.

3.2 Grown structures dependency on growth temperature

Figure 4 (a) shows the appearance ratio of wire structures as a function of the growth temperature. The underlying poly-Si deposition temperature and mask opening diameter were 300 or 600°C and 100 nm, respectively. The highest appearance ratio for wire formation was obtained at ~700°C. This tendency is similar to the T_G dependency of the growth rate of GaAs NWs on Si(111) substrates, as shown in Fig. 4(b). These results clearly indicate that the appearance ratio of wire structures on poly-Si is correlated with the NW growth rate in the

<111>B direction. This relationship can be explained by the growth model presented below. The temperature dependence of the GaAs NW growth rate indicates that the amount of growth species migrating to the NW top surface from the side surface of the grown structures and surrounding SiO_2-masked area decreases as the temperature is increased [18]. Under high T_G conditions, re-evaporation (desorption) of source materials from the surface is dominant, so the wire growth rate decreases while the wire appearance ratio decreases. Under low T_G conditions, the GaAs NW growth rate is also suppressed because the effective coverage of As is high under this condition, so an As overlayer covers the As-terminated (111)B surface, resulting in the formation of stable As trimmers [24]. These trimmers prevent growth from proceeding on the (111) B surface, so the growth rate is reduced. This is the main reason few wire structure were observed on poly-Si thin layers under low T_G conditions. These results for growth condition dependence indicate that the growth mechanism of GaAs nanowires on poly-Si by SA-MOVPE is attributable to the faceting-growth mechanism [19], in which the growth rate of each facet has a strong relationship with the growth conditions, including T_G, the same as for growth on single-crystalline GaAs and Si, for which the growth direction is also <111>B. Moreover, a growth condition that results in a higher growth rate in the <111>B direction results in an increase in the appearance ratio of wire mode growth on poly-Si.

3.3 Grown structures dependency on poly-Si deposition temperature

Finally, we grew GaAs on substrates that had been deposited at different temperatures with T_G and d_0 fixed at 760°C and 100 nm, respectively. As shown in Fig. 5, the appearance ratio of wire structures increased with T_S. Since re-crystallization of Si is enhanced at higher temperature during Si deposition [25], the openings most likely had a single-crystalline surface even if the mask opening diameter was the same because the grain size of poly-Si is enlarged during the deposition of Si under higher temperature conditions. As a result, a nucleus was preferentially formed in the mask openings, which promoted stable wire growth. These results show that increasing the size of the grains by optimizing the Si deposition temperature effectively improves wire yield. This controllability of the growth mode is promising for formation of nanowires with complex structures, such as core-shell heterostructures and pn junctions, on poly-Si thin layers.

4. Summary

We investigated the SA-MOVPE growth of GaAs nanowires on poly-Si thin layers by clarifying the dependence on the growth conditions and Si deposition temperature. Our investigation of the GaAs growth morphology dependency on the mask opening diameter showed that nanowire yield correlates with the diameter of the openings and the grain size of the poly-Si. We also showed that GaAs nanowires grown on a poly-Si substrate have the same growth mechanism as

conventional GaAs nanowires grown on a GaAs substrate. The nanowire yield can be improved by adjusting the growth conditions so that the growth rate is higher in the <111>B direction. Finally, we also showed that the wire structure yield is improved by increasing the size of the grains and/or the temperature during Si deposition. The key parameters for nanowire yield are the grain size of the poly-Si layer and the growth conditions. This ability to control the growth mode is promising for the formation of nanowires with complex structures, such as core-shell heterostructures and pn junctions, on poly-Si thin layers.

ACKNOWLEDGMENTS

References

[1]   Tomioka K, Yoshimura M and Fukui T 2012 A III-V nanowire channel on silicon for high-performance vertical transistors. *Nature* **488** 189–92

[2]   Mohan P, Motohisa J and Fukui T 2006 Fabrication of InP⁄InAs⁄InP core-multishell heterostructure nanowires by selective area metalorganic vapor phase epitaxy *Applied Physics Letters* **88** 133105

[3]   Noborisaka J, Motohisa J, Hara S and Fukui T 2005 Fabrication and characterization of freestanding GaAs⁄AlGaAs core-shell nanowires and AlGaAs nanotubes by using selective-area metalorganic vapor phase epitaxy *Applied Physics Letters* **87** 093109

[4]   Heiss M, Gustafsson A, Conesa-Boj S, Peiró F, Morante J R, Abstreiter G, Arbiol J, Samuelson L and Fontcuberta i Morral A 2009 Catalyst-free nanowires with axial InxGa1-xAs/GaAs heterostructures. *Nanotechnology* **20** 075603

[5]   Yang L, Motohisa J, Takeda J, Tomioka K and Fukui T 2006 Size-dependent photoluminescence of hexagonal nanopillars with single InGaAs⁄GaAs quantum wells fabricated by selective-area metal organic vapor phase epitaxy *Applied Physics Letters* **89** 203110

[6]   Fuhrer A, Fröberg L E, Pedersen J N, Larsson M W, Wacker A, Pistol M-E and Samuelson L 2007 Few electron double quantum dots in InAs/InP nanowire heterostructures. *Nano letters* **7** 243–6

[7]   Minot E D, Kelkensberg F, Van Kouwen M, Van Dam J A, Kouwenhoven L P, Zwiller V, Borgström M T, Wunnicke O, Verheijen M A and Bakkers E P A M 2007 Single quantum dot nanowire LEDs. *Nano letters* **7** 367–71

[8]   Zwiller V, Akopian N, Van Weert M, Van Kouwen M, Perinetti U, Kouwenhoven L, Algra R, Gómez Rivas J, Bakkers E, Patriarche G, Liu L, Harmand J-C, Kobayashi Y and Motohisa J 2008 Optics with single nanowires *Comptes Rendus Physique* **9** 804–15

[9]   Duan X, Huang Y, Cui Y, Wang J and Lieber C M 2001 Indium phosphide
        nanowires as building blocks for nanoscale electronic and optoelectronic
        devices. *Nature* **409** 66–9

[10]   Qian F, Li Y, Gradecak S, Wang D, Barrelet C J and Lieber C M 2004
        Gallium nitride-based nanowire radial heterostructures for nanophotonics
        Nano Letters **4** 1975–9

[11]   Tomioka K, Motohisa J, Hara S, Hiruma K and Fukui T 2010 GaAs/AlGaAs
        core multishell nanowire-based light-emitting diodes on Si. *Nano letters* **10**
        1639–44

[12]   Duan X, Huang Y, Agarwal R and Lieber C M 2003 Single-nanowire
        electrically driven lasers. *Nature* **421** 241–5

[13]   Wang J, Gudiksen M S, Duan X, Cui Y and Lieber C M 2001 Highly polarized
        photoluminescence and photodetection from single indium phosphide
        nanowires. *Science* **293** 1455–7

[14]   Goto H, Nosaki K, Tomioka K, Hara S, Hiruma K, Motohisa J and Fukui T
        2009 Growth of Core–Shell InP Nanowires for Photovoltaic Application by
        Selective-Area Metal Organic Vapor Phase Epitaxy *Applied Physics Express*
        2 035004

[15]   Tomioka K, Motohisa J, Hara S and Fukui T 2008 Control of InAs nanowire
        growth directions on Si. *Nano letters* **8** 3475–80

[16]   Tomioka K, Kobayashi Y, Motohisa J, Hara S and Fukui T 2009
        Selective-area growth of vertically aligned GaAs and GaAs/AlGaAs core-shell
        nanowires on Si(111) substrate. *Nanotechnology* **20** 145302

[17]   Motohisa J, Takeda J, Inari M, Noborisaka J and Fukui T 2004 Growth of
        GaAs/AlGaAs hexagonal pillars on GaAs (111)B surfaces by selective-area
        MOVPE *Physica E: Low-dimensional Systems and Nanostructures* **23**
        298–304

[18]   Ikejiri K, Sato T, Yoshida H, Hiruma K, Motohisa J, Hara S and Fukui T 2008 Growth characteristics of GaAs nanowires obtained by selective area metal-organic vapour-phase epitaxy *Nanotechnology* **19** 265604

[19]   Ikejiri K, Noborisaka J, Hara S, Motohisa J and Fukui T 2007 Mechanism of catalyst-free growth of GaAs nanowires by selective area MOVPE *Journal of Crystal Growth* **298** 616–9

[20]   Kobayashi N P, Wang S-Y, Santori C and Williams R S 2006 Growth and characterization of indium phosphide single-crystal nanoneedles on microcrystalline silicon surfaces *Applied Physics A* **85** 1–6

[21]   Kobayashi N P, VJ L, Saif Islam M, Li X, Straznicky J, Wang S-Y, Stanley Williams R and Chen Y 2007 Hydrogenated microcrystalline silicon electrodes connected by indium phosphide nanowires *Applied Physics Letters* **91** 113116

[22]   Wang C, Murphy P F, Yao N, McIlwrath K and Chou S Y 2011 Growth of straight silicon nanowires on amorphous substrates with uniform diameter, length, orientation, and location using nanopatterned host-mediated catalyst. *Nano letters* **11** 5247–51

[23]   Gudiksen M S, Wang J and Lieber C M 2002 Size-Dependent Photoluminescence from Single Indium Phosphide Nanowires *The Journal of Physical Chemistry B* **106** 4036–9

[24]   Hayakawa T, Morishima M and Chen S 1991 Surface reconstruction limited mechanism of molecular-beam epitaxial growth of AlGaAs on (111)B face *Applied Physics Letters* **59** 3321

[25]   Wakayama Y, Tagami T and Tanaka S 1999 Formation of Si islands from amorphous thin films upon thermal annealing *Journal of Applied Physics* **85** 8492

Figure Captions

Fig. 1   (a) Schematic illustration of growth substrate. SEM birds-eye-view images of grown substrate (b), wire structure (c), hillock structure (d), and no growth (e) for opening diameter of 100 nm and growth on poly-Si substrate at 700°C. Substrate poly-Si deposition temperature was 600°C.

Fig. 2   Appearance ratios for three types of growth morphologies against mask opening diameter. T_G and T_S were 700 and 600°C, respectively.

Fig. 3   Cross-sectional transmission electron microscopy (TEM) images of GaAs nanowire grown at 700°C on poly-Si substrate. Substrate was deposited at 600°C. Incident angle of electron beam was parallel to (1-10) side facet of GaAs nanowire. (a) Overall image of GaAs nanowire. (b) and (c) Enlarged images of open square near nanowire tip and base shown in (a), respectively. (d) and (e) High-resolution TEM images of Si grain near base of GaAs nanowire and GaAs nanowire, respectively. Insets show selected area diffraction patterns of each area obtained through fast Fourier transformation process. (f) Schematic illustration of TEM image in (c).

Fig. 4   (a) Appearance ratio of wire structures for T_S = 300 and 600°C against T_G. (b) Growth rate of nanowires on Si (111) against T_G.

Fig. 5   Appearance ratio of wire structures against T_S when T_G and d were fixed at 760°C and 100 nm, respectively.

Figure 1

(a)

a

d_0

SiO$_2$ Mask

Poly-Si Layer

SiO$_2$ Layer

Si(001) Substrate

Equivalent Glass Substrate
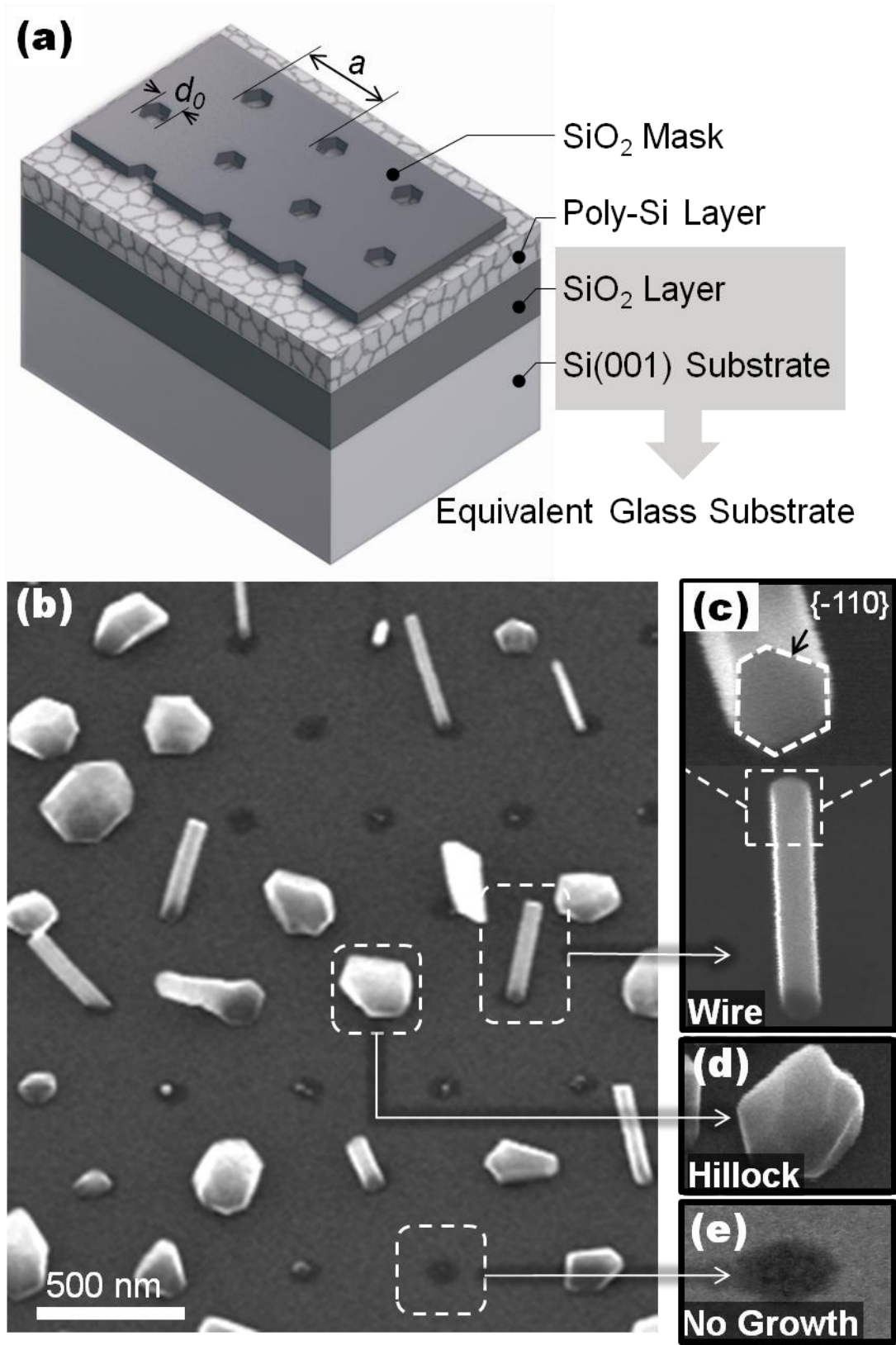
(b)

500 nm

(c) {-110}

Wire

(d) Hillock
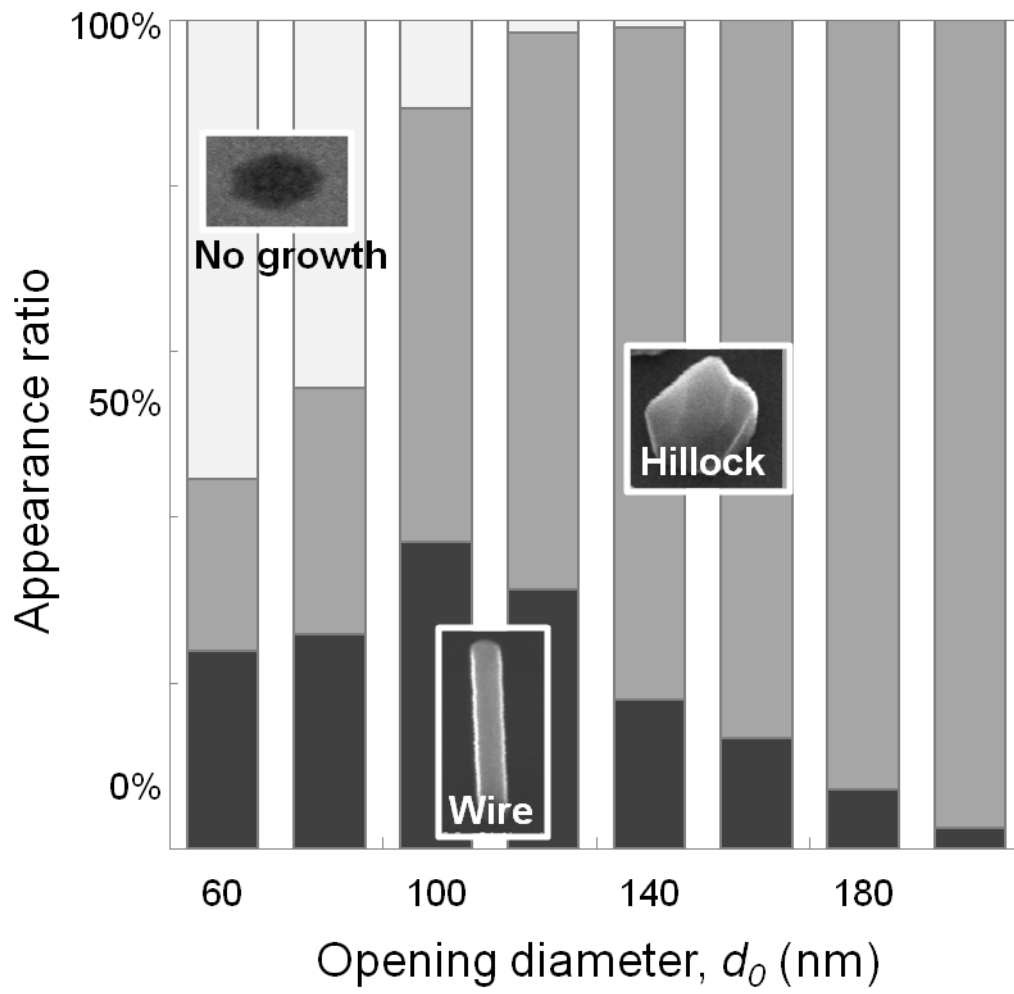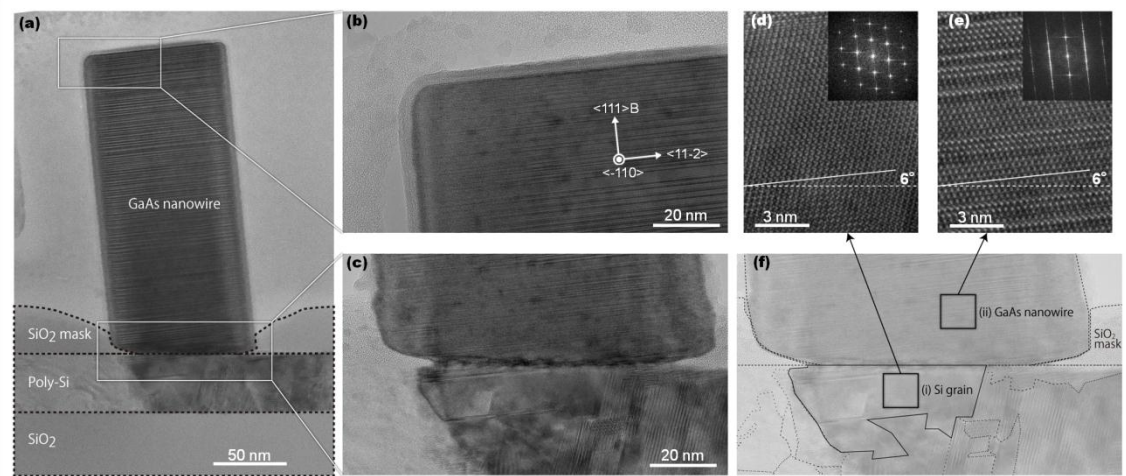
(e) No Growth

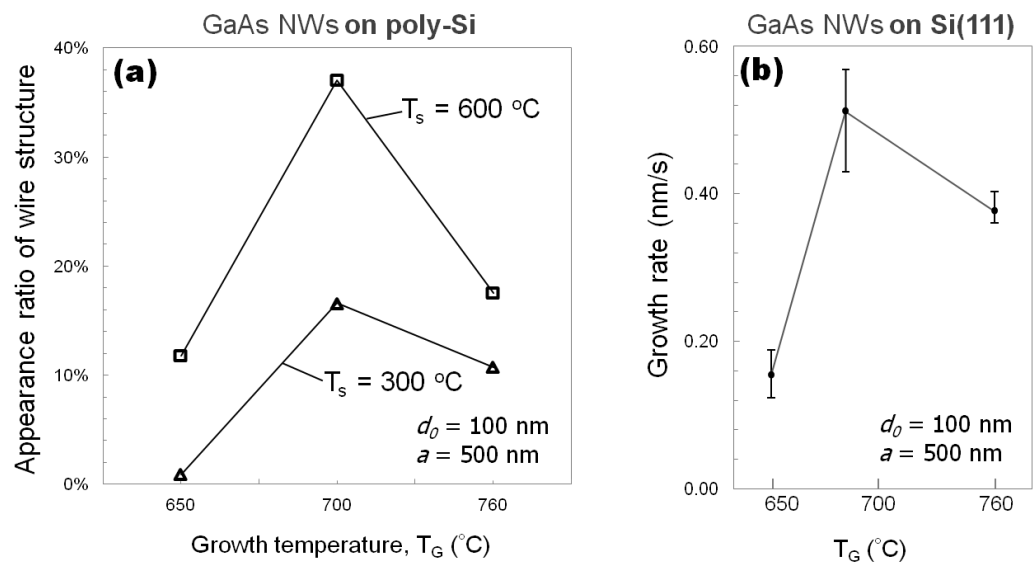Figure 2 (Fig2_rev.tif)

Figure 3 (Fig3_rev.tif)

Figure 4 (Fig4_rev.tif)

Figure 5 (Fig5_rev.tif)