LETTERS

GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies

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Compound semiconductors like gallium arsenide (GaAs) provide advantages over silicon for many applications, owing to their direct bandgaps and high electron mobilities. Examples range from efficient photovoltaic devices[1,2] to radio-frequency electronics[3,4] and most forms of optoelectronics[5,6]. However, growing large, high quality wafers of these materials, and intimately integrating them on silicon or amorphous substrates (such as glass or plastic) is expensive, which restricts their use. Here we describe materials and fabrication concepts that address many of these challenges, through the use of films of GaAs or AlGaAs grown in thick, multilayer epitaxial assemblies, then separated from each other and distributed on foreign substrates by printing. This method yields large quantities of high quality semiconductor material capable of device integration in large area formats, in a manner that also allows the wafer to be reused for additional growths. We demonstrate some capabilities of this approach with three different applications: GaAs-based metal semiconductor field effect transistors and logic gates on plates of glass, near-infrared imaging devices on wafers of silicon, and photovoltaic modules on sheets of plastic. These results illustrate the implementation of compound semiconductors such as GaAs in applications whose cost structures, formats, area coverages or modes of use are incompatible with conventional growth or integration strategies.

Some of the most daunting technical challenges associated with established methods for using GaAs occur in terrestrial photovoltaics, where the extremely high efficiencies of GaAs solar cells[7,8] might otherwise offer compelling opportunities. Here, the demands on cost and the necessity for integration over large areas on glass or other foreign substrates lead to requirements that lie well outside current capabilities. Previously known techniques, most notably epitaxial lift-off[9–12], separate GaAs solar cells from their growth substrates to reduce their cost or weight[10,11], but difficulties in handling the lifted materials[12] limit their use. Despite continuing progress[11,12], photovoltaic epitaxial lift-off has remained as a research topic for over 30 years, with no commercial implementation. More tractable, yet still difficult, problems appear in advanced electronics and optoelectronics where, as examples, device-level integration of compound semiconductors with silicon electronics can improve high speed operation in radio-frequency systems[13], add capabilities for light emission in devices for lightwave communications[14] or enable efficient photodetection for night-vision cameras[15]. Wafer bonding[16], heteroepitaxy[17], pick-and-place techniques[18] and chip-scale packaging methods[19] can meet certain requirements of these and other applications, but not without some combination of disadvantages that include restricted scales or modes for integration, limited substrate compatibility and poor cost effectiveness.

Alternative methods that avoid these drawbacks and, at the same time, provide realistic means of distributing large quantities of material over large areas on amorphous substrates could have significant practical value. Recent work by us and others demonstrates potential for compound semiconductor nanomaterials and unusual guided or deterministic assembly methods to address some of these challenges[20–22]. Limitations in the amounts and formats of these materials, difficulties in their scalable integration into devices and/or uncertain compositions and properties frustrate their use for many important applications. We present here concepts that overcome these issues by exploiting device-quality compound semiconductor films epitaxially grown in thick, multilayer formats specially designed for separation from one another, release from the wafer and subsequent integration in diverse layouts on various substrate types. This approach greatly reduces the need for wafer refinishing, compared to analogous single-layer lift-off approaches, and eliminates cycles of loading and unloading of wafers into the growth chamber. In favourable cases, the net effect can be an increase in throughput and a decrease in cost of more than an order of magnitude (Supplementary Information). The outcomes are applicable to every area of use for compound semiconductors, from electronics to optoelectronics and photovoltaics, as illustrated in the following.

The basic strategy appears in Fig. 1. Metal organic chemical vapour deposition (MOCVD) forms multiple layers of GaAs and/or AlGaAs or other related materials with compositions and layouts that match device requirements, with separating films of AlAs ($Al_{0.95}Ga_{0.05}As$). Figure 1a presents a simple case of 14 such layers, similar to designs used in the electronics examples described next. Figure 1b shows secondary ion mass spectrometry (SIMS) depth profiles of the composition of a structure with the layout of Fig. 1a, illustrating well defined layers with abrupt interfaces. Many more layers are possible, limited by layer morphologies, doping profiles and differential stresses and, ultimately for certain systems (for example, Fig. 1e), by practical constraints on growth times (Supplementary Information). Patterned vertical etching through the entire stack exposes the sidewalls of the layers and delineates the material into separated blocks with desired lateral dimensions. Immersion in hydrofluoric acid (HF) selectively eliminates the AlAs layers, thereby releasing large collections of pieces of GaAs (and/or multilayers with AlGaAs or other materials), with sizes that can range from micrometres to centimetres, and thicknesses from several nanometres to micrometres.

Figure 1c shows a cross-sectional scanning electron microscope (SEM) image of the system schematically illustrated in Fig. 1a after vertical etching and brief immersion in HF. The etching rate for $Al_xGa_{1-x}As$ over GaAs depends on the aluminium fraction[23].

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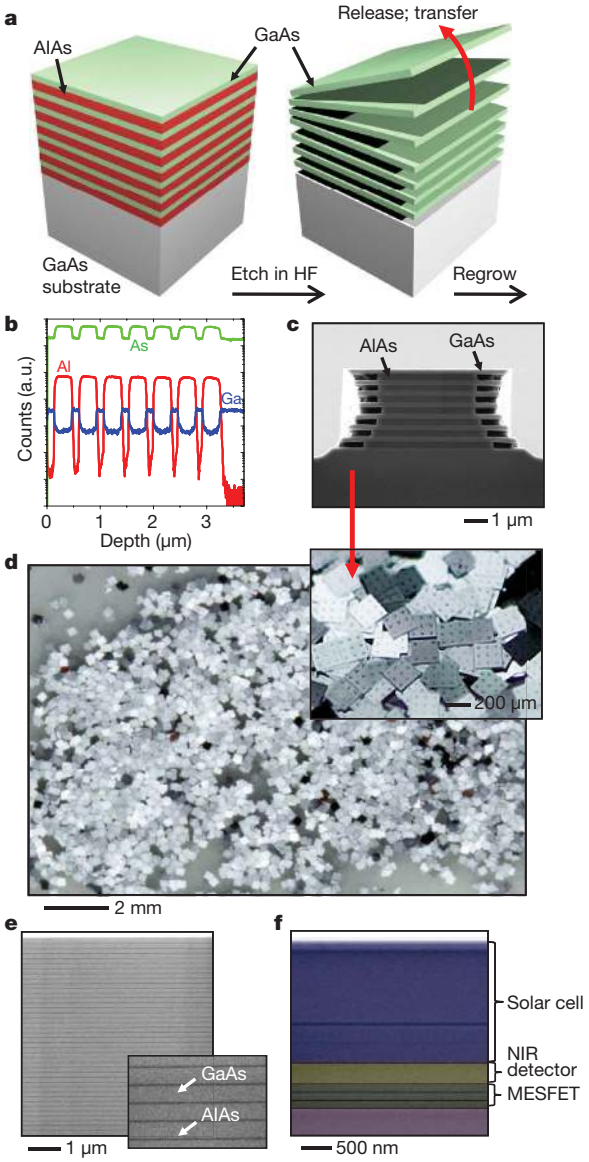

Figure 1 | Schematic illustration, optical and SEM images, and SIMS profile of GaAs/AlAs multilayers. a, Schematic illustration of a multilayer stack of GaAs/AlAs and schemes for release through selective etching of the layers of AlAs. **b**, Corresponding SIMS profile of this stack. **c**, Cross-sectional SEM image after partial etching of the AlAs layers. **d**, Optical image of a large collection of GaAs solar cells formed by release from a three-layer stack, and then solution casting onto another substrate. Inset, high magnification view. **e**, Cross-sectional SEM image of a 40 repeat multilayer stack of GaAs (200 nm)/AlAs with ultrathin (20 nm) AlAs sacrificial layers. Inset, high-magnification view. **f**, Cross-sectional SEM image (coloured) of a heterogeneous multilayer stack composed of three layers for MESFETs (green), one layer for an NIR detector (yellow) and one layer for a single junction solar cell (blue). The substrate is purple. Each of the device layers is separated by 20 nm AlAs (red). Details of stack design and corresponding SIMS profile are in Supplementary Information.

Increasing the fraction (for $x > 0.7$) results in highly enhanced rates of etching in HF. For example, etching of GaAs occurs at a rate 10^6 times lower than that of AlAs (ref. 24). The GaAs component can incorporate other layers of epitaxial materials, with the constraint that their etching rate is sufficiently low in HF and that thermally driven diffusion of any mobile species during growth does not lead to adverse effects. In the following, we exploit this flexibility to grow multilayer stacks for metal semiconductor field effect transistors (MESFETs), Schottky diodes, near-infrared (NIR) photodetectors and single-junction photovoltaic cells. Figure 1d shows a macroscopic pile of such cells (square platelets ~200 μm on a side, and ~4.5 μm thick), formed from an AlAs-separated three-layer assembly of GaAs stacks that each consist of six Zn and Si doped layers of GaAs and AlGaAs; details appear below. The collective assembly on the growth wafer incorporates 22 epitaxial layers, with a total thickness of ~17 μm. In this case, and others, the wafer surface can be refinished after complete lift-off to prepare it for additional growths. These concepts can be extended to extremely large multilayer stacks (for example, 40-layer repeats; Fig. 1e) and to heterogeneous collections of devices (for example, solar cells, transistors and photodetectors; Fig. 1f).

To demonstrate the simplest example first, we formed multilayers (seven repeats) of n-type GaAs (200 nm; Si-doped to 4×10^{17} cm^{-3}) and AlAs (300 nm) on a (100)GaAs substrate, for building MESFETs. Complete etching and release of GaAs active elements, followed by solution assembly on a target substrate, represents one conceivable route to device integration. Here we use extensions of deterministic assembly procedures described elsewhere[25,26], in which each of the individual GaAs layers in the stack is released and then transfer printed one at a time, in a step and repeat fashion, onto a glass substrate coated with a thin layer of polyimide. Printing tools, with yields >99.5%, submicrometre placement accuracy and throughputs corresponding to millions of dies per hour, are under commercial development. Details, including cost estimates, appear in Supplementary Information. Fabricating MESFETs from the printed GaAs membranes involves patterned etching to define the channel regions, followed by additional processing to create ohmic source and drain contacts (Pd/Ge/Au) and Schottky gates (Ti/Au). Figure 2a and b shows schematic illustrations and optical images, respectively. Figure 2c and d presents current/voltage (I/V) characteristics and transfer curves of representative devices (with channel widths of 130 μm, channel lengths of 25 μm and gate lengths of 3 μm) from each of the top five layers in the stack. In all cases the layer-to-layer variations in properties are random, with magnitudes comparable to device-to-device variations observed in any given single layer.

The electrode layouts enable probing of high frequency response with a vector network analyser. Representative results appear in Fig. 2e, which plots the current gain (H_{21}) and maximum available gain (MAG) as a function of frequency for the fourth layer device, indicating that the unity current gain frequency (f_T) and unity power gain frequency (f_{max}) are around ~2 and ~6 GHz, respectively, even for this relatively coarse channel dimension, as expected on the basis of the high electron mobility in GaAs (ref. 27). This response, as well as the maximum transconductances (~3.4 mS), on/off current ratios (~10^6), maximum current outputs per channel width (~1.1×10^{-5} A μm^{-1}) and other parameters inferred from electrical testing, is consistent with expectation based on devices with similar designs formed on a GaAs wafer. Integration of multiple MESFETs yields logic gates, as a step towards integrated circuits. Figure 2f shows optical images of NAND and NOR gates that each consist of three interconnected devices. The load and switching transistors have channel lengths of 55 and 25 μm, respectively, both with gate lengths of 3 μm and channel widths of 130 μm. Figure 2g and h presents output–input characteristics of NAND and NOR gates, respectively. In both cases, the logic '0' and '1' input signals correspond to −3 V and 1 V, respectively, for V_{dd} (the drain voltage of the load transistor) equal to 5 V. The logic '0' and '1' outputs of the NAND gate are 0.5–0.9 V and 5 V, respectively; the corresponding outputs of the NOR gate are 0.3–0.6 V and 5 V.

NIR imagers composed of interconnected arrays of GaAs photodiodes and blocking diodes provide a second, more advanced and different means of exploiting the multilayer concepts. Figure 3a provides a schematic illustration of the device layout in this case. The epitaxial stacks include bilayers of undoped GaAs (500 nm thick) and n-type GaAs (50 nm thick; Si-doped to 8×10^{16} cm^{-3}), in a four-layer assembly separated by AlAs (300 nm thick). To demonstrate a processing option different from that for the MESFETs, we built fully functional, interconnected systems using each active layer on the growth wafer, followed, in sequential fashion, by transfer to a target substrate. We chose silicon in this case owing to its established use for

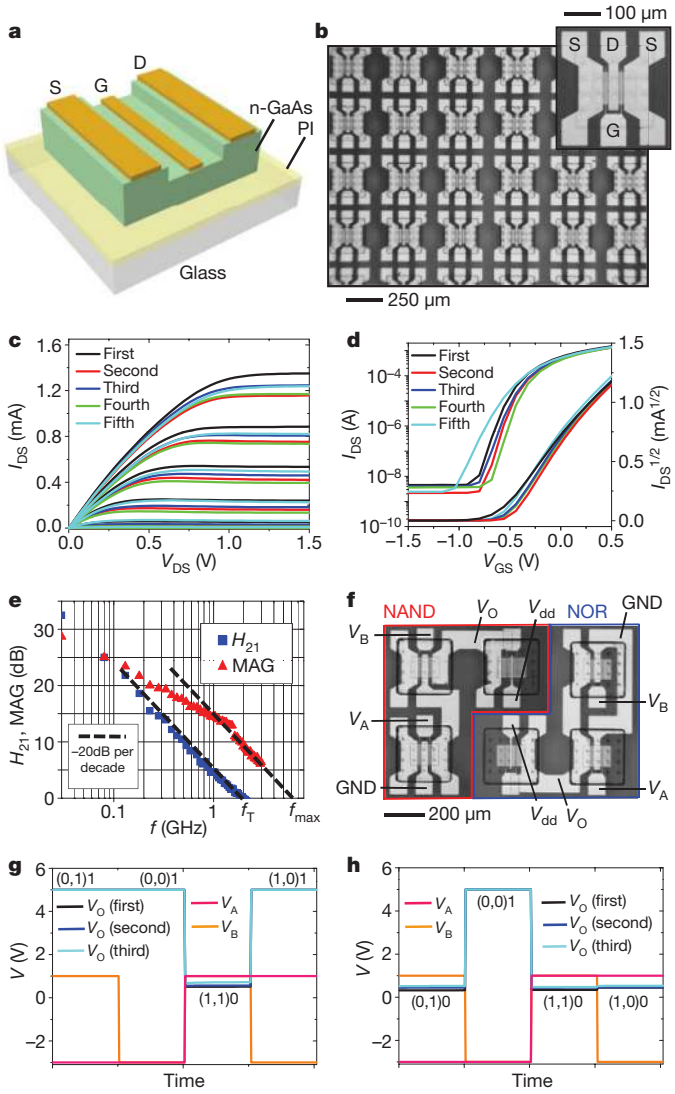

Figure 2 | Multilayer GaAs MESFETs and logic circuits. **a**, Schematic illustration of a GaAs MESFET on a polyimide (PI) coated glass substrate. **b**, Optical image of arrays of MESFETs on glass substrate. Inset, a single MESFET with source (S), drain (D) and gate (G) metal layers. **c**, V_{DS} (drain–source voltage) versus I_{DS} (drain–source current) curves of MESFETs fabricated from first, second, third, fourth and fifth layers at gate–source voltages (V_{GS}) of 0.4, 0.2, 0, −0.2, −0.4 and −0.6 V, from top to bottom. **d**, I_{DS} versus V_{GS} transfer curves of MESFETs fabricated from first, second, third, fourth and fifth layers, at V_{DS} = 1.5 V. **e**, Amplitude plots for current gain (H_{21}) and MAG measured from the fourth layer device. The unity current gain frequency (f_T) and unity power gain frequency (f_{max}) are ~2 and ~6 GHz, respectively. **f**, Optical image of NAND and NOR gates on polyimide (V_A, V_B, input voltages for switching transistors; V_{dd}, drain voltage for load transistor; V_O, output voltage). **g**, Output–input characteristics of NAND gates using devices from the first, second and third layers. **h**, As **g** but for NOR gates.

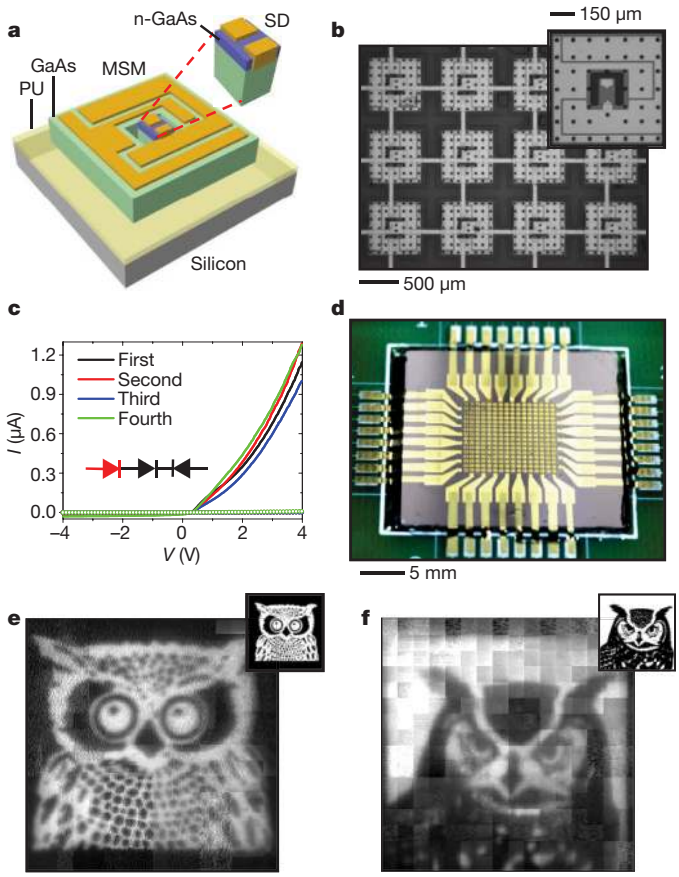

Figure 3 | Multilayer GaAs NIR imagers. **a**, Schematic illustration of a GaAs metal–semiconductor–metal (MSM) NIR detector on a Si wafer coated with a photocurable polyurethane (PU). Inset, Schottky blocking diode (SD). **b**, Optical image of a NIR imager consisting of a 16 × 16 array of detectors (12 pixels are shown). Inset, a unit cell before interconnect metallization. **c**, I/V characteristics of a cell formed with material from the first, second, third and fourth layers. Open circles and lines correspond to responses in the dark and under NIR illumination (wavelength 830 nm), respectively. **d**, Photograph of an NIR imager mounted on a printed circuit board. **e**, Image acquired with an NIR imager formed with material from the second layer. **f**, As **e** but using material from the fourth layer. Insets in **e** and **f** correspond to objects that were imaged.

image processing in conventional infrared cameras formed by solder bump bonding[28]. Forming Schottky contacts (Ti/Au) to the top, undoped GaAs layers yields metal–semiconductor–metal diodes. Such contacts combined with ohmic contacts (Pd/Ge/Au) to the Si-doped GaAs provide Schottky diodes. The metal–semiconductor–metal devices enable NIR detection, while the Schottky diodes block the reverse bias current to prevent crosstalk for passive matrix readout of the array.

Figure 3b shows an image of the layout of a photodiode/blocking diode pair, in the geometry used for the NIR imagers. Figure 3c presents representative I/V characteristics and photoresponse for typical devices formed using the first, second, third and fourth layers in the stack. The open circles and lines correspond to responses in the dark and under NIR illumination (830 nm), respectively. The data indicate comparable and reproducible behaviour for all layers. Ratios of currents in the on and off states are ~200, sufficient for passive matrix readout. A spin cast, photodefinable epoxy serves as a mechanical support and substrate for metal interconnection lines between 256 such devices, to yield independently addressable arrays (16 × 16 elements) for imaging. Transfer printing delivers the completed system to a silicon wafer that mounts on a printed circuit board interface to a computer for image acquisition (Fig. 3d). The yields of properly functioning pixels were better than ~96% in individual pixels and ~70% in interconnected arrays, limited mainly by breaks in interconnection metals. Figure 3e and f shows images of pictures of owls collected with NIR illumination and two separate cameras formed with the second and fourth layers, respectively. Image collection involved a scanning mode[29], to achieve an effective level of resolution much higher than that defined by the numbers of pixels and to provide oversampling for minimizing adverse effects of non-uniformities and malfunctioning pixels.

The third demonstration is in photovoltaics, where six-layer stacks of Zn and Si doped GaAs and AlGaAs form single-junction solar cells, epitaxially grown in trilayer assemblies separated by layers of AlAs (1 μm thick). Figure 4a illustrates the layout of the materials and the

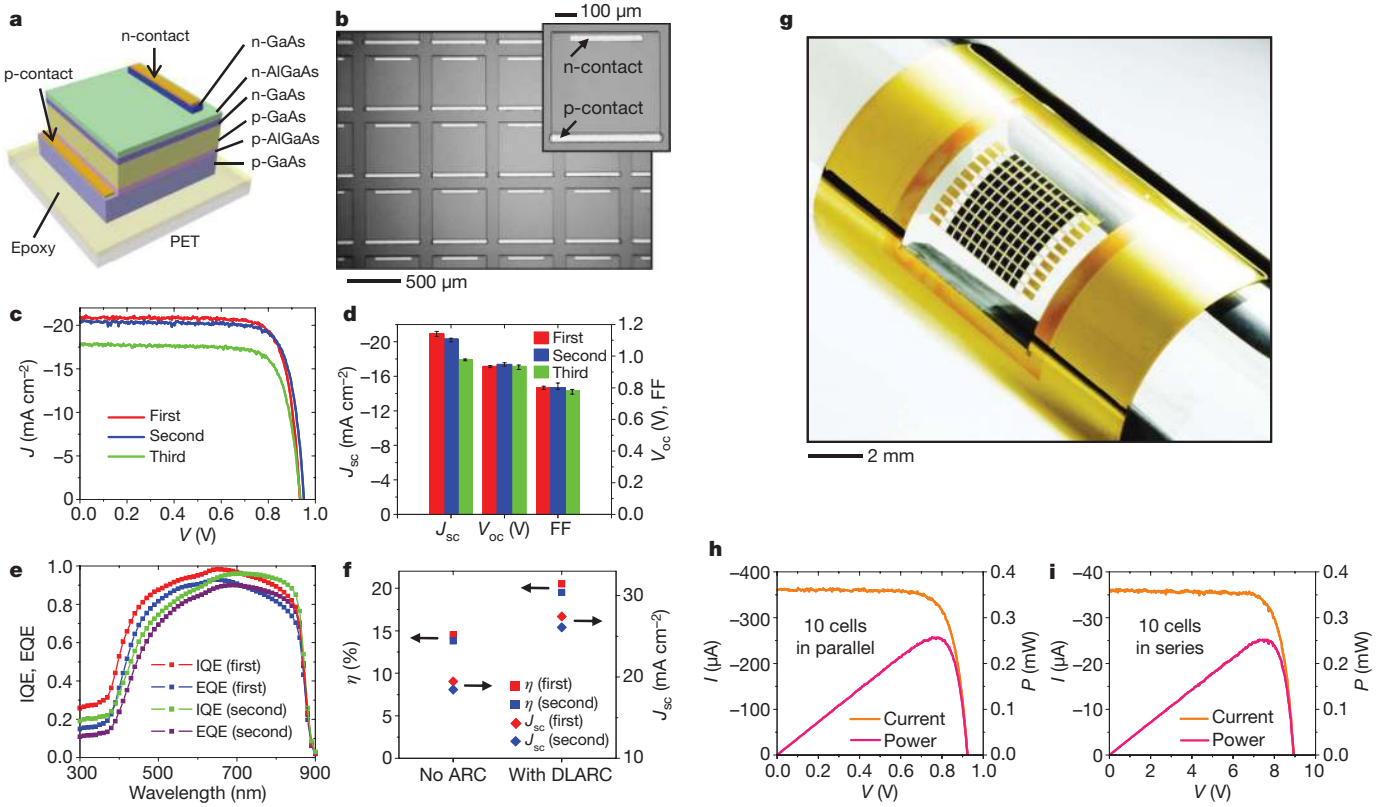

Figure 4 | Multilayer GaAs single-junction solar cells. a, Schematic illustration of GaAs single-junction solar cell on a PET substrate coated with a photodefinable epoxy. **b**, Optical image of arrays of such devices formed on the source wafer. Inset, magnified view of top (n-type) and bottom (p-type) contacts. **c**, Representative light current density (J)-voltage (V) curves for Zn-doped solar cells formed from the first (top), second (middle) and third (bottom) layers, under AM1.5D illumination measured on the source wafer with a single-layer ARC of Si_3N_4. **d**, Short-circuit current density (J_{sc}), fill factor (FF) and open circuit voltage (V_{oc}) of first, second and third layer devices. Error bars, max./min. **e**, IQE and EQE of first and second layer devices. **f**, Projected efficiencies (η) and J_{sc} values without ARC and with double-layer ARCs (DLARC; MgF_2/ZnS) for devices formed using material from the first and second layers. **g**, Photograph of a solar module consisting of a 10 × 10 array of GaAs solar cells (each ~500 μm × 500 μm) on a PET substrate. **h**, Light current–voltage (I/V) and power–voltage (P/V) curves for such a module with parallel interconnection of 10 cells. **i**, As **h** but with series interconnection. Both measurements were made in a flat configuration.

geometry of the contacts. Each GaAs and AlGaAs epitaxial construct consists of an n-type top contact layer (0.2 μm thick GaAs; Si-doped), an n-type window layer (40 nm thick $Al_{0.4}Ga_{0.6}As$; Si-doped), an n-type emitter (0.1 μm thick GaAs; Si-doped), a p-type base (2 μm thick GaAs; Zn-doped), a p-type back surface field layer (0.1 μm thick $Al_{0.3}Ga_{0.7}As$; Zn-doped) and a p-type bottom contact layer (2 μm thick GaAs; Zn-doped). Vertical etching delineates arrays of cells with lateral dimensions of ~500 × 500 μm on the source wafer. Controlled etching of selected regions (35 × 500 μm) near the edges of these cells exposes the bottom p-contact layer. This process, followed by removal of all but a small part of the top n-contact layer (30 × 330 μm) prepares the wafer for deposition and patterning of contact metals. The n and p contacts consist of Pd/Ge/Au and Pt/Ti/Pt/Au, respectively (Fig. 4b). Current density/voltage (J/V) curves and extracted characteristics of individual cells from each layer measured under simulated AM1.5D (air mass 1.5 direct) illumination (1,000 W m^{-2}) at room temperature with a single-layer antireflection coating (ARC; Si_3N_4) appear in Fig. 4c and d, respectively, where the current densities correspond to the active areas of the cells. AM1.5D illumination provides measurements that are relevant to terrestrial concentrator photovoltaics.

Moderate decreases in J from the top to the bottom layer are systematic, and can be attributed to the diffusion of Zn in the p-type GaAs layers, as revealed by SIMS analysis (Supplementary Information). This behaviour might be eliminated by the use of alternative dopants, such as carbon, that have negligible diffusion coefficients. Figure 4e shows external and internal quantum efficiencies (EQE and IQE, respectively) with an ARC for top and middle layer devices. The calculated efficiencies based on these measurements and AM1.5D reference spectrum without an ARC are ~14.5% and ~13.5% for top and middle layer devices, respectively (Fig. 4f). A double-layer ARC (such as MgF_2/ZnS; Fig. 4f) can increase the efficiency to ~20.5% (~19.5% for the middle layer; see Supplementary Information), which approaches the performance of some of the best reported devices designed for ultrahigh concentration (~20.6%)[30]. The performance can be further improved by the use of optimized cell designs and ARCs. These ultrathin cells provide other interesting features, such as the ability to integrate onto thin (~50 μm) sheets of polyethylene terephthalate (PET) for mechanically flexible modules capable of bending to radii of curvature of <5 mm without degradation in performance. Figure 4g presents an image of such a device, consisting of 100 interconnected cells (10 × 10 array), wrapped onto a cylindrical support. The cells can be combined in series and/or parallel configurations to yield output power at high or low voltages (or anything in between), thereby highlighting an important advantage of the use of large collections of small cells. Figure 4h and i presents output characteristics of devices that use parallel and series interconnects for output voltages of 0.93 V and 8.9 V, respectively, with similar total maximum output power (0.23 mW and 0.25 mW, respectively). Similar processing steps can be used with large (>1 cm) devices, as described in the Supplementary Information. Edge recombination, even at 100 μm cell sizes, reduces the efficiency by less than 1% (Supplementary Information).

In conclusion, approaches reported here provide advantages in integration possibilities, designs and cost, to create opportunities that are inaccessible to established technologies. The remaining technical barriers to commercialization are specific to the application. For example, solar cells that incorporate tunnel junctions may

require special growth strategies for production in thick, multilayer configurations. Exploring other material systems, such as gallium nitride and indium phosphide, and other devices, such as light emitting diodes, lasers and sensors, represent additional promising directions for future work.

METHODS SUMMARY

Multilayer structures for MESFETs, NIR imagers and single-junction solar cells were grown on (100)GaAs substrates by MOCVD. Etching through the top GaAs layer (or GaAs/AlGaAs stack) with a mixture of citric acid and hydrogen peroxide created vertical trenches. Partially etching into the underlying, exposed AlAs layer with HF created a slight undercut around the periphery of the trenches. Spin coating a layer of photoresist and patterning it by photolithography formed structures that, after complete etching of the AlAs, tethered fully released GaAs membranes to the underlying wafer. Techniques of transfer printing were used to integrate the released GaAs/AlGaAs structures onto substrates of interest. Repetitive application of this sequence of steps separated each of the layers in the original stack, and integrated them onto target substrates. For MESFETs and logic gates, n-type GaAs membranes were transfer printed to a glass substrate coated with a partially cured polyimide. A sequence of photolithography, electron beam evaporation and annealing steps yielded ohmic source and drain electrodes and Schottky gate electrodes to form the MESFETs and logic gates. For NIR imagers, fully interconnected device arrays were formed on the source wafer. After undercut etching, the arrays were transfer printed to a Si wafer coated with a photocurable polyurethane, and connected to a computer for image acquisition. For single-junction solar cells, individual cells were formed through bottom contact exposure, top contact etch, isolation and ohmic contact formation. Si_3N_4 served as an ARC. Arrays of the resulting cells were released by undercut-etching and then were transfer printed to a PET substrate coated with a photodefinable epoxy, followed by fabrication of metal interconnects and encapsulation layers. Current–voltage measurements were conducted using a direct-current (d.c.) source meter and a full-spectrum solar simulator. External and internal quantum efficiencies were measured using a spectroradiometer system.

Full Methods and any associated references are available in the online version of the paper at www.nature.com/nature.

Received 9 December 2009; accepted 25 March 2010.

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Supplementary Information is linked to the online version of the paper at www.nature.com/nature.

Acknowledgements We thank T. Banks, J. Soares and T. Spila for help using facilities at the Frederick Seitz MRL; D. Stevenson, S. Robinson and D. Sievers for help with photography, SEM and four point probe measurements, respectively; and A. Gray for guidance in calculating the cell conversion efficiency and the calibration of the solar simulator. J.Y. thanks D. Shir for help with optics simulation. This paper is based partly on work supported by a National Security Science and Engineering Faculty Fellowship (NIR cameras and MESFETs) and by the US Department of Energy, Division of Materials Sciences (DEFG02-91ER45439), through the Frederick Seitz MRL and Center for Microanalysis of Materials at the University of Illinois at Urbana-Champaign (materials, growth aspects) and the Division of Energy Efficiency and Renewable Energy (DE-FG36-08GO18021) (solar cells). We also acknowledge the Center for Nanoscale Chemical Electrical Mechanical Manufacturing Systems in the University of Illinois, which is funded by the National Science Foundation (DMI-0328162) (printing-based manufacturing) and separate funding from the National Research Foundation of Korea through a grant (K2070400000307A050000310, Global Research Laboratory Program) provided by the Korean Ministry of Education, Science and Technology. J.J.C. acknowledges support by the Center for Energy Nanoscience, an Energy Frontier Research Center funded by the US Department of Energy, Office of Science, Office of Basic Energy Sciences (DE-SC0001013). J.Y. acknowledges support from a Beckman Institute postdoctoral fellowship. S.J. thanks the Korea Research Foundation for a postdoctoral fellowship (KRF-2008-357-D00134).

Author Contributions J.Y., S.J., I.S.C., I.J., H.-S.K., M.M., E.M., X.L., J.J.C., U.P. and J.A.R. designed the experiments; J.Y., S.J., I.S.C., I.J., H.-S.K., M.M., E.M., X.L., J.J.C., U.P. and J.A.R. performed experiments and analyses; and J.Y., S.J., I.J. and J.A.R. wrote the paper.

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METHODS

Epitaxial multilayer growth. Multilayer structures for MESFETs, NIR imagers and heterogeneous devices (MESFETs, NIR photodetectors and solar cells) were grown on an n-type Si-doped GaAs(100) substrate using a Thomas Swan atmospheric pressure MOCVD reactor. In all cases, a GaAs buffer layer with thickness of 200 nm was formed first, at 800 °C. Trimethyl gallium, trimethyl aluminium and arsine (AsH_3) served as precursors for Ga, Al and As, respectively. Disilane (Si_2H_6) and dimethylzinc were used for Si (n-type) and Zn (p-type) doping, respectively. Purified hydrogen served as the carrier gas. The growth temperature in all cases was 800 °C. Epitaxial multilayer structures for the MESFETs consisted of either seven or forty bilayers of n-type GaAs (200 nm, 4×10^{17} cm^{-3}, Si-doped) and $Al_{0.95}Ga_{0.05}As$ (300 nm for 7 bilayers, 20 nm for 40 bilayers). For the NIR imagers, the structure included four repeats of n-type GaAs (50 nm, 8×10^{16} cm^{-3}, Si-doped), undoped GaAs (500 nm) and $Al_{0.95}Ga_{0.05}As$ (300 nm). Details on heterogeneous stacks appear in the Supplementary Information. Multilayer structures for n-on-p type single-junction solar cells were grown by Epiworks Inc. with its commercial EpiSure solar cell growth processes in a low-pressure MOCVD production system (modified Aixtron 2600G3). The materials were deposited on (100)GaAs substrates (2° off towards the nearest [111] plane) using standard precursors including trimethyl gallium, AsH_3, trimethyl aluminium, dimethylzinc and Si_2H_6. The multilayer structures for single-junction solar cells were composed of three repeats of n-type GaAs (200 nm, (4–5) $\times 10^{18}$ cm^{-3}, Si-doped), n-type $Al_{0.4}Ga_{0.6}As$ (40 nm, 2×10^{18} cm^{-3}, Si-doped), n-type GaAs (100 nm, 2×10^{18} cm^{-3}, Si-doped), p-type GaAs (2 μm, 3×10^{17} cm^{-3}, Zn-doped), p-type $Al_{0.3}Ga_{0.7}As$ (100 nm, 1×10^{19} cm^{-3}, Zn-doped), p-type GaAs (2 μm, 4×10^{19} cm^{-3}, Zn-doped) and $Al_{0.95}Ga_{0.05}As$ (1.0 μm).

Multilayer release and assembly. Vertical etching through the entire thickness of a multilayer stack in a mixture of citric acid (100 g of citric acid monohydrate (Sigma-Aldrich); 83 ml of deionized water) and hydrogen peroxide (H_2O_2, 30%, Fisher Scientific) at a 10:1 volume ratio, followed by removal of the AlAs in HF, yielded solution suspensions of released GaAs structures. Subsequent assembly onto a target substrate provided one route to devices. For work reported here, vertical etching of trenches through the top GaAs layer (or GaAs, AlGaAs stack) and partially into the underlying AlAs layer by brief immersion in HF created a slight undercut around the periphery of the trenches. A layer of photoresist formed structures that tethered fully released pieces of GaAs to the underlying wafer after complete etching of the AlAs. Techniques of transfer printing were used to integrate the released GaAs structures onto substrates of interest. Repetitive application of this sequence of steps completed the process. The Supplementary Information provides additional details.

MESFETs and logic circuits. Etching according to procedures described above prepared the GaAs source wafer (Fig. 1a) for delivery of organized collections of GaAs membranes to a glass substrate coated with a partially cured layer of polyimide. Removing residual photoresist with acetone, and fully curing the polyimide by baking at 250 °C for 2 h completed the process. A sequence of photolithography, electron beam evaporation and annealing steps yielded ohmic source and drain electrodes (Pd/Ge/Au (5/35/80 nm); 175 °C for 60 min) and Schottky gate electrodes (Ti/Au (10/100 nm)) to form the MESFETs. Similar procedures formed interconnects for the logic gates. d.c. measurements of MESFETs were carried out using a semiconductor parameter analyser (Agilent, 4155C). High frequency measurement used a network analyser (Agilent, 8720) calibrated with a standard-open-load-through technique. The Supplementary Information provides additional details.

NIR imagers. Ohmic and Schottky contacts used Pd/Ge/Au (5/35/80 nm, annealed at 175 °C for 60 min) and Ti/Au (30/100 nm), respectively. Wet etching with a mixture of citric acid and hydrogen peroxide at a 10:1 volume ratio removed the n-type GaAs layer. A photodefinable epoxy (SU8, Microchem) served as a support structure for interconnecting metal lines and as an encapsulation layer. After etching the AlAs in concentrated HF, the entire NIR imager array was transferred to a silicon wafer coated with a photocurable polyurethane as an adhesive (NOA 61, Norland Products). Electrical measurements of individual pixels were conducted using a semiconductor parameter analyser (Agilent, 4155C). The detector was mounted in a printed circuit board and connected to a computer for image acquisition. The Supplementary Information provides additional details.

Solar cells and flexible modules. The p-type bottom contact layer was exposed by etching with mixtures of citric acid and hydrogen peroxide at different volume ratios (citric acid:H_2O_2 = 10:1 and 4:1) in a sequential manner. Next, most of the top contact layer except the area for the ohmic contact was selectively etched away with a 4:1 mixture of citric acid and hydrogen peroxide. Etching with a 10:1 mixture of citric acid and hydrogen peroxide provided isolation of individual cells. Ohmic contacts for both top and bottom contact layers were then formed by electron beam evaporation of Pd/Ge/Au (5/35/80 nm) and Pt/Ti/Pt/Au (10/40/10/80 nm) for n-type and p-type contacts, respectively. Annealing at 175 °C under N_2 atmosphere was used for the n-type ohmic contact. Before the *I*/*V* measurements on the source wafer, Si_3N_4 (thickness: ~80 nm, $n \approx 1.76$) was deposited by plasma enhanced chemical vapour deposition (PlasmaTherm SLR) as a single-layer ARC. Arrays of the resulting cells were undercut-etched in HF and transfer printed to PET substrates using a photodefinable epoxy (SU8, Microchem) as an adhesive. Patterning holes through the SU8 followed by lift-off of metals (Cr/Au: 10/300 nm) deposited by sputtering formed interconnects. Encapsulating with SU8 completed the entire process. *I*/*V* measurements were carried out using a d.c. source meter (Keithley, 2400) and a 1,000 W full-spectrum solar simulator (Oriel, 91192). External and internal quantum efficiencies of GaAs solar cells on the source wafer were measured using an automated spectroradiometer system (Optronic Lab., OL-750) in the wavelength range of 280–1,100 nm with 10 nm resolution. The Supplementary Information provides additional details.