GaAs pillar array-based light emitting diodes fabricated by metal-assisted chemical etching

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We demonstrate GaAs pillar array-based light emitting diodes (LEDs) with axial p-i-n junctions fabricated using a room-temperature metal-assisted chemical etching (MacEtch) method. Variations in vertical etch rates for all three doping types of GaAs are investigated as a function of etching temperature, oxidant/acid concentration ratio, and dilution of the etching solution. Control over nanopillar morphologies is demonstrated, simply through modification of the etching conditions. Optical emission enhancement from the MacEtched p-i-n GaAs nanopillar LED is observed, relative to the non-etched planar counterpart, through room-temperature photoluminescence and electroluminescence characterization. © *2013 AIP Publishing LLC*.
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I. INTRODUCTION

The metal-assisted chemical etching (MacEtch) method for localized material removal from semiconductor surfaces, as first established in the year 2000,[1] allows for the formation of high aspect-ratio nanostructures,[2–4] deep vertical pits,[5,6] and porous nano-membranes.[7,8] Potential device applications in photonics,[9,10] optoelectronics,[11] bio-sensing,[12,13] energy conversion,[14–16] and energy storage[17] have been envisioned. However, the current state of research in this field is such that focus is primarily placed upon the etching of Si,[18] Ge,[19] and semiconductor heterostructures composed thereof.[20,21] To date, only few studies have been published in which MacEtch of high aspect-ratio compound III–V semiconductors has been explored.[22] Furthermore, systematic investigations regarding neither the role of dopant impurities nor the influence of low- to room-temperature MacEtch of high aspect-ratio GaAs structures have yet been established for fabricating device structures.

The MacEtch mechanism relies, principally, on the satisfaction of two conditions: (1) partial coverage of a semiconductor material by a layer composed of a noble metal (typically, Au, Ag, or Pt), which acts as a catalyst for the injection of holes (h^+) and, thereby, oxidation of the semiconductor directly below the interface and (2) submerging of the metal-coated semiconductor into an etching solution containing an oxidant, which may accommodate h^+-injection through the metal/semiconductor interface by way of a reduction reaction, and an acid, capable of dissolving the oxidized semiconductor where it is interfaced with the metallic catalyst layer.[18,23] The continual repetition of such an oxidation and material dissolving cycle allows for anisotropic etching of the semiconductor material, forcing the metal layer to sink into the semiconductor.[18,23]

In comparison to other means of semiconductor nanopillar array fabrication, MacEtch offers several key advantages. The need for hazardous gases, a high thermal budget, and high vacuum conditions are avoided with MacEtch, while otherwise required not only in conventional top-down approaches such as reactive ion etching (RIE), deep-RIE (Bosch process), and inductively couple plasma (ICP)-RIE,[23] but also in the case of bottom-up crystal growth methods such as selective-area epitaxy (SAE)[24,25] or metal-seeded, vapor-liquid-solid (VLS) epitaxy of nanowire (NW) arrays.[26,27] Furthermore, MacEtch relieves the potential for ion-beam-induced damage or plasma-induced charging damage that may result from RIE processes,[28,29] and eliminates the likelihood of forming non-uniform sidewall features (scalloping) that may result from iterative Bosch etching.[30] Contrary to conventional masked RIE methods, achievable etch depths are not limited by the lateral extent of the masked features in the MacEtch approach, thereby allowing for the formation of high aspect-ratio features.[23]

The aforementioned RIE-based techniques are routinely employed in surface-texturing of III-V's for the enhancement of light output efficiency of light emitting diodes (LEDs).[31] Although LEDs may be engineered with internal quantum yields approaching unity,[32] the emission of light from a planar and high refractive index active region into free space is limited by a narrow escape cone and, therefore, prone to internal reflection and re-absorption.[32,33] As such, exterior designs such as truncated inverted pyramid geometries[34,35] are widely used for minimizing internal reflection in commercial LEDs. In addition, surface texturing may be introduced, by way of "natural lithography" (combination of nano-sphere lithography and RIE)[36,37] or through the use of colloidal microlenses[38] as a highly effective route toward angular randomization of photon scattering, accommodating a dramatic enhancement of light extraction beyond the critical angle.[32,33,36–38]

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MacEtch of III–V compound semiconductors may be introduced as a simpler alternative to the RIE process for similar applications where surface topography management is desired. Here, we present a simplified, room-temperature, and top-down process for the fabrication of highly ordered and large-area GaAs nanopillar arrays by way of MacEtch. Vertical etch rates of p-type, n-type, and intrinsic GaAs are studied as a function of the etching solution parameters, including temperature, oxidant concentration, and dilution. Etching of all three doping types are achieved in a single etching step, allowing for the formation of GaAs nanopillar arrays containing a vertical, epitaxially stacked p-i-n junction. Furthermore, we demonstrate the capability to control nanopillar morphologies through modulation of the competing lateral etch rate. Finally, an enhancement of optical emission is presented as a function of nanopillar morphology through room-temperature photoluminescence (PL) studies, and the emission spectra of planar and MacEtched nanopillar array p-i-n GaAs LEDs are compared via electroluminescence (EL) characterization.

II. EXPERIMENTAL DETAILS

In the current study, GaAs (100) substrates of various doping types and concentrations were used. Semi-insulating (SI) and n-type ($n = 1 \times 10^{18} cm^{-3}$) epi-ready substrates were used as purchased (AXT, Inc.), while p-type GaAs and p-i-n GaAs samples were epitaxially grown using an atmospheric pressure Thomas Swan metalorganic chemical vapor deposition (MOCVD) reactor. For p-i-n stacked samples, a 300 nm thick un-intentionally doped GaAs layer was grown at 720 °C on epi-ready n-type substrates, followed by the growth of a 300 nm thick, heavily Zn-doped GaAs layer grown at 600 °C. The dopant concentration of the p-type samples was determined to be $1 \times 10^{19} cm^{-3}$, based on Hall measurements. Prior to surface patterning, all GaAs wafers were subjected to native oxide removal in dilute HCl and surface degreasing with standard solvents, followed by electron-beam evaporation of a 35 nm thick Au film. Soft-lithography (SL) patterning was carried out by first spin-coating GaAs wafers with a thin layer of a photo-curable epoxy (8% SU-8). A polydimethylsiloxane (PDMS) stamp was then pressed against the SU-8 coated substrate, followed by curing performed at 95 °C. After SL stamping, the Au-coated regions exposed through the SU-8 mask were etched using TFAC Au etchant (Transene Company, Inc.) and the overlaying SU-8 grid was dissolved in PG Remover (MicroChem Corp.). This resulted in a square-grid-patterned Au layer on the GaAs substrate, where the exposed GaAs windows are $\sim 1 \times 1 \mu m^2$ separated by a spacing of ~ 550 nm. The current approach improves upon our previously reported SL patterning method for GaAs[22] by ensuring a pristine Au/GaAs interface, thereby guaranteeing uniform MacEtch over the entire patterned areas. MacEtch was performed in a solution containing potassium permanganate ($KMnO_4$) as the oxidant, and hydrofluoric acid (HF) as the source for removal of the oxidized material, and de-ionized water (DI). Oxidant concentrations were varied such that the mass of $KMnO_4$ in the etching solutions were tuned within

the range of 0.025–0.20 g. Acid dilution levels were modified within an HF:DI volumetric ratio range of 5:1 to 1:5 at a constant total volume of 30 ml in all etch tests. This corresponds to a $HF:KMnO_4$ molar ratio of 0.14 M:7.9 μM to 0.70 M:1.6 μM. All etch durations were fixed at 10 min., unless otherwise stated. LED fabrication was carried out by first selectively etching the Au layer from the as-etched p-i-n GaAs samples, followed by spin-coating of an SU-8-2 resist layer. A 150 s oxygen-plasma RIE procedure allowed for the planarization of the SU-8-2 layer and the exposure of the MacEtched nanopillar tips. Next, a 250 nm thick indium-tin-oxide (ITO) layer was sputtered on the exposed nanopillar tips as a transparent and conductive contact layer, followed by partial coverage with an electron-beam evaporated Au top contact of 500 nm thickness, situated around the active pillar array. The backside of the n-type GaAs substrate was contacted by a Ni/Au (5 nm/500 nm) stack. Finally, the fabricated devices were subjected a 30 s rapid thermal annealing (RTA) procedure for the formation of Ohmic contacts.

Inspection of the MacEtched nanopillars and general imaging were carried out using a Hitachi S-4800 scanning electron microscope (SEM). All PL and EL experiments were performed at room-temperature using a Renishaw inVia micro-PL system, equipped with a CCD camera. For PL experiments, excitation was provided by a 633 nm HeNe pump laser source. In EL experiments, the laser source was shuttered and the devices were operated in continuous mode as power was supplied by an Agilent E3649A DC source in a two-point probe configuration.

III. RESULTS AND DISCUSSION

A tilted-view SEM image obtained from a p-GaAs sample subjected to MacEtch in a solution of 15 ml HF, 15 ml DI, and 0.025 g $KMnO_4$ is shown in Figure 1, with the inset showing a high-magnification view of the same sample. The square-shaped pillars are 1.8 μm tall and roughly 1 μm wide laterally (aspect ratio of 1.8), as predefined by the SL mask employed. The continuous Au catalyst layer can be
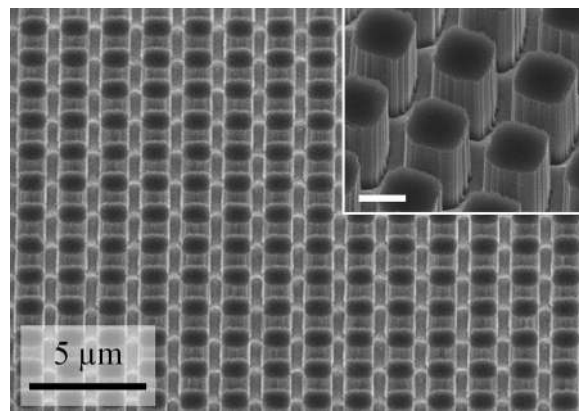

FIG. 1. Tilted view SEM image of a p-GaAs sample after MacEtch in a solution of 15 ml HF, 15 ml DI, and 0.025 g $KMnO_4$. The inset shows a higher magnification view of the same sample (scale bar represents a 1 μm length). The sidewall roughness exhibited in the inset results from the direct projection of the Au layer edge roughness.

observed at the base of the pillars, characteristic of the MacEtch mechanism, as previously described. Note that the vertical grooves on the sidewalls of the pillars are a direct consequence of the edge roughness of the Au pattern, which is faithfully engraved onto the sidewalls of the GaAs pillars. We believe the metal edge roughness originates from the Au liftoff step during SL patterning, where wet etching of the polycrystalline Au film likely attacks the grain boundaries preferentially, leaving a saw-tooth edge pattern. In contrast, much smoother sidewalls were produced by MacEtch using evaporated Au patterns,[22] although the drawback of that patterning method is the risk of leaving organic resist residues between Au and the GaAs surface. In the current approach, direct patterning of the Au layer allows for more reproducible and uniform MacEtch over large (wafer-scale) areas.

First, the dependence of vertical etch rate (VER) is studied as a function of etching temperature. Figure 2(a) quantifies this trend, based on p-, i-, and n-type GaAs samples MacEtched in a common solution consisting of 15 ml HF, 15 ml DI, and 0.05 g $KMnO_4$. All data points represent measurements obtained from sample populations consisting of 25 pillars, while the error bars represent one standard deviation (some error bars may not be distinguished, as they represent values smaller than the extent of the data points). A near linear progression in vertical MacEtch rate is noted with increasing temperature, from 0 to 40 °C, beyond which the VER saturates. This trend, as previously observed in the case of Si MacEtch,[39] is attributed to increased thermal promotion of h^+ diffusion through the catalyst layer and enhanced mass transport of dissociated ions. Importantly, this demonstrates for the first time that room-temperature MacEtch of high-aspect ratio nanopillars can be achieved for all doping types of GaAs. While the etch rates of n- and i-type GaAs remain comparable, p-type samples etched under identical conditions exhibit a higher VER by a factor of roughly 2.3 at room temperature. The fact that doping type changes the etch rate with identical Au pattern feature sizes indicates that charge transport, instead of mass transport, is the rate determining factor. It has been reported that the Schottky barrier height, which can be affected by the metal work function, thickness, and size, as well as the semiconductor doping type and level, can affect the etch rate, with faster etch rates for n-type GaN[40] and thicker Au for p-type Si.[41] The Schottky barrier height analysis used in the case of GaN[40] cannot explain the doping type dependence observed in the current study, possibly because the etching condition that is low in oxidant concentration makes the majority carrier transport in the semiconductor play a dominant role in determining the etch rate. Although the exact nature of this VER enhancement has not been explored in this study, we believe it is related to the inherent excess presence of holes in p-type samples and, therefore, improved oxidation rates. Under the conditions described above, room-temperature MacEtch proceeds with a VER of 318 ± 9 nm/min, 132 ± 6 nm/min, and 141 ± 8 nm/min for p-, i-, and n-type GaAs, respectively, with negligible lateral etching.

Next, the effect of acid dilution on VERs is considered. Figure 2(b) shows the VER as a function of HF:DI ratio, resulting from room-temperature etching at a constant
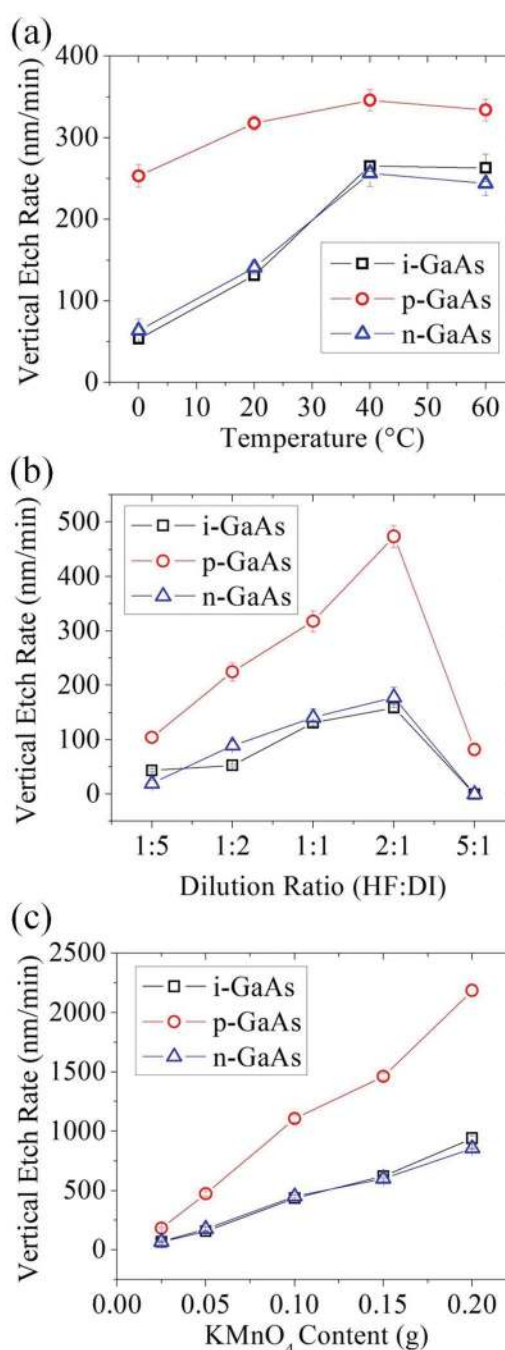

FIG. 2. Quantification of VER as a function of (a) solution temperature, (b) acid dilution ratio, and (c) oxidant concentration. Etch rates for p-, i-, and n-GaAs samples are represented by red circles, black squares, and blue triangles, respectively. Each data point represents mean VER values obtained from sample sets of 25 nanopillars (with vertical sidewall structures), while error bars represent ± one standard deviation from the mean.

oxidant concentration of 0.05 g. Figure 2(b) demonstrates that the optimal (highest) VER is realized for a volumetric acid dilution ratio of 2:1. For a fixed total solvent volume, increasing the acid content is associated with a higher rate of dissolution of oxidized material. However, below a critical dilution level (2:1 in the current case), the etch rate is dramatically reduced. This highlights the significance of the role of DI as a surfactant in III–V MacEtch. Thus, DI serves to reduce the surface tension between the acid and the semiconductor surface and allows for the acid to access

the oxidized material. Similar trends in VER with acid dilution were observed for all three GaAs doping types. Optimal VERs of 474 ± 16 nm/min, 159 ± 7 nm/min, and 177 ± 18 nm/min were measured for p-, i-, and n-type GaAs, respectively.

Lastly, the influence of oxidant concentration on VER is considered, as plotted in Figure 2(c). In this room-temperature MacEtch experiment, optimal HF and DI volumes of 20 ml and 10 ml, respectively, were employed, while $KMnO_4$ concentrations were varied from 0.025–0.20 g. As anticipated from previous GaAs MacEtch experiments,[22] VER increases monotonically with oxidant concentration. It should be noted that in the current study, the maximum $KMnO_4$ concentration employed is equal to the minimum level of what had previously been reported for GaAs MacEtch.[22] Reducing oxidant levels minimizes the risk of porosity in the nanopillar sidewalls.[2] The p-type samples again exhibit accelerated etch rates, by a factor of 2.6 ± 0.3, in comparison to n- and i-type samples for all oxidant concentrations.

The lateral etch rate (LER) of GaAs nanopillars may also be tuned as a function of the MacEtch solution, by decreasing acid content and increasing oxidant concentrations. Figure 3(a) shows an SEM image of a nanopillar array etched for 30 min. at room temperature in a solution consisting of 10 ml of HF, 20 ml of DI, and 0.1 g of $KMnO_4$. While the MacEtched nanopillars shown in Figure 1 adopted the exact dimensions (pillar widths of 1 μm) of the Au-catalyst mesh layer, those shown in Figure 3(a) clearly show a distinct lateral width reduction (aspect ratio of $\sim$7.3). In the latter case, the use of an etching solution consisting of higher oxidant and lower acid concentrations allows for enhanced h^+ generation and, when not consumed immediately, the h^+ diffuse, thereby promoting the oxidation of material further from the Au/GaAs interface. By successively reintroducing nanopillar samples to distinct MacEtch solutions, each tuned to specific VERs and LERs, nanopillar morphologies can be engineered. Figure 3(b) shows a sample that has been etched in two steps, first in the same high LER solution described above for a period of 10 min., followed by a 3.5 min. etch in a solution consisting of 20 ml of HF, 10 ml of DI, and 0.1 g of $KMnO_4$. In this case, GaAs pillars (aspect ratio of $\sim$2.5) are formed with tapered tips, consistent with an enhanced LER profile, and square base segments, consistent with a MacEtch scheme where lateral etching is effectively suppressed. This demonstrates a key advantage of the MacEtch process, as standard RIE methods do not allow for such morphological tuning and independent control of the lateral profile to generate three-dimensional hierarchical structures.

Shown in Figure 4 are room-temperature PL spectra acquired from 3 distinct p-i-n GaAs MacEtched samples compared with that obtained from the planar p-i-n GaAs counterpart. The red, blue, and green curves correspond to samples shown in Figures 1, 3(a) and 3(b), respectively, while the black curve corresponds to the planar control sample, which was not subjected to MacEtch. Whereas all spectra demonstrate a broad peak with center wavelength of 876 nm, associated with band-to-band radiative recombination in GaAs, the PL emission intensity is strongly correlated to nanopillar morphology. All MacEtched nanopillar
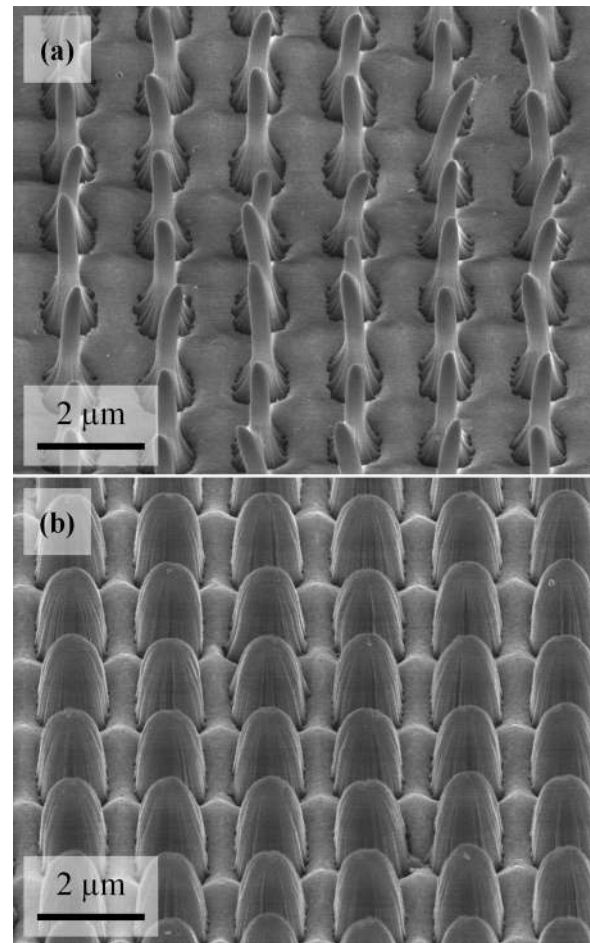

FIG. 3. Tilted view SEM images demonstrating nanopillar morphology control. (a) Sample etched in a solution of 10 ml of HF, 20 ml of DI, and 0.1 g of $KMnO_4$ for 30 min. (b) Sample etched in a two step process: first in the same solution as (a) for 10 min, followed by 3.5 min in a solution of 20 ml of HF, 10 ml of DI, and 0.1 g of $KMnO_4$ where lateral etching is quenched.

samples show stronger PL than the planar structure. For all of the pillar structures, the results indicate that increasing the volume of the exposed GaAs nanopillars enhances the photon escape probabilities and, thus, PL intensity. It should be
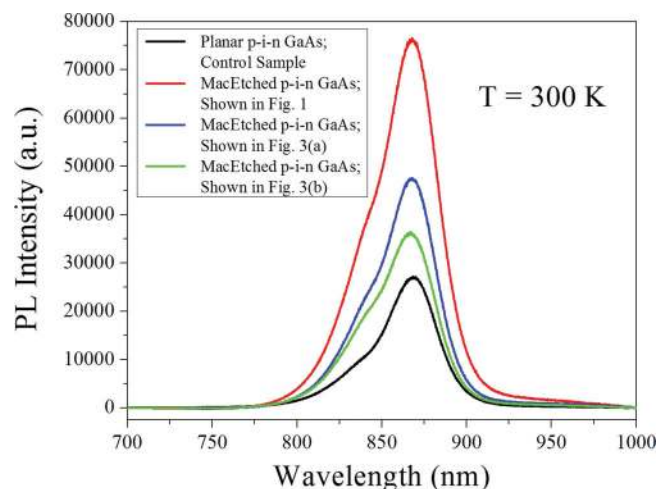

FIG. 4. Room-temperature PL spectra obtained from planar GaAs control sample (black curve) and MacEtched samples shown in Figure 1 (red curve), Figure 3(a) (blue curve), and Figure 3(b) (green curve).
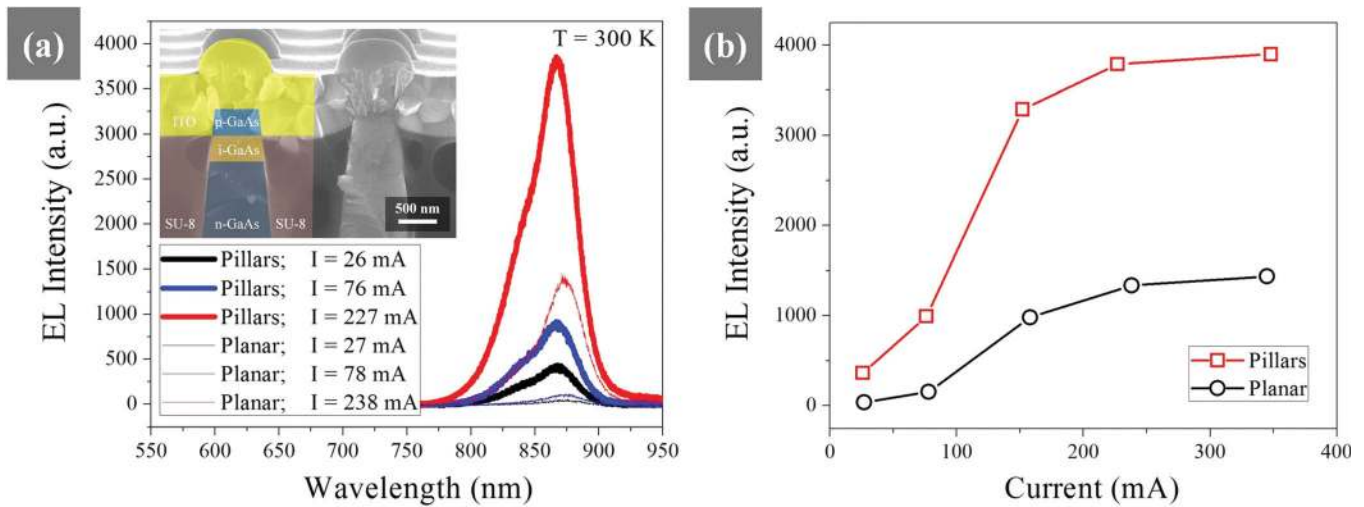
FIG. 5. (a) Room-temperature EL spectra obtained from MacEtched nanopillar p-i-n GaAs LEDs (thick, solid curves) and planar p-i-n GaAs control sample LEDs (thin, dashed curves) at various current levels. The inset is a cross-sectional SEM image showing the LED device structure with superimposed device schematic. (b) Plot of EL intensity as a function of injected current for both samples.

noted that comparison of room-temperature PL spectra obtained from MacEtch- and ICP-RIE-fabricated p-i-n GaAs pillar arrays of similar dimensions shows a small (∼10%) intensity difference, in favor of the MacEtched sample. The optical quality of MacEtched structures may far surpass those produced by RIE as the pillar size becomes smaller and surfaces play a bigger role. This further demonstrates that MacEtch may indeed serve as a competitive process to conventional RIE techniques for such applications.

Room-temperature EL spectra obtained from both nanopillar arrays (thick, solid curves) and planar (thin, dashed curves) p-i-n GaAs LED samples are shown in Figure 5(a) at varying levels of current injection. The inset to Figure 5(a) shows a cross-sectional SEM image of a LED fabricated from MacEtch-produced p-i-n GaAs nanopillars arrays, according to the processing scheme described above, after a 7.5 min MacEtch process in a solution of 20 ml HF, 10 ml DI, and 0.1 g KMnO$_4$. This results in the formation of 2.2 μm tall nanopillars with base and tip widths of approximately 800 nm and 600 nm, respectively. The top ITO layer is formed such that only the p-GaAs segment is contacted. Figure 5(b) plots the EL intensity as a function of the current injection level for both the nanopillar array (red) and the planar control (black) samples. The most notable feature is that EL intensity from the nanopillar sample exceeds that of the planar sample at all comparable current levels (as also indicated by the EL spectra). Larger enhancement is observed with increasing injection current, implying better current spreading with the pillar structure, analogous to the micropixel LED geometry.[42,43] It should be noted that improved current spreading in such geometries should also yield greater internal quantum efficiencies at high injection current densities.[44] Beyond 225 mA (equivalent to a current density of 1.4 A/cm^2), where intensity saturation was first noted, the EL from the MacEtched nanopillar array exceeds the intensity measured from the planar stack by a factor of roughly 3. Note that no surface passivation is employed for the pillar-based LED sample in this study. With more surface

area introduced due to the pillar structure, lower emission efficiency would have been expected if surface related nonradiative recombination dominated, as was the case for micro InGaN LEDs where RIE was used for mesa formation.[44] The fact that intensity degradation is not observed in the current study implies that MacEtch does not cause detrimental damage to the sidewalls. Additionally, we attribute this enhanced efficiency to the light extraction improvement from the nanopillar array, allowing for more efficient photon escape as well as multiple scattering interactions, which reduce the probability of photon re-absorption.[32–37,45] The LED performance is expected to greatly improve by optimizing the pillar size, spacing, and height, as well as applying surface passivation and better metal contact schemes. A broader impact of this work relates to overcoming the "efficiency droop" phenomenon[44] by employing damage-free, high aspect ratio pillar-based LED designs in a wide range of compound semiconductors, particularly in InGaN green LEDs.

IV. CONCLUSIONS

In conclusion, we have demonstrated a room-temperature method for site-selective material removal from p-, i-, and n-type GaAs via MacEtch. A linear trend exists for VERs as a function of temperature and oxidant concentrations. By tuning dilution levels, the competition between material oxidation and etching may be varied such that nanopillar morphologies can be manipulated. Room-temperature PL and EL characterization reveal that optical emission intensity increases with volume of the exposed nanopillars. This method offers a simple, room-temperature, and low cost technique for the formation of high-aspect ratio GaAs nanostructures and has been shown to enhance emission intensity of p-i-n GaAs nanopillar array LEDs in comparison to their planar counterparts. The nanopillar array-based LED structure may provide a solution to current crowding and efficiency droop issues. Our future efforts will focus on the

influence of pillar geometries on the EL emission efficiency as well as MacEtch of other III–V compounds, including ternary and quaternary alloys and heterostructures, for applications in LEDs, lasers, and photovoltaics.

ACKNOWLEDGMENTS

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