Gain Enhancement of Millimeter-Wave on-Chip Antenna through an Additively Manufactured Functional Package

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***Abstract*—Antenna-on-chip (AoC) presents an excellent solution for applications requiring higher integration levels and lower cost, however, its radiation performance is poor due to the inherent lossy Si substrate in conventional complementary metal–oxide–semiconductor (CMOS) processes. It is well known that every chip requires a package to protect it from the environment, however this package does not provide any functionality, despite adding to the cost and required space. In this paper, we propose a functional package which has been designed to enhance the gain of the AoC. A 71 GHz coplanar waveguide (CPW) fed on-chip monopole antenna, driven by a voltage-controlled oscillator (VCO) and frequency doubler, was realized in standard 0.18 µm CMOS technology. As a first step to enhance its gain, the AoC was designed on top of an Artificial Magnetic Conductor (AMC) surface. Further gain enhancement was achieved by transforming the chip package into a combination of a superstrate layer and a Fresnel lens, qualifying this as a System-on-Package (SoP). The package has been realized through additive manufacturing to maintain the low-cost aspect. Overall, the measured gain of the packaged AoC is 6.8 dBi, which has been enhanced by ~20 dBs as compared to the unpackaged antenna without an AMC layer.**

***Index Terms*—Antenna-on-chip (AoC), Artificial Magnetic Conductor (AMC), superstrate, Fresnel lens, System-on-Package (SoP), gain enhancement**

I. Introduction

With the availability of millimeter-wave (mm-wave) bands, there has been a surge in wireless communication applications [1,2]. The multi-GHz of available bandwidth at the mm-wave bands makes it an ideal candidate for high data rate wireless applications [3]. Moreover, the wavelength at these frequency bands is in the range of 1–10 mm, which is small enough to realize the AoC [4-8]. Integrating the AoC and integrated circuits (ICs) in standard CMOS processes can reduce the number of off-chip components in the system as well as eliminate the uncertain influence from the bond wires between the antenna and the ICs. However, the conventional AoC usually suffers from low gain and low radiation efficiency due to the lossy Si substrate in standard CMOS technology. Fig.1 shows the stack up of a standard CMOS process. One of the main challenges is the low resistivity (10–15 Ω-cm) of the Si substrate used in standard CMOS technology. The low resistivity can avoid latch-up in the IC design [9], but in the AoC design, it causes most of the radio-frequency (RF) power to be absorbed by the Si rather than being radiated by the AoC. In addition, due to the high relative permittivity (ε_r = 11.9) and relatively large electrical thickness of the Si, high order surface wave modes are excited, which further degrades the antenna's radiation performance [2]. Another challenge is the mutual coupling between the AoC and the nearby metals in the circuit (such as the interconnection wires, inductors, capacitors, and dummy metals), which can affect current distribution in the AoC. As a result, the radiation performance and impedance matching are further deteriorated [10].

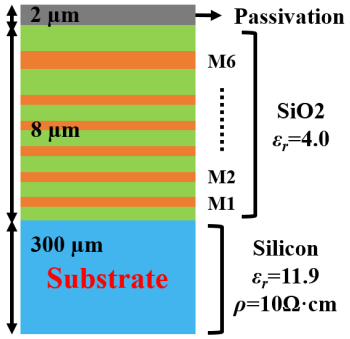

Fig. 1. Standard CMOS stack up

To overcome these challenges, several solutions have been proposed [11-20]. One solution is to alter the structure of the lossy Si substrate through micromachining to reduce the Si thickness [11,16,20]. In [20], an air cavity was formed at the backside of the Si substrate underneath the AoC, so the losses in the Si substrate were reduced because of the thinner substrate. Another option is to implant protons in the Si substrate to increase its resistivity, which can decrease the RF power absorption in the Si [12,19]. Aside from changing the properties of the lossy Si substrate, a micro-electromechanical system (MEMS) structure has been used for gain enhancement [18]. By applying a DC control voltage, the on-chip bowtie antenna can be lifted to move away from the lossy Si, thus achieving gain enhancement. Although micromachining, proton implantation, and MEMS structures can successfully improve the AoC radiation performance, they are not compatible with standard CMOS processes and require significantly more complicated post-fabrication processes.

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Alternatively, the AMC surface can be applied to isolate the AoC from the lossy Si substrate. For example, in [3,14,15], the AMC surfaces were realized using the metal layers in the CMOS stack up to enhance the AoC gain. In-phase reflection occurs when electromagnetic (EM) waves from the AoC are incident on the AMC surface, so the boresight radiation can be boosted by the constructive superposition of the AoC's direct radiation and in-phase reflection. In addition to the on-chip gain enhancement approaches, some studies have used off-chip structures to enhance the AoC radiation performance [13,17].

An interesting approach to enhance the AoC gain is to functionalize the chip package since every chip needs a package for protection from the environment. However, typically, these packages are mere protectors and do not have any functionality, despite adding to the cost and required space. In this work, we introduce an SoP design concept, where the chip package has been optimized to work as a superstrate layer as well as a Fresnel lens, thus enhancing the antenna's gain in addition to providing the required protection to the chip. Overall, the AoC with the functional package demonstrated a gain enhancement of ~20 dBs compared to the unpackaged AoC. The initial simulation results of the on-chip antenna with a superstrate are shown in [21]. This paper covers the detailed design steps for the on-chip antenna with an AMC, the enhancement of gain through a functional package comprising of a superstrate and Fresnel lens, the additive manufacturing of the package, the measured results of the standalone chip, and the complete SoP. The results of this work are promising and indicate that a compact and low-cost AoC, which was previously only useful for very short-range applications, can also be used for medium or even longer range applications by smartly packaging the ICs.

The paper is organized as follows: Section II presents the design of the on-chip AMC structure. Section III shows the detailed design for the functional package and resultant gain enhancement in simulations. Section IV briefly describes the antenna's driving circuits. Section V presents the fabrication of the functional package and the overall measured results.

II. On-Chip AMC Surface as a Reflector

The standard 0.18 μm CMOS process consists of a 6–10 μm thick inter-metal dielectric embedding 6–9 metal layers, as shown in Fig. 1. The AoC is usually implemented on the top metal layer because this layer provides sufficient metal thickness for the realization of the AoC. Moreover, it helps direct the radiation into the free space. A standalone quarter-wavelength monopole antenna has been simulated with the CMOS stack-up. However, only -13.6 dBi antenna gain is obtained because of the lossy Si substrate. Ideally, in order to isolate the AoC from the lossy Si substrate, a Perfect Electrical Conductor (PEC) surface could be placed on the Metal 1 (M1) layer. However, in this case, the PEC surface becomes electrically too close to the AoC where the distance is around 7 – 8 μm, as a result, the induced image current on the PEC can negatively affect the antenna's radiation performance. According to the boundary conditions, a Perfect Magnetic Conductor (PMC) surface can resolve this issue because the PMC surface can have an in-phase reflection rather than the out-of-phase reflection from a PEC surface. Since no PMC surface exists in nature, an AMC surface, which is a combination of a periodic structure and a ground plane (Fig. 2 (a)), was proposed to mimic a PMC surface within a specific frequency band.

In this work, the AMC structure consists of a square patch-based periodic frequency selective surface on the M1 layer and a ground plane at the backside of the Si substrate as shown in Fig. 2 (a). The square patch was selected as the AMC unit cell because it has larger bandwidth and lower substrate loss compared to other basic AMC unit cell structures [22].

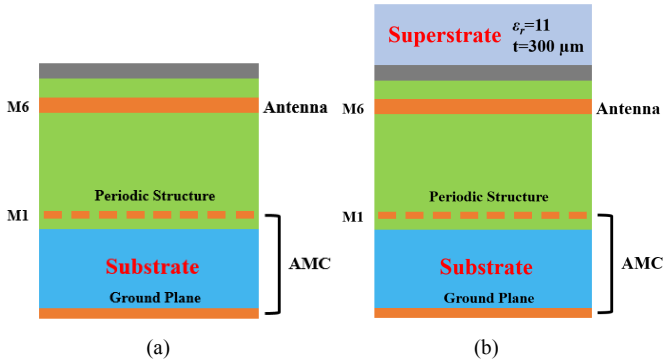


Fig. 2. Stack up of (a) the AoC integrated with the AMC structure, and (b) the AoC integrated with the AMC and superstrate

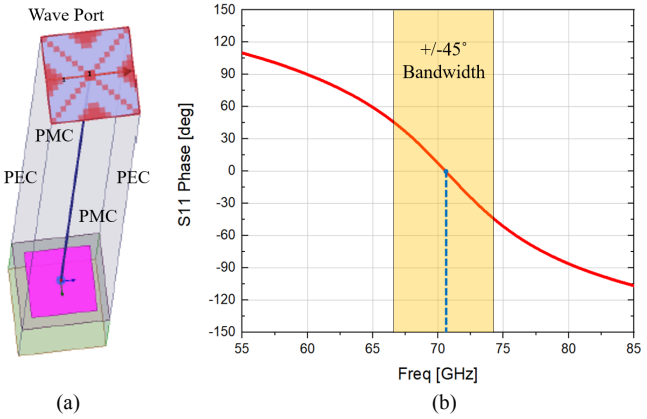


Fig. 3. (a) High Frequency Simulation Sotfware (HFSS) model for an AMC cell and (b) reflection phase of the AMC structure

Fig. 3 (a) shows the simulation model of the square patch AMC unit cell in HFSS. To mimic the infinite AMC surface, PEC and PMC boundary wall conditions were used in the simulations, as shown in Fig. 3 (a). The wave port was assigned on the top of the square patch at a distance of quarter wavelength. Later, the wave port was de-embedded to the surface of the AMC surface to eliminate the additional transmission phase shift [21]. The dimension of the square patch was optimized to achieve the in-phase reflection at 71 GHz, as shown in Fig. 3 (b). A bandwidth of 7.4 GHz was achieved, in which the AMC operating bandwidth is defined as the frequency range within +/- 45° of the phase of the reflection coefficient.

In theory, the AMC surface needs to be infinite to behave as

a PMC surface, however, this has not been possible to realize on a very small chip. In order to determine a reasonable size for the AMC structure, a CPW fed quarter-wavelength monopole antenna was simulated on top of varying AMC surface sizes. Fig. 4 illustrates that, as expected, the gain of the on-chip monopole was enhanced with the increasing number of AMC unit cells. However, the AMC surface size is restricted by the chip size, which is 1.5 mm × 1.5 mm. As a tradeoff between size and maximum antenna gain, an AMC size of 6 × 8 unit cells (0.48 mm^2) was selected.

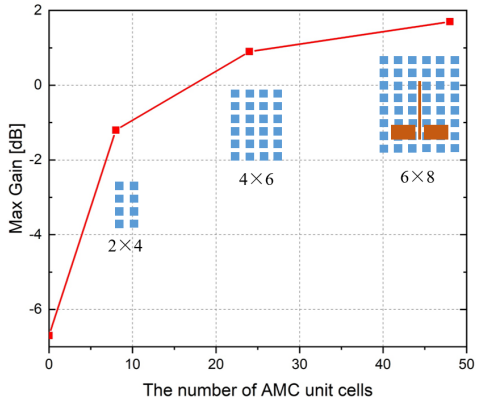


Fig. 4. Maximum gain of a monopole antenna versus the AMC surface size

III. Functional Chip Package for Gain Enhancement

A. Superstrate Layer

A superstrate with a high permittivity can increase the antenna's coupling into free space, thus improving the boresight radiation and reducing substrate losses as less EM waves are absorbed in the lossy Si substrate. Fig. 2 (b) demonstrates the superstrate integration with the AMC-backed AoC. In this design, the superstrate material is PREFERM FLX 1100, which has a high permittivity of ε_r = 11 and a low loss tangent of $tan\delta$ = 0.006 at 71 GHz.

In order to investigate the effect of the superstrate thickness, a CPW-fed AoC (quarter-wavelength monopole antenna) was optimized for the best radiation efficiency for varying thicknesses of the superstrate. As Fig. 5 shows, maximum radiation efficiency was achieved with a superstrate thickness equal to 300 μm, while the second maximum was obtained with a superstrate thickness of around 900 μm. This result indicates that the radiation efficiency is maximized when the thickness of the superstrate layer is equal to odd multiples of $\lambda_d/4$, where λ_d is the wavelength in the medium. In terms of the transmission line equivalent model, the superstrate layer behaves as a quarter wavelength impedance transformer, thereby improving the antenna's coupling to free space [23]. Consequently, this design uses a superstrate thickness of 300 μm.

Since the superstrate is quite thick ($\lambda_d/4$), it is capable of providing good protection for the chip. Therefore, the superstrate can act as the chip package as well provide gain enhancement. In addition, no metal patterning or alignment is required during the superstrate preparation, so it is easy to realize the superstrate.

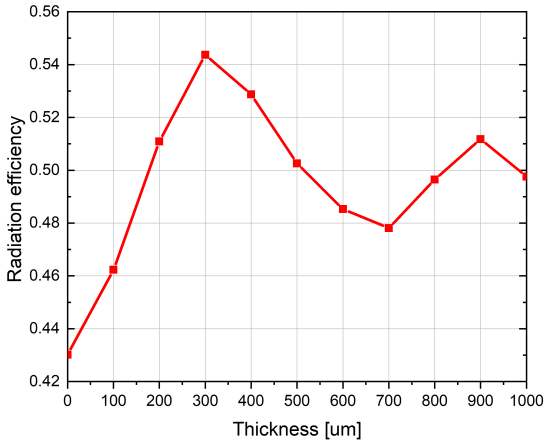


Fig. 5. Radiation efficiency versus superstrate thickness

B. Fresnel Lens Package

Further gain enhancement can be achieved by incorporating a lens. A Fresnel lens can be used for gain enhancement through beam shaping, which is realized by diffraction instead of refraction in the conventional hyperboloid lens [24]. A Fresnel lens is a phase-correcting lens that consists of a set of planar grooved circular plates which should be made of a low-loss material [25]. As Fig. 6 illustrates, the EM waves from the AoC located at the focal point propagate an additional distance Δ from the outer surface of the sphere to the edge of each zone plate.

$$\Delta = n \times \frac{\lambda_0}{P} \tag{1}$$

Where n is the number of planar plates and P is the number of different phases for realizing phase correction. For example, P is equal to 2 and 4 in half-wavelength and quarter-wavelength phase-correcting lenses, respectively. The beam-focusing performance improves with a larger P.

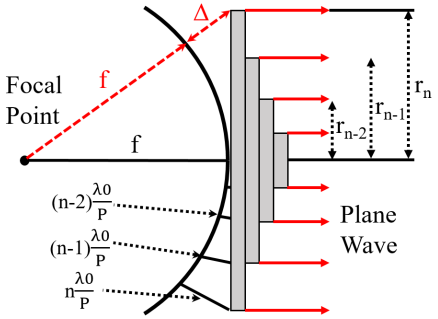


Fig. 6. Geometry of the wave propagation in a Fresnel lens package

For a quarter-wavelength phase-correcting lens, if the AoC is placed at the focal point, the EM waves radiated from the AoC will pass through different parts of the zone plates with less than a 90° phase shift. Then, the plane wave is formed after passing through the lens, as shown in Fig. 6. Thus, the beam-focusing function is achieved by the phase-correcting zone plates. The radius of each zone plate, r_n, is calculated by the right triangle formula [26].

$$r_n = \sqrt{2f\frac{n\lambda_0}{P} + (\frac{n\lambda_0}{P})^2} \quad (1)$$

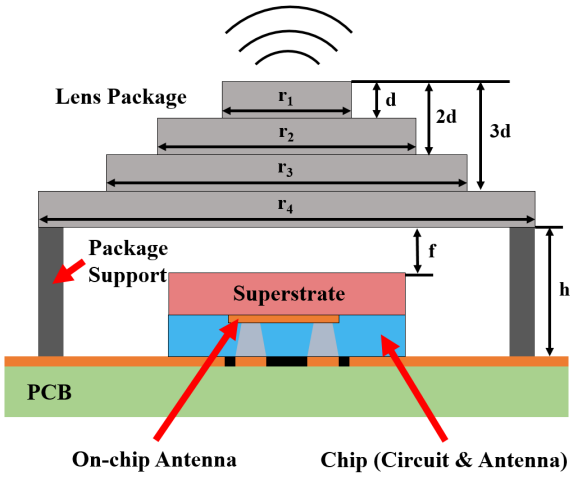
In this design, P = 4 was chosen, which is a good compromise between the focusing ability of the Fresnel lens and the complexity of the lens fabrication. The focal length is equal to 2.7 mm, resulting in a relatively low F/D ratio of 0.21 but ensuring a compact SoP design. The quarter-wavelength lens was grooved into four-layer zone plates with depths of d, $2d$, and $3d$. The depth, d, is provided in [26].

$$d = \frac{\lambda_0}{4(\sqrt{\varepsilon_r} - 1)} \quad (2)$$

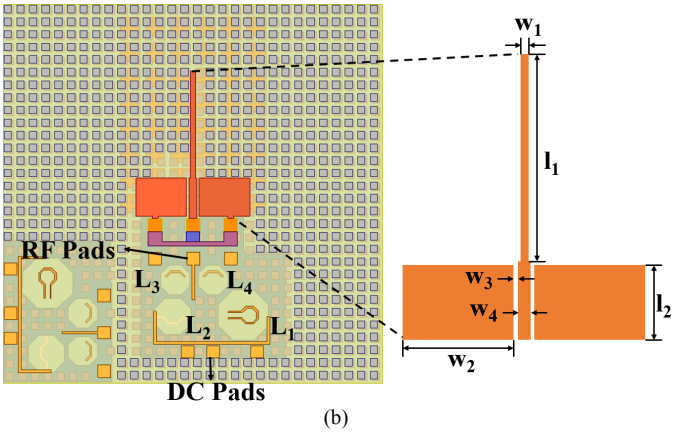
Where ε_r is the permittivity of the lens material. It is noted that the lens thickness is inversely proportional to the permittivity. Therefore, a high permittivity material (PREFERM 3D ABS filament, ε_r = 10, $tan\delta$ = 0.02 at 71 GHz) was chosen to ensure a compact design.

Fig. 7 (a) shows a cross-sectional view of the SoP design, which contains the AoC, on-chip AMC surface, functional package in the form of a superstrate, and Fresnel lens. A gap length of f = 2.7 mm was achieved through pillars constructed of the same packaging material. This gap helps maintain the required focal distance between the antenna and the lens. The combination of the superstrate and Fresnel lens not only provides protection from the environment, but it also provides gain enhancement.

The final simulation model also included the connection to the driving circuit output, as shown in Fig. 7 (b). In order to improve the accuracy of the simulation model, the circuit wires, inductors, capacitors, and dummy metals were all included in this simulation. Since this is the top view of the multilayered CMOS chip, only the top metal layer (M6) is clearly visible. The top layer of the circuit shows the VCO inductor L_1, the frequency doubler inductor L_2, the matching network inductors L_3 and L_4, ground-signal-ground (GSG) pads of the circuit RF output, and the three pads for the DC power supply. The detailed information of the circuit is presented in Fig. 10.



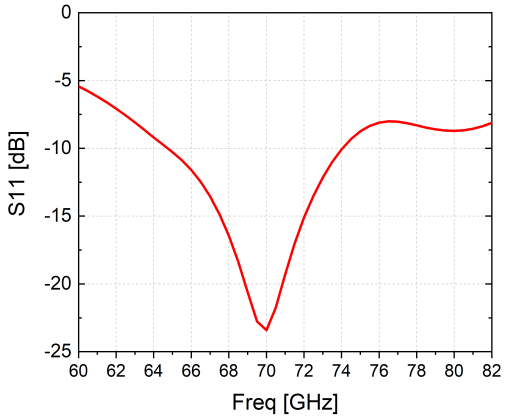
(a)



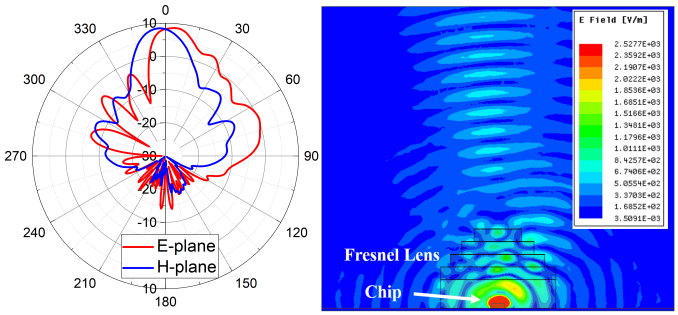
(b)

Fig. 7. HFSS simulation models. (a) The proposed SoP model, r_1 = 5.46, r_2 = 8.28, r_3 = 10.78, r_4 = 13.16, d = 1.44, h = 3.26, f = 2.7 (all in mm). (b) The AoC and the configuration of the CPW-fed monopole antenna, chip size: 1.5×1.5 mm^2; w_1 = 20, w_2 = 200, w_3 = 10, w_4 = 30, l_1 = 425, and l_2 = 130 (all in μm).

The optimized SoP design demonstrates a simulated return loss of -19.3 dB at 71 GHz, as shown in Fig. 8 (a), indicating a good impedance match at the frequency of interest. The 10-dB impedance bandwidth is around 9.4 GHz, from 64.8 GHz to 74.2 GHz. Fig. 8 (b) provides the simulated radiation patterns of the proposed design. It can be seen that the proposed antenna shows a directive boresight radiation with a maximum gain of 8.8 dBi, which achieves approximately 22 dBs of gain enhancement in the simulation compared to the standalone AoC. The antenna shows a good symmetric radiation pattern in the H-plane, however, there are multiple ripples in the E-plane radiation pattern, as shown in Fig. 8 (b), which are mainly caused by the presence of the relatively large ground plane in the driving circuit part. This is also the main reason that the antenna boresight beam is slightly titled. Fig. 8 (c) shows the electric field distribution of the proposed SoP design. The plane wave with a reduced beam width is clearly formed after passing through the Fresnel lens, verifying the beam-focusing ability of the functional package.



(a)



(b) (c)

Fig. 8. HFSS simulation results of the proposed design: (a) return loss versus frequency, (b) 2D radiation pattern (*E*-plane and *H*-plane), and (c) electric field distribution

IV. On-Chip Antenna Driving Circuit Design

In real world applications, an on-chip antenna must be fed by the driving circuits, and it must operate well in the presence of circuits, interconnects, bond pads, etc. Therefore, for realistic testing of the on-chip antenna in the presence of circuits, the driving circuits were also designed. Fig. 9 shows the schematic of the on-chip driving circuits, which included a VCO, a frequency doubler, and a matching network that feeds the AoC. The VCO generates a 35.5 GHz RF signal. Since the cutoff frequency of the transistor in the 0.18 μm CMOS technology (used for this project due to its lower cost) is 52 GHz, the VCO cannot generate a 71 GHz RF signal efficiently. Therefore, a frequency doubler was designed to double the VCO output frequency to 71 GHz. The matching network was used to match the impedance between the AoC and the frequency doubler to ensure maximum power transmission.

Fig. 10 (a) shows the schematic of the VCO. The cross-coupled NMOS transistors (M_1 and M_2) generate the negative resistance to cater for losses from the LC tank (L_1, C_1, and C_2). By tuning the control voltage V_{tune}, the capacitance of the two varactors (C_1 and C_2) can be adjusted accordingly. As a result, the oscillating frequency of the LC tank can be tuned. The VCO outputs a 35.5 GHz RF signal at the port between $+V_{out}$ and $-V_{out}$, which is applied to the port between V_{in}+ and V_{in}- for the frequency doubler, as shown in Fig.10 (b). The two transistors (M_5 and M_6) are biased to generate the 2nd order harmonic (71 GHz) at the inductive load L_2 where the 2nd harmonic and other even harmonics add up constructively while all the odd harmonics cancel with each other. The conventional LC matching network was applied to transform the output impedance of frequency doubler to 50 Ω, which is consistent with the AoC input impedance. The simulations of the driving circuit were conducted in Cadence. Fig. 11 depicts the simulated spectrum of the driving circuit output. It can be seen that a 71.2 GHz RF signal with -12.1 dBm power is obtained at the 2nd order harmonic.

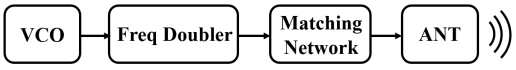


Fig. 9. Schematic of the on-chip system

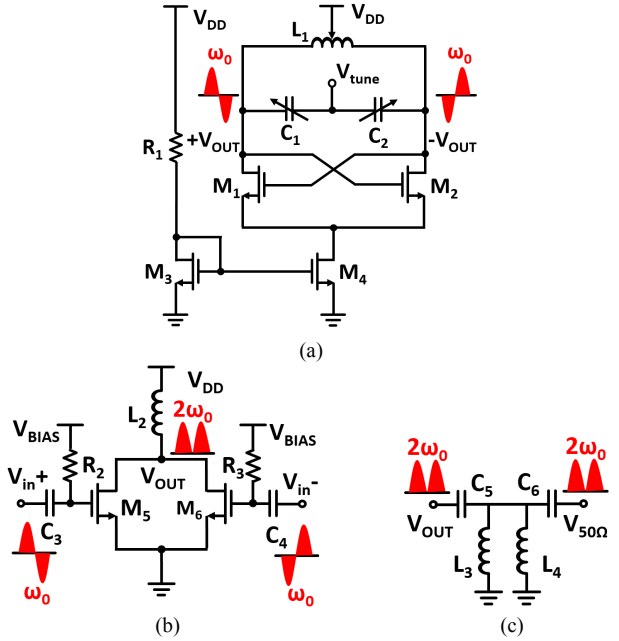


Fig. 10. Schematic of the (a) VCO, (b) frequency doubler, and (c) matching network

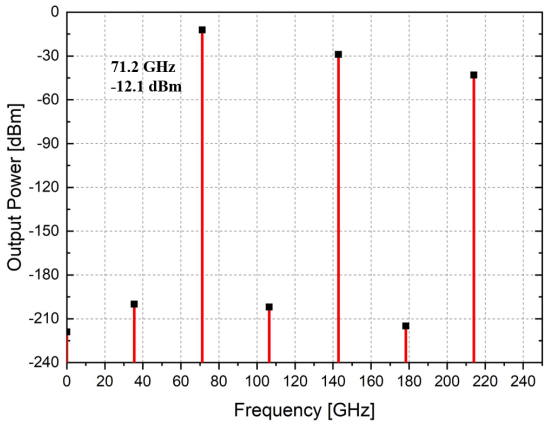


Fig. 11. Frequency spectrum of the driving circuit output

V. Measurement and Analysis

A. Driving Circuit Measurement

The driving circuit and AoC were monolithically integrated in a single chip, which has been fabricated in the Taiwan Semiconductor Manufacturing Company (TSMC) 0.18 μm CMOS process. The microscopic view of the chip is shown in Fig. 12. The total area of the chip is 1.5 mm × 1.5 mm. The AoC occupies an area of 0.6 mm × 0.8 mm, while the driving circuits occupy an area of 0.56 mm × 0.50 mm. Fig. 13 shows the block diagram of the circuit measurement setup. The driving circuit is powered up, and its output is connected to the spectrum analyzer through the RF signal path, which consists of the RF probe, the RF cables, and the mixer. The uncalibrated power spectrum was obtained from the spectrum analyzer, after which the loss of the RF signal path mentioned above was calibrated by replacing the driving circuit shown in Fig. 13 with a signal generator.

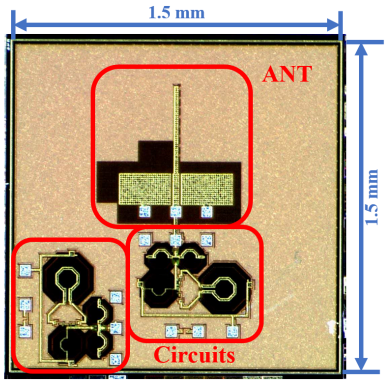


Fig. 12. Microscopic view of the chip

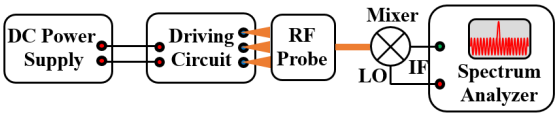


Fig. 13. Block diagram of the driving circuit measurement setup

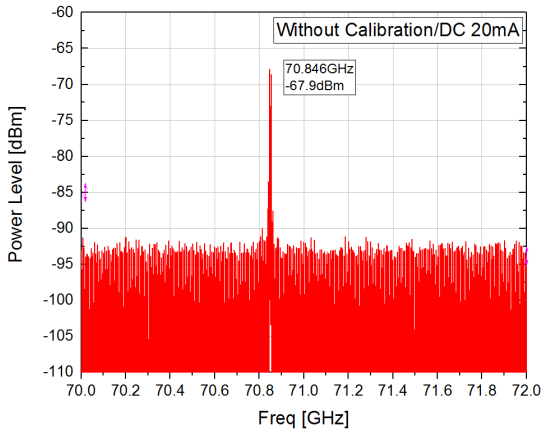


Fig. 14. Driving circuit power spectrum

According to the circuit output power spectrum in Fig. 14, the driving circuit generates a 70.84 GHz RF signal when a supply voltage of 1.8 V is applied. The circuit consumes 25.2 mW of DC power. The power level of the RF signal received by the spectrum analyzer is -67.9 dBm. After calibration, the 54.3 dB path loss is added back to the measured output power level, so the real circuit output power is -13.6 dBm at 70.84 GHz. This is 1.5 dB lower than predicted by the simulations. This discrepancy may be due to an error in the manual path loss calibration.

B. On-chip Antenna Passive Measurement and Analysis

The driving circuit and AoC are connected through a short transmission line. To characterize the AoC independently without the circuit's loading effect, the transmission line must be disconnected from the antenna. This was accomplished through the focus ion beam (FIB), as shown in the magnified portion of Fig. 15. The compact mm-wave anechoic chamber shown in Fig. 16 was used to characterize the reflection coefficient and radiation performance of the proposed AoC [27].

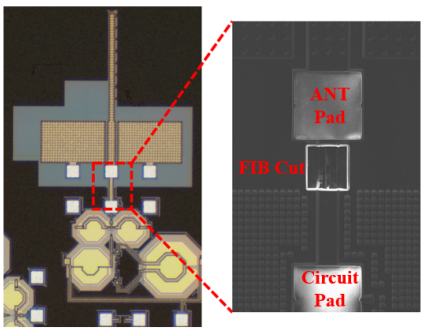


Fig. 15. Transmission line cut by FIB

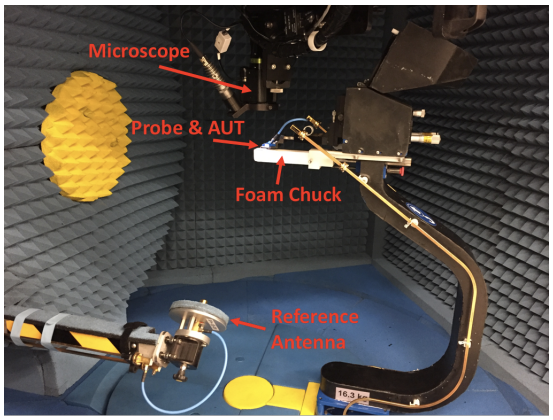


Fig. 16. µ-lab mm-wave anechoic chamber

The antenna under test (AUT) was placed at the center of the chamber on top of a foam chuck to avoid metallization effect from a metal chuck. For this passive testing, the antenna needs to be fed from an RF probe. For that purpose, a set of GSG pads were provided on this chip. The AUT was connected to the power network analyzer (PNA) through the probe and the waveguide. The reference antenna, a horn antenna with a gain of 16 dBi at 71 GHz, was connected to the scanning arm and aligned its boresight to the AUT. The microscope and the vision system were used to assist the alignment and landing of the probe with respect to the AUT. Before the radiation pattern measurement, the path loss in this measurement setup was calibrated by directly connecting the two ports with a known loss cable. For the return loss measurement, the probe was calibrated by landing it on the short, open, and load of the impedance standard substrate prior to the S_{11} measurement.

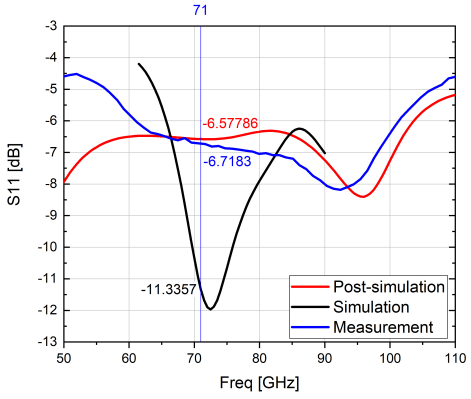
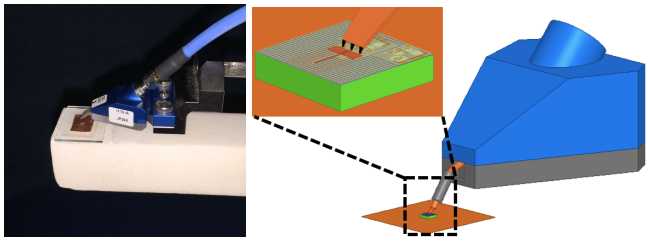


Fig. 17. Simulated and measured return loss of the AoC integrated with the AMC



(a) (b)

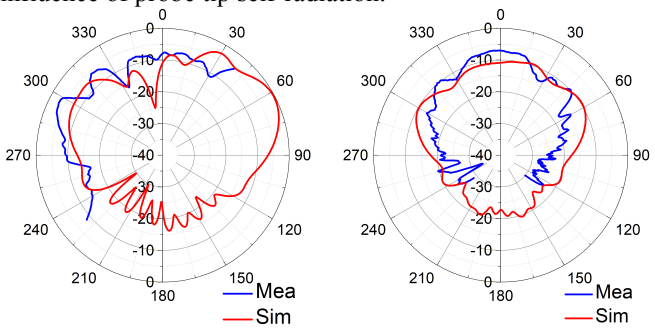
Fig. 18. (a) Probe landed on the antenna pads. (b) Probe simulation model

Fig. 17 shows the simulated and measured reflection coefficients for the AoC. Some obvious discrepancies exist between the measurement (blue) and simulation (black) results. In the simulations, the antenna is well matched at 71 GHz, however, it is not matched well at the frequency of interest in the measurements. After a detailed investigation, we discovered two main reasons for this discrepancy.

- The coupling effects between the AoC and the driving circuits: The AoC and the driving circuits are integrated in a single chip and placed close to each other to reduce transmission loss. The inductors, capacitors, interconnection lines, and dummy metal sheets in the circuit part can lead to unwanted EM coupling when the AoC is excited.
- The probe effect: Although the probe's inner impedance was de-embedded through the calibration, the large metallic body of the probe in close vicinity to the antenna remains a problem. In addition, the probe tips are not completely covered with the absorber, resulting in unwanted coupling between the probe tips and the circuit under the probe [28].

The accurate circuit model, dummy metal fills, and probe model were not included in the initial simulation, therefore, there are major discrepancies between the simulated and measured results. In order to verify the two above-mentioned effects, the accurate circuit model, dummy metal fills, and probe model were included in the post-simulation, as shown in Fig. 18. It can be seen that the post-simulation results (red) show a good agreement with the measurement results (blue) in the range of 60-110 GHz. This result verifies the hypothesis that the discrepancy was caused by coupling effects between the antenna and probe as well as some parts of the driving circuits.

Fig. 19 shows the measured and simulated radiation patterns of the AoC with the integrated AMC surface. A measured boresight gain of -7.3 dBi was obtained. The measured radiation pattern follows similar trends, however, there are some discrepancies between the simulated and measured results. The chamber has a measurement arm (as can be seen in Fig. 16), which blocks the radiation pattern measurements for the range of 40° ≤ theta ≤ 230° in the E-plane. We anticipate that the main reason for the discrepancy is the presence of the probe near the AoC. The probe tip itself radiates, so the measured radiation patterns are actually the supposition of probe self-radiation and antenna radiation. The probe body is a close-by conductor, and it can reflect the EM waves radiated by the antenna and cause interference at certain angles [29]. Though, we have an approximate probe model in the simulations, but at this frequency, a more accurate model is necessary to capture what occurs in the measurements. In the future, customized mm-wave absorbers could be used to cover the conductor body to avoid EM reflection and decrease the influence of probe tip self-radiation.



(a) (b)

Fig. 19. Measured and simulated radiation patterns. (a) *E*-plane and (b) *H*-plane

C. *Active Measurements for SoP Implementation*

The functional package was fabricated through additive manufacturing technologies, including inkjet and 3D printing. The DC connections between the on-chip circuit pads and the printed circuit board (PCB) were fabricated through inkjet printing technology instead of traditional bond wiring technology. This absence of bond wires enables a smooth attachment of the superstrate layer to the chip. A dielectric isolation layer was first inkjet printed on top of the on-chip circuit area to avoid short circuiting the printed DC connections with the circuits. The DC connections (ground and power supply) were printed from the on-chip pads to the edge of the chip, as shown in Fig. 20. Subsequently, a silver paste was applied to connect the chip edge to the PCB, as shown in Fig. 21(a). A 300 μm layer of PREFERM FLX 1100 was used as the superstrate layer. The Fresnel lens package and its support shown in Fig. 21(b) were fabricated through 3D printing technology with the PREFERM 3D ABS filament ($\varepsilon_r = 10$, $tan\delta = 0.02$ at 71 GHz).

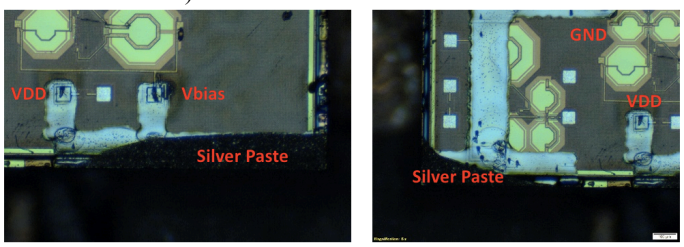
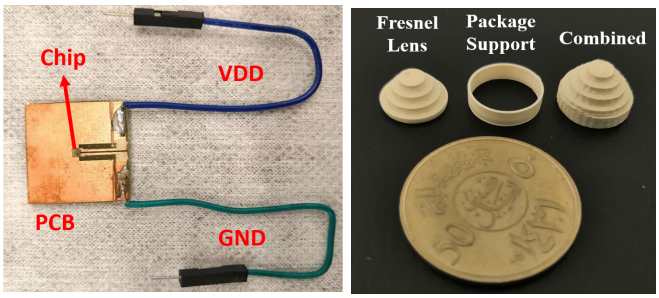


Fig. 20. Inkjet printed on-chip DC connection lines



(a) (b)

Fig. 21. (a) DC connection of a 3D-printed chip package. (b) Additively manufactured Fresnel lens package

Once the chip is packaged (with an additively manufactured Fresnel lens), the GSG pads are not accessible for probe-based measurements, so active measurements were performed to assess the gain enhancement performance as predicted by the simulations. Fig. 22 illustrates the dedicated setup used for active measurements as these could not be performed conventionally in the chamber.

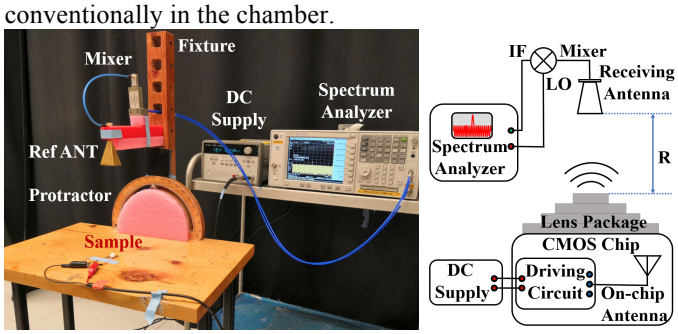


Fig. 22. AoC active measurement setup: (a) photograph and (b) block diagram

For active measurements, the driving circuit is first powered up by the DC power supply. The driving circuit generates the RF signal with a power level of -13.6 dBm at 70.84 GHz, which is fed to the AoC as the transmitted power. The receiving antenna is a V-band reference horn antenna with a gain of 24 dBi at 50–75 GHz. The receiving antenna and the AUT are aligned in a boresight-to-boresight configuration with a distance of R = 30 cm, which is larger than $r = 2D^2/\lambda_0$, satisfying the far-field condition. The antenna's largest aperture dimension and free-space wavelength at 71 GHz are D and λ_0, respectively. The RF signal received by the reference horn antenna is then transmitted to the spectrum analyzer through RF cables and the mixer with a total path loss L of 51.2 dB at the operating frequency. The received power is measured by the Agilent E4448A spectrum analyzer. The absolute gain of the AUT is obtained by applying the Friis transmission equation, as shown below:

$$G_t = P_r - P_t - G_r - 20\log_{10}\left(\frac{\lambda_0}{4\pi R}\right) - L \qquad (3)$$

Where G_t and G_r are the gains of the transmitting antenna (AUT) and the reference horn antenna, P_r and P_t, are the received and transmitted power, respectively. L is the total path loss and the R is the boresight distance between the AUT and the reference antenna.

Fig. 23 shows the measured radiation patterns of the E- and H-planes compared to the simulated radiation patterns for all four cases: the AoC integrated with the AMC; the AoC integrated with the AMC and superstrate; the AoC integrated with the AMC and Fresnel lens; and the AoC integrated with the AMC, superstrate, and Fresnel lens. These four cases were simulated and measured for investigating the gain enhancement performance of the AMC, superstrate, and Fresnel lens. Due to the constraints of the active measurement setup, the measurements of the radiation patterns were only performed for the range of -50° ≤ theta ≤ 50°. As shown in Fig. 23, there is acceptable agreement between the simulated and measured radiation patterns. It can be seen that the final SoP (the AoC integrated with the AMC, superstrate, and Fresnel lens) displays the narrowest beam width compared to other cases.

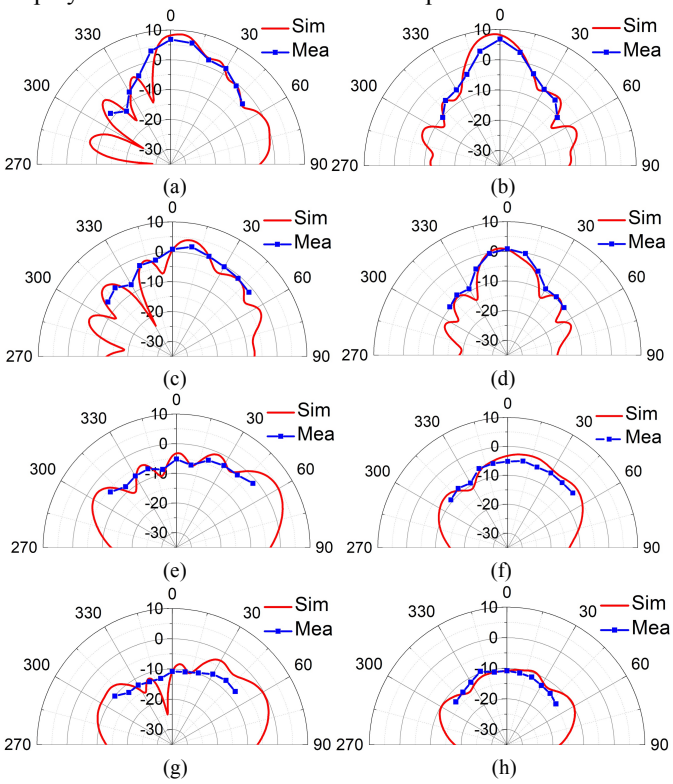


Fig. 23. Simulated and measured radiation patterns in E-plane (left) and H-plane (right). (a)(b) AoC integrated with the AMC, superstrate, and Fresnel lens; (c)(d) AoC integrated with the AMC and Fresnel lens; (e)(f) AoC integrated with the AMC and superstrate; (g)(h) AoC integrated with the AMC

TABLE I. THE COMPARISON OF RADIATION PERFORMANCE

Cases	AoC Boresight Radiation Performance		
	Description	*Simulation*	*Measurement*
1	Standalone AoC	-13.8 dBi	NA
2	AoC + AMC	-10.8 dBi	-9.7 dBi
3	AoC + AMC + superstrate	-3.2 dBi	-5.2 dBi
4	AoC + AMC + Fresnel lens	0.6 dBi	0.8 dBi
5	AoC + AMC + superstrate + Fresnel lens	8.3 dBi	6.8 dBi

Table I summarizes the boresight radiation performance for all the cases in the measurements and simulations. The combination of AMC, superstrate, and Fresnel lens enhanced the gain by ~20 dBs compared to the AoC alone. This is a very large enhancement in gain considering the fact that this is coming from the package of the chip, which would not add anything to the gain in normal circumstances. As can be seen from Table I, the Fresnel lens provides around 12 dBs of gain enhancement, if we compare the gains in Case (3) and Case (5). In addition, according to the comparison between Case (2) and Case (3), around 7 dBs of gain enhancement is obtained by using the superstrate layer. Comparing the simulation results of Case (1) and Case (2) reveals that the AMC adds up to 3 dBs of gain compared to the standalone AoC. The standalone AoC gain measurement could not be performed because the AMC is built into the chip during the chip fabrication process.

VI. Conclusion

The AoC has been considered an excellent solution for mm-wave applications that require high integration levels and low costs. However, the AoC suffers from low gain because of the lossy Si substrate. In addition, it is well known that all chips need to be packaged. In mm-wave ranges, the presence of the chip package can further deteriorate the AoC performance. This paper proposes one method to enhance the gain by shaping the chip package into a specially designed functional package structure, which combines a superstrate layer and a Fresnel lens. This functional package can improve the antenna's radiation performance as well as provide chip protection. Furthermore, an on-chip AMC surface is also used to enhance the AoC gain. In this work, a 71 GHz CPW fed on-chip monopole antenna was implemented in a 0.18 μm standard CMOS process. The proposed AoC integrated with an AMC and functional package achieved a measured gain of 6.8 dBi at 71 GHz with an impedance bandwidth of 9.2 GHz. The gain enhancement of the overall combination was experimentally demonstrated to be 20.6 dB, indicating a substantial gain enhancement over a standalone AoC.

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