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GaN Metal Oxide Semiconductor Field Effect Transistors

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ABSTRACT

A GaN based depletion mode metal oxide semiconductor field effect transistor (MOSFET) was demonstrated using $Ga_2O_3(Gd_2O_3)$ as the gate dielectric. The MOS gate reverse breakdown voltage was > 35V which was significantly improved from 17V of Pt Schottky gate on the same material. A maximum extrinsic transconductance of 15 mS/mm was obtained at V_{ds} = 30 V and device performance was limited by the contact resistance. A unity current gain cut-off frequency, f_T, and maximum frequency of oscillation, f_{max} of 3.1 and 10.3 GHz, respectively, were measured at V_{ds} = 25 V and V_{gs} = -20 V.

DISCLAIMER

A number of GaN field effect transistors (FETs) and AlGaN/GaN heterostructure FETs have been reported showing excellent device breakdown characteristics[1-5]. The conventional low resistance n^+-cap layer structure used to reduce parasitic resistances in GaAs technology is generally not applied in nitride devices as it is difficult to perform the gate recess step. This is due to the high chemical stability of GaN which makes wet etching very difficult except at high temperatures or under optical stimulation.[6,7] The drawback of dry etching for pattern transfer is the ion bombardment induced damage. This damage then causes a low gate breakdown voltage.[8]

These problems can be overcome by using a metal oxide semiconductor FET (MOSFET) approach of the type recently reported for GaAs and InGaAs. [9,10] The $Ga_2O_3(Gd_2O_3)$ films were deposited on GaAs or InGaAs using e-beam evaporation from a single crystal of $Ga_2O_3(Gd_2O_3)$ in an MBE chamber. As a result, both n- and p-type enhancement mode MOSFETs could be demonstrated. In this study, a similar approach has been applied to fabrication of $Ga_2O_3(Gd_2O_3)$/GaN devices resulting in the demonstration of the first GaN MOSFET.

The GaN layer structure was grown on c-Al_2O_3 substrates prepared initially by $HCl/HNO_3/H_2O$ cleaning and an in-situ H_2 bake at 1070 °C. A GaN buffer <300 Å thick was grown at 500 °C using trimethylgallium and ammonia and crystallized by ramping the temperature to 1040 °C. The same precursors were used again to grow ≥ 3 μm of undoped GaN ($n < 10^{16}$ cm^{-3}) and an ~8000 Å Si-doped ($n = \sim 3 \times 10^{17}$ cm^{-3}) active layer.[11]

A cross-sectional view of the schematic GaN MOSFET is shown in Figure 1. Device fabrication started with isolation and achieved with Cl_2/Ar dry etching in a Plasma Therm ICP system. An oxide of $Ga_2O_3(Gd_2O_3)$ mixture was then deposited as a gate oxide using the technique similar to that previously reported for GaAs MOSFET.[12] Followed with oxide removal in the source and drained regions prior to the ohmic contact deposition with a HCl

solution and Ti/Al/Pt/Au was employed as the ohmic metallization. Then. the gate contact was defined with a standard photoresist lift-off process of Pt/Ti/Pt/Au.

A cross-sectional TEM of the $Ga_2O_3(Gd_2O_3)$/GaN is shown in Figure 2. A sharp $Ga_2O_3(Gd_2O_3)$/GaN interface was obtained which is consistent with our x-ray reflectivity data.[13] The $Ga_2O_3(Gd_2O_3)$ is amorphous and there was no stress observed in the oxide layer. The dc characteristics of a $1.2 \times 60\ \mu m^2$ gate dimension GaN MOSFET is shown in Figure 3. This is the first demonstration of GaN based MOSFET. A maximum extrinsic transconductance of 15 mS/mm was obtained at V_{ds} = 30 V, which was limited by the parasitic resistance. The use of a thin and heavily doped channel (< 800 Å and > 10^{18} cm^{-3}) will improve both transconductance and reduce the contact resistance. The extrinsic RF characteristics of a typical GaN MOSFET is illustrated in Figure 4. The device was measured at drain and gate voltage of 25V and -20V, respectively. The unity gain cut-off frequency and maximum frequency of oscillation of 3.1 and 11.2 GHz, respectively, were achieved. The device rf performance was also limited by contact resistance and extrinsic capacitance.

In summary we have demonstrated GaN depletion mode MOSFETs and showed both dc and rf characteristics. The device performance can be improved by optimizing the layer structure using a thin and heavily doped channel layer which will reduce the contact resistance and enhance trnasconductance.

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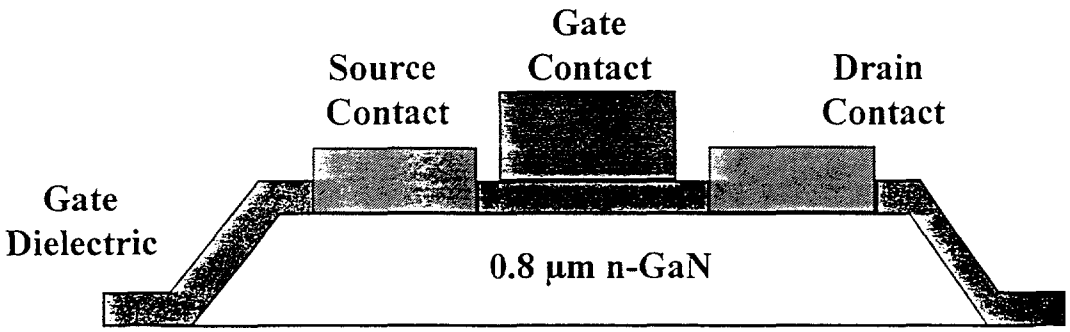
Figure Captions

Figure 1. A cross-sectional view of GaN metal oxide semiconductor field effect transistor(MOSFET).

Figure 2. A cross sectional TEM of $Ga_2O_3(Gd_2O_3)$/GaN sample.

Figure 3. Drain I-V characteristics of an $1.2 \times 60\ \mu m^2$ gate dimensional GaN MOSFET.

Figure 4. Rf characteristics of an $1.2 \times 60\ \mu m^2$ gate dimensional GaN MOSFET measured at V_{ds} = 25 V and V_{gs} = -20 V .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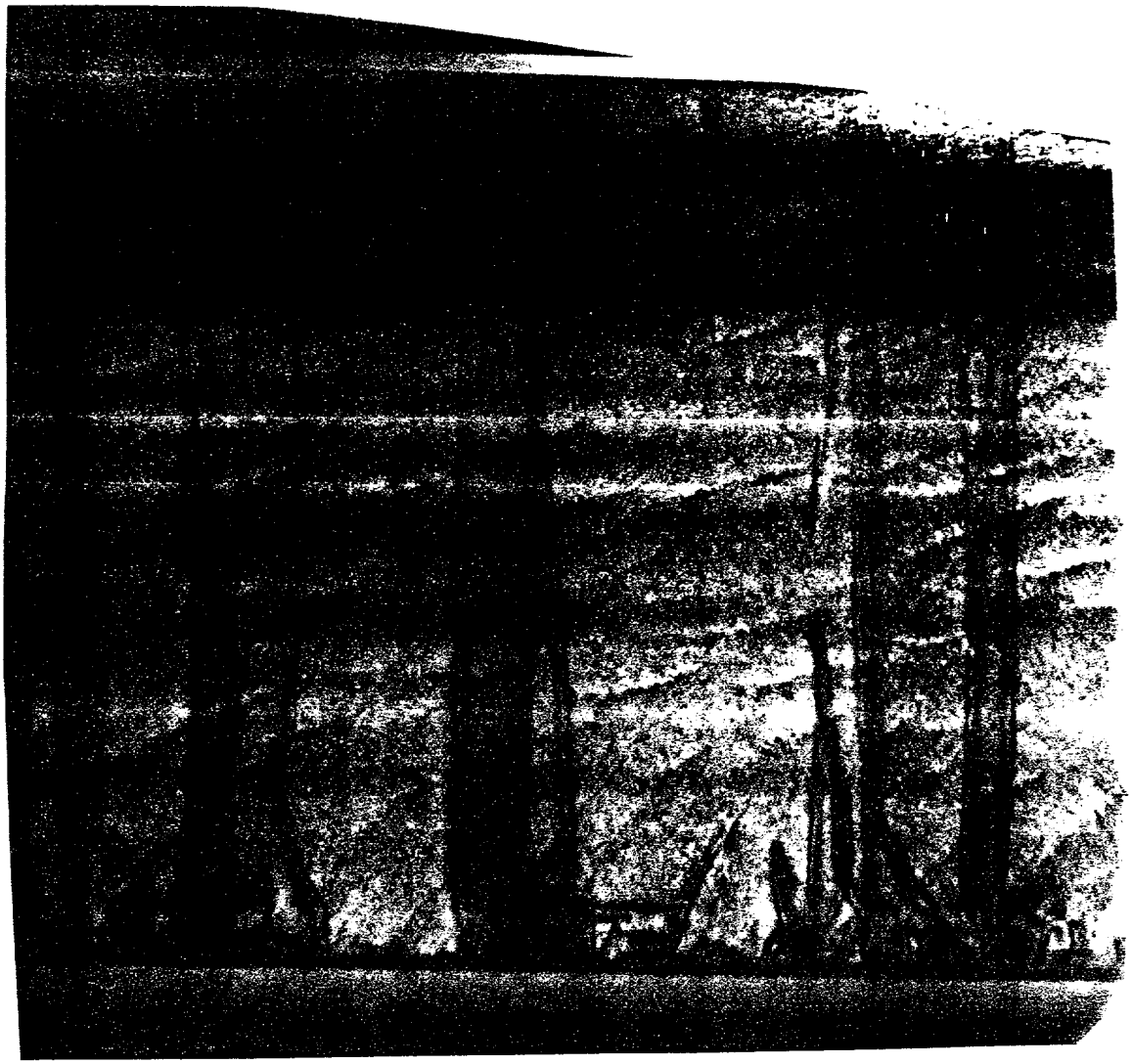

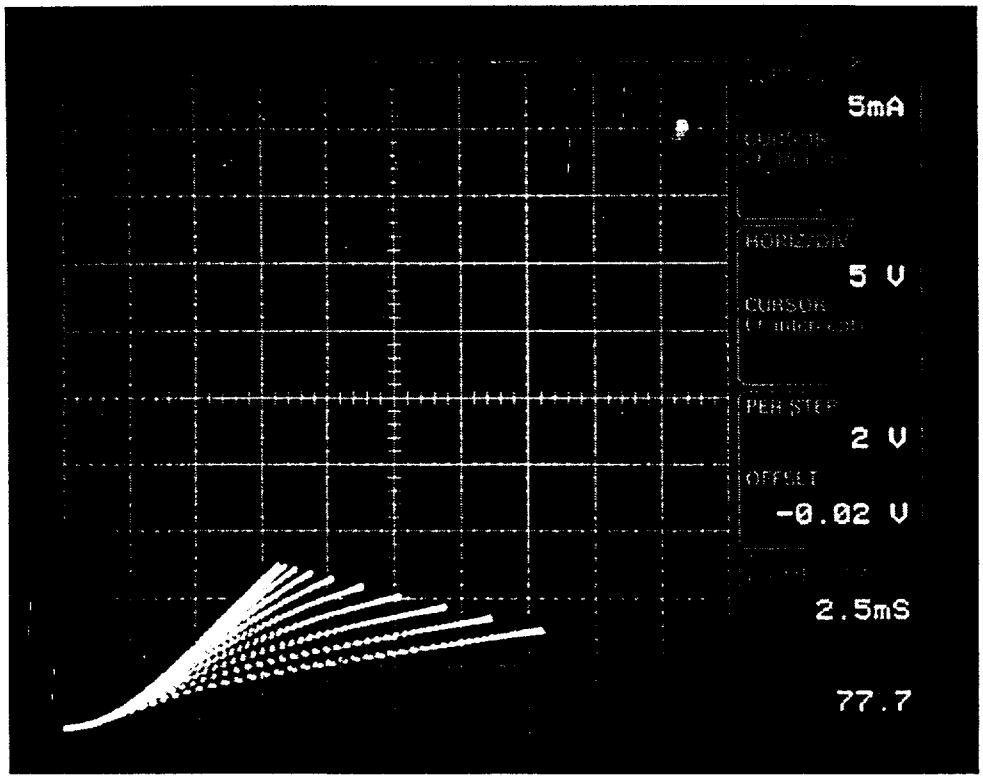
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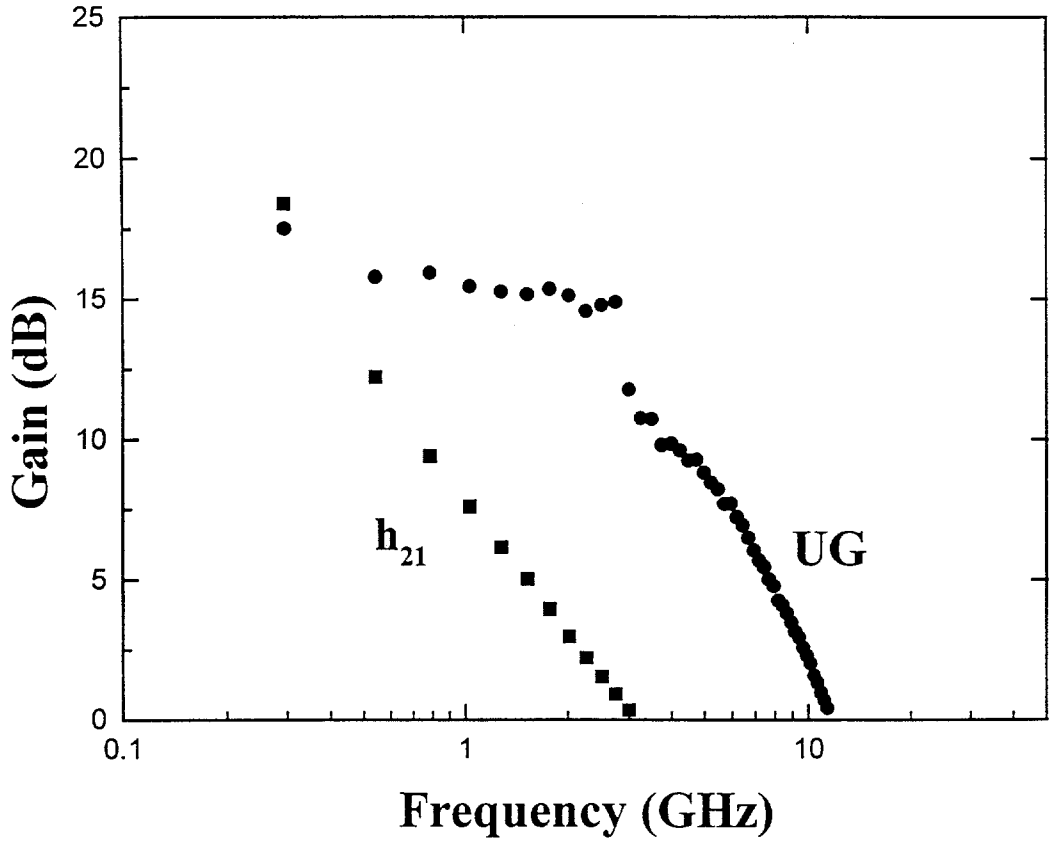
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