Published in final edited form as:

*IEEE Electron Device Lett*. 2018 February ; 39(2): 184–187. doi:10.1109/LED.2017.2785785.

# GaN Nanowire MOSFET with Near-Ideal Subthreshold Slope

**Wenjun Li**,
University of Notre Dame, Notre Dame, IN 46656 USA

**Matt D. Brubaker**,
National Institute of Standards and Technology, Boulder, CO 80305 USA

**Bryan T. Spann**,
National Institute of Standards and Technology, Boulder, CO 80305 USA

**Kris A. Bertness [Senior Member, IEEE]**, and
National Institute of Standards and Technology, Boulder, CO 80305 USA

**Patrick Fay [Fellow, IEEE]**
University of Notre Dame, Notre Dame, IN 46656 USA

## Abstract

Wrap-around gate GaN nanowire MOSFETs using $Al_2O_3$ as gate oxide have been experimentally demonstrated. The fabricated devices exhibit a minimum subthreshold slope of 60 mV/dec, an average subthreshold slope of 68 mV/dec over three decades of drain current, drain-induced barrier lowering of 27 mV/V, an on-current of 42 μA/μm (normalized by nanowire circumference), on/off ratio over $10^8$, an intrinsic transconductance of 27.8 μS/μm, for a switching efficiency figure of merit, $Q=g_m/SS$ of 0.41 μS/μm-dec/mV. These performance metrics make GaN nanowire MOSFETs a promising candidate for emerging low-power applications such as sensors and RF for the internet of things.

### Index Terms

Gallium nitride; MOSFET; nanowire

## I. INTRODUCTION

To continue the trend of reduced power consumption and improved device performance even as device scaling becomes ever more challenging, alternative device architectures are needed. By using a wrap-gate and one-dimensional channel geometry, nanowire (NW) MOSFETs are a promising option to achieve sufficient electrostatic control in an ultra-scaled, highly-integrated transistor design [1], [2]. NW MOSFET scaling not only allows higher current density and lower power consumption, but also enables higher device speed for low-power and high-frequency applications, as required for future wireless internet of

The review of this letter was arranged by Editor XXX.

things (IoT) nodes [2], [3]. For these applications, highly-efficient switching is essential to achieve the power efficiency and performance required.

While Si and C-based NW devices have been demonstrated with excellent results [4], [5], gallium nitride (GaN) is an alternative channel material for NW MOSFETs that offers some unique features. The wide band gap of GaN ($E_g$ ~ 3.4 eV) can suppress the device off-current, while the high electron mobility ($\mu_e$ ~ 1000-2000 $cm^2$/V-s) and comparatively large density of states mass (m* ~ 0.2 $m_0$) enables high current density for high switching speed [6]-[14]. On the other hand, the wide band gap and chemical resistance also make GaN nanowire MOSFETs promising for operation in harsh environments (such as high temperature, radiation, and extreme pH levels).

Nanowires in GaN can be formed by direct nanowire growth (e.g. [7]-[12]) or by top-down lithography and etch processing (e.g. [13, 14]). While excellent device results have been obtained using top-down approaches [14], direct growth of nanowire structures offers the potential for tighter dimensional control (via selective-area growth approaches) [8, 9] and the avoidance of dry-etch related sidewall damage that must be ameliorated (typically through additional wet-etch steps) in top-down process flows [13, 14]. In this Letter, GaN NW MOSFETs based on selectively-grown GaN nanowires exhibiting both appreciable transconductance ($g_m$)—desirable for high-frequency operation—as well as near-ideal subthreshold slope (*SS*), is advantageous for improving detection sensitivity in sensors and reducing power consumption for signal processing in low-power applications, are demonstrated. This combination of high $g_m$ and low SS leads to a record-high intrinsic switching efficiency figure of merit, Q=$g_m$/SS, for directly grown GaN nanowire FETs of 0.41 μS/μm-dec/mV. The impact of oxide-semiconductor interface states and parasitic access resistances on transistor performance are analyzed in detail. This study provides key insights into the primary performance limiters in selectively-grown GaN NW MOSFETs as a promising device candidate for future ultra-scaled, low-power technology.

## II. Experiment

The GaN NWs used in this work were grown using catalyst-free selective-area plasma-assisted molecular beam epitaxy (MBE) on Si (111) substrates. Compared with other NW formation approaches such as dry etching and vapor-liquid-solid (VLS) growth, the catalyst-free selective-area growth is beneficial to avoid defects from etch damage and impurities from the catalyst, while yielding good control of the wire diameter during growth. The detailed growth process and conditions can be found in [15] and [16]. The NWs used here were uniformly doped with Si at a concentration of $1 \pm 0.1 \times 10^{18}$ $cm^{-3}$, as estimated by Raman spectroscopy using the method described in [17].

Fig. 1 (a) shows an oblique SEM image of a typical lateral wrap-around-gated GaN NW MOSFET. The nanowires were removed from the growth substrate by ultrasonic agitation and dispersed onto the target substrate ($10^{15}$ $cm^{-3}$ p-type silicon sample coated with 285 nm thick $SiO_2$ deposited by plasma-enhanced atomic layer deposition (ALD)). To fabricate the devices, source and drain contacts were defined with electron beam lithography (EBL) and electron-beam evaporation of Ti/Au (20/100 nm). The gate oxide $Al_2O_3$ was then formed by

thermal ALD using trimethylaluminum (TMA) as the precursor and $H_2O$ as oxidant at 300 °C. The detailed ALD process can be found in [18]. A Ni/Au (20/100 nm) gate finger was then defined on top of the gate oxide by EBL, evaporation, and lift-off. To passivate $Al_2O_3$ and $Al_2O_3$/GaN interface, the devices were annealed in forming gas (10% $H_2$/90% $N_2$) at 350 °C for 30 minutes. Four-point test structures have been fabricated alongside the FETs using nanowires from the same growth run to measure wire transport [10].

From the cross-sectional TEM taken under the gate in Fig. 1 (b), a conformal $Al_2O_3$ film of ~16 nm is found to be formed at the hexagonal sidewall surface; the sidewalls of the nanowire are m-plane. The asymmetric hexagonal structure in Fig. 1 (b) arises from occasional imperfections in the electron beam lithography opening or buffer layer morphology. Due to the large surface-to-volume ratio, the nanowire MOSFET is sensitive to surface charges from the water vapor adsorption [19]. To minimize this effect, the sample was measured in nitrogen and stored under vacuum. The device performance can be recovered by heating the sample above 100 °C in nitrogen or forming gas; this effect can be minimized by dielectric passivation.

## III. Results and discussions

Fig. 2 shows the measured transfer and output characteristics of a typical GaN NW MOSFET with a gate length ($L_G$) of ~274 nm and NW diameter of ~146 nm; the current densities are normalized to circumference. In the transfer characteristics in Fig. 2(a), the device shows a sharp turn-on behavior that exhibits an average SS ($SS_{avg}$) of 68 mV/dec for three decades of drain current and a drain-induced barrier lowering (DIBL) of ~ 27 mV/V. As can be seen in Fig. 3 (a), the measured SS does not depend on $V_{DS}$. The transfer characteristics are insensitive to gate sweep direction; in the inset in Fig. 3(a), the transfer curves at $V_{DS}$=1.0 V for gate sweeps in upward and downward direction are shown. Threshold voltage hysteresis of less than 50 mV was measured, and the $SS_{avg}$ was nearly unchanged (65 mV/dec for upward sweeps, vs. 68 mV/dec for downward sweeps). The SS versus drain current shown in Fig. 3(a) (for both forward and reverse sweeps) shows that the minimum SS approaches the thermionic limit of 60 mV/dec. The low $SS_{avg}$ and $SS_{min,}$ as well as small DIBL highlight the tight electrostatic control enabled by the wrap-around gate geometry and good dielectric/semiconductor interface quality.

The off-current ($I_{OFF}$) and gate current ($I_G$) are on the order of $10^{-7}$ μA/μm (limited by the semiconductor parameter analyzer noise floor), and the $I_{ON}/I_{OFF}$ ratio is larger than $10^8$. Breakdown of the gate oxide occurs at a gate bias of 10 V, corresponding to an electric field of ~6.3 MV/cm. The depletion-mode threshold voltage (−4.2 V) evident in Fig. 2 (a) is mainly caused by the large NW diameter, which requires a negative gate bias to fully deplete the channel. The output characteristics in Fig. 2 (b) exhibit good saturation with $V_{DS}$, but an offset voltage can be observed in the turn-on region, suggesting the presence of Schottky barriers at the contacts. Based on temperature-dependent measurements of the drain current at small $V_{DS}$, a Schottky barrier height at the contacts of 0.29 eV was extracted. An on-current of 42 μA/μm was obtained at the drain bias of 4 V.

To study the quality of semiconductor/dielectric interface, the devices were also measured at temperatures from 77 to 297 K. Fig. 3 (b) shows the $SS_{avg}$ versus temperature ($T$) relationship at $V_{DS}$=2.5 V. From a linear fit, $SS_{avg}$ reduces with $T$ at a rate of 0.22 mV/dec-K. In the subthreshold region, the semiconductor capacitance from the depleted channel is much smaller than the gate oxide $C_{ox}$. Using the gate-all-around MOSFET model, the oxide capacitance can be expressed as $C_{ox}=\varepsilon_{ox}/(R\ln(1+t_{ox}/R))$ per gate area [20]. For the device reported here, $C_{ox}$ is calculated to be 0.4 μF/cm$^2$. Consequently, the density of interface trap states $D_{it}$ can be estimated using [21]:

$$D_{it} \leq \frac{C_{ox}}{q^2}\left(\frac{SS}{T}\frac{q}{\ln(10)k} - 1\right) \quad (1)$$

where $k$ is the Boltzmann constant and $q$ is the electron charge. The average $D_{it}$ near the conduction band edge is extracted to smaller than ~ 2.7 × 10$^{11}$ cm$^{-2}$eV$^{-1}$ in the subthreshold region. The minimum "spot" SS measured, 60 mV/decade, suggests that the mid-gap $D_{it}$ is approaching 2.5×10$^{10}$ cm$^{-2}$eV$^{-1}$. This low effective $D_{it}$, in conjunction with the favorable electrostatics of the wrap-gate nanowire geometry, enables near-ideal $SS$ in these devices.

The transconductance ($g_m$) of a typical device is shown in Fig. 4. The extrinsic $g_m$ (solid line) peaks at 10.5 μS/μm for $V_{DS}$=2.5 V. Due to the combination of the small source and drain contact area, the Schottky-like nature of the unoptimized Ti/Au contacts, and the small cross section of the NW, the parasitic access resistance can contribute significantly to the MOSFET on-resistance ($R_{ON}$). The nanowire resistivity $\rho$ is measured to be 0.03 Ω-cm from four-point test structures fabricated alongside the FETs, corresponding to a bulk mobility of 208 cm$^2$/V-s in the nanowire. The gate underlap region at drain or source side is approximately 150 nm, contributing a series resistance of ~5.4 kΩ. The access resistance, including the resistance contribution from contacts and NW bulk region, can be de-embedded from the transconductance to extract the intrinsic transconductance. The intrinsic transconductance $g_{m,int}$ can be estimated by the following expression [22]:

$$g_{m,int} = \frac{g_m^0}{1-(R_D+R_s)g_d(1+R_s g_m^0)} \quad (2)$$

where $g_m^0 = \frac{g_m}{1-R_s g_m}$, $R_S$ and $R_D$ are the access resistance at source and drain sides, respectively, and $g_m$ and $g_d$ are the measured transconductance and output conductance, respectively [22]. $R_S$ and $R_D$ are differential access resistance from the $V_{DS}$-$I_{DS}$ curve at $V_{GS}$=4 V calculated at the corresponding $V_{DS}$ bias points (i.e. 0.5, 1.0, 1.5, 2.0 and 2.5 V). Under these bias conditions, the drain Schottky contact is forward biased, while the source Schottky contact is reverse biased. Therefore, the drain contact resistance $R_D$ was assumed to be negligible relative to the source-side contribution $R_S$. After correcting for the access resistance, the estimated $g_{m,int}$ has been greatly improved, especially at open-channel biases. At $V_{DS}$=2.5 V, the peak $g_{m,int}$ is estimated to be 27.8 μS/μm.

Fig. 4 (b) presents a benchmarking comparison of $g_m$ versus $SS_{avg}$ for GaN nanowire FETs fabricated from directly grown wires. Contours of constant $g_m/SS_{avg}$ are plotted to delineate different levels of low-power switching efficiency [23]. The devices reported in this work have the best switching efficiency (intrinsic Q=0.41 μS/μm-dec/mV) reported for any GaN nanowire FET using directly-grown nanowires, suggesting that these devices are promising for low-power applications. The main limitations of the current devices for low-power circuits are the high knee voltage and the negative threshold voltage. These factors can be addressed by optimizing the device design and fabrication. Optimized source/drain contacts (e.g. Ti/Al and optimized anneal conditions) can reduce the knee voltage. The threshold voltage can be controlled by both gate metal work-function engineering and reducing the nanowire doping. Numerical simulations (not shown) indicate that enhancement-mode operation can be expected for Ni/Au gates with nanowire doping of $1\times10^{17}$ $cm^{-3}$.

## IV. Conclusions

GaN NW MOSFETs with near-ideal *SS*, minimized DIBL, on/off ratio over $10^8$, appreciable $I_{ON}$ of 42 μA/μm, measured extrinsic $g_m$ of 10.5 μS/μm, intrinsic $g_{m,int}$ of 27.8 μA/μm and intrinsic switching efficiency Q of 0.41 μS/μm-dec/mV are demonstrated in this work. Based on temperature-dependent measurements, the average $D_{it}$ at the GaN/$Al_2O_3$ interface is calculated to be $2.7 \times 10^{11}$ $cm^{-2}eV^{-1}$. Improvements in the contact resistance and access resistance (through self-aligned processing), as well as improved oxide/semiconductor interface quality, NW diameter and gate length scaling are promising for achieving enhancement mode operation as well as higher $I_{ON}$ and $g_m$ in GaN nanowire MOSFETs.

## Acknowledgments

The authors would like to acknowledge Prof. A. Seabaugh for access to his cryogenic probe station and S. Rouvimov and T. Orlova for TEM imaging support.

This work is supported by the Center for Low Energy Systems Technology, one of the six centers of STARnet, a Semiconductor Research Corporation Program sponsored by Microelectronics Advanced Research Corporation and the Defense Advanced Research Projects Agency, under Grant 2013-MA-2383.

## References

1. Wernersson L-E, Thelander C, Lind E, Samuelson L. III-V nanowires—extending a narrowing road. Proc IEEE. Dec; 2010 98(12):2047–2060. DOI: 10.1109/JPROC.2010.2065211
2. Lind E. High frequency III-V nanowire MOSFET. Semicond Sci Technol. Aug.2016 31(9): 093005.doi: 10.1088/0268-1242/31/9/093005
3. Aitken R, Chandra V, Myers J, Sandhu B, Shifren L, Yeric G. Device and technology implications in the Internet of Things. Symp VLSI Technol, Dig Tech Papers. Jun.2014 :1–4. DOI: 10.1109/VLSIT.2014.6894339
4. Singh N, Agarwal A, Bera LK, Liow TY, Yang R, Rustagi SC, Tung CH, Kumar R, Lo GQ, Balasubramanian N, Kwong D-L. High-performance fully depleted silicon nanowire (diameter 5 nm) gate-all-around CMOS devices. IEEE Electron Device Lett. May; 2006 27(5):383–386. DOI: 10.1109/LED.2006.873381
5. Franklin AD, Luisier M, Han S-J, Tulevski G, Breslin CM, Gignac L, Lundstrom MS, Haensch W. Sub-10 nm Carbon Nanotube Transistor. Nano Lett. Jan; 2012 12(2):758–762. DOI: 10.1021/nl203701g [PubMed: 22260387]

6. Vandenbrouck S, Madjour K, Théron D, Dong Y, Li Y, Lieber CM, Gaquiere C. 12 GHz GaN/AlN/AlGaN Nanowire MISFET. IEEE Electron Device Lett. Apr; 2009 30(4):322–324. DOI: 10.1109/LED.2009.2014791
7. Huang Y, Duan X, Cui Y, Lieber CM. Gallium nitride nanowire nanodevices. Nano Lett. Jan; 2002 2(2):101–104. DOI: 10.1021/nl015667d
8. Blanchard PT, Bertness KA, Harvey TE, Sanders AW, Sanford NA, George SM, Seghete D. MOSFETs made from GaN nanowires with fully conformal cylindrical gates. IEEE Trans Nanotechnol. May; 2012 11(3):479–482. DOI: 10.1109/TNANO.2011.2177993
9. Blanchard PT, Bertness KA, Harvey TE, Mansfield LM, Sanders AW, Sanford NA. MESFETs Made From Individual GaN Nanowires. IEEE Trans Nanotechnol. Nov; 2008 7(6):760–765. DOI: 10.1109/TNANO.2008.2005492
10. Mansfield LM, Bertness KA, Blanchard PT, Harvey TE, Sanders AW, Sanford NA. GaN nanowire carrier concentration calculated from light and dark resistance measurements. J Electron Mater. Apr; 2009 38(4):495–504. DOI: 10.1007/s11664-009-0672-z
11. Gačević Ž, López-Romero D, Mangas TJ, Calleja E. A top-gate GaN nanowire metal–semiconductor field effect transistor with improved channel electrostatic control. Appl Phys Lett. Jan.2016 108:033101.doi: 10.1063/1.4940197
12. Rumyantsev SL, Shur MS, Levinshtein ME, Motayed A, Davydov AV. Low-frequency noise in GaN nanowire transistors. Appl Phys Lett. Mar.2008 103:064501.doi: 10.1063/1.2895398
13. Jo Y-W, Son D-H, Lee D-G, Won C-H, Seo JH, Kang IM, Lee J-H. First demonstration of GaN-based vertical nanowire FET with top-down approach. Proc 73rd Annu Device Res Conf (DRC). Jun.2015 :35–36. DOI: 10.1109/DRC.2015.7175539
14. Yu F, Rümmler D, Hartmann J, Caccamo L, Schimpke T, Strassburg M, Gad AE, Bakin A, Wehmann H-H, Witzigmann B, Wasisto HS, Waag A. Vertical architecture for enhancement mode power transistors based on GaN nanowires. Appl Phys Lett. May.2016 108:213503.doi: 10.1063/1.4952715
15. Brubaker MD, Duff SM, Harvey TE, Blanchard PT, Roshko A, Sanders AW, Sanford NA, Bertness KA. Polarity-Controlled GaN/AlN Nucleation Layers for Selective-Area Growth of GaN Nanowire Arrays on Si(111) Substrates by Molecular Beam Epitaxy. Cryst Growth Des. 2016; 16(2):596–604. DOI: 10.1021/acs.cgd.5b00910
16. Bertness KA, Sanders AW, Rourke DM, Harvey TE, Roshko A, Schlager JB, Sanford NA. Controlled nucleation of GaN nanowires grown with molecular beam epitaxy. Adv Funct Mater. Jul; 2010 20(17):2911–2915. DOI: 10.1002/adfm.201000381
17. Robins LH, Horneber E, Sanford NA, Bertness KA, Brubaker MD, Schlager JB. Raman spectroscopy based measurements of carrier concentration in n-type GaN nanowires grown by plasma-assisted molecular beam epitaxy. Appl Phys Lett. Sep.2016 120:124313.doi: 10.1063/1.4963291
18. Li W, Digiovanni D, Fay P. Comparative study of dielectric/semiconductor interface for $Al_2O_3$ on non-polar m-plane and Ga-polar c-plane GaN. to be published.
19. Wang Q, Puntambekar A, Chakrapani V. Co-adsorption of water and oxygen on GaN: Effects of charge transfer and formation of electron depletion layer. J Chem Phys. Sep.2017 147:104703.doi: 10.1063/1.4991322 [PubMed: 28915758]
20. Iñíguez B, Jiménez D, Roig J, Hamid HA, Marsal LF, Pallarès J. Explicit continuous model for long-channel undoped surrounding gate MOSFETs. IEEE Trans Electron Devices. Aug; 2005 52(8):1868–1873. DOI: 10.1109/TED.2005.852892
21. Sze, SM., Ng, KK. Physics of Semiconductor Devices. John Wiley & Sons; 2006.
22. Chou SY, Antoniadis DA. Relationship Between Measured and Intrinsic Transconductances of FET's. IEEE Trans Electron Devices. Feb; 1987 34(2):448–450. DOI: 10.1109/T-ED.1987.22942
23. Doornbos G, Passlack M. Benchmarking of III–V n-MOSFET Maturity and Feasibility for Future CMOS. IEEE Electron Device Lett. Oct; 2010 31(10):1110–1112. DOI: 10.1109/LED.2010.2063012

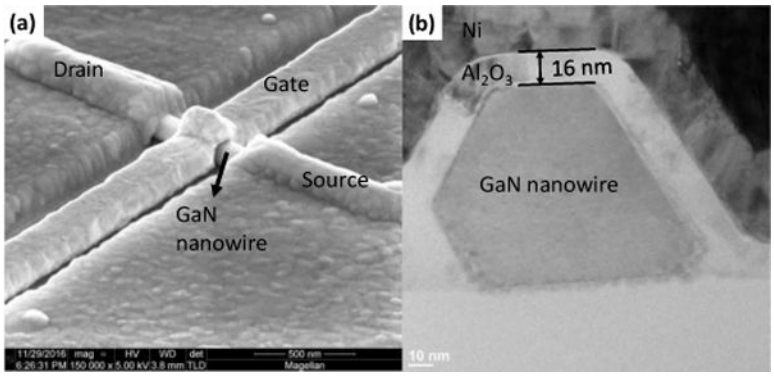


**Fig. 1.**

Typical fabricated GaN NW MOSFET (a) oblique SEM image; (b) cross-sectional TEM image under the gate.

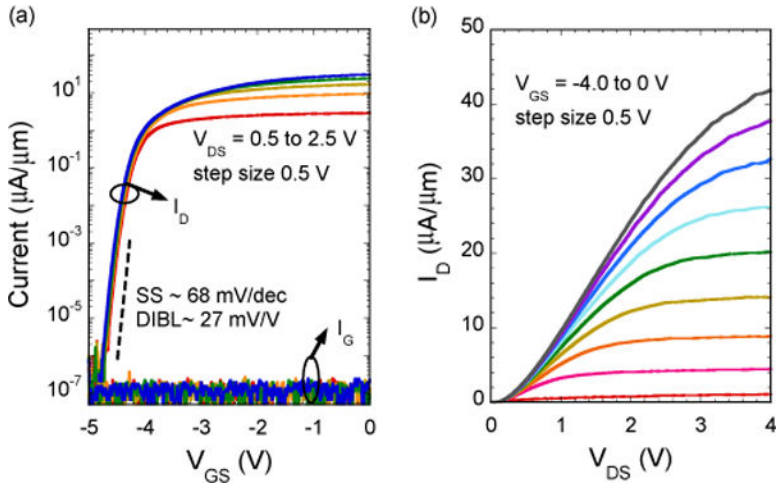


**Fig. 2.**

Measured performance of a typical GaN NW MOSFET with ~ 274 nm gate length and ~146 nm wire diameter: (a) transfer characteristics; (b) common-source output characteristics.

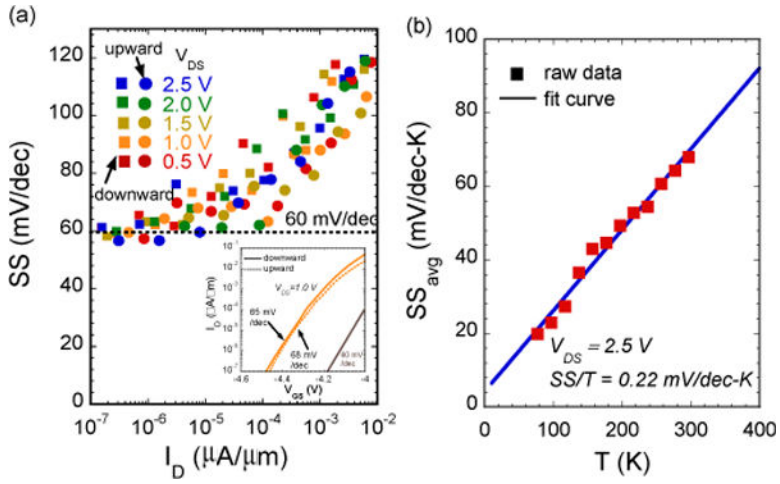


**Fig. 3.**

(a) *SS* versus drain current at room temperature. Squares: downward $V_{GS}$ sweep, dots upward sweep. Inset: detail of the subthreshold transfer curves at $V_{DS}$=1.0 V for downward and upward gate voltage sweeps. (b) average *SS* versus temperature, the line is least-squares fit to data (squares).

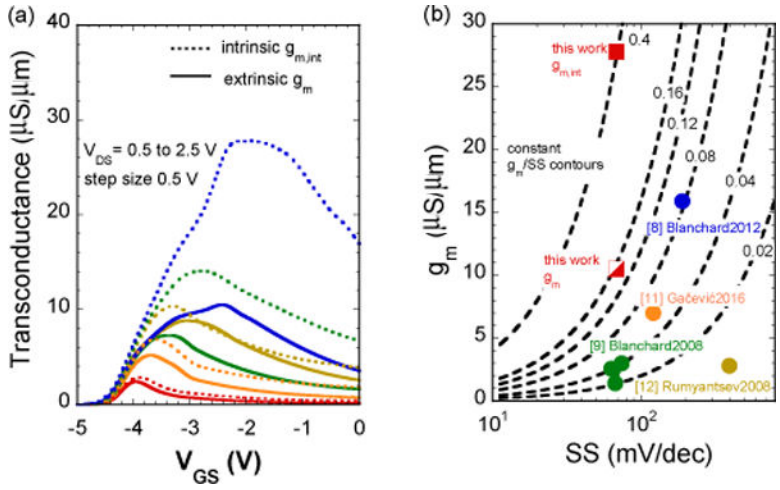


**Fig. 4.**

(a) GaN NW MOSFET measured transconductance $g_m$ (solid line) and estimated intrinsic transconductance $g_{m,int}$ after correcting for the access resistance (dashed line). (b) The benchmark plot of $g_m$ versus $SS$ for GaN nanowire FETs fabricated from directly grown wires reported in the literature. The filled square represents the $g_{m,int}$ in this work and the half-filled square represent the $g_m$. The dashed lines are the constant $g_m/SS$ contours.