GaN-on-Si Quasi-Vertical Power MOSFETs

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***Abstract*— We demonstrate the first GaN vertical transistor on silicon, based on a 6.7-µm-thick n-p-n heterostructure grown on 6-inch silicon substrate by metal organic chemical vapor deposition (MOCVD). The devices consist of trench-gate quasi-vertical metal–oxide–semiconductor field-effect transistors (MOSFETs) with a 4 µm-thick drift layer, exhibiting enhancement-mode (E-mode) operation with a threshold voltage of 6.3 V and an on/off ratio of over 10^8. A high off-state breakdown voltage of 645 V along with a specific on-resistance of 6.8 mΩ·cm^2 were achieved thanks to the high-quality 4 µm-thick GaN drift layer presenting a relatively low defect density and very high electron mobility (720 cm^2/V·s). This excellent performance represents a major step towards the realization of high-performance GaN vertical power transistors on low-cost silicon substrates.**

***Index Terms* – Gallium nitride, vertical transistors, GaN-on-Si, power, semiconductor, devices, MOSFETs.**

I. Introduction

Wide-bandgap III-nitride semiconductors have a great potential for the next generation of efficient and compact power systems. To date, the majority of the research has been directed towards lateral high electron mobility transistors (HEMTs) based on an AlGaN/GaN heterostructure [1]-[3]. This is due to the advantages offered by the high-density and high-mobility two-dimensional electron gas (2DEG) induced at the hetero-interface, which allow high-voltage devices with large switching speeds and reduced on-resistances. However, for high-voltage and high-current applications (over 1.2 kV/100 A), the lateral topology presents limitations in scalability to reach large chip areas with high breakdown at the desired high operating current level [4]. With a vertical topology, the implementation of high voltage chips is possible by increasing the thickness of the drift region, without sacrificing the device size. In contrast to lateral devices, vertical GaN MOSFETs are less sensitive to surface traps states, which can reduce the degradation in dynamic on-resistance and mitigate current collapse issues. In addition, vertical MOSFETs can display normally-off operation, which is an important feature for power switching applications [5]-[7]. Rapid progress has been reported for high-performance vertical GaN transistors grown on n-type GaN substrates [8]-[20], mainly attributed to the capability of growing thick drift layers and the

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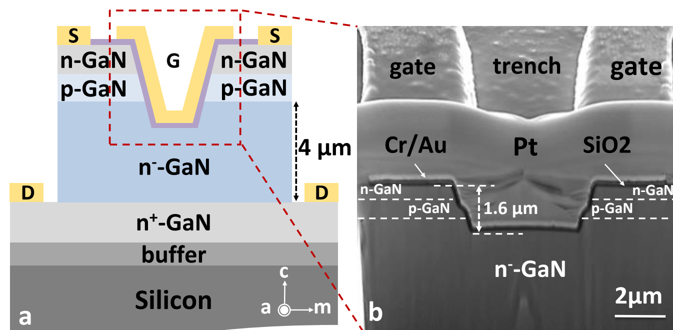

Fig. 1. Cross-sectional (a) schematic, and (b) SEM image of the fabricated quasi-vertical trench gate MOSFETs on Si substrate.

flexibility to form electrodes on the top and bottom of the devices. However, the high cost and availability of only small-size bulk GaN substrates limit their use for mass production. The GaN-on-Si platform offers a cost-effective alternative for vertical GaN MOSFETs, due to its low cost, large-scale availability, and a mature fabrication technology, including for substrate removal.

In recent years, GaN-on-Si technology has been developed extensively for several different areas, such as high-brightness light emitting diodes [21], high-power lateral HEMTs [2], [3], [22] and high-power vertical diodes [23]-[28]. However, there have been no reports up-to-date on GaN-on-Si vertical transistors, due to the challenge in obtaining high-quality n-p-n GaN heterostructures on silicon substrates. On one hand, the doping profile needs to be carefully engineered for abrupt heterojunctions; and on the other hand, a thick and continuous GaN drift layer with high electron mobility and low defect density is highly desired for low on-resistance and large breakdown voltage. This is especially challenging on silicon substrates considering the large mismatch between GaN and Si, both in lattice constant and thermal expansion coefficient.

In this work, we demonstrate the first GaN-on-Si vertical transistors fabricated on a 6.7 µm-thick n-p-n heterostructure grown on 6-inch silicon substrates. This structure contained a 4 µm-thick GaN drift layer, with a dopant concentration of 2×10^{16} cm^{-3}. With an optimized buffer and doping profile, the lateral electron mobility in the drift layer was as high as 720 cm^2/V·s. To the best of our knowledge, this is the highest electron mobility in vertical GaN on Si. The fabricated vertical trench MOSFETs exhibited E-mode operation with a threshold voltage (V_{th}) of 6.3 V and an on/off ratio of over 10^8. A specific on-resistance of 6.8 mΩ·cm^2 and a high off-state breakdown voltage of 645 V were achieved. This excellent performance shows the great potential of GaN-on-Si to serve as a platform for future power electronic applications.

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II. Device Structure and Fabrication

Fig. 1 (a) depicts a cross-sectional schematic of the fabricated quasi-vertical trench gate MOSFETs, in which the gate trench is aligned along the a-axis. The n-p-n heterostructure used in this work was grown on 6-inch Si (111) substrates by metal organic chemical vapor deposition (MOCVD). From bottom to top, the n-p-n structure consisted of a 1.1 μm-thick buffer layer, a 1 μm-thick n-type GaN layer (Si: ~ 1×10^{19} cm^{-3}), a 4 μm-thick n-type GaN layer (Si: ~ 2×10^{16} cm^{-3}), a 350 nm-thick p-type GaN layer (Mg: ~ 4×10^{19} cm^{-3}), a 200 nm-thick n-type GaN layer (Si: ~ 5×10^{18} cm^{-3}), and a 20 nm-thick n-type GaN layer (Si: ~ 1×10^{19} cm^{-3}). The x-ray diffraction (XRD) omega-rocking curves showed a small full width at half-maximum (FWHM) value of 235 arcsec and 307 arcsec near the GaN (002) and (102) reflections, respectively. For the growth of thick, continuous GaN on Si with low threading dislocation density, high quality buffer layers are important, especially the AlN nucleation layer. AlN buffer on Si with high crystalline quality ($FWHM_{(002)}$ < 1000 arcsec) and smooth surface was obtained by optimizing the AlN growth technology. With the high-quality AlN buffer layers, thick GaN on Si was grown without relaxation of the compressive stress during growth, which is important for compensating the tensile stress during cooling down. The value for wafer bowing after growth was X~-57 μm, Y~-45 μm. The lateral mobility of the n-type GaN drift layer was 720 $cm^2/V\cdot s$ for a Si dopant concentration of 2×10^{16} cm^{-3}, measured with a Hall system on n-GaN/i-GaN/buffer/Si.

The device fabrication started with a plasma-based dry etching process of GaN using $Cl_2/BCl_3/Ar$ with SiO_2 hard mask to form the trench structures with a depth of 1.6 μm for the vertical gate. The sample was then treated with a 5% Tetra Methyl Ammonium Hydroxide (TMAH) solution at 85°C for 60 minutes. The TMAH wet etch was found effective in removing the damages from dry-etched GaN sidewalls [29], [30]. To activate the buried p-type GaN, a rapid thermal annealing (RTA) was performed at 850°C for 20 min in a N_2 ambient. Subsequently, a 100 nm-thick SiO_2 gate dielectric for the vertical MOSFETs was deposited on the top surface and trenches by atomic layer deposition (ALD). After opening contact holes by reactive ion etching (RIE), a double-layer metal stack of Cr/Au was evaporated to form both the source and gate electrodes for the vertical MOSFETs. Finally, a 5 μm-deep etching was performed using a BCl_3/Cl_2-based inductively coupled plasma (ICP) etch, followed by the evaporation of Cr/Au drain electrodes.

Fig. 1 (b) shows the cross-sectional image of the quasi-vertical MOSFETs taken by focused ion beam-scanning electron microscope (FIB-SEM), in which a 3 μm-thick Pt was deposited at the gate region for surface protection. The depth in the etched trench was 1.6 μm, reaching the drift layer, and the trench sidewalls were inclined by 13.2° from the *c*-axis. The trench width was 4.0 μm and 5.5 μm at the bottom and the top, respectively. The angle of the trench sidewall can be improved with optimized dry etching conditions and further smoothened with longer TMAH treatment [29]-[31]. The small kink observed at the middle of the sidewall might be due to erosion of the SiO_2 hard mask edge during dry etching [30].

III. Results and Discussion

The transfer characteristics of the vertical trench MOSFETs in Fig. 2 (a) show a current on/off ratio of over 10^8 and a sub-threshold slope of 250 mV/dec. The low off-state leakage current level, below 10^{-8} kA/cm^2, reveals the effective current blocking by the n-p-n heterostructure in off state. The slight increase in gate leakage from 1.2×10^{-9} kA/cm^2 at $V_{GS} = 0$ V to 2.5×10^{-6} kA/cm^2 at $V_{GS} = 15$ V can be further reduced by optimizing the trench fabrication and the gate dielectric.

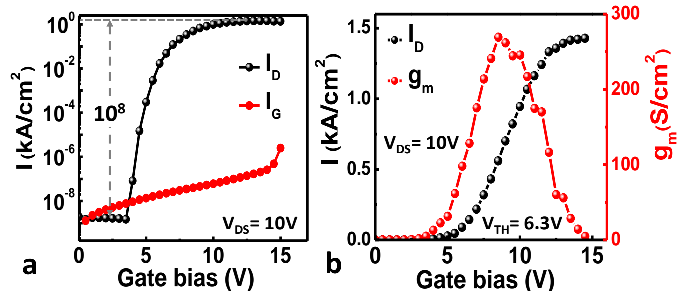

Fig. 2. (a) Semi-log, and (b) linear-scale transfer characteristics of the vertical trench gate MOSFETs on silicon substrate.

Fig. 2 (b) shows normally-off operation with a threshold voltage of 6.3 V (obtained by linear extrapolation) and peak transconductance of 269 S/cm^2. The high V_{th} is preferable for high-power applications to guarantee a safe operation and better noise immunity. The channel mobility (μ_{ch}) extracted using the equation from Ref. [8] in the liner region was 17.8 $cm^2/(V\cdot s)$, which is comparable to the value in Ref. [11] but lower than those from Refs. [8] and [9] (this value is underestimated due to additional series resistance induced by the thick drift layer (4 μm) [32]). The lower μ_{ch} is likely due to the typically larger defect density of GaN on silicon compared to that on bulk GaN substrates. In addition, μ_{ch} can be enhanced by improving the sidewall smoothness with an optimized TMAH treatment process [29], [30].

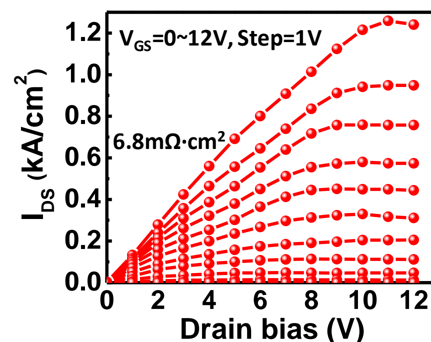

Fig. 3. Output I-V characteristics of the fabricated vertical trench gate MOSFETs on silicon substrate.

The output characteristic (I_D-V_{DS}) normalized by the trench area (Ref. [33]) is shown in Fig. 3. Good saturation behavior and an on-state current of ~ 1.3 kA/cm^2 were observed at V_{GS} = 12 V and V_{DS} = 11 V. The specific on-resistance ($R_{ON,SP}$) estimated from the linear region was 6.8 $m\Omega\cdot cm^2$. The calculated resistivity of each individual layer was 1.28×10^{-6} $m\Omega\cdot cm^2$, 3.78×10^{-6} $m\Omega\cdot cm^2$, 1.77×10^{-3} $m\Omega\cdot cm^2$ for the source, drain, and drift layers, respectively (the contribution from

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contact resistances in vertical devices can be neglected [34]). These values are much smaller than the measured $R_{ON,SP}$, suggesting that the p-GaN channel layer and the spreading resistance in the drift region [35] are the main factor for the on-resistance. The larger channel resistivity is mainly due to our poorer channel mobility of 17.8 $cm^2/(V\cdot s)$, compared to 131 $cm^2/(V\cdot s)$ in Ref. [9].

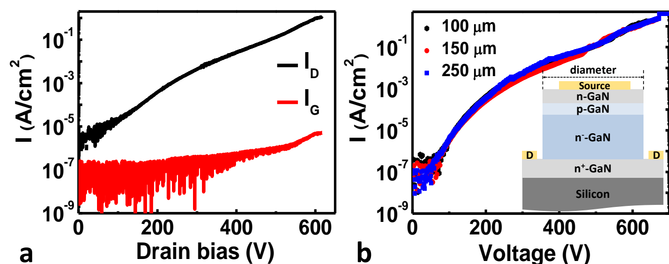

Fig. 4. (a) Off-state I-V characteristics measured at V_{GS} = 0 V for the fabricated trench gate MOSFETs on silicon substrate, and (b) two terminal I-V characteristics of the as-grown n-p-n structure. The inset shows the schematic view of the measured n-p-n structure.

Fig. 4 (a) shows the off-state I-V characteristics measured at V_{GS} = 0 V for the fabricated trench gate MOSFET with floating substrate. The vertical MOSFETs exhibited a large hard breakdown voltage (V_{Boff}) of 645 V, while the gate current remained at a low value below 10^{-5} A/cm², indicating that the breakdown occurred mainly between the source and drain terminals. The observed breakdown was destructive and mainly happened at the mesa edges. By introducing field-plates and edge-termination technologies to these devices, the electric field at the junction edge could be reduced, which would further enhance their breakdown voltage. However, the performance observed even without edge termination is quite remarkable which reveals the enormous potential for GaN on Si vertical transistors.

The measured V_{Boff} was consistent with the vertical breakdown voltage measured from two-terminal circular n-p-n test structures of 679 V (Fig. 4 (b)). The similar leakage current density observed from these test structures with different mesa diameters (100 µm, 150 µm, and 250 µm), shown in Fig. 4 (b), indicates that the device leakage current mainly flows through the heterostructure, instead of the etched sidewalls [30]. The relation between leakage current density (I) and the average electric field (E) in the drift layer reveals the off-state leakage mechanism [36]. The nearly linear dependence of $\ln(I) \propto E$ (extracted from Fig. 4 (a)) for the vertical MOSFETs indicates that the dominant leakage mechanisms in our devices is variable-range hopping [37].

Fig. 5 shows the performance of our vertical trench gate MOSFETs on silicon substrates benchmarked against state-of-the-art E-mode vertical transistors on sapphire and GaN substrates [7], [12]-[20]. The V_{Boff} of 645 V and $R_{ON,SP}$ of 6.8 mΩ·cm² resulted in a very good Baliga figure-of-merit (FOM) of 61 MW/cm², which is superior than devices fabricated on sapphire substrates. The FOM of these GaN-on-Si vertical MOSFETs can be significantly improved: 1. By utilizing TMAH treatment in the trenches with higher TMAH concentrations and longer durations to reduce $R_{ON,SP}$; 2. By designing field plates and edge terminations to enhance the V_{Boff}; 3. By substrate removal, as a fully vertical transistor would significantly reduce current crowding in the bottom n-GaN layer towards the drain contact, thus reducing $R_{ON,SP}$;

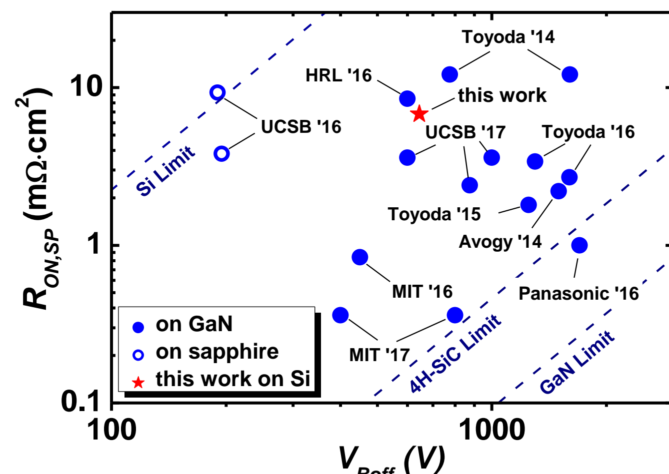

Fig. 5. $R_{ON,SP}$ versus V_{Boff} benchmarks of the vertical trench gate MOSFETs on silicon substrates with state-of-the-art E-mode vertical transistors on sapphire and GaN substrates.

IV. Conclusion

In summary, we have successfully demonstrated the first GaN vertical trench gate MOSFETs on 6-inch silicon substrates with a blocking voltage of 645 V. Normally-off operation was achieved with a threshold voltage of 6.3 V and an on/off ratio of over 10^8. A specific on-resistance of 6.8 mΩ·cm² was obtained. These results are very promising for the future adoption of GaN-on-Si for cost-effective high-voltage and high-power electronic applications.

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