2019

GaN Power Devices: Discerning Application-Specific Challenges and Limitations in HEMTs

Andrew Binder
University of Central Florida

GAN POWER DEVICES: DISCERNING APPLICATION-SPECIFIC CHALLENGES AND LIMITATIONS IN HEMTS

by

ANDREW BINDER

B.S. University of Arkansas, 2013

A dissertation submitted in partial fulfilment of the requirements
for the degree of Doctor of Philosophy
in the Department of Electrical Engineering and Computer Science
in the College of Engineering and Computer Science
at the University of Central Florida
Orlando, Florida

Spring Term
2019

Major Professor: Jiann S. Yuan

ABSTRACT

GaN power devices are typically used in the 600 V market, for high efficiency, high power-density systems. For these devices, the lateral optimization of gate-to-drain, gate, and gate-to-source lengths, as well as gate field-plate length are critical for optimizing breakdown voltage and performance. This work presents a systematic study of lateral scaling optimization for high voltage devices to minimize figure of merit and maximize breakdown voltage. In addition, this optimization is extended for low voltage devices ($<$ 100 V), presenting results to optimize both lateral features and vertical features. For low voltage design, simulation work suggests that breakdown is more reliant on punch-through as the primary breakdown mechanism rather than on vertical leakage current as is the case with high-voltage devices. A fabrication process flow has been developed for fabricating Schottky-gate, and MIS-HEMT structures at UCF in the CREOL cleanroom. The fabricated devices were designed to validate the simulation work for low voltage GaN devices. The UCF fabrication process is done with a four layer mask, and consists of mesa isolation, ohmic recess etch, an optional gate insulator layer, ohmic metallization, and gate metallization. Following this work, the fabrication process was transferred to the National Nano Device Laboratories (NDL) in Hsinchu, Taiwan, to take advantage of the more advanced facilities there. Following fabrication, a study has been performed on defect induced performance degradation, leading to the observation of a new phenomenon: trap induced negative differential conductance (NDC). Typically NDC is caused by self-heating, however by implementing a substrate bias test in conjunction with pulsed I-V testing, the NDC seen in our fabricated devices has been confirmed to be from buffer traps that are a result of poor channel carrier confinement during the dc operating condition.

ACKNOWLEDGMENTS

First, I would like to express thanks to my research advisor, Professor Jiann S. Yuan, whose guidance, support, and expert technical advice has made all this work possible. Professor Yuan has been an excellent advisor to me; he has given me incredible opportunities during my graduate studies, and provided essential lab resources and software tools to conduct the research work. I am deeply grateful for his guidance and support.

I would like to thank the members of my dissertation committee, Dr. Kalpathy Sundaram, Dr. Vikram Kapoor, Dr. Tania Roy, and Dr. Lee Chow for the assistance they provided and their time in evaluating my dissertation and providing valuable feedback. In addition I would like to thank Dr. Sundaram for his guidance and the opportunities he has given me along the way.

I am incredibly grateful to my industry mentors Dr. Patrick Shea and Dr. Balakrishnan Krishnan for their guidance on my projects and the professional advice they have given me. They have invested considerable time both in my academic and professional development; their profound knowledge on semiconductor devices and fabrication has been instrumental during the course of my research.

I am grateful to all my colleagues: Qutaiba Hasan, Aiman Salih, Wen Yang, Safayat Shochib, Sakeenah Khan, Jie Lin, and Shayan Taheri. Qutaiba has been a great friend with which I have had many great conversations and good laughs. I would like to thank my colleagues working on semiconductor devices, Wen, Aiman, Sakeenah, and Safayat, for the discussions and help in my research.

Lastly, I would like to thank my family, especially my wife Laura for her support, all the late night meals, and for her empathy and encouragement through the years. My parents have my deepest gratitude for their direction and guidance throughout my life.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

The power electronics industry is driven by device miniaturization and system power density improvements, both of which are enabled by wide bandgap (WBG) device technology. When evaluating WBG technology, Gallium Nitride (GaN) heterojunction devices have superior material characteristics compared to Silicon Carbide (SiC) devices: although both enable higher operating frequency and higher voltage operation than silicon-based electronics [1]. According to a market report by P&S Market Research [2], GaN is expected to be the major wide bandgap competitor for silicon for device ratings less than 600 V. This is due in part to the miniaturization enabled by wide bandgap technology, and also due to the higher performance and lower figure of merit ($R_{DS(on)} \times Q_G$) of GaN devices compared to silicon. Despite these advantages, GaN devices still have extensive hurdles to overcome before they can replace silicon: chiefly including a comparative manufacturing cost and significant long-term reliability concerns.

This chapter presents an overview of GaN materials advantages, heterostructure design, a synopsis of modern device structures, and introduces some prominent failure mechanisms for GaN HEMTs. In addition, an outline of this work is presented at the end of the chapter.

1.1 GaN Overview and Materials Advantages

As mentioned, compared to silicon, GaN has superior material characteristics which allow for higher frequency operation, and higher breakdown voltage. This is due to reduced switching loss from the higher mobility and saturation velocity, and reduced conduction

losses since the device length can be reduced for the same given breakdown voltage due to a higher critical electric field. Figure 1.1 presents an overview of the merits of using GaN compared to silicon with the graph normalized to the properties of GaN to show scale.

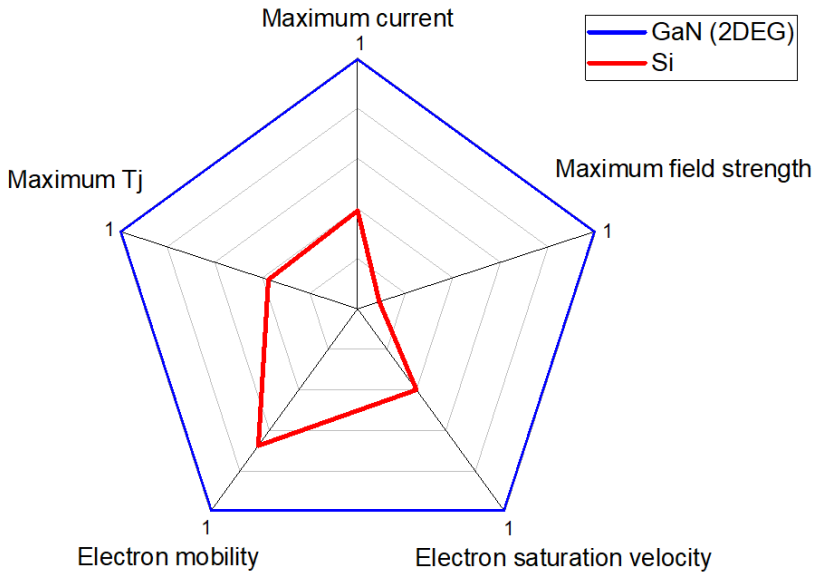


Figure 1.1: Merits of using GaN compared to silicon from a materials perspective.

The channel in AlGaN/GaN devices is composed of a two dimensional electron gas (2DEG) which is created by spontaneous and piezoelectric polarization due to lattice mismatch between the two respective layers. This 2DEG has a higher mobility than that of bulk GaN. Compared to silicon devices in which the channel is formed by doping a region, in GaN the channel is naturally formed and requires no doping. This means there is no impact on carrier mobility and velocity due to impurity scattering resulting from doping: leading to a very high channel electron mobility.

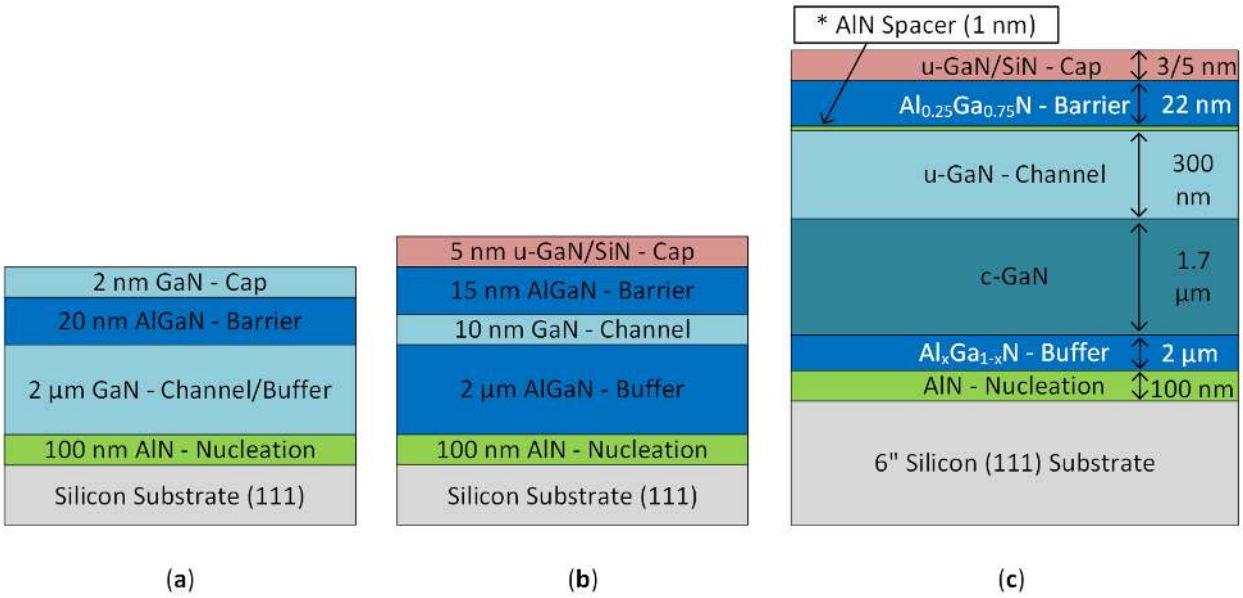


Figure 1.2: GaN heterostructure types showing (a) the single heterostructure (AlGaN/GaN), (b) the double heterostructure (AlGaN/GaN/AlGaN), and (c) an advanced double heterostructure design.

1.2 Heterostructure Design

Lateral GaN transistors require a multi-layer heterostructure design which is highly dependent on the starting wafer used for growth. GaN is most commonly grown on silicon but also can be grown on silicon carbide or sapphire. Due to the lack of availability, the high cost, and small wafer size, GaN wafers are very rarely used in GaN processing, especially for lateral transistors. GaN is most commonly grown by metal organic chemical vapor deposition (MOCVD). Concerning heterostructure design, a standard baseline structure is shown in Figure 1.2(a); this structure is typical for GaN-on-Si wafers. Silicon substrates give cost and availability advantages compared to SiC or sapphire substrates, although GaN-on-silicon has a larger lattice mismatch compared to SiC or sapphire. The large lattice mismatch will cause poor quality GaN growth on Si, so to facilitate better bonding, a nucleation (seed) layer is needed. For GaN-on-Si wafers, AlN is typically used as the

nucleation layer. On top of the nucleation layer, the channel/buffer region is grown, with a typical defect density of 10^9 cm^{-3}. The interface between the channel and barrier layer is where the 2DEG forms, which lies on the channel side of the interface.

Concerning heterostructure design, Figure 1.2(b) depicts a double heterostructure (AlGaN/GaN/AlGaN). The double heterostructure results in better breakdown voltage and on-state resistance performance compared to the single heterostructure. This is due to improved channel carrier confinement, decreasing buffer leakage, and a higher critical electric field of the buffer layer which improves breakdown voltage.

Finally, there are some advanced structure design considerations which can result in improved reliability and performance (Figure 1.2(c)). Typically a carbon doped GaN layer is used below the channel region. Carbon doping makes the region more semi-insulating, which prevents current punch-through at high electric fields, and also helps to confine the 2DEG. A carbon doped ”back barrier” will improve breakdown voltage at the expense of increased dynamic on-state resistance. Doping with carbon creates trap sites in GaN, which can act as acceptor- or donor-like traps depending on whether carbon serves as an interstitial for gallium or nitrogen in the GaN lattice. These traps can lead to current collapse and will adversely impact reliability and breakdown performance. Carbon doping can be done by modifying the temperature of the growth process, where a low temperature process results in more carbon in the GaN lattice, and a high temperature process results in better quality GaN with less carbon.

In addition to carbon doping, another way to improve electrical characteristics is to add an AlN spacer between the AlGaN barrier and GaN channel. The AlN interlayer will increase electron density in the channel, and can improve interface roughness, leading to an increase in mobility. The thickness of the AlN interlayer is critical however, as a thick layer can cause structural degradation due to partial strain relaxation.

Lastly, a superlattice buffer can be used to reduce defect and mismatch compared to a typical graded AlGaN buffer structure. These layers are intended for stress relief, which also can improve passivation adhesion, resulting in fewer surface states. The trade-off for a superlattice buffer is a reduced thermal performance compared to a graded buffer structure.

1.3 Device Structures

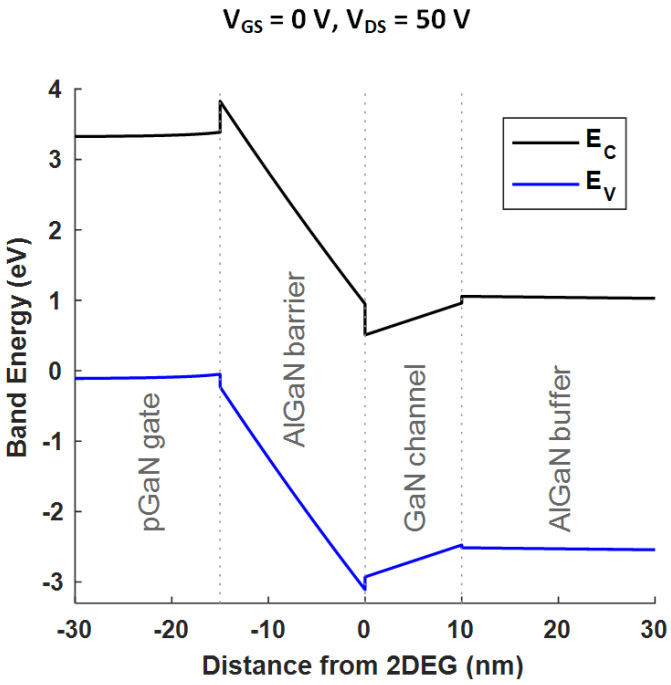


Figure 1.3: Energy band diagram for an enhancement-mode AlGaN/GaN HEMT.

AlGaN/GaN devices are naturally depletion-mode, meaning they are normally on devices. These devices require structure changes to make them enhancement-mode, or normally off devices. For power electronics, it is necessary to use enhancement-mode devices so that if there is a circuit failure the system will fail in the off-state rather than in the on-state which can be dangerous and destructive when under load. An enhancement-mode device has a band diagram like the one seen in Figure 1.3, where the 2DEG quantum-well formed

at the barrier/channel interface is above the Fermi level, and thus depleted. In this section we will discuss enhancement-mode structures, and present some more modern device structures used in GaN power device design.

1.3.1 Enhancement-Mode Structures

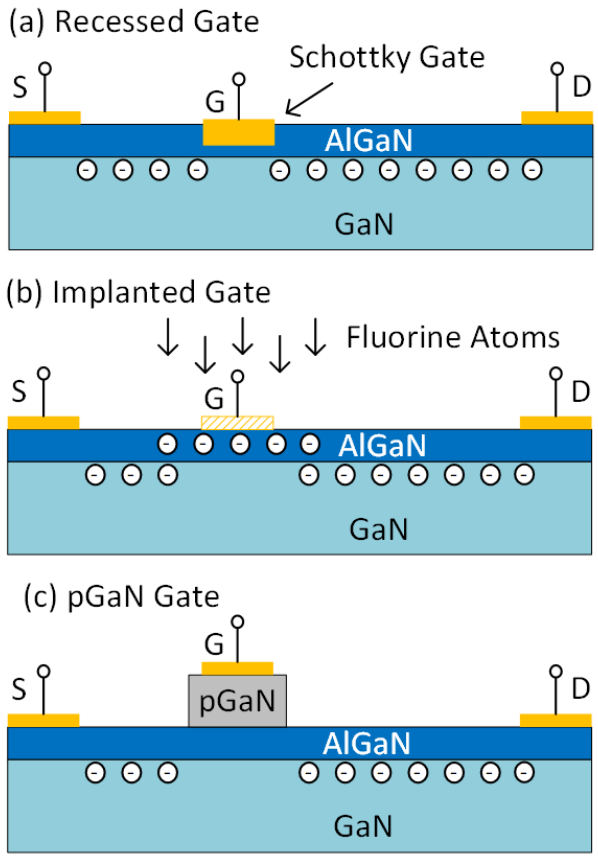


Figure 1.4: Enhancement-mode structures for AlGaN/GaN devices showing (a) recessed gate, (b) implanted gate, and (c) pGaN gate technologies.

There are three common techniques for create an enhancement-mode device: recessed gate, implanted gate, and pGaN gate. These structures are shown in Figure 1.4. The pGaN gate enhancement-mode structure is by far the most common of the three. From a fabrication perspective it is the most reliable, as recess gate has threshold voltage instability

issues and implanted gate can contribute to trapping issues leading to reliability concerns. However, pGaN gate devices suffer from more gate leakage than recessed or implanted gate structures.

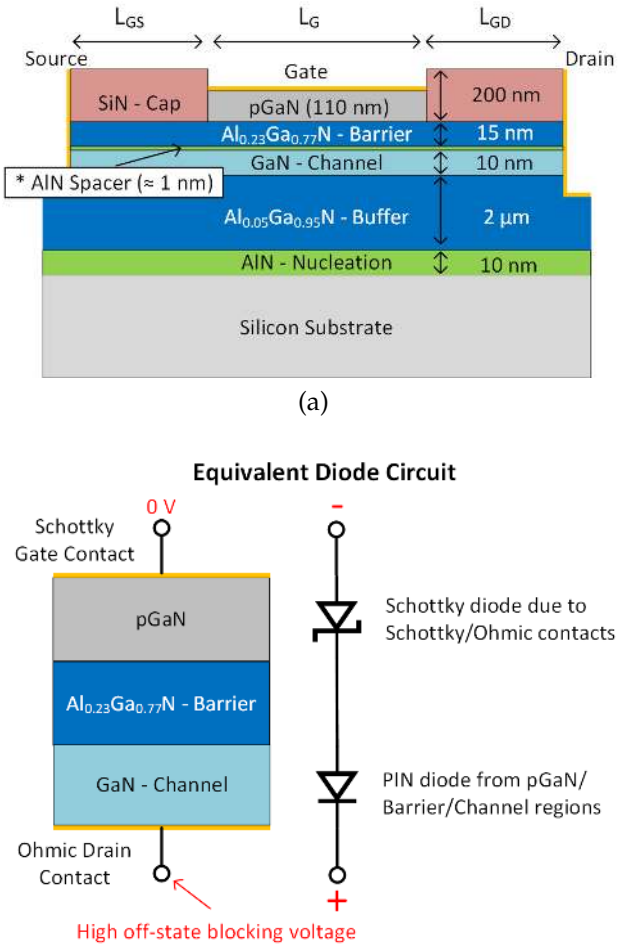


Figure 1.5: (a) Device structure for a pGaN gate HEMT and (b) equivalent circuit model of series diodes for off-state operation.

In the pGaN gate structure (shown in Figure 1.5(a)), a p-doped GaN layer is grown on top of the AlGaN barrier which serves to deplete the channel under the gate. This p-doped GaN layer along with the AlGaN barrier and GaN channel together forms a *pin*-diode, which can add about 10 µA/mm of gate current. Replacing the ohmic gate contact with a Schottky contact will significantly reduce the on-state gate current as the Schottky-diode

is now in series with the *pin*-diode (Figure 1.5(b)), thereby increasing the diode forward voltage and reducing the gate current. The Schottky-gate pGaN HEMT is a popular method for achieving low off-state leakage currents and normally-off operation. A combination of gate recess and pGaN (or pAlGaN) doping can be used to further improve threshold voltage.

1.3.2 Modern Device Structures

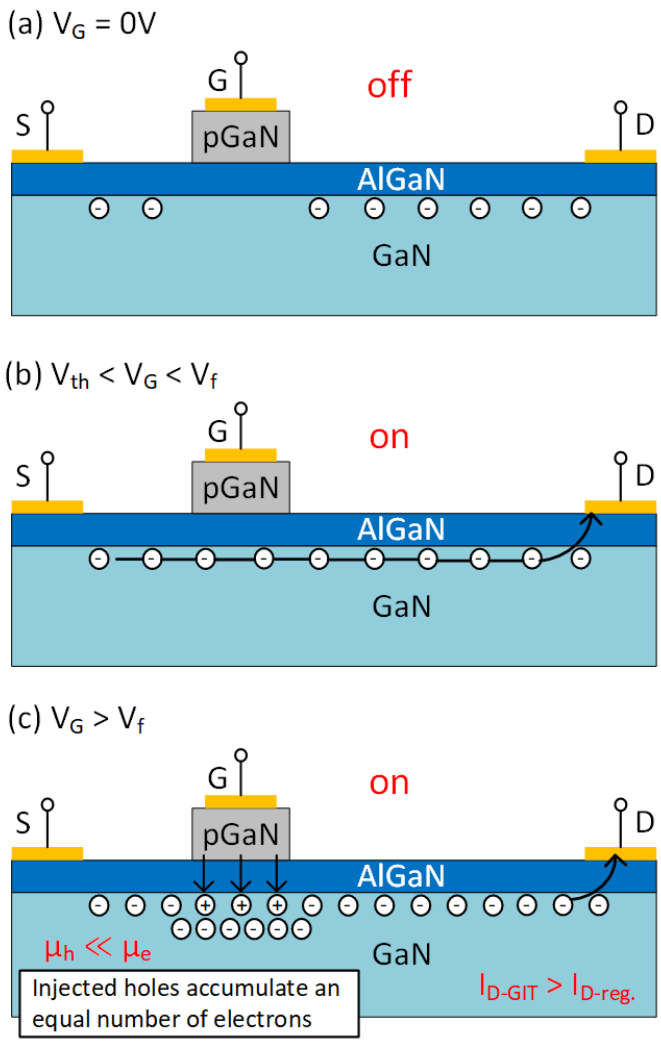


Figure 1.6: Gate injection transistor (GIT) operating with (a) zero gate voltage, (b) in the on-state but below the forward voltage, and (c) in the on-state in injection condition.

Two spin-offs of the pGaN gate structure are the gate injection transistor (GIT) and the hybrid-drain gate injection transistor (HD-GIT). Both build on the principles of pGaN gate operation, but provide unique advantages to aid in device operation and reliability. The gate injection transistor (Figure 1.6) provides the benefit of conductivity modulation (higher I_{DS}), but comes at the cost of a larger gate current compared to the conventional pGaN gate device. The GIT has three modes of operation: the off-state at $V_G = 0V$, the on-state at $V_{th} < V_G < V_f$, and the injection state at $V_G > V_f$. In the off-state and on-state, the device operates just as a conventional pGaN gated device. However, if the gate voltage exceeds the series diodes forward voltage the gate will inject holes into the device. Due to charge neutrality, the injected holes accumulate an equal number of electrons in the channel, which increases I_{DS}. The accumulated electrons increase current density, but the injected holes mostly stay around the gate area and do not significantly contribute to the drain current. This is due to a large mobility imbalance between holes and electrons: hole mobility is at least two orders of magnitude lower than electron mobility.

The HD-GIT is designed to eliminate current collapse by adding an additional pGaN region near the drain. This hybrid drain serves to inject holes under the drain in the off-state condition with a high drain bias, effectively releasing trapped electrons during the process of switching. This solves the current collapse issue and can be used for high voltage (600V) devices. One drawback of this approach is that it uses both pGaN gate and gate recess technology to make the device enhancement-mode. For the HD-GIT structure, the AlGaN barrier layer needs to be roughly twice as thick compared to a normal pGaN gate structure. This is so that the pGaN hybrid drain does not deplete the channel and act as a second gate. From a fabrication perspective this complicates things, as it requires etching and regrowth of a pGaN layer, and it also introduces possible threshold voltage variation issues as are seen with gate recess devices. The HD-GIT structure can be seen in Figure 1.7.

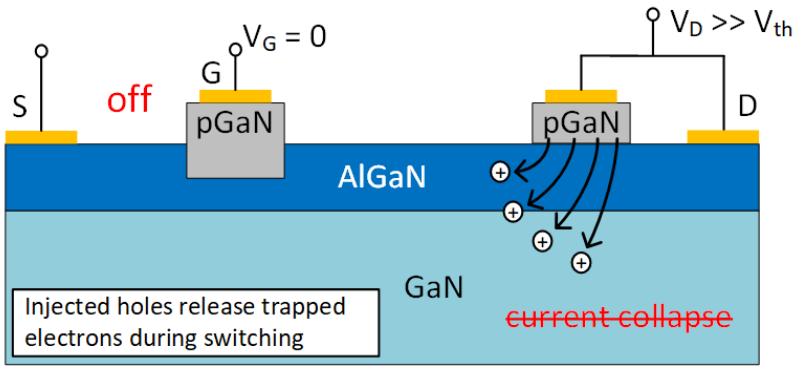


Figure 1.7: HD-GIT device operating in the off-state.

1.4 Failure Mechanisms

As a significant portion of this work covers device optimization in regards to performance and breakdown, it is prudent to cover some prominent failure mechanisms in the introduction. GaN devices primarily suffer from a few dominant failure mechanisms, although each of these mechanisms may contribute to other failure modes. Failure mechanisms can be isolated by the dominant leakage current path: whether gate-leakage, drain- or source-leakage, or substrate-leakage. This leakage can be due to punch-through, impact ionization, gate leakage, or vertical leakage paths within the device. These failure mechanisms are depicted in Figure 1.8(a). To evaluate the source of the failure mechanisms the leakage current can be examined, and the dominate leakage path can point towards impact ionization, punch-though, or vertical leakage current depending on the source. An example of this is given in Figure 1.8(b).

Vertical leakage current is due to breakdown at the silicon substrate, as silicon has a much lower critical electric field than GaN. This can be avoided by proper buffer thickness optimization. This tends to be a dominant breakdown factor for high voltage devices, thus buffer thickness is a critical factor to high voltage design.

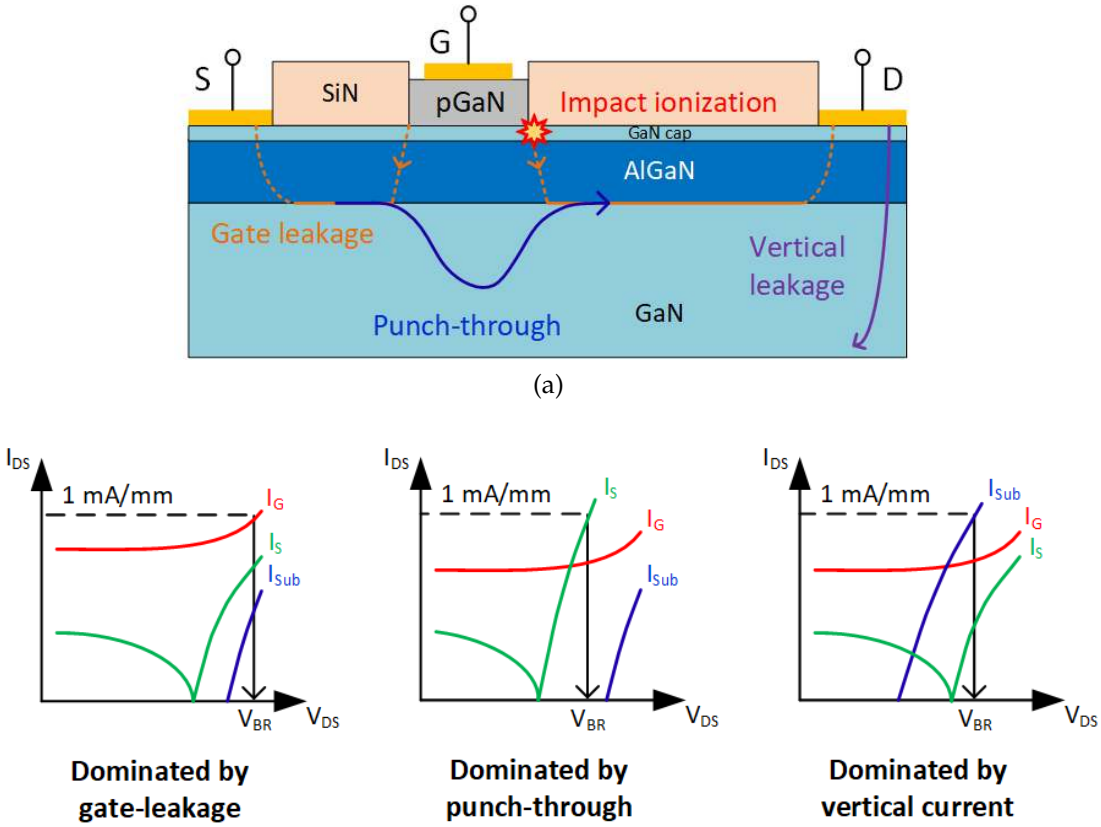
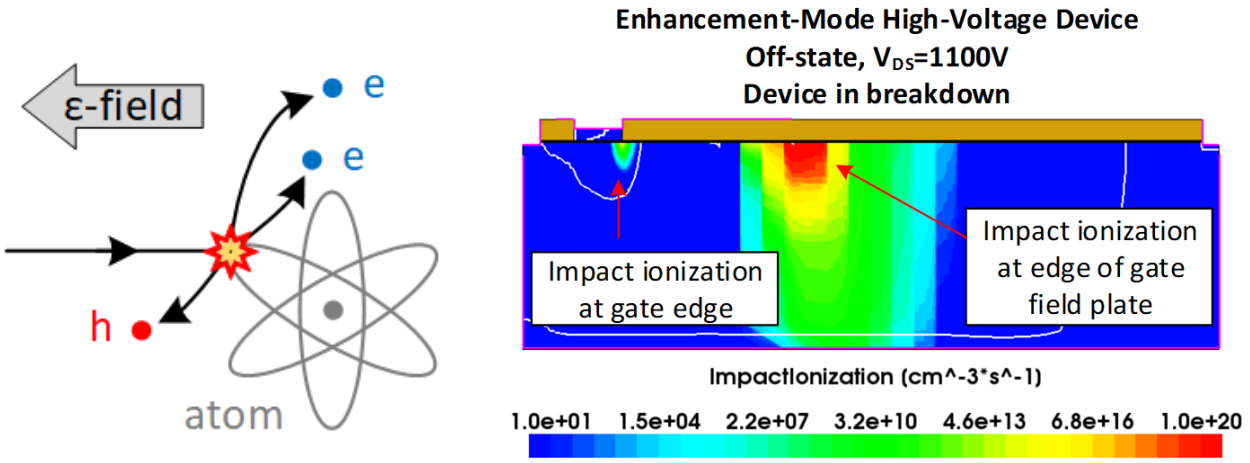


Figure 1.8: (a) Failure mechanisms in GaN HEMTs and (b) leakage current evaluation of breakdown mechanisms.

Punch-through occurs in off-state at a high drain bias, where electrons travel through the bulk underneath the turned-off gate and "punch-though" what should be a depleted region below the gate. This buffer leakage current can be a large contributor to off-state I_{DS}. Solutions to reduce punch-through include increasing the gate length, making the buffer more semi-insulating (e.g. carbon doping), or reducing the trap density in the buffer. This issue will be discussed in more detail in Chapter 3.

Impact ionization occurs at the drain-side gate edge, or at the edge of the gate-field-plate. A high electric field causes high-energy electrons to knock other electrons out of the valence band into the conduction band: creating electron-hole pairs and raising the

current (depicted in Figure 1.9(a)). This may continue to avalanche condition, resulting in unrecoverable breakdown. To reduce impaction ionization, electric-field peaks and hotspots must be reduced. This can be done by multiple field-plate structures. An example of impact ionization occurring in a high-voltage device is shown in Figure 1.9(b).



(a) (b)

Figure 1.9: (a) Simplified impact ionization model and (b) impact ionization occurring in a high voltage device.

1.5 Dissertation Organization

The outline of this work is as follows:

Chapter 2 covers lateral optimization trends for high voltage ($>$ 600V) GaN HEMTs. Drift length and length of the gate field plate are scaled to exhibit the influence of these terms on the on-state resistance, gate charge, and breakdown voltage. Novelty of this study comes from a comprehensive look at drift length and field plate optimization for high voltage and low figure of merit designs. This optimization maps out $R_{DS(on)}$ and Q_G to suggest designs which optimize

conduction losses versus switching losses for specificity in power electronics system design.

Chapter 3 presents a fabless design approach for lateral optimization of low voltage GaN power HEMTs. This optimization covers lateral scaling terms including gate-to-drain, gate, and gate-to-source lengths to minimize figure of merit for a target breakdown voltage. Low voltage design optimization showed heavy influence of buffer trap density and thickness on breakdown performance.

Chapter 4 gives insight into heterostructure design and the impact on performance for low voltage GaN power HEMTs. Low voltage simulations reveal less dependence on vertical leakage current and substrate breakdown compared to high voltage designs, and more reliance on buffer leakage and punch-through as the dominant factors leading to breakdown. Optimization curves are presented for breakdown voltage, on-state resistance, and gate charge. Trends are presented for the optimization of the channel layer thickness, barrier layer thickness and molar fraction, impact of an AlN interlayer, and optimization of buffer layer thickness.

Chapter 5 covers the fabrication strategy for Schottky-gate and MIS-HEMT device fabrication in the UCF CREOL cleanroom. This chapter also covers the fabrication effort through collaboration at the National Nano Device Laboratories in Hsinchu, Taiwan.

Chapter 6 introduces a new phenomenon discovered during testing of our fabricated devices: trap induced negative differential conductance. Negative differential conductance (NDC) seen in the drain current saturation region is typically attributed to selfheating effects in GaN HEMTs. In this chapter, it is demonstrated that NDC is due to trap states in the buffer resulting from poor carrier confinement in the channel during saturation which leads to stray electrons

exiting the channel and becoming trapped. Lastly, this chapter presents an overview of defect induced performance degradation.

Chapter 7 concludes the results obtained in this work, and presents an outlook for future work on GaN power HEMTs.

CHAPTER 2: LATERAL SCALING AND OPTIMIZATION FOR HIGH-VOLTAGE GAN HEMTS

GaN power devices are typically used in the 600 V market, for high efficiency, high power-density systems. For these devices, the lateral optimization of gate-to-drain, gate, and gate-to-source lengths, as well as gate field-plate length are critical for optimizing breakdown voltage and performance. This work presents a systematic study of lateral scaling optimization for high voltage devices to minimize figure of merit ($R_{DS(on)} \times Q_G$) and maximize breakdown voltage.

This chapter demonstrates the effects of lateral scaling on the figure of merit for a high-voltage pGaN, enhancement-mode HEMT. To this end, the drift length (L_{drift}) and the length of the gate field plate (L_{GFP}) have been scaled to exhibit the influence of these terms on the on-state resistance ($R_{DS(on)}$), gate charge (Q_G), and breakdown voltage (V_{BR}). Results conclude that for a given field plate length, the increase in breakdown voltage as L_{GD} increases, saturates when L_{GD} is greater than $L_{GD(sat)}$. For this design, with L_{GFP} at 5 μm, the saturation length $L_{GD(sat)}$ was 6 μm. Novelty of this study comes from a comprehensive look at drift length and field plate optimization for high voltage and low figure of merit designs, specifically for the enhancement-mode pGaN structure. Taking this optimization one step further, we have mapped out $R_{DS(on)}$ and Q_G to suggest designs which optimize conduction losses versus switching losses for specificity in power electronics system design.

A. Binder and J. S. Yuan, "*Optimization of an enhancement-mode AlGaN/GaN/AlGaN DHFET towards a high breakdown voltage and low figure of merit,*" in 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), 2017, pp. 122–126.

2.1 Introduction

Fueled by the desire for higher performance devices, designers have investigated various GaN device structures and methods to improve breakdown voltage, FOM, and reliability. Power electronics systems almost exclusively employ enhancement-mode (e-mode) devices; however, most studies have been conducted on the effects of employing a gate field plate on GaN depletion-mode (d-mode) devices. This is due to the relative ease of fabrication in comparison to E-mode devices. For this study we present a comprehensive look at FOM optimization and it is imperative not to limit these device studies to D-mode devices. Towards this end, we investigate the effect of drift length and field plate scaling on breakdown voltage and FOM for a pGaN, E-mode, double heterostructure field effect transistor (DHFET). The purpose of this work is to demonstrate how to optimize the lateral design of a pGaN HEMT towards a high breakdown voltage and low figure of merit. This is accomplished by showing how the drift length (L_{drift}) and length of the gate field plate (L_{GFP}) effect on-state resistance ($R_{DS(on)}$), gate charge (Q_G), and breakdown voltage (V_{BR}). The results of this work are an aid to device designers for the purpose of enabling application specific power electronics design.

2.2 Device Design and Simulation Model

2.2.1 Theoretical Analysis

For device modeling, it is well understood that increasing the drift length or length of the gate field plate results in an increase in breakdown voltage (eq. 2.1). The relationship between breakdown voltage and drift length holds true when $L_{GD} < L_{GD(sat)}$, a point at which increasing L_{GD} further no longer increases the breakdown voltage (as is well

detailed in [3]).

$$BV \propto L_{drift}, L_{GFP} \tag{2.1}$$

Since the focus of this paper is, in part, on examining device FOM variation as lateral dimensions scale, it is necessary to first understand the general relationship between $R_{DS(on)}$, Q_G, and the lateral dimensions at the center of this study, L_{drift} and L_{GFP}. The relationship between drift resistance and drift length is given by eq. 2.2 where the drift resistance is directly proportional to drift length, while R_{drift} remains independent from L_{GFP} (eq. 2.3). Finally, concerning gate charge, it should be noted that gate charge is directly proportional to the length of the gate field plate, but is independent from the drift length (eq. 2.4).

$$R_{drift} = \frac{L_{drift}}{q \cdot \mu_{drift} \cdot N_{drift}} \tag{2.2}$$

$$R_{drift} \propto L_{drift} \tag{2.3}$$

$$Q_G \propto L_{GFP} \tag{2.4}$$

2.2.2 Device Description

The cross section of the device as simulated, shown in Fig. 2.1, displays the vertical device dimensions. As mentioned, this study focuses on the lateral dimensions to optimize breakdown voltage and FOM. The simulated structure is an AlGaN/GaN/AlGaN double

heterostructure field effect transistor (DHFET) which results in better breakdown voltage and on-state resistance performance compared to the single heterostructure device [3]. This device is made enhancement-mode by the incorporation of the pGaN region above the AlGaN barrier and under the gate. Doping the GaN layer above the channel prevents the polarization of the AlGaN/GaN interface, which stops the channel from forming under the gate resulting in shifting the threshold voltage positive [4].

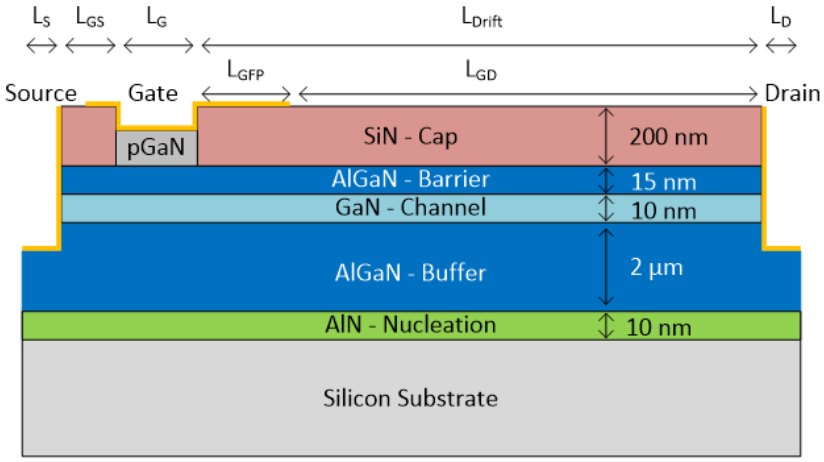


Figure 2.1: Cross-section representation of proposed AlGaN/GaN/AlGaN enhancement-mode DHFET with gate field plate.

For simulation purposes, the device cross-section excludes the silicon substrate as this layer does not affect the on-state resistance, gate charge, or electric field distribution near the surface. The effects of the inclusion or exclusion of the substrate on simulation results can be seen elsewhere in [5]. Simulations of the GaN HEMT were performed using Sentaurus TCAD (Synopsys) [6].

The basic lateral device dimensions for the following simulation trials are shown in Table 2.1 where L_{GFP} and L_{GD} are varied while all other parameters are held constant.

Table 2.1: Design Parameters for Lateral Layer Stack-Up.

Region	L_S	L_{GS}	L_G	L_{GFP}	L_{GD}	L_D
Thickness	0.5 µm	1 µm	1.4 µm	1-5 µm	1-20 µm	0.5 µm

2.3 Results and Discussion

It is generally understood that the breakdown voltage of a lateral FET is proportional to the drift length, however, as mentioned previously, it is also known that this relationship tends to saturate once the drift length is increased beyond a certain threshold [3]. For this simulated structure, when L_{GFP} is 5 µm, the correlation between breakdown voltage and L_{drift} disappears after L_{GD} increases beyond 6 µm as seen in Fig. 2.2. This phenomenon can be explained intuitively by looking at the electric field distribution within the device.

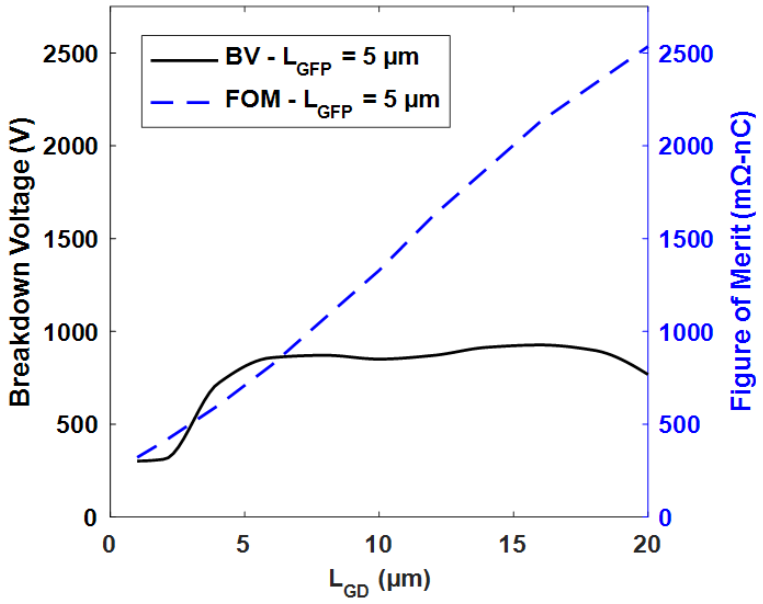


Figure 2.2: Breakdown voltage and FOM analysis for DHFET-based device at L_{GFP} = 5 µm.

This saturation of the breakdown voltage is in part due to the thickness of the buffer

region. Notice in Fig. 2.3 that the electric field distribution extends uniformly through the buffer region in a vertical fashion, rather than staying contained near the channel. When investigating breakdown at the substrate interface, considering the lower critical electric field of Si compared to GaN, increasing the buffer region thickness would also increase the breakdown limit, however there are ultimately limitations to how thick the buffer region can be grown [7]. Alternatively, considering breakdown to be due to leakage current in the buffer, using the space-charge-limited current (SCLC) conduction mechanism, a thinner buffer layer results in a higher breakdown voltage [8]. Both methods show a strong dependence of breakdown voltage on buffer layer thickness.

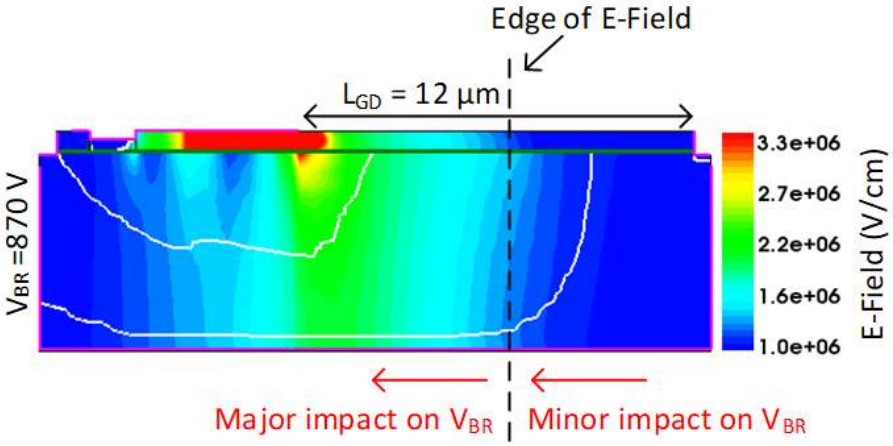


Figure 2.3: Electric field profiles of proposed DHFET with gate field plate for L_{GFP} = 5 µm.

From the electric field distribution plot, an intuitive understanding of how scaling L_{GD} affects V_{BR} can be obtained. For a given field plate length, the impact of scaling L_{GD} is broken down by dividing the device into two regions that are separated by the edge of the electric field as shown in Fig. 2.3. Scaling up to the edge of the E-field will have very little effect on V_{BR}; scaling beyond this will result in a significant reduction in breakdown voltage.

Looking at the cross-sectional plots for L_{GD} = 6, 4, and 2 µm we see the trend demonstrated (Fig. 2.4). At L_{GD} = 6 µm (the length corresponding to the edge of the E-field shown in

Fig. 2.3), the breakdown voltage is at a comparable level to before any scaling. As L_{GD} is reduced beyond the edge of the E-field, the breakdown voltage drops off sharply.

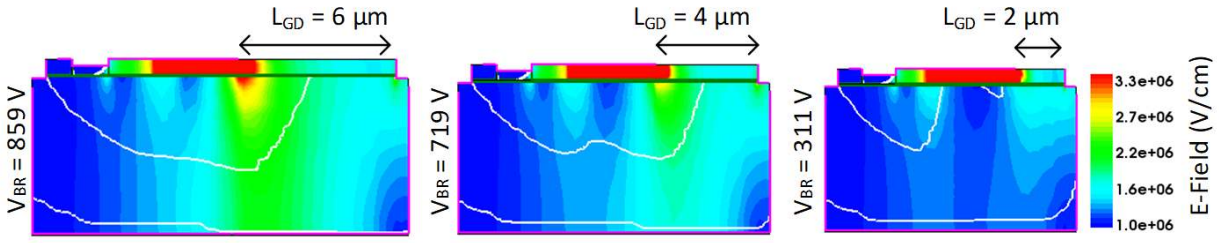


Figure 2.4: Electric field profiles as L_{GD} is reduced.

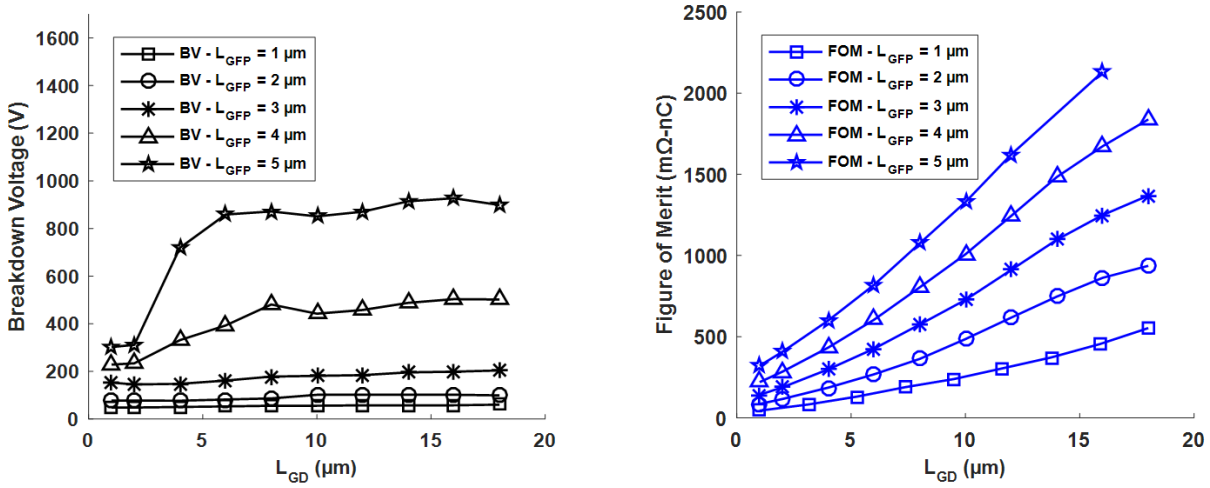


Figure 2.5: Breakdown voltage and FOM as a function of L_{GD} and L_{GFP}.

To understand the effect of varying L_{GD} and L_{GFP} on breakdown voltage and FOM, a series of simulations were run, the results of which can be seen in Fig. 2.5. A contour plot was generated for both breakdown voltage and FOM optimization to better aid in the interpretation of these results. The top subplot in Fig. 2.6 represents a breakdown voltage optimization for any given combination of L_{GFP} and L_{GD}, where blue represents low voltage and red areas designate high voltage. The bottom subplot displays a FOM

optimization which follows a very basic principle: smaller devices with a shorter field plate will have a lower figure of merit.

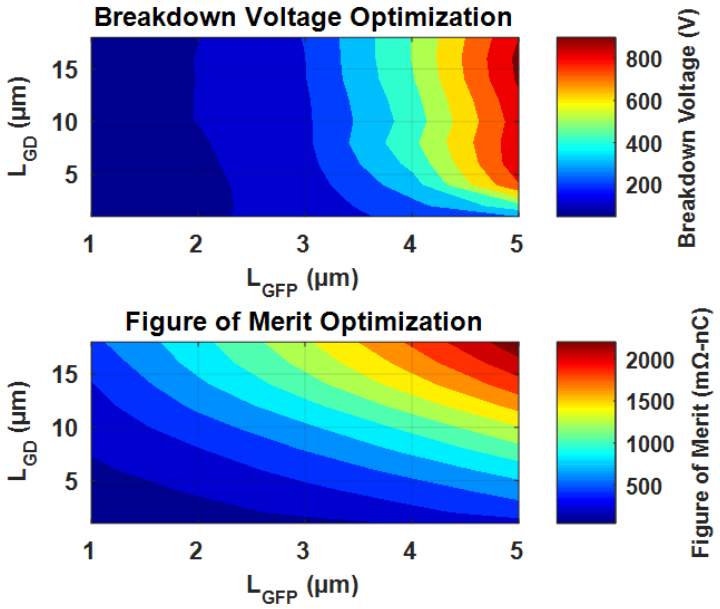


Figure 2.6: Optimization plots for breakdown voltage and figure of merit.

To help designers better understand how to design for high breakdown voltage and low figure of merit, another visual aid has been created. Combinating the previous two subplots (Fig. 2.6) results in the 3D plot shown in Fig. 2.7, which shows the breakdown voltage as a function of L_{GD} and L_{GFP} where the color bar represents various levels of FOM optimization. In this case, red regions are optimized well towards FOM (low FOM) while blue regions have high FOM for any given breakdown voltage level. Simply put, high peaks that are red in color are optimum designs for high voltage devices.

The specific trade-off between $R_{DS(on)}$ and Q_G, when targeting a certain breakdown voltage threshold, allows for the optimization of a device towards higher current operation or higher switching frequency operation (lower conduction loss or lower switching loss). To understand how the individual components of FOM are affected, namely $R_{DS(on)}$ and Q_G, they must be individually examined.

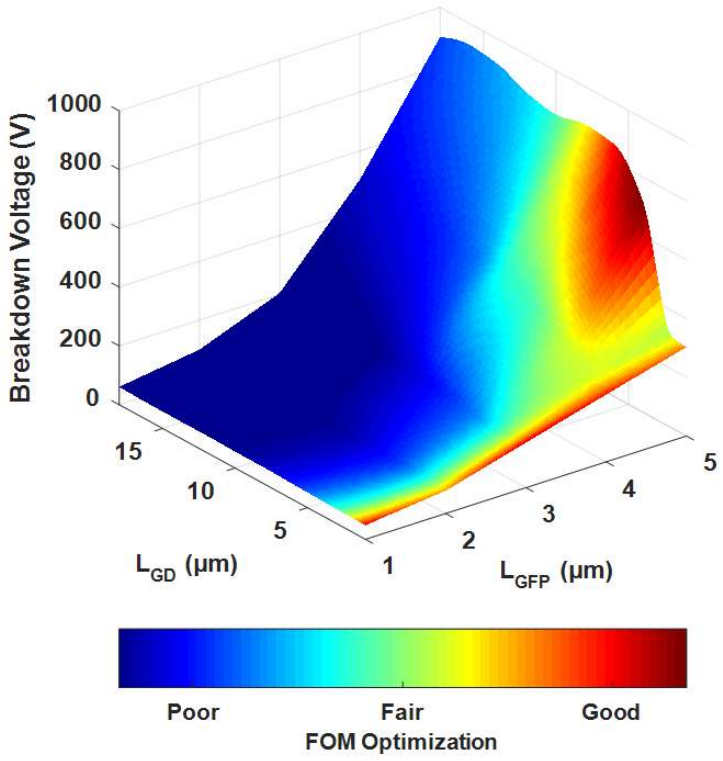


Figure 2.7: 3D optimization of breakdown voltage as a function of FOM, L_{GFP}, and L_{GD} for proposed DHFET.

Looking at the $R_{DS(on)}$ optimization plot in Fig. 2.8, it shows an expected trend where the smallest size device produces the lowest resistance. One thing to note is that $R_{DS(on)}$ increases with L_{GFP} because the drift length here is defined as L_{GD} + L_{GFP}. So when L_{GFP} increases, L_{GD} is held constant and the entire device length increases. Drift length increases proportionally with L_{GFP}. Examining the Q_G optimization plot shows that the smallest field plate length results in the lowest Q_G, however, it also shows that as L_{GD} increases, Q_G decreases. This is because both Q_G and $R_{DS(on)}$ have been normalized to the device size. So, as L_{GD} increases, Q_G stays the same, but normalized Q_G will decrease. Ultimately, this analysis represents a comprehensive look at the optimization of an E-mode pGaN HEMT from the perspective of a power electronics designer.

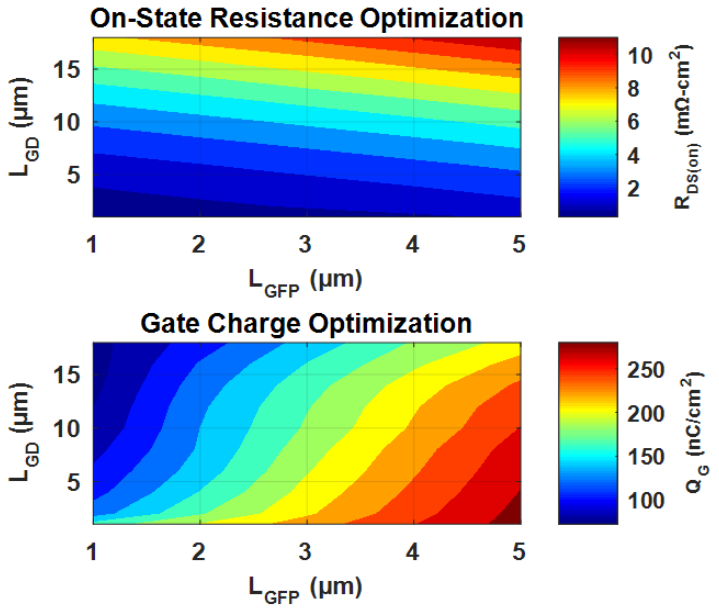


Figure 2.8: Optimization of on-state resistance and gate charge as a function of L_{GD} and L_{GFP}.

2.4 Conclusion

This chapter demonstrates a full optimization process to target optimum gate-to-drain length and gate field plate length for a normally on, high voltage, pGaN HEMT. To optimize field plate geometry and drift length scaling, device simulations were performed using Sentaurus TCAD. Based on this optimization, a device can be designed for a specific breakdown voltage, targeting the minimum figure of merit. For this simulated structure, when L_{GFP} is 5 µm, the correlation between breakdown voltage and L_{drift} disappears after L_{GD} increases beyond 6 µm. This phenomenon was explained intuitively by looking at the electric field distribution within the device where it was shown that scaling up to the edge of the E-field has very little effect on V_{BR} where-as scaling beyond this results in a significant reduction in breakdown voltage. From these simulation results, a 3D optimization plot was generated to show the breakdown voltage and FOM optimization as

a function of L_{GD} and L_{GFP}. Additionally, the specific trade-off between $R_{DS(on)}$ and Q_G is presented when targeting a certain breakdown voltage threshold. This trade-off allows for the optimization of a device towards higher current operation or higher switching frequency operation (lower conduction loss versus lower switching loss).

Finally, this work demonstrated the semi-independence of breakdown voltage from drift length given that the drift length is scaled past $L_{GD(sat)}$ at the edge of the E-field. Observing the electric field for the cross-sectional plot of the device validates this finding. In total, these results represent a comprehensive look at the optimization of L_{GFP} and L_{GD} for a high-voltage, e-mode, pGaN DHFET as an aid to device designers for the purpose of enabling application specific power electronics design.

CHAPTER 3: FABLESS DESIGN APPROACH FOR LATERAL OPTIMIZATION OF LOW VOLTAGE GAN POWER HEMTS

As mentioned previously, GaN power devices are typically used in the 600 V market, and the adoption of GaN in the low voltage sector has had limited success. This is in part due to the GaN FOM not being competitive yet compared to Si for these low voltage devices. To address why, we present a simulation work to demonstrate a fabless design approach for the lateral optimization of a low voltage GaN power HEMT. Optimization of lateral scaling terms such as gate-to-drain, gate, and gate-to-source lengths allows for minimization of the figure-of-merit ($R_{DS(on)} \times Q_G$) for a targeted breakdown voltage. Results show a FOM of 11 mΩ-nC for a device with a breakdown voltage $>$ 50 V. These results are for a given heterostructure design and estimated trap densities, and the effects of changing these estimated trap densities have been demonstrated to heavily influence breakdown behavior. As such, the focus of this study is on the relative difference between results rather than the absolute numbers. For this given design, results suggest that by shrinking L_{GD} further the FOM can be reduced to 6.68 mΩ-nC with a breakdown of 71 V: representing a 74% decrease in FOM compared to the EPC 2023 device (30 V device) [9].

3.1 Introduction

High electron mobility transistors (HEMTs) designed from wide bandgap materials have advantages over silicon transistors for both high switching frequency and low loss opera-

A. Binder, J.-S. Yuan, B. Krishnan, and P. M. Shea, *"Fabless design approach for lateral optimization of low voltage GaN power HEMTs,"* Superlattices and Microstructures, vol. 121, pp. 92–106, Sep. 2018.

tion [10], giving GaN a materials based advantage over Si. However, this advantage in materials so far has not translated well to better device performance for low voltage power devices. GaN benefits from a higher critical electric field than Si, that combined with the large bandgap means that for any given breakdown voltage the total device length can be reduced compared with Si devices. Reducing the device length results in lower on-state resistance, and a higher power density, both critical elements to power electronics design [1]. Additionally, the high electron mobility of the two-dimensional-electron-gas (2DEG) that constitutes the device channel, a unique feature of GaN HEMTs, allows high switching frequency operation at low losses. However, if the device is not optimized well, then it will perform poorly.

As technology advances, simulation tools for semiconductor device modeling have become more numerous and have increased in popularity. With the availability of these simulation and modeling programs, such as Silvaco or Sentarus TCAD, comes the option for more robust fabless design of high performance semiconductors. Earlier fabless designs relied on analytical equations for predicting breakdown voltage and performance metrics before fabrication, then required iterations after fabrication to improve on these designs. A fabless design approach based on simulation modeling has the potential to reduce the required iterations after initial fabrication, especially if the simulation model is well calibrated to previous fabricated device results [11]. Reducing the required fabrication iterations drastically lessens the cost of getting a product from concept to market.

The drawback of a fabless design approach is that in order to generate true predictions, each structure simulated will need a fabricated benchmark device to calibrate the simulation to experimental results. However, even without a benchmark, while there is some questionable accuracy in exact numbers reported, it can be verified that trends seen in simulation are correct. Based on this knowledge, a comparative study can be done, looking for relative difference and not exact accuracy. From this study, accurate predictions can be

made to suggest design improvements that will improve breakdown voltage, performance, and perhaps reliability of devices. This paper aims to demonstrate a design optimization and simulation approach for low voltage GaN power HEMTs. The simulation results shown focus on the comparative difference between results, rather than exact numbers reported, to generate trends that will optimize the device performance.

3.2 Device Structure and Simulation Methodology

3.2.1 GaN HEMT Device Structures

For GaN HEMTs, fabless design has three critical components: device structure, vertical layer thickness optimization, and lateral feature length optimization. Examination of the downselect process for device structures is as follows. Device structure covers two principal areas: device types and heterostructure layer selection. For power devices, the HEMT must be enhancement-mode rather than depletion-mode; this ensures that failure of the device results in an open circuit rather than a short circuit. Following this thought, enhancement-mode HEMTs employ the following methods to provide normally-off operation: recessing of AlGaN barrier layer (known as gate recess technique) [12–14], and adding a p-GaN material under the gate (known as p-GaN gate) [15–17]. Additionally, there is a method whereby fluorine implantation under the gate results in negative trap sites in the barrier layer that deplete the 2DEG channel under zero bias [17]. Of these methods, the p-GaN gate is the most popular and is used by several institutions leading to commercial devices available on the market [18] (pp. 24). The p-GaN gate, enhancement mode device is the chosen device for the focus of this paper.

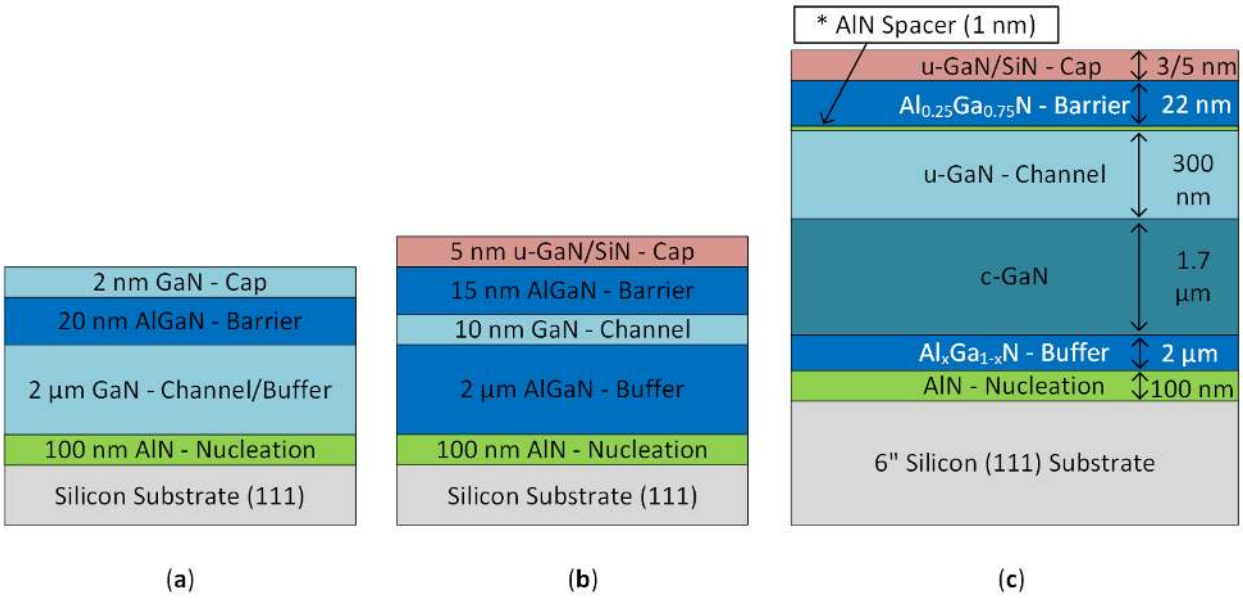


Figure 3.1: (a) Single heterostructure: the most basic design; (b) double heterostructure: has improved breakdown voltage and on-state resistance performance compared to single heterostructure design; (c) advanced heterostructure design builds off the double heterostrucuture and includes a carbon doped semi-insulating layer and thicker channel region to reduce defect density near channel.

Concerning heterostructure design given p-GaN gate type device, there are several considerations for improving device performance further beyond the single heterostructure layer stack-up. The single heterostructure design, shown in Figure 3.1 (a), makes use of an AlGaN/GaN barrier/channel interface to form the 2DEG. This is the most basic design type. Following the single heterostructure is the double heterostructure field effect transistor (DHFET) shown in Figure 3.1 (b). This design makes use of an AlGaN/GaN/AlGaN barrier/channel/buffer region which results in better $R_{DS(on)}$ performance and higher breakdown voltage than the single heterostructure design due to improved carrier confinement in the channel and higher critical electric field of the AlGaN buffer layer [3]. Finally, improvements can be made on DHFET structure such as adding a semi-insulating carbon doped c-GaN region between the buffer and channel to reduce buffer leakage current [19], or increasing the channel thickness to reduce the defect density near the the channel as

shown in Figure 3.1 (c). In addition, other improvements can be made such as adding an AlN spacer to block leakage current through the cap layer or gate and enhance transport properties [20], or using a super-lattice buffer to further reduce defects and mismatch compared to a typical graded AlGaN buffer [21].

3.2.2 *Simulation Methodology and Simulation Parameters*

For this paper, simulation results will focus on the p-GaN gate, DHFET structure shown in Figure 3.2. From the previous downselect, it is clear that the p-GaN gate double heterostructure provides a good baseline for optimization upon which further experiment-enhanced simulation work can be later compared to.

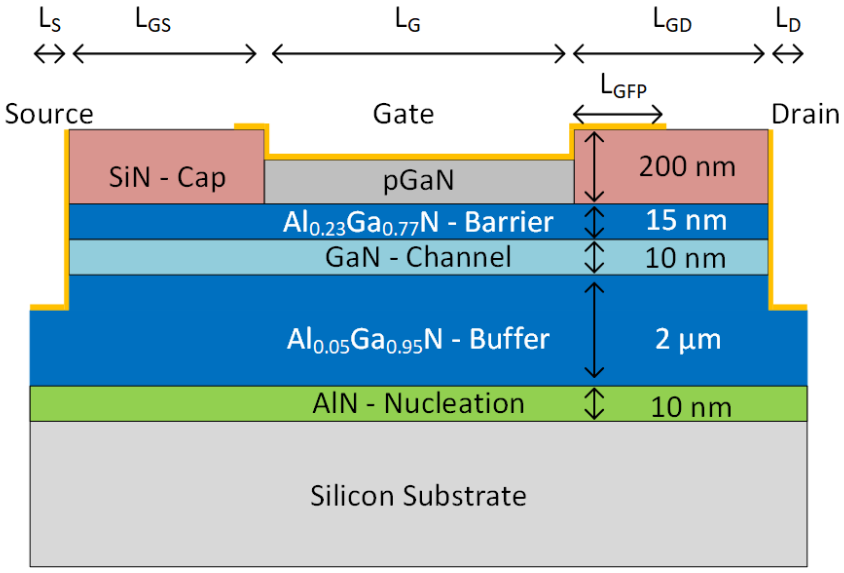


Figure 3.2: Enhancement mode, p-GaN gate, DHFET structure used in simulations.

Concerning device design, the gate electrode is Schottky type (barrier height = 0.6 eV). For this device design (pGaN, Schottky gate), gate current will not significantly contribute to device breakdown. Gate current is negligible for these off-state breakdown simulations as the device is normally off and thus the gate voltage is held at 0 V. With a high drain voltage

and zero gate voltage, the Schottky gate diode remains reverse biased and turned off. The intrinsic pin diode and the added Schottky diode due to the gate metal are in series, thus raising the forward voltage and significantly reducing on-state gate leakage (Figure 3.3). In addition, the Schottky type gate also serves to extend the reverse breakdown voltage of the gate due to high drain bias in the off-state condition.

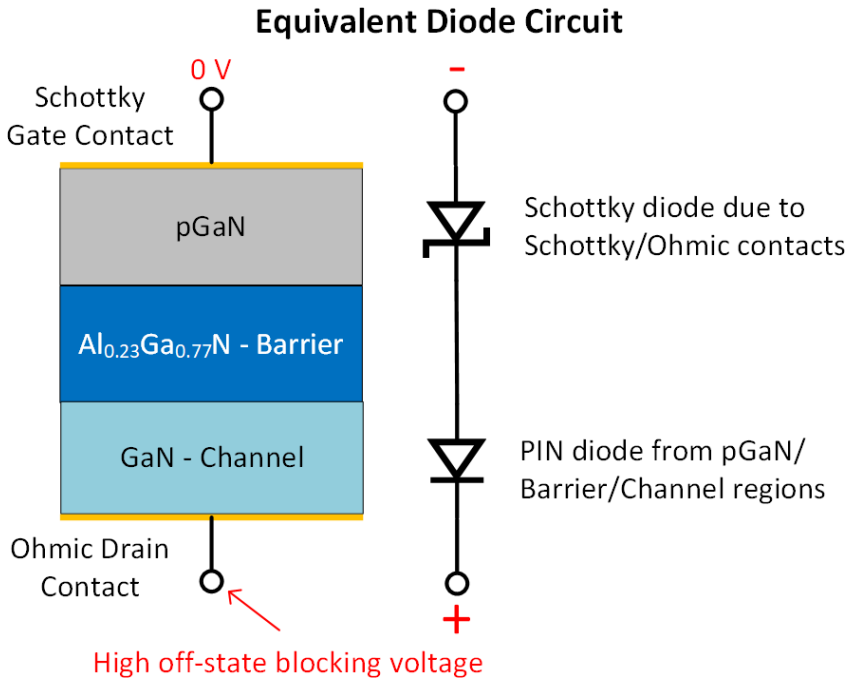


Figure 3.3: Equivalent circuit model of series diodes for off-state operation.

Details on the specified doping levels within the device are given in Table 3.1. For simulation purposes the impurity species are specified as boron for p-type and arsenic for n-type as that is how Sentaurus requires them to be defined (due to limited doping species availability). The dopants specified in the channel and buffer are intended to reflect N-doping as is natural for an unintentionally doped GaN material due to nitrogen vacancies, gallium interstitials, or oxygen incorporation [22].

Trap formation within GaN devices has a significant impact on device performance. As such, accurate specification of trap location, concentration, and energy level within GaN

HEMTs is critical to robust simulation design. Details on trap concentration specified for the following simulation work are given in Table 3.2. The surface traps are specified as donor traps and are set conservatively a small margin higher than our experimental results. Additionally, surface traps are reported for a similar concentration and energy level in several sources [23, 24]. Bulk GaN traps have been reported for a similar concentration in [8] and since the AlGaN buffer is very low molar fraction, the trap density set for the simulation has been estimated to be similar to bulk GaN trap levels. A brief review on reported trap energy levels in GaN devices is given in [22]. Additionally, other simulation reports have assumed similar values for trap concentrations and energy levels [22, 25–27].

Table 3.1: Doping Concentration and Specified Impurity Species.

Layer	**pGaN gate**	**Barrier**	**Channel**	**Buffer**
Doping Concentration	$3 \times 10^{17} cm^{-3}$	$1 \times 10^{18} cm^{-3}$	$1 \times 10^{15} cm^{-3}$	$1 \times 10^{14} cm^{-3}$
Impurity Species	Boron	Arsenic	Arsenic	Arsenic

Physics based simulators such as Sentaurus use mathematical models to describe the simulated device. These models consist of a set of fundamental equations which are derived from Maxwells laws and consist of Poissons Equation, the continuity equations, and the transport equations. Of these equations, Poissons equation and the carrier continuity equations provide the baseline, or general framework for device simulation, however, further secondary equations are needed to show certain unique device characteristics [28].

Table 3.2: Properties of Specified Traps in Simulated Structure.

Interface/Region	**Type**	**Concentration**	**Energy Level**
SiN/AlGaN (cap/barrier)	Donor	$5 \times 10^{13} cm^{-2}$	0.6 eV above midband
GaN/AlGaN (channel/buffer)	Acceptor	$6 \times 10^{12} cm^{-2}$	0.23 eV below cond. band
AlGaN (buffer)	Acceptor	$1 \times 10^{15} cm^{-3}$	0.45 eV below cond. band
AlGaN/AlN (buffer/nucl.)	Acceptor	$5 \times 10^{13} cm^{-2}$	0.6 eV above midband

The models used for the simulation results shown in this work, are presented in Table 3.3 and detailed below.

Table 3.3: Physics Models for Sentaurus Simulation.

Model Type	**Model Used**
Transport model for heterostructure devices	*Thermionic emission model*
Carrier transport	*Drift-diffusion model*
Mobility models	*Doping dependence & High field saturation*
Charge distribution model	*Fermi-Dirac statistics*
Band structure	*No bandgap narrowing*
Generation-Recombination	*Shockley-Read-Hall (SRH)*
Piezoelectric polarization	*Strain model*
Traps and fixed charges	*eBarrierTunneling*

The thermionic emission model is required for heterojunctions as the conventional transport equations are not valid at heterojunction interfaces. An interface-specific model must be used for carrier transport, of these models, the thermionic current model is set for both electron and hole current at a material-interface heterojunction. For modeling carrier transport, the drift-diffusion model is used which is also the default model for Sentaurus simulations. Carrier transport models are usually established as some form of simplification to the Boltzmann Transport Equations. Different assumptions result in models such as the drift-diffusion model or the hydrodynamic model. In most cases, the drift-diffusion model is the simplest and is quite adequate for most devices. This model falls short for nano-scale devices, however, since GaN power devices are on a much larger scale, the drift-diffusion model is sufficiently accurate for simulation purposes [7]. For mobility models, doping dependence incorporates degredation due to impurity scattering. Also, adding high field saturation includes the effect of velocity saturation for high electric fields. Sentaurus allows for different models to be used in calculating band structure and bandgap narrowing. The main difference between models available is how they handle bandgap narrowing. For these results, no bandgap narrowing is chosen so as not to unnecessarily

complicate the simulation. In terms of charge distribution models, Fermi-Dirac statistics are used instead of Boltzmann statistics as it is a more accurate model especially for high values of carrier densities [6]. Generation and recombination processes are modeled by the Shockley-Read-Hall (SRH) recombination model, which is recombination through deep defect levels in the gap. For computing polarization effects, Sentaurus provides two models (strain and stress). The strain model in this case uses a simplified model by Ambacher. Using this, the piezoelectric polarization vector P can be expressed as a function of the local strain tensor. The statement eBarrierTunneling allows traps to be coupled to nearby interfaces by tunneling. eBarrierTunneling allows coupling to the conduction band.

For clarity, a band diagram of the DHFET structure has been included (Figure 3.4) with the band energy calculated through a vertical cut in the center of the device (under the gate), in the off-state, at V_{DS} = 50 V.

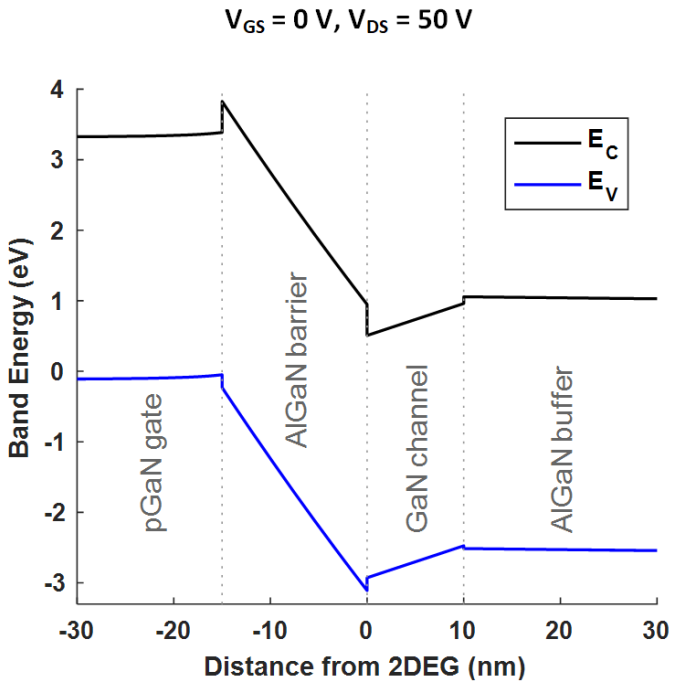


Figure 3.4: Energy band diagram of DHFET structure in the off-state with 50 V applied bias.

3.2.3 *Definitions for Parameter Extraction*

As the results presented in this work center around breakdown voltage, on-state resistance, and gate charge, the definitions for those parameters must be explicitly stated. Breakdown voltage is often defined in industry as the off-state voltage at which the drain leakage current exceeds 250 A [29,30], however, this definition does not account for scale of design: specifically the device width. Another definition that is commonly used which incorporates device width is to define breakdown at 1 mA/mm of leakage current [28,31,32]. This definition is much improved compared to the other, however, in our simulations, even with this definition, depending on the device size and the shape of the breakdown curve, this definition did not produce comparable breakdown results across all simulations. Therefore, the breakdown definition was expanded to include an area factor normalization parameter, and the definition for breakdown used in our simulation results has been modified to 10 mA/mm^2. Breakdown voltage plots are given in Figure 3.5 showing both linear and log scales.

Concerning on-state resistance, $R_{DS(on)}$ is extracted from an $I_D - V_D$ curve when the device is operating in the linear region. The voltage is sampled at I_D = 0.1 A/mm and the resistance is calculated as the inverse of the slope at that point. This extraction method is one of the frequently used industry standard methods. Gate charge has been extracted at V_G = 6 V with the drain voltage at 30 V bias.

This method of extraction is in line with the industry standard. An example of the curves used to extract $R_{DS(on)}$ and Q_G are shown in Figure 3.6.

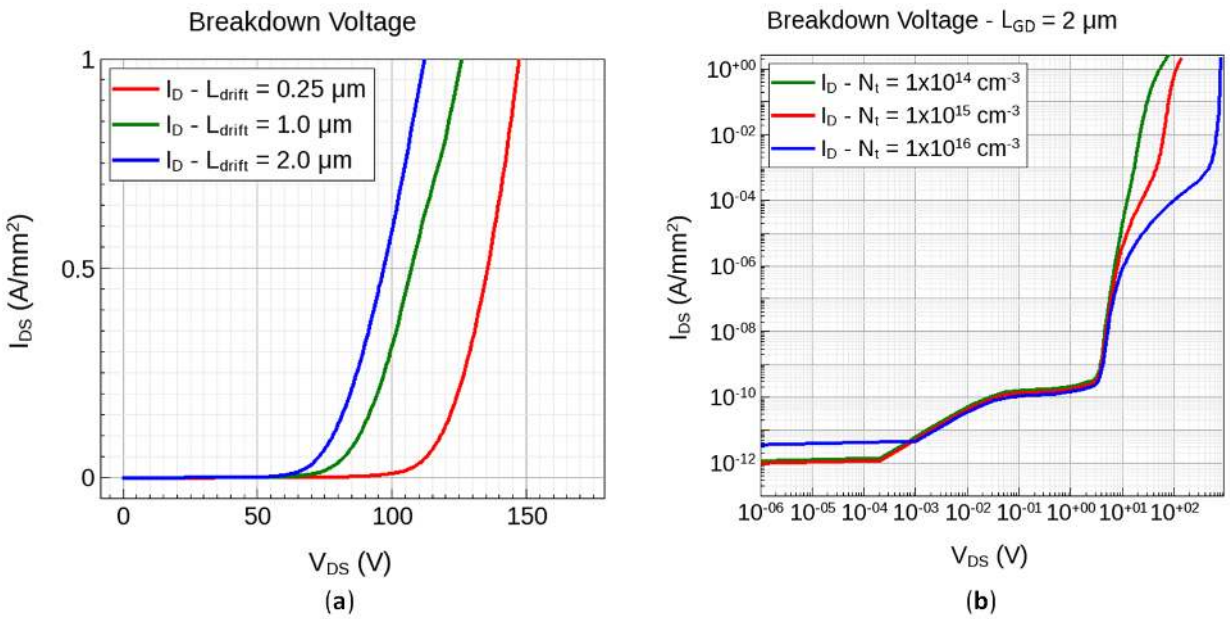


Figure 3.5: Breakdown voltage shown both in linear (a) and log (b) scales.

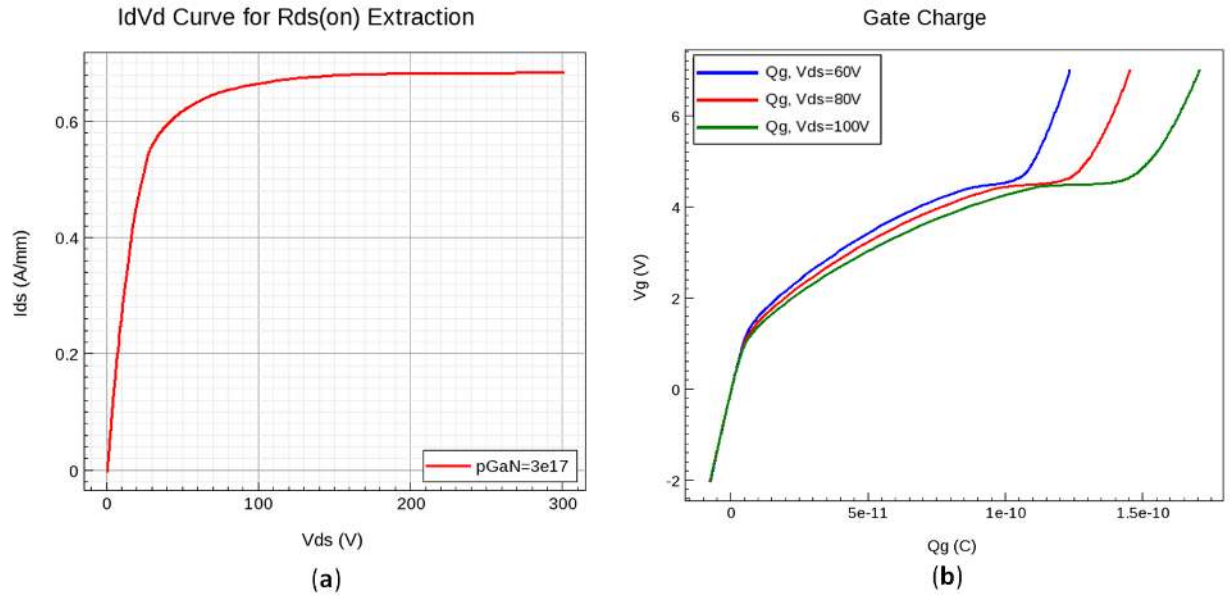


Figure 3.6: Curves used to extract $R_{DS(on)}$ (a) and Q_G (b).

3.3 Results and Discussion

3.3.1 Sentaurus Simulation: Design of Experiment

The simulation results presented here are from Sentaurus TCAD. Sentaurus software enables device design and simulation to extract critical semiconductor device parameters and to study device operation. Low voltage device design has a distinct set of design challenges compared to high voltage device design [33]. High voltage devices typically have a long gate-to-drain region, and shorter gate and gate-to-source lengths, while low voltage devices are much more laterally balanced. As GaN is typically used for the 100-650 V range, most publications focus on the design of high voltage GaN devices and not on low voltage design. This provides a unique opportunity for research on the challenges of low voltage design.

The simulation data reported is from a three terminal device (drain/gate/source) with a floating body contact. Other simulation data (not shown in the paper) shows negligible difference between the three terminal and four terminal results. From our simulation results for this device (comparing three terminal results to four terminal results), there is no known influence on breakdown characteristics resulting from the substrate electrode. Note however that the influence of a substrate electrode will be dependent on the device setup; and a different device design may result in different results. As vertical leakage current is not a significant breakdown factor in our simulation results, it should be expected that a substrate electrode would not have much impact on this device.

For these simulations, benchmark values were set for both lateral and vertical dimensions, then results were compared against the benchmark. The test setup was organized such that one parameter was varied at a time while the rest were held at a constant value. From this, a series of curves can be generated to show relative difference in results when varying

only one parameter. The baseline dimensions (both lateral and vertical) are shown in Table 3.4. These values should be used for reference throughout this document.

The simulation data presented throughout is from 2D simulations, however, in Sentaurus an area factor is set for 2D simulations which gives devices a specified width. The width specified for these simulations is 1 mm.

Table 3.4: Default Benchmark Values for Simulation Trials.

Lateral Dimensions	L_{GD}	L_{GFP}	L_G	L_{GS}	L_D	L_S
	1 µm	0 µm	2 µm	1 µm	0.25 µm	0.25 µm
Vertical Dimensions	t_{pGaN}	t_{cap}	$t_{barrier}$	$t_{channel}$	t_{buffer}	$t_{nucleation}$
	110 nm	200 nm	15 nm	10 nm	2 µm	10 nm

*W = 1 mm.

From the benchmark values given in Table 3.4, a set of simulations can be run to optimize gate-to-drain length (L_{GD}), gate length (L_G), gate-to-source length (L_{GS}), and gate field plate length (L_{GFP}) by generating trends for breakdown voltage and FOM as length is varied. Trends for breakdown voltage as impacted by buffer layer thickness are shown in Figure 3.7. Upon examination of Figure 3.7, it is apparent that the design of the heterostructure, specifically buffer layer thickness, has a heavy impact on breakdown voltage performance. The simulation results show the conventional nature of lateral scaling on breakdown voltage for the thinner buffer layer structure: primarily that an increase in length will increase the breakdown voltage. However, the simulation results also suggest that this proportionality between breakdown voltage and device length can be saturated depending on the buffer layer thickness. This unconventional phenomenon is well documented for high voltage GaN design [3,33]. While the relative trends shown in Figure 3.7 are known to be valid [8], it should be noted that the absolute numbers seen are not necessarily good predictions for an experimental device considering the dependent relationship between buffer layer thickness and trap density in reality [8,34]. This will be

discussed in more detail in section 3.3.2.

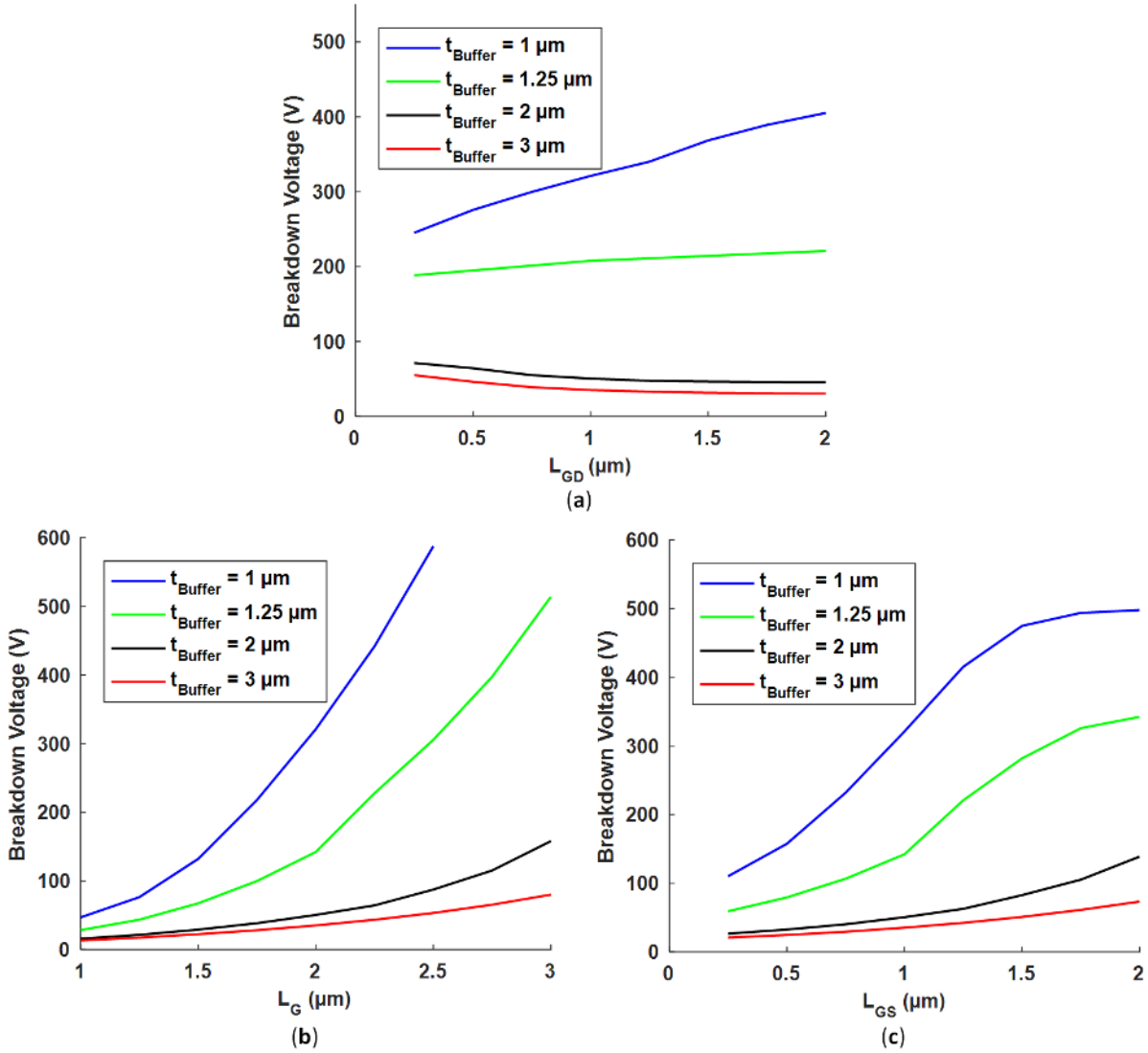


Figure 3.7: Simulation results for L_{GD} (a), L_G (b), and L_{GS} (c) demonstrating the impact of buffer layer thickness on breakdown voltage

Considering the nature of the buffer thickness versus breakdown voltage curves shown previously, the trends shown in Figure 3.7 are contrary to the classical understanding of breakdown voltage versus buffer thickness for high voltage design. Maximum breakdown voltage in GaN HEMTs is generally limited by the silicon substrate due to parasitic conduction at the buffer/substrate interface [31–33, 35–37]. In this case, increasing the

buffer layer thickness is known to increase the breakdown voltage by reducing the electric field at the substrate. However, breakdown at the substrate is known to be caused by high electric fields due to high blocking voltages. Considering lower electric fields ($<$ 1kV), breakdown can be due to punch-through leakage current, vertical substrate leakage current, and buffer leakage current [28, 38, 39]. For these conditions, it is reasonable to expect that breakdown voltage is proportional to the trap density, and that the trap density increases as the thickness decreases. This expectation is derived from the traps-filled-limit voltage which is proportional to trap density [8, 40]. The breakdown can be estimated to shift linearly with the traps-filled-limit voltage which is the point at which a sharp transition occurs in the breakdown current. As the off-state voltage increases, injected carriers are captured by traps, developing a negative potential. When the applied potential is greater than this negative potential due to traps, a sharp transition occurs in the current leading to breakdown. As trap density increases, the negative potential due to traps will increase, leading to a higher breakdown voltage.

The breakdown trends resulting from either substrate breakdown or breakdown due to traps are opposite in nature. Generally for high voltage devices, the breakdown voltage increases for increasing buffer thickness, but for low voltage devices, the breakdown voltage can decrease with increasing buffer thickness depending on the dominating influence. This behavior is presented in Figure 3.8 showing the competing breakdown trends.

Regarding the data presented in Figure 3.7, the nominal case where the buffer layer thickness is 2 m has been selected for further study of FOM trends. Note that for the selected case of t_{Buffer} = 2 μm, the results start to fall into that more saturated regime (the more unconventional data). This data has been selected because it corresponds with the nominal case for both buffer layer thickness and the corresponding trap density in the buffer. The results of these simulations for L_{GD}, L_G, and L_{GS} are shown in Figure 3.9.

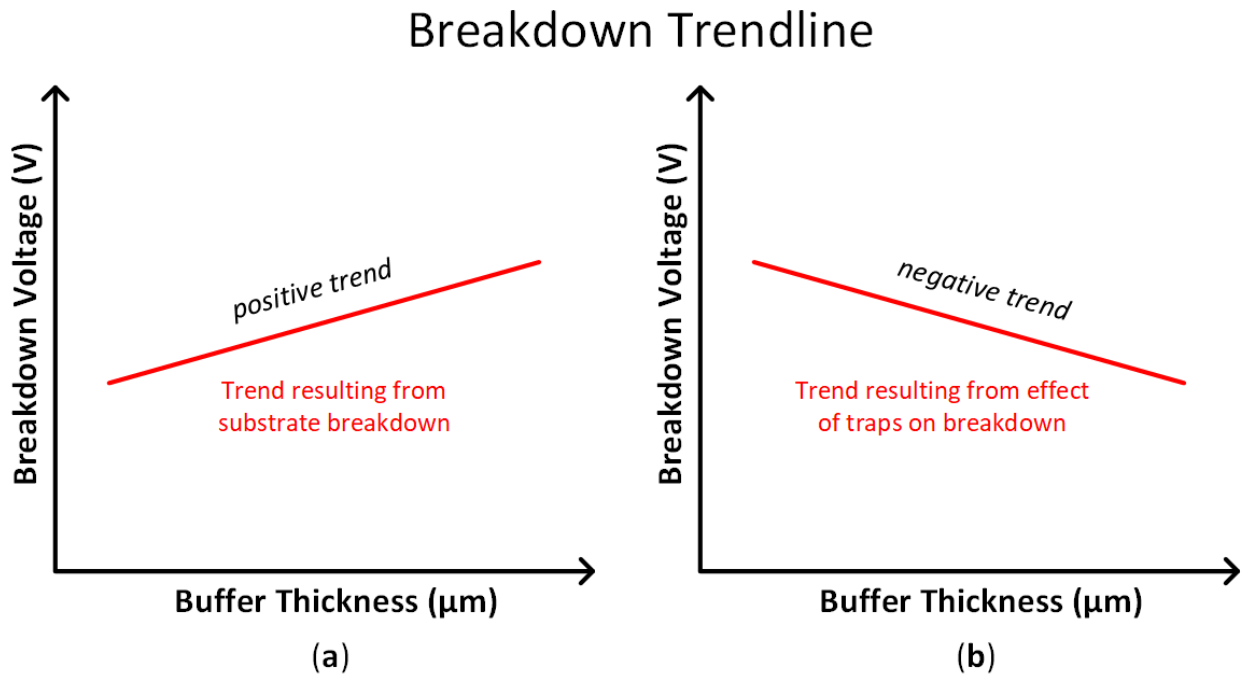


Figure 3.8: (a) for high voltage devices: breakdown is caused by parasitic conduction at the buffer/substrate interface; (b) for medium to low voltage devices: breakdown can be caused by buffer leakage current or punch-through.

For the dimensions specified in Table 3.4 and a gate field plate length of zero, it is possible to design a device with an extremely low figure of merit of 11 mΩ-nC for a breakdown voltage $>$ 50 V. While it is critical to point out that the number reported in simulation will likely be different from the exact number from experimental results, the trends showing how to obtain the lowest FOM for a given breakdown voltage are correct for how this device was specified (for a given trap level and given structure setup). The real merit of this study is in presenting scaling trends which result in the optimization of a low voltage device. This is done by individually examining the contributions of each scaling parameter towards breakdown voltage and FOM as well as the underlying physics driving that behavior.

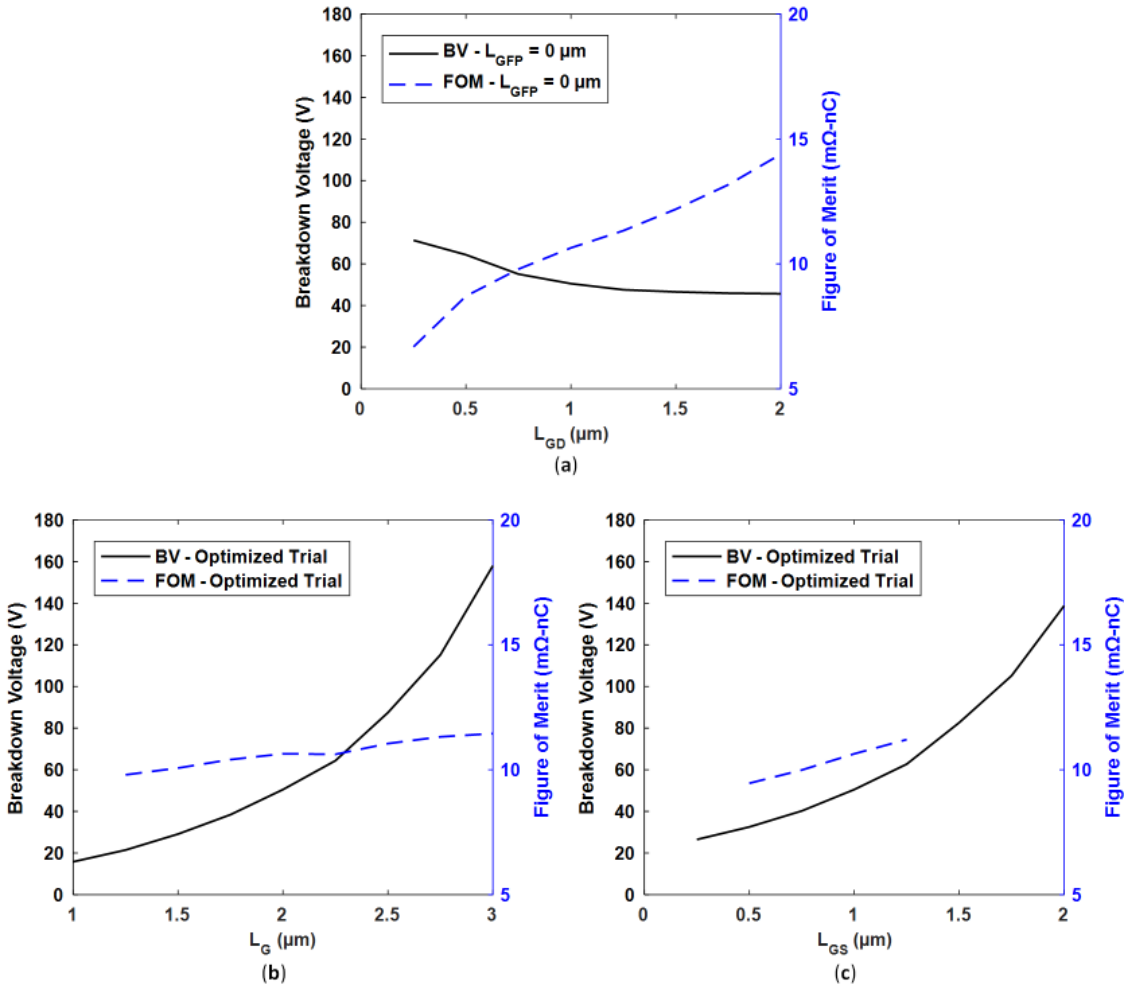


Figure 3.9: Simulation results for L_{GD} (a), L_G (b), and L_{GS} (c) presenting breakdown voltage and FOM trends to enable optimization of device performance.

3.3.2 *Gate-to-Drain Length: Breakdown Voltage and FOM Optimization*

Upon examination of the gate-to-drain length curves, notice in Figure 3.9 (a) that the breakdown voltage decreases with increasing L_{GD} when it is normally understood that the breakdown voltage increases as L_{GD} increases. Generally, the breakdown voltage increases proportionally with an increase in L_{GD} when breakdown is primarily due to the high electric field at the drain side of the gate edge. Increasing L_{GD} in this case will reduce the electric field at the gate edge by increasing the distance between the drain

and gate. However, this is not the only phenomena that impacts breakdown voltage performance [38]. Punch-through leakage current, vertical substrate leakage current, and buffer leakage current also contribute to breakdown. In this case, buffer leakage and punch-through leakage dominate, leading to this heavy saturation and decline of breakdown voltage as L_{GD} increases. For reference, in this simulation, decreasing the buffer layer thickness (for the same given trap density) or increasing the trap density both result in making the relationship between L_{GD} and V_{BR} heavily dependent again on electric field at the gate edge as the dominant influence (as shown in Figure 3.10). Hinoki et al. [8] have demonstrated the physical behavior of the trends presented in Figure 3.10. Note that for these simulations, as the buffer thickness is varied the trap density is held constant and vice-versa. This is an effective way to show the isolated effects of increasing buffer thickness or trap density, but not an accurate representation of a real scenario where buffer layer thickness and trap density are in reality co-dependent. As buffer thickness increases, trap density will decrease [8, 34], and that relationship is critical in processing and will yield different results than the independent study shown here.

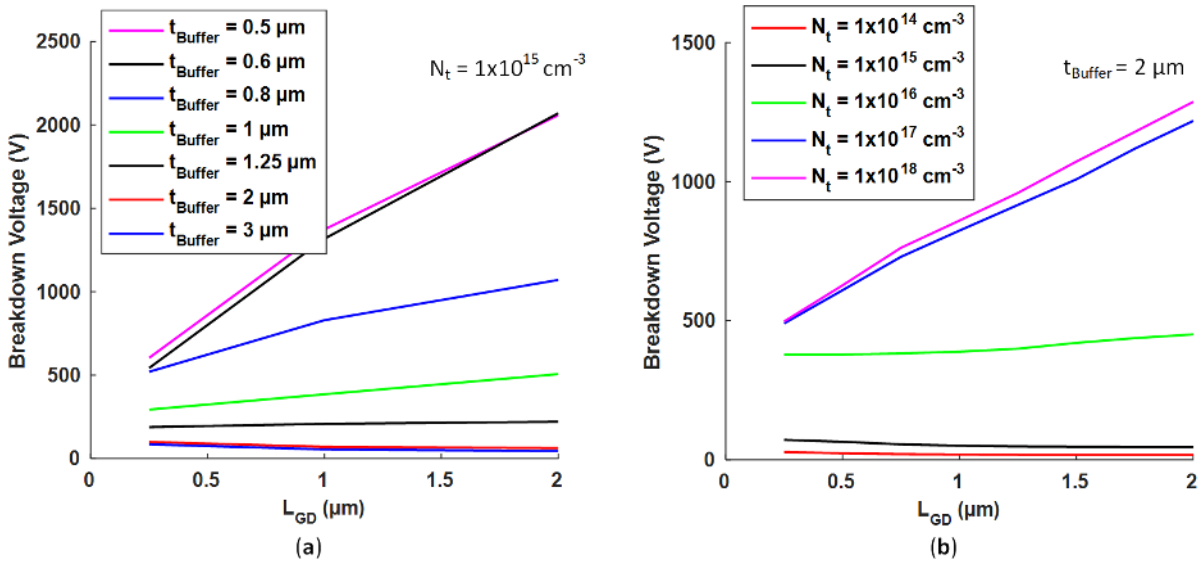


Figure 3.10: Influence of buffer thickness (a) and buffer trap density (b) on breakdown voltage.

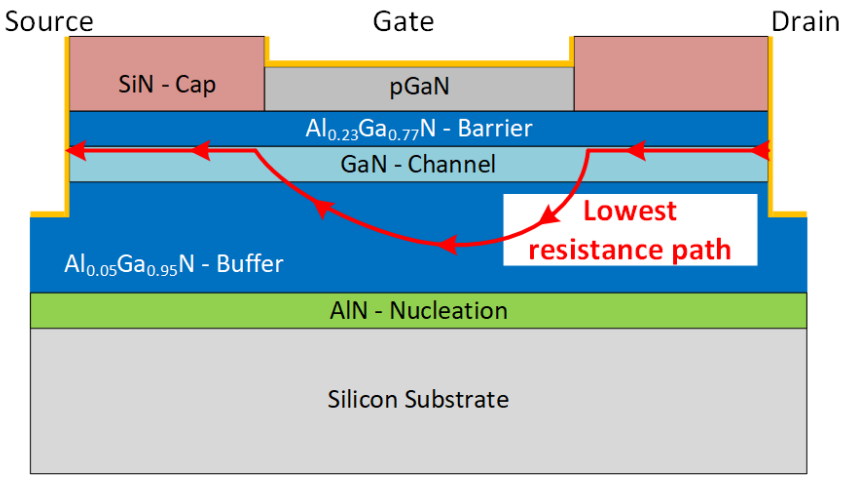


Figure 3.11: Lowest resistance current leakage path for device in off-state.

Examination of the trend shown in Figure 3.10 (a) reveals that a thin buffer layer results in a relationship between V_{BR} and L_{GD} such that $V_{BR} \propto L_{GD}$, whereas for a thicker buffer $V_{BR} \propto 1/L_{GD}$. This is due to the breakdown being highly dependent on the conductivity of the buffer layer as a result of the high density of buffer layer traps. As buffer thickness increases the buffer resistance decreases, and as the length increases the bulk resistance increases. However, since the lowest resistance path is from the drain contact through the channel to the gate edge, then through the buffer to the source-side channel (path shown in Figure 3.11), increasing L_{GD} effectively increases the width of the current leakage path from the drain-side channel through the buffer (as it increases the distance current can travel through the channel). The explanation of effective current path width increase is only valid for extremely small gate-to-drain distances and the effect is basically eliminated at $L_{GD} > 1$ µm. Increasing this width effectively lowers the resistance through that path, which increases the overall leakage current, thereby reducing the breakdown voltage. Were it not for the effect of the width of the current path causing a slight decrease in breakdown voltage for very small gate-to-drain distances, the trend in Figure 3.9 (a) could be considered to be saturated. Simply put, due to breakdown being highly dependent on the traps in the buffer, L_{GD} should have very little effect on breakdown voltage for

the specified buffer thickness and trap density. Note that specifying a different buffer thickness or trap density produces a more conventional behavior as shown in Figure 3.10. Simulation extremes such as $t_{Buffer} < 1\mu m$ and $N_t > 1 \times 10^{17} cm^{-3}$ are shown to demonstrate saturation of the increase in breakdown voltage due to change thickness or trap density. It is likely that in reality a saturated node exists, where the effects of the traps-filled-limit breakdown is outweighed by other effects. Such extreme designs for buffer thickness or trap density are unlikely to be desirable for standard GaN processing as it will have an adverse impact on lifetime and reliability. Additionally, since other factors can also contribute heavily to breakdown voltage performance, it is unlikely that in the extreme cases a real device would have such a high breakdown voltage. As the simulation results presented in this paper are for a more conventional buffer thickness and trap density ($t_{Buffer} = 2\mu m$ and $N_t = 1 \times 10^{15} cm^{-3}$), the requirement for accuracy in the extreme cases can be relaxed to some degree.

Given the specified trap density, buffer leakage at this point becomes the principle failure mechanism leading to breakdown as the buffer thickness increases. As this shift occurs (the shift in dominant failure mechanisms), the relationship between V_{BR} and L_{GD} shifts from a directly proportional relationship to a saturated and independent relationship. This same behavior can be seen in the current density plots shown in Figure 3.12. Notice how the pathwidth of current flow is increased from L_{GD} at 0.25 μm compared to L_{GD} at 2 μm, verifying the previous explanation.

3.3.3 Gate Length: Breakdown Voltage and FOM Optimization

As mentioned previously, the dominant contributor to breakdown leakage current in these simulations is from buffer leakage current and punch-through. These high levels of leakage current in the buffer are shown in Figure 3.13 where the partial depletion under the gate can also be clearly seen. As a result, increasing the gate length will suppress

punch-through [41] and improve breakdown voltage as shown in Figure 3.9 (b).

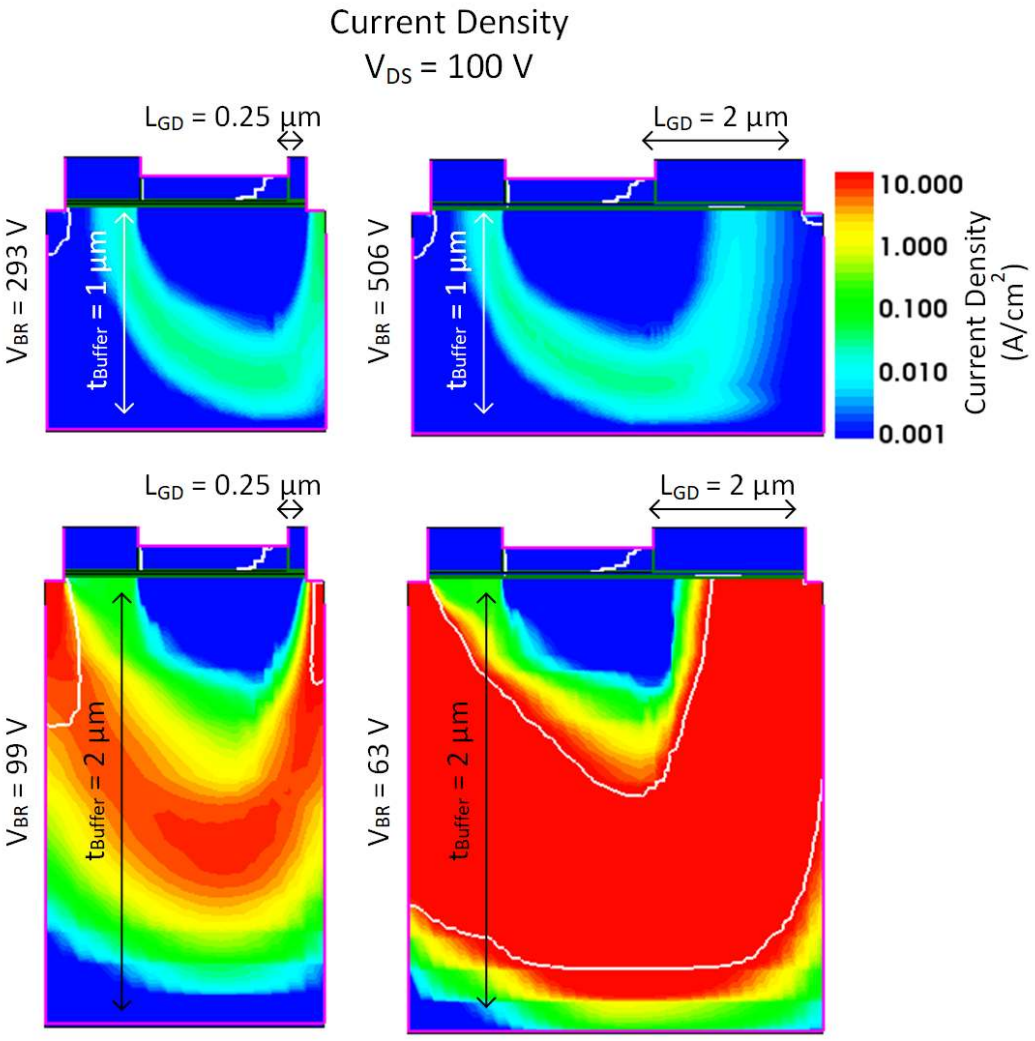


Figure 3.12: Current density plots showing breakdown voltage as buffer thickness and gate-to-drain distance vary.

In addition to suppressing punch-through, having a longer gate length can also lower the impact ionization at the drain-side gate edge, which significantly lowers the leakage current seen. Figure 3.14 shows electron concentration in off state for 1 µm and 2 µm gate lengths with no V_{DS} bias and with high V_{DS} bias. It can be seen that for the longer gate length, the high electric field region at the drain-side gate edge has a lower electron concentration compared to the smaller gate length device. This in turn reduces the impact

ionization hot spot that forms there as impact ionization is due to a high field region with a high electron concentration. Reducing either the electron concentration or the high e-field will result in reducing impact ionization. Additionally, a larger gate length suppresses drain induced barrier lowering more effectively [42].

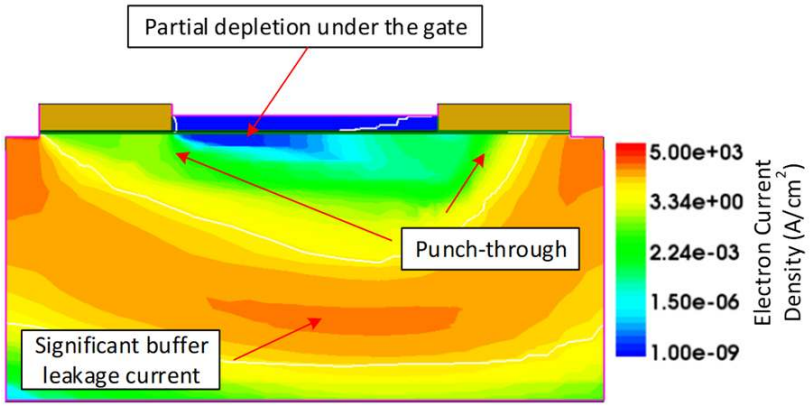


Figure 3.13: Cross-section view of leakage current contributing to breakdown in the off-state.

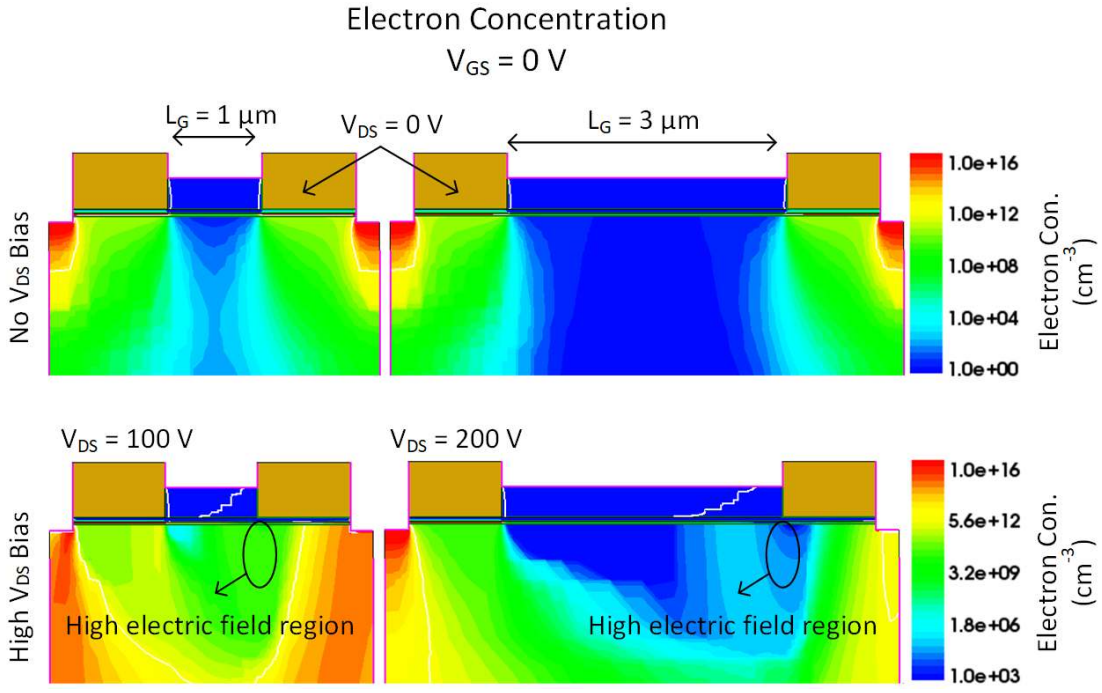


Figure 3.14: Larger gate length suppresses punch-through and lowers impact ionization.

3.3.4 *Gate-to-Source Length: Breakdown Voltage and FOM Optimization*

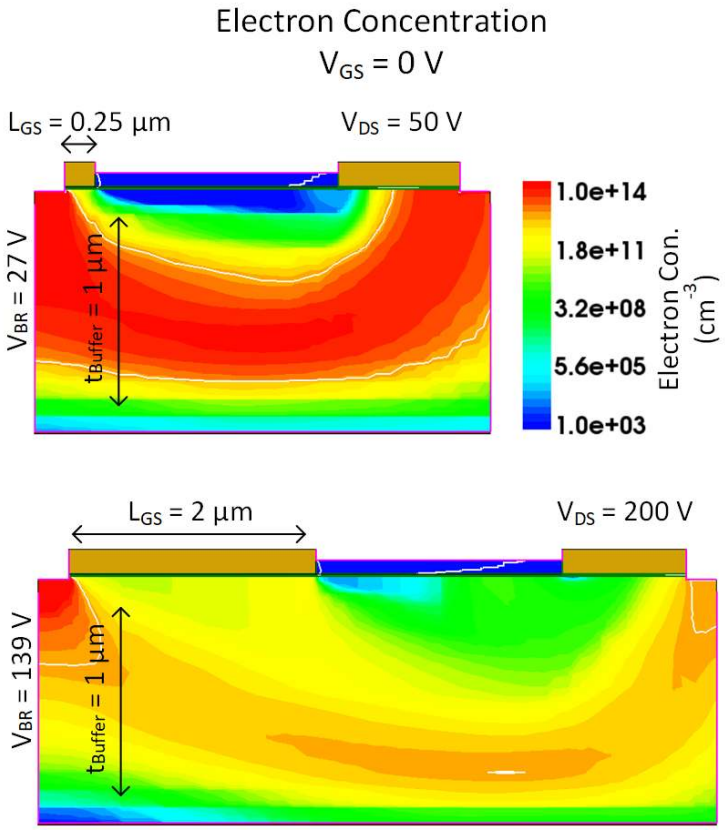


Figure 3.15: Longer gate-to-source length increases buffer resistance and there-by increases breakdown voltage.

Most of the focus in optimizing the lateral dimensions of high voltage power transistor is on L_{GD} and L_G, with not a much focus on L_{GS}. Most commonly, L_G is optimized to reduce punch-through, and to effectively deplete the region under the gate even in high bias conditions. Likewise, following conventional understanding, L_{GD} is optimized to increase breakdown voltage by lowering the electric field at the drain-side gate edge, the hot spot for impact ionization. The optimization of L_{GS} has neither of these concerns, yet from Figure 3.9 (c) it is obvious that for a low voltage device, L_{GS} has a significant impact on the breakdown voltage of the device. This is due to what is called source injection buffer leakage (SIBL) [32] which results in that leakage path that was shown previously in

Figure 3.13. At high levels of SIBL, the current path is from the source terminal, through the buffer, to the drain-side channel and to the drain contact. Unlike how increasing L_{GD} caused the breakdown voltage to decrease by increasing the path width of current flow (by effectively increasing the length of channel the current can conduct through), increasing the length of L_{GS} does not increase the leakage path width, as at high leakage the current flows primarily through the source terminal, not the source-side channel. Due to this, increasing L_{GS} will result in increasing the resistance of the buffer layer, and there-by increasing the breakdown voltage. This can be seen in figure Figure 3.15.

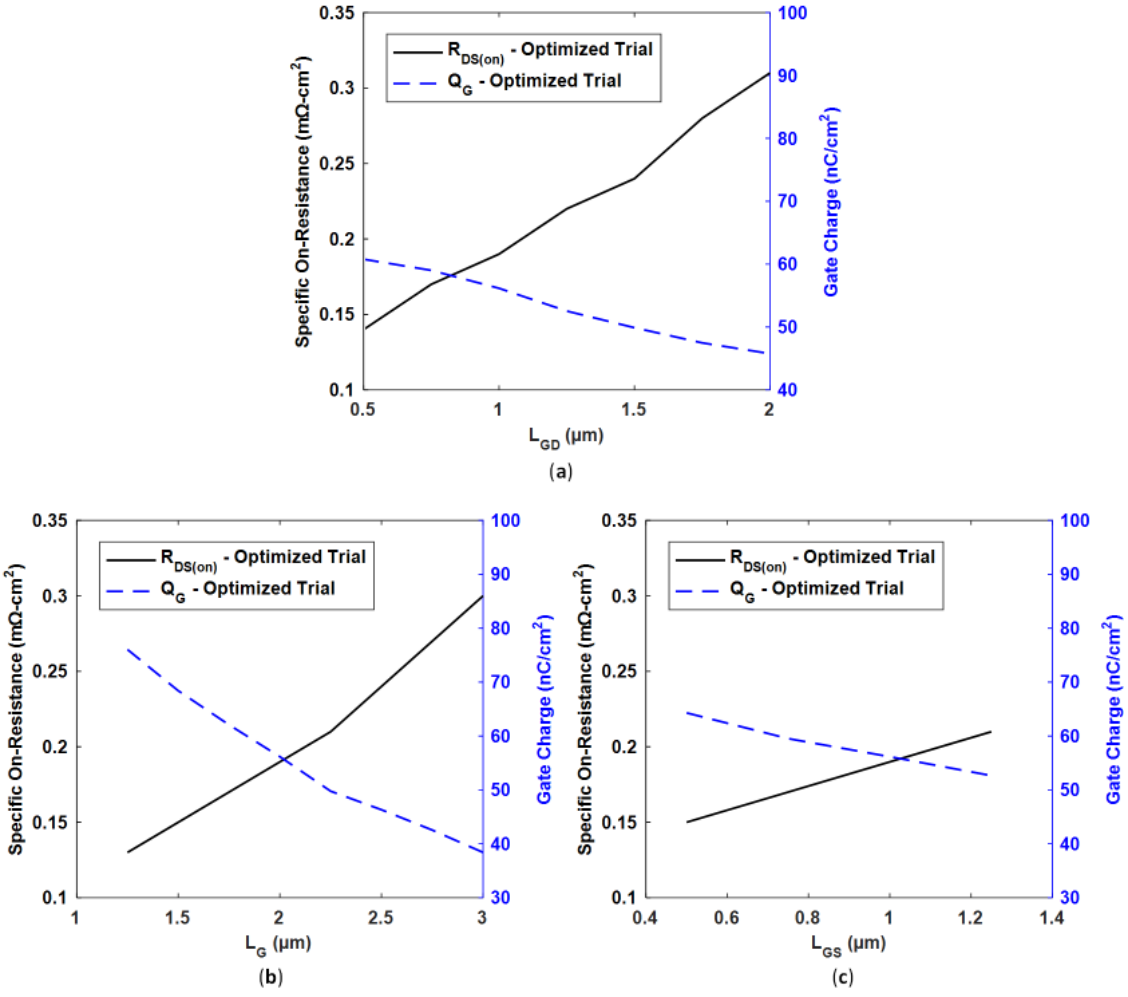


Figure 3.16: Lateral scaling effect for on-state resistance and gate charge for L_{GD} (a), L_G (b), and L_{GS} (c).

3.3.5 *Impact of On-State Resistance and Gate Charge Individually on FOM*

Concerning the individual contributions of on-state resistance and gate charge to the figure of merit, the results from scaling gate-to-drain length shown in Figure 3.16 (a) follow the well understood convention. An increase in device length will result in increasing the resistance, and in this case gate charge stays the same (though the normalized gate charge decreases due to an increased area factor). For both L_{GD} and L_{GS} (Figure 3.16 (a) and (c)) the gate charge stays the same as length increases, but the normalized gate charge decreases. All three $R_{DS(on)}$ curves follow a well understood trend, however, the gate charge as gate length increases would normally be expected to increase. In this case, as gate length increases Q_{GD} decreases which results in a lower overall gate charge as shown in Figure 3.16 (b). This phenomena has presented itself for the first time in these low voltage simulations, as high voltage GaN devices simulated on the same platform did not present with this trend [33]. This reverse trend is attributed to the significantly reduced lateral dimensions. In Figure 3.16 (b), both L_{GD} and L_{GS} are only 1 μm, which contributes to some current crowding and other second order effects due to the reduced size as mentioned previously. As mentioned, there is some reduction in Q_{GD} as L_G increases causing the overall Q_G to decrease. One method to understand this decrease in Q_{GD} is to evaluate C_{GD} as L_G increases. The gate-to-drain capacitance is a function of the area of the two electrodes ($L_G \times$ W and $L_{contact} \times$ W), the permittivity of the medium, and inversely proportional to the distance between the two electrodes (gate and drain). As L_G increases, the area of the gate electrode increases while the drain electrode stays the same size, which will not result in an increase in capacitance unless both electrodes increase in size. However, the median distance between electrodes (center to center spacing d = $L_{GD} + \frac{1}{2} L_G$) increases, which would result in a reduction in capacitance: an effect that would be exaggerated for small values of L_{GD}. It is also possible that the permittivity of medium between electrodes changes as a result of high levels of drain-side current crowding, but proving a change in

permittivity would be difficult. If we consider that C_{GD} decreases due to the increase in median distance between electrodes, then it is valid to also consider Q_{GD} to be reduced as Q = C $\times$ V.

3.3.6 Gate Field Plate and Discussion of Results

Based on these results, the only further thing to consider is whether a gate field plate is needed. Adding a gate field plate increases breakdown voltage but comes at the cost of additional gate charge, and thus a higher FOM. For a low voltage device, targeting a breakdown voltage between 30 V and 50 V, it is apparent a gate field plate is not required for this design (Figure 3.17). In this simulation, L_{GD} = L_{GFP} + 1 μm, meaning that the distance from the drain edge to the edge of the field plate is held constant at 1 μm, and increasing the length of the field plate increases the device length as well.

To target a breakdown voltage of 50 V, for a device operating in the 12-30 V range, these results suggest a design with no gate field plate, and lengths L_{GD}, L_G, and L_{GS} set to 1 μm, 2 μm, and 1μm respectively. This design target is highly subjective however to the estimated trap density in the device as well as the specifications for the vertical dimensions and design of the heterostructure. From these results, it is suggested a FOM of < 10 mΩ-nC could be achieved for a low voltage GaN HEMT. As pointed out previously, while the exact number may change from simulation to fabrication, the trends demonstrated are verified, and therefore the fabless design method is valid. Further optimization of the vertical design of the heterostructure can yield improved performance and reduced trap density within the buffer which also has a significant impact on breakdown.

Other results suggest that by shrinking L_{GD} further, it is possible to achieve a FOM of 6.68 mΩ-nC with a breakdown voltage of 71 V for L_{GD} = 0.25 μm. This improvement is heavily dependent on the estimated trap density within the buffer. It was previously

mentioned that as the trap density increases the relationship between L_{GD} and V_{BR} changes significantly. Considering this, the prediction for this extremely low FOM is only true for this one case, and in all other situations, a more conservative estimate would be to set L_{GD} $\approx$ 1 µm and calculate FOM from that design size ($\approx$ 11 mΩ-nC).

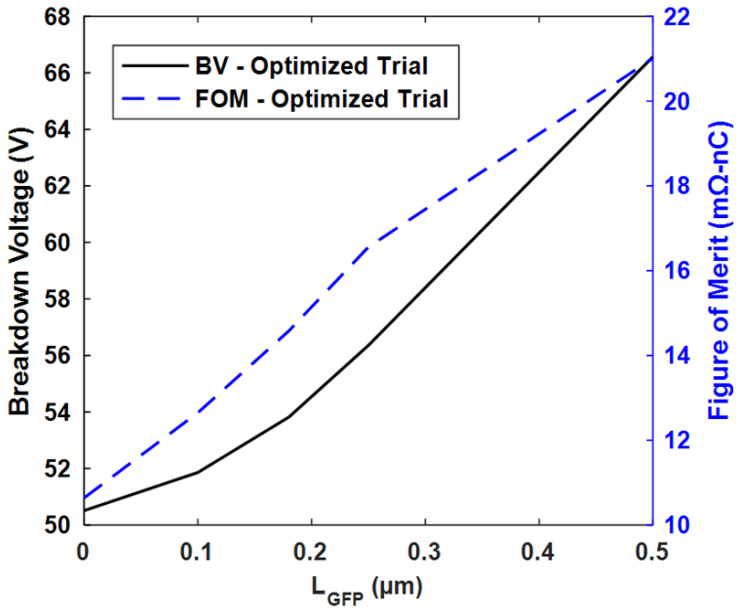


Figure 3.17: Simulation results for L_{GFP} presenting breakdown voltage and FOM trends to enable optimization of device performance ($L_{GD} = L_{GFP} + 1$ µm).

3.4 Conclusion

A fabless design approach for optimization allows for reduced design iterations and enhanced insight into device physics: enabling the reduction of time and cost in taking a design from concept to market. The lateral optimization approach presented here suggests a FOM of <10 mΩ-nC and a breakdown voltage of 50 V for a DHFET design with no gate field plate, and lengths L_{GD}, L_G, and L_{GS} set to 1 µm, 2 µm, and 1 µm respectively. These results were shown to be heavily influenced by trap density in the buffer layer: showing the leading contributor to breakdown voltage to be source injection buffer leakage. According

to the heterostructure design and the specified trap density, the results suggested that the FOM could be further improved by reducing the gate-to-drain length further. However, this suggested improvement is so heavily influenced by the estimated trap density that it is recommended for a more conservative FOM estimation that the initial design be based on a longer L_{GD} (≥ 1 μm). With the results being dependent on estimated trap densities, it is noted that while the absolute numbers reported have a degree of error, the trends shown are known to be correct. For this reason the emphasis is placed on trends leading to an improvement in FOM: specifically that increasing the gate length for a low voltage device shows a significant improvement in breakdown voltage with less detriment to FOM performance compared to increasing L_{GD} or L_{GS}.

CHAPTER 4: EFFECTS OF HETEROSTRUCTURE DESIGN ON PERFORMANCE FOR LOW VOLTAGE GAN POWER HEMTS

Following the lateral optimization of low-voltage power HEMTs, it is necessary to study the impact of heterostructure design (vertical scaling) on performance. This chapter presents a fabless design approach focusing on the impact of heterostructure design on the performance of low voltage GaN power HEMTs. Compared to the standard high voltage design process, low voltage design (< 100 V) comes with a unique set of challenges especially concerning breakdown rules. Low voltage simulations reveal less dependence on vertical leakage current and substrate breakdown compared to high voltage designs, and more reliance on buffer leakage and punch-through as the dominant factors leading to breakdown. To analyze the impact of heterostructure design on the device performance, optimization curves are presented for breakdown voltage, on-state resistance, and gate charge. Simulations are performed in Sentaurus TCAD and correlated to known existing experimental results where possible. Trends are presented for the optimization of the channel layer thickness, barrier layer thickness and molar fraction, impact of an AlN interlayer, and optimization of buffer layer thickness.

4.1 Introduction

Gallium Nitride (GaN) based high electron mobility transistors (HEMTs) have tremendous potential in the power electronics market as inherent material advantages compared to silicon give rise to high switching frequency and low loss operation [1, 10]. Attractive

material properties such as a high critical electric field, higher electron mobility and saturation velocity, as well as a high two-dimensional electron gas (2DEG) density at the barrier/channel interface serve to improve power density compared to silicon based devices [1]. For heterojunction devices such as GaN HEMTs, the design of the heterostructure has an enormous impact on performance and reliability which adds another layer of complexity to the design process.

Typically the research and design of GaN HEMTs is split into two areas: heterostructure design, generally done with a focus on material science, and post-heterostructure design – which generally starts with the purchase of a heterostructure from a vendor and includes all the fabrication work after the design of the heterostructure. Due to this split in design, these separate areas of work often do not have crossover. Heterostructure designers are typically designing to improve material properties: i.e. designing for low defect density, suppression of propagating defects from the nucleation layer, balancing the semi-insulating effect of carbon doped layers with the added defects due to carbon, reducing film stress, and improving 2DEG density among others. The impact of changing layer thicknesses can be directly measured through changes in material properties as measured through various test structures and equipment. With this data, heterostructure designers can predict improvements in device performance and that is typically the extent of the overlap between heterostructure designers and post-heterostructure (device) designers for GaN HEMTs. While the effects of carrier confinement, 2DEG density, trap density and location as well as other material properties can be measured, their direct impact on device performance can only be inferred, and it falls to device designers to evaluate these structures for their performance impact on devices. This creates a need for data on heterostructure design from a device performance perspective. To fill this need, devices could be fabricated on an array of different heterostructures, however this process is very expensive and time consuming. TCAD simulations can aid in this process, where device simulations on an array of varying heterostructures can predict performance trends. From these trends, a

few prominent designs can be selected to then be fabricated to verify simulation results.

This fabless design process is the focus of this paper: to examine the performance impact of scaling heterostructure layer thicknesses. To this end, the vertical layer optimization approach investigates the impact of scaling the channel thickness ($t_{channel}$), barrier layer thickness ($t_{barrier}$) and molar fraction ($x_{barrier}$), buffer thickness (t_{buffer}), and the thickness of an AlN interlayer between the barrier and channel (t_{AlN}). The advantage of a fabless design is that in addition to demonstrating a vertical layer optimization by presenting results over a range of thicknesses, a deeper dive into the fundamental explanation of why these changes occur can be studied. This is possible by presenting results showing band diagrams, lateral electric field distribution, drain induced barrier lowering (DIBL), carrier confinement and concentration among others for further insight into optimization. A significant portion of this work is dedicated to presenting trends for breakdown voltage (V_{BR}), on-state resistance ($R_{DS(on)}$), gate charge (Q_G), and figure of merit (FOM = $R_{DS(on)} \times Q_G$), which will aid in the optimization and design of a heterostructure for low voltage (< 100 V) power devices. This figure of merit ($R_{DS(on)} \times Q_G$) is selected as the primary evaluation criterion as it is used in high-switching-frequency power-electronics applications such as CPU power supplies [43] which is one of the primary intended applications for low voltage GaN technology.

4.2 Device Structure and Simulation Methodology

This work is an extension of our previous work which focused on the lateral optimization and design of low voltage GaN power HEMTs [44]. As such, a more detailed look into the simulation setup, models and physics used, as well as other details regarding methodology can be found in that manuscript. A brief summary of the simulation parameters and setup are given in this section for reference.

As this work focuses on a fabless design approach, it is important to note that in the absence of fabrication results with which to calibrate the simulation models, the data presented should be viewed in terms of the trends generated, and the underlying principles of why those trends occur. Even without a physical benchmark to compare against, it can be verified that the trends seen in simulation are correct. For this reason, the focus is on understanding the trends and the relative difference, with less emphasis on the exact accuracy. Towards the goal of calibrating the results with experimental data, we are fabricating devices in collaboration with National Nano Device Laboratory in Hsinchu, Taiwan, and also in local facilities at the University of Central Florida in Orlando, Florida. In the future we will be able to calibrate the models more thoroughly with those results. An extensive calibration process has been performed by Bahat-Treidel [28] and that process highlights some of the more critical models that can be used for more accurate results. We have followed those recommendations in lieu of device results for now.

4.2.1 Device Structure

The baseline device for this simulation is a pGaN-gate GaN HEMT as shown in Figure 4.1. This structure is a somewhat conservative implementation in that the heterostructure and device operation has less complexity compared to more advanced structures. Heterostructure designers for GaN HEMTs have recently pushed towards the use of superlattice buffer layers to reduce stress and suppress the propagation of defects [34]. Demonstrating effects of a superlattice buffer in simulation would likely significantly reduce the accuracy of the simulation. The results of such a simulation would become increasingly more reliant on the modeling of the effects of tunneling between layers and the accurate accounting of trap densities within the device. This adds a significant level of complexity to the simulation and more variables that can affect the results. Thus a more simplified approach is favorable which will lead to better understanding of the outcome with fewer variables.

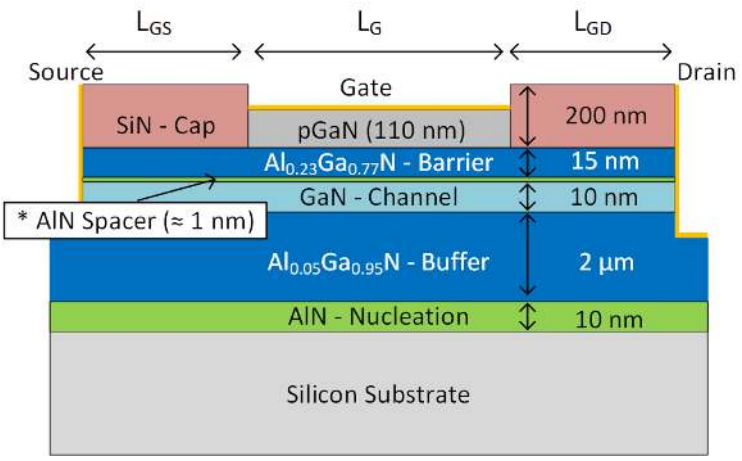


Figure 4.1: Enhancement mode, p-GaN gate, DHFET structure used in simulations.

In regards to operation, the selected device operates as a standard enhancement-mode, pGaN-gate device. More complex structures can be used to eliminate certain reliability concerns or to improve performance, however these structures come at the cost of increased simulation complexity. Some standard modifications to this structure will be introduced so as to understand the advantages and disadvantages of using the simpler device model. Our device model uses a Schottky type gate which serves to reduce the gate leakage and increase the forward voltage of the associated gate diode. This increases the top-end gate voltage limit the device can operate in without passing the diode forward voltage (V_f). By doing this, there is limited current injection from the gate. In contrast, if this condition ($V_{th} < V_G < V_f$) is not met, the device will operate as a Gate Injection Transistor (GIT). Injection of holes through the gate can significantly increase the drain current by means of conductivity modulation but at the cost of increased gate leakage current [45, 46]. Furthermore, adding a second pGaN region near the drain can create what is known as a Hybrid-Drain Gate Injection Transistor (HD-GIT) where the pGaN near the gate injects holes under the drain in the off-state with a high drain bias. This effectively releases trapped electrons during the process of switching which effectively eliminates current collapse. As a result, the HD-GIT does not have dynamic $R_{DS(on)}$ concerns like

conventional GaN based transistors [47, 48]. An illustration depicting gate injection in the on-state condition and the hybrid-drain contribution during the off-state condition is shown in Figure 4.2. Both of these structure changes, while beneficial to device operation, add significant complexity to the simulation model. For the sake of providing more robust results and to generate concise conclusions, a simpler device has been chosen.

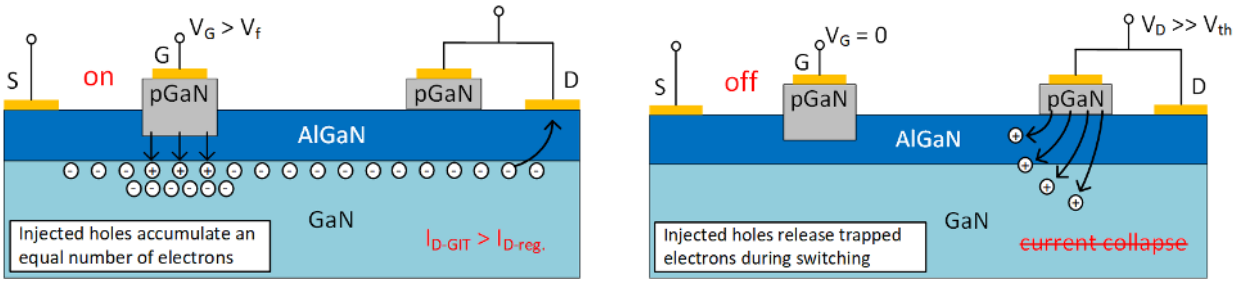


Figure 4.2: Example of the HD-GIT structure showing (a) gate injection operation in on-state to increase drain current and (b) hybrid-drain injection of holes in off-state to eliminate current collapse.

4.2.2 *Simulation Methodology and Simulation Parameters*

The simulations presented from Sentaurus TCAD [6] aim to optimize the device towards low voltage design. Compared to high voltage design, low voltage devices have a distinct set of design challenges. Low voltage devices tend to be much more balanced laterally, while high voltage devices generally have a long gate-to-drain region with shorter gate and gate-to-source lengths. These challenges present a unique opportunity for research on low voltage power devices as most publications in GaN focus either on high voltage power devices or low voltage RF devices.

Electrically, the device is setup as a three terminal device (drain/source/gate) with a floating body contact. Our simulation results (not shown in this paper) show a negligible

difference in breakdown voltage characteristics when comparing results from three and four terminal devices. This is due in part to a shift in breakdown voltage behavior for low voltage devices [33, 44]. From our simulations, vertical leakage current is not a significant breakdown factor for these low voltage devices, so it follows that the impact of substrate electrode on performance would be lessened. It is important to note, however, that the amount of influence that a substrate electrode has on performance is dependent on device design and that a different device design may be more heavily influenced when including a fourth electrode.

For the experiment setup, a baseline device has been constructed with fixed lateral and vertical dimensions. In each simulation experiment, a vertical dimension is selected and all other parameters are held constant while the selected dimension is varied. This results in a set of curves showing the influence of each layer on device characteristics and performance. These simulations are run as 2D experiments in Sentaurus, however, an area factor has been set which gives the devices a specified width. For these devices the width is 1 mm. The baseline dimensions as well as the the range of dimensions which are varied for each experiment are given in Table 4.1.

Table 4.1: Default Benchmark Values for Simulation Trials and Varied Dimensions for Each Experiment.

Lateral Dimensions		L_{GD}	L_G	L_{GS}	x_{buffer} [a]		
		1 μm	2 μm	1 μm	0.05		
Vertical Dimensions	t_{pGaN}	t_{cap}	$t_{barrier}$	$t_{interlayer}$	$t_{channel}$	t_{buffer}	$t_{nucleation}$
	110 nm	200 nm	15 nm	0 nm	10 nm	2 μm	10 nm
Varied Dimensions		$x_{barrier}$ [b]	$t_{barrier}$	$t_{interlayer}$	$t_{channel}$	t_{buffer} [c]	
		0.2-0.3	10-20 nm	0-3 nm	5-15 nm	0.5-3 μm	

[a] Molar fraction of the buffer layer ($Al_xGa_{1-x}N$).

[b] Molar fraction of the barrier layer ($Al_xGa_{1-x}N$).

[c] These simulations were done in our previous work [44] and are summarized here.

*W = 1 mm.

Table 4.2: Doping Concentration and Specified Impurity Species.

Layer	**pGaN Gate**	**Barrier**	**Channel**	**Buffer**
Doping Concentration	3×10^{17} cm^{-3}	1×10^{18} cm^{-3}	1×10^{15} cm^{-3}	1×10^{14} cm^{-3}
Impurity Species	Boron	Arsenic	Arsenic	Arsenic

Doping concentration and associated impurity species as specified for the simulation model are given in Table 4.2. Due to the limited availability of doping species within Sentaurus, and the issues associated with defining doping species, the p-type dopants have been specified as boron, and n-type dopants as arsenic. Channel and buffer doping as specified are intended to reflect naturally occurring N-doping for an unintentionally doped GaN material due to gallium interstitials, nitrogen vacancies, or oxygen incorporation [22].

Accurate specification of traps within GaN HEMTs is critical to robust simulation design as trap formation has a tremendous impact on performance and reliability. Estimates used in the simulations for trap type, concentration, and energy level are specified in Table 4.3. The surface traps have been specified as donor traps and are conservatively set a small margin higher than our experimental results from devices with a comparable heterostructure. Additionally, several other sources also report a similar concentration and energy level for surface traps [23,24]. AlGaN buffer layer trap levels have been estimated to be similar to bulk GaN trap levels since the Al molar fraction is quite low. The buffer trap levels specified for our model are similar to those reported in Ref. [8]. Other simulation reports also assume similar values for trap concentrations and energy levels [22,25–27]. For a brief review on reported trap energy levels, refer to Ref. [22].

For details on physics models used in these simulations, please refer to our previous work for a detailed list and explanation of models used [44].

Table 4.3: Properties of Specified Traps in the Simulated Structure.

Interface/Region	Type	Concentration	Energy Level
SiN/AlGaN (cap/barrier)	Donor	$5 \times 10^{13} cm^{-2}$	0.6 eV above midband
AlGaN/AlN (barrier/interlayer)[a]	Acceptor	$6 \times 10^{12} cm^{-2}$	0.23 eV below cond. band
AlN/GaN (interlayer/channel)[a]	Acceptor	$6 \times 10^{12} cm^{-2}$	0.23 eV below cond. band
GaN/AlGaN (channel/buffer)	Acceptor	$6 \times 10^{12} cm^{-2}$	0.23 eV below cond. band
AlGaN (buffer)	Acceptor	$1 \times 10^{15} cm^{-3}$	0.45 eV below cond. band
AlGaN/AlN (buffer/nucl.)	Acceptor	$5 \times 10^{13} cm^{-2}$	0.6 eV above midband

[a]Only specified when an interlayer is used in the simulation.

4.2.3 Definitions for Parameter Extraction

When extracting simulation data, in nearly all cases we follow the industry standard for data extraction, except in the cases where a modification of the standard produces more meaningful results. For example, breakdown voltage is typically defined in testing as the off-state drain-to-source voltage at which the drain leakage current exceeds 250 μA [29, 30], however, this does not account for device scale. In order to accommodate device scale, breakdown is alternatively defined as the voltage at which the drain leakage current exceeds 1 mA/mm [28, 31, 32]. The definition used for breakdown voltage in our simulations has been modified further to include area factor. This change is necessary to accommodate how the plot of breakdown current will change shape when altering lateral dimensions. In order to keep consistency with our previous work [44], the definition for breakdown used in our simulations has been modified to 10 mA/mm^2. Using current density for the breakdown criterion keeps the results consistent as the shape of the I-V curve changes. This is more significant when modifying lateral dimensions, but even with the alteration of vertical dimensions the breakdown I-V curve will change shape. This information can be used to evaluate particular leakage mechanisms and breakdown factors (such as traps-filled-limit-voltage).

On-state resistance and gate charge extraction follow the industry standard methods.

$R_{DS(on)}$ is extracted from an I_D-V_D curve with the device in the linear region. Extraction is performed at V_G = 6 V with the drain voltage sampled at I_D = 0.1 A/mm. The resistance is then calculated as the inverse of the slope at that point. Gate charge is extracted at V_D = 30 V and V_G = 6 V from a standard Q_G-V_G plot. For more information, examples of the curves used for extraction are presented in our previous work [44].

4.3 Results and Discussion

In the subsections to follow we will discuss, in order, the optimization of the channel layer thickness, barrier layer and molar fraction, impact of an AlN interlayer, and briefly discuss the influence of the buffer layer. The impact of buffer layer thickness and associated trap density in the buffer has been evaluated in detail in our work in Ref. [44].

4.3.1 Channel Layer Optimization

Optimization of channel layer thickness depends on many factors including the conductivity of the channel layer, the density of the 2DEG layer, the impact on the lateral electric field, and depending on the heterostructure orientation, it can also impact gate control. In general, increasing the channel thickness is known to suppress buffer-related current collapse: suggesting that a thicker GaN channel serves to reduce the deep traps in the channel and to reduce electron capture probability by deep traps in the buffer layer [49]. This will serve to improve breakdown performance and reliability as the channel thickness is increased. However, in addition to this, there are multiple competing influences on breakdown voltage and device performance that can be seen when investigating the underlying physics behind the trends. For example, the breakdown voltage trend seen in Figure 4.3 is demonstrated to increase as the channel thickness increases; however, breakdown voltage is influenced by $R_{DS(on)}$, drain induced barrier lowering (DIBL), the

traps-filled-limit voltage (V_{TFL}), and lateral electric field peaks. These factors each contribute to breakdown voltage but in a competing fashion: three out of four of them suggest breakdown voltage should decrease, and of these factors only the lateral electric field results suggests that breakdown should increase. These factors will each be discussed in length, and from these results, it is apparent that the effect of the lateral electric field is the dominating factor determining breakdown voltage behavior. Examining the simulations results gives critical insight into device physics. The results for breakdown voltage, figure of merit, $R_{DS(on)}$, and Q_G as channel thickness is scaled are given in Figure 4.3.

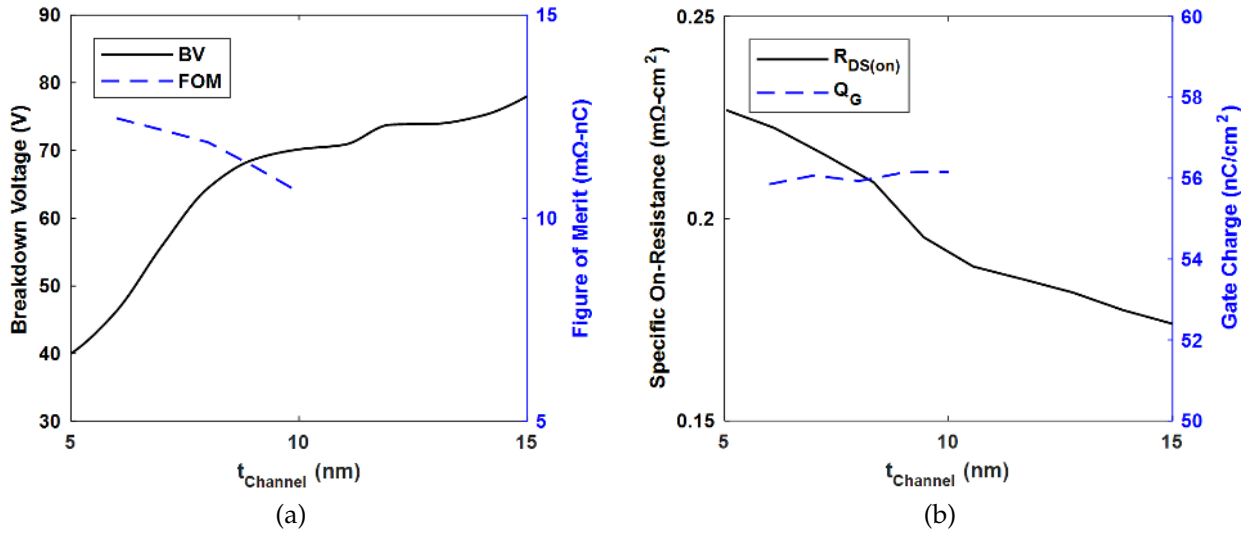


Figure 4.3: Simulation results for $t_{Channel}$ presenting (a) breakdown voltage and FOM trends as well as (b) on-state resistance and gate charge trends.

As mentioned previously, when considering breakdown performance, there are several factors to consider. On-state resistance is known to decrease as channel thickness increases [50]. This is due to a wider current path and higher 2DEG concentration resulting from the thicker channel region. This trend for $R_{DS(on)}$ is verified in Figure 4.3(b). Excluding all other factors, a lower channel resistance should trend towards lowering the breakdown voltage.

Another factor that influences breakdown voltage results from a change in drain-induced-barrier-lowering (DIBL). As seen in Figure 4.4(a) the energy barrier at the source side of the gate becomes increasingly lower as the drain voltage increases. This is called the DIBL effect, which is commonly known to occur in short channel devices, and can be greater after the application of off-state stress [51–53]. As the barrier height is lowered, electrons from the source region can punch through the buffer layer resulting in buffer leakage current. Comparing results from Figure 4.4(a) to Figure 4.4(b) shows more DIBL for the device with the thicker channel, which will result in more punch through leakage. Leading to the conclusion that increasing the channel thickness should result in influencing the breakdown voltage to decrease due to the effects of DIBL. One last thing to note about DIBL is that the values reported from the simulation are quite small ($\ll 1$ eV) and will have a very small impact on the device performance or breakdown voltage.

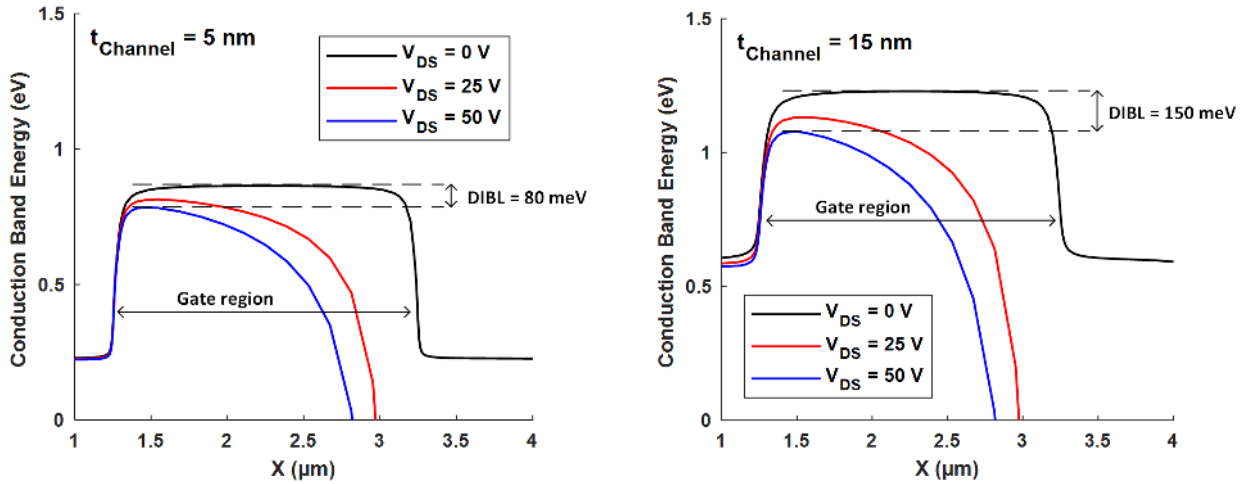


Figure 4.4: Drain-induced-barrier-lowering increases as the channel thickness increases showing (a) $t_{Channel}$ = 5 nm and (b) $t_{Channel}$ = 15 nm.

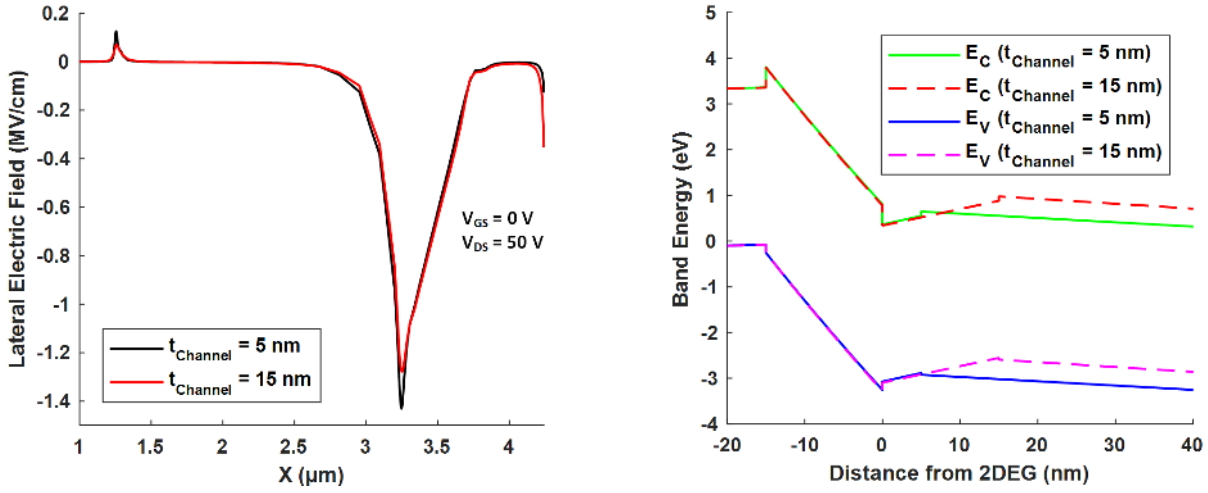
Concerning traps-filled-limit voltage (V_{TFL}): the simulation results are inconclusive to show the change in traps-filled-limit voltage as the channel thickness increases. In reality, the trap density in the channel will decrease as the channel thickness increases according

to Hinoki *et al.* [8]; this in turn will lower the breakdown voltage as the trap density increases when considering the effect resulting from the change in the traps-filled-limit voltage. However, the simulation has been designed to keep the trap density constant as the channel thickness is varied, so the effect of V_{TFL} on breakdown is not represented in the results shown.

Breakdown voltage is known scale inversely with the electric field intensity, which is why high voltage devices employ various types of field plates to reduce the electric field and thereby increase the breakdown voltage [3,54,55]. Impact ionization resulting from the high electric field can cause high off-state current, contribute to or result in device breakdown, and generate long-term reliability issues. In addition, high electric field in the buffer can generate defects due to grain-boundary states [50,53]. As the electric field is increased, more defects are produced leading to a high defect density which can develop into an additional electron leakage path as defects overlap or develop into large clusters [56,57]. In any case, reducing the electric field intensity is critical to increasing breakdown voltage. Results from Figure 4.5(a) show that increasing the channel thickness results in a lower electric field, which in turn leads to a higher breakdown voltage. These results for the lateral electric field are taken at the channel/buffer interface. Comparing the maximum electric field from both devices, the peak lateral electric field intensity for the thinner channel device is 12% higher than for the thicker device.

A summary of the influence of the individual components on breakdown voltage as channel thickness varies is presented in Table 4.4. Note that this table is not an exhaustive list of the phenomena affecting breakdown voltage, but just a summary of some of the significant factors that contribute to breakdown. Trap related effects mentioned in the beginning of this section are challenging to display in simulation (such as the influence of channel thickness on electron capture probability) and were therefore not subject to independent examination like the parameters in this table. For reference, the energy band

diagrams have been included for $t_{Channel}$ = 5 nm and 15 nm (Figure 4.5(b)). Overall, the breakdown results from Figure 4.3(a) are in agreement with those reported elsewhere [49,50].



(a) (b)

Figure 4.5: (a) Lateral electric field calculated along the channel/buffer interface with different channel thickness values (5 nm and 15 nm). (b) Energy band diagrams for $t_{Channel}$ = 5 nm and 15 nm in off-state with 50 V applied bias.

Table 4.4: Influence of Individual Components on Breakdown as Channel Thickness Increases.

	$R_{DS(on)}$	DIBL	V_{TFL}	Lateral ε-field
$as\ t_{Channel} \uparrow$	$\downarrow$	$\uparrow$	$\downarrow$	$\downarrow$
Resulting Effect	$V_{BR} \downarrow$	$V_{BR} \downarrow$	$V_{BR} \downarrow$	$V_{BR} \uparrow$

4.3.2 Barrier Layer Optimization

Thickness of the barrier layer is a critical factor as it affects 2DEG concentration and can impact breakdown voltage behavior by affecting the vertical gate ε-field. As such, the impact of barrier layer thickness should be evaluated by examining maximum drain

current, peak transconductance, and breakdown characteristics. It is generally understood that increasing the barrier layer thickness will increase the drain current while lowering transconductance [58, 59]. For that reason, it is desirable to have a thicker barrier layer if power density is critical (such as for power electronics) and consequently a low barrier thickness is desirable to maximize high-frequency performance and to minimize short-channel effects [58]. This trend is supported by our simulation work shown in Figure 4.6(a). Additionally, the barrier layer thickness impacts breakdown voltage by affecting the vertical gate ε-field which in turn affects punch-through, gate leakage current, and device degradation. A thicker barrier layer will reduce the vertical ε-field thereby lowering the breakdown voltage. This effect can be seen in Figure 4.7(a). In contrast, a thinner barrier layer is known to reduce gate leakage current [60] and improve punch-through control. The barrier thickness also heavily impacts threshold voltage [shown in Figure 4.6(b)] due to gate capacitance being directly proportional to barrier thickness. These observations are supported by device models, other simulation work, and experimental data in Refs. [58–61]. A summary of these effects is presented in Table 4.5. It is important to note that this simulated barrier layer optimization does not account for the dependency of layer quality and robustness on layer thickness. Layer quality and robustness cannot be effectively modeled for simulation, however those parameters are of critical importance and will depend on device structure as well as growth conditions.

Table 4.5: Summary of Factors Influenced by AlGaN Barrier Thickness.

	N_{2DEG}	$I_{G-leakage}$	V_{th}	**Vertical ε-field**	**Punch-through**	V_{BR}
$as\ t_{Barrier} \uparrow$	$\uparrow$	$\uparrow$	$\downarrow$	$\downarrow$	$\uparrow$	$\downarrow$

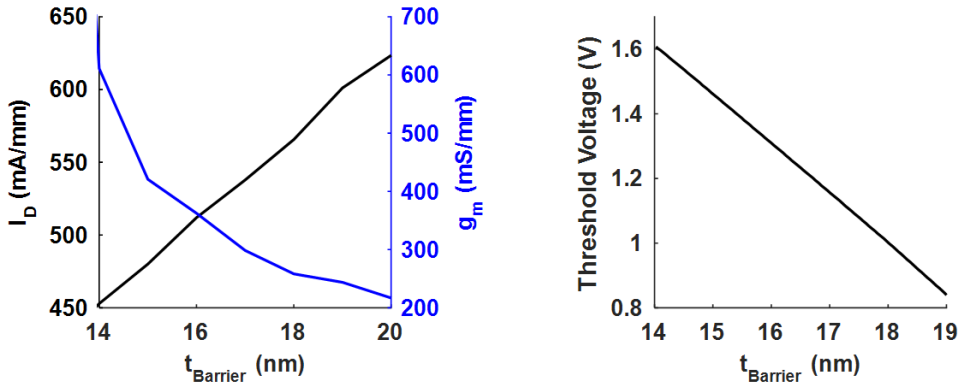


Figure 4.6: Simulation results for $t_{Barrier}$ presenting (a) maximum drain current and transconductance as well as (b) threshold voltage trends.

Concerning device performance, the increase in 2DEG concentration resulting from an increase in $t_{Barrier}$ thickness will result in lowering $R_{DS(on)}$ as shown in Figure 4.7(b). However, the increase in 2DEG concentration resulting from increasing the barrier thickness will eventually saturate due to strain relaxation [62, 63]. Considering the effect on gate charge, it is reasonable to expect that an increase in barrier thickness would result in a decrease in gate charge. As the distance between the channel and gate increases, the capacitance between those figurative electrodes will decrease. Therefore it is valid to consider that Q_G will decrease as $Q = C \times V$. This trend is demonstrated Figure 4.7(b).

Another important factor to consider when optimizing the barrier layer is the impact of the Al molar fraction (x_{AlGaN}) in the barrier layer on device performance. Higher molar fraction is known to increase 2DEG concentration in the channel, increase carrier mobility (ideally), and also increase carrier confinement [59]. However, fabricating AlGaN layers with molar fraction above 0.3 is challenging due to the large lattice mismatch between GaN and AlN [64, 65]. Consequently, the poor quality barrier layer resulting from a high molar fraction AlGaN layer would result in electrical degradation. Additionally, a higher molar

fraction can lead to larger interface roughness which in turn reduces electron mobility. Considering this, the most optimum design for an AlGaN barrier layer generally targets a molar fraction between 0.2 - 0.3. Within this range, increasing the molar fraction results in an increase in 2DEG concentration and mobility (ignoring interface roughness) which will yield a reduction in $R_{DS(on)}$ as a result. Accordingly, as the on-state resistance drops, the breakdown voltage will follow. The drop in gate charge can be attributed to a decrease in capacitance partially due to the increased molar fraction, which consequently leads to a drop in threshold voltage as well. This decrease in capacitance is due to the change in permittivity (eq. 4.1) as the dielectric constant is dependent on the molar fraction (eq. 4.2, where y is the molar fraction) [59]. Additionally, the gate charge waveform changes shape as the molar fraction is increased; Q_{GS} is reduced by two-thirds and V_T is reduced by 0.9 V causing an overall decrease in gate charge as molar fraction is increased. These trends are displayed in Figure 4.8.

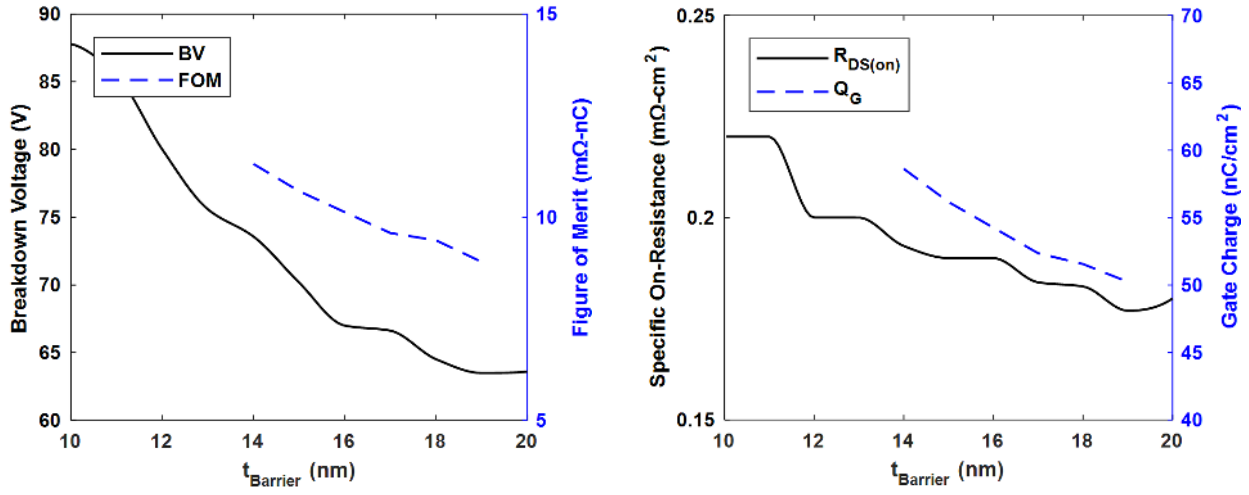
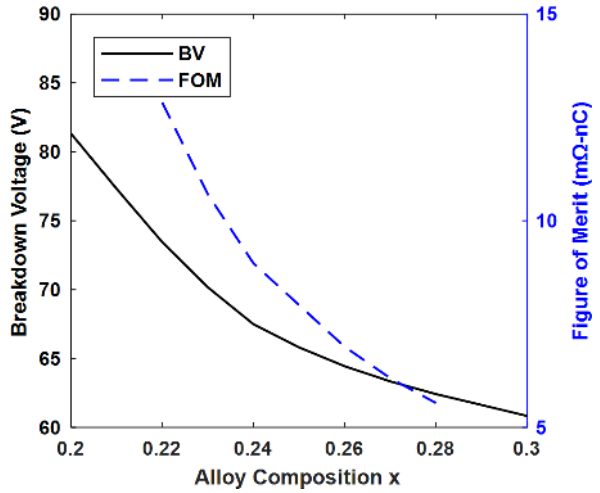
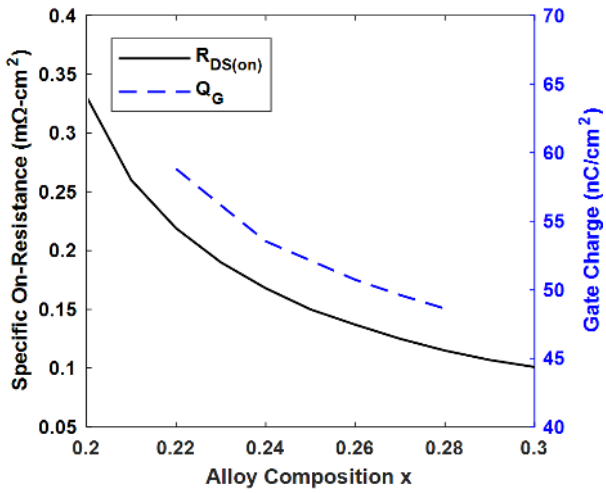


Figure 4.7: Simulation results for $t_{Barrier}$ presenting (a) breakdown voltage and FOM trends as well as (b) on-state resistance and gate charge trends.



(a)



(b)

Figure 4.8: Simulation results for x_{AlGaN} presenting (a) breakdown voltage and FOM trends as well as (b) on-state resistance and gate charge trends.

$$C_{AlGaN} = \varepsilon_{AlGaN} / t_{AlGaN} \tag{4.1}$$

$$\varepsilon_{AlGaN} = (8.9 - 1.9y)\varepsilon_y \tag{4.2}$$

4.3.3 AlN Interlayer Optimization

After investigating the impact on barrier layer thickness and aluminum molar fraction, it is natural to suggest the use of an AlN interlayer to reap the benefits of a high Al content barrier layer without the drawbacks associated with it. The primary reason why high molar fraction AlGaN layers are not used is due to the large lattice mismatch causing structural issues and leading to electrical degradation. However, adding an AlN interlayer alleviates this issue as the interlayer can be kept below a critical thickness that would cause

lattice mismatch to affect the structure growth or cause strain relaxation [66]. Adding an AlN interlayer can improve 2DEG concentration, help to reduce vertical leakage current (depending on the thickness of the layer), increase carrier mobility, and improve carrier confinement [64, 66, 67]. These effects can have a significant impact in device performance in regards to breakdown voltage, on-state resistance, and gate charge as seen in Figure 4.9. The addition of an AlN interlayer serves to lower the FOM, however the thickness of the interlayer is critical concerning the impact on breakdown voltage as an interlayer that is too thick can precipitously lower breakdown voltage performance. In our simulation, depositing a uniform AlN interlayer thicker than 3 nm can result in blocking all vertical current across that region rendering the device inoperable. This is the result of how AlN is defined in the simulation model, and is in contrast to most literature on AlN/GaN devices where the critical thickness can be as high as 9 nm [68]. In most cases, the critical thickness is a factor of lattice mismatch between the two materials, however, this cannot be effectively modeled in simulation. Results from our simulations suggest significant improvement in performance with the addition of an ultra-thin interlayer.

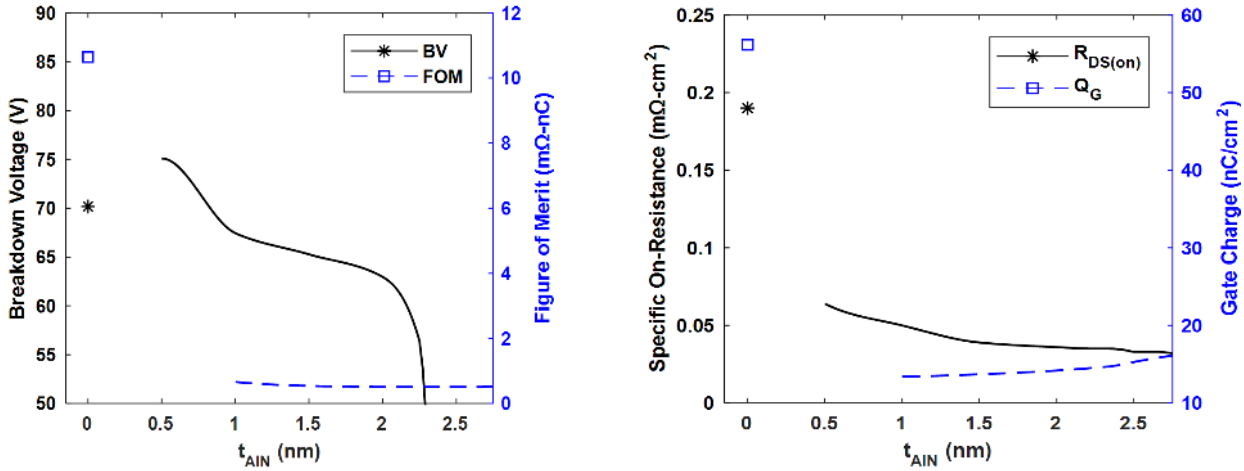


Figure 4.9: Simulation results for t_{AlN} presenting (a) breakdown voltage and FOM trends as well as (b) on-state resistance and gate charge trends.

The significant drop in $R_{DS(on)}$ seen in Figure 4.9(b) when adding an AlN interlayer can be attributed primarily to the significant increase in 2DEG density. Simulation data shows a four-fold increase in electron density in the channel as a result of adding a 1.5 nm AlN layer as shown in Figure 4.10. This increase in 2DEG density is also supported in other works, although the change is not as severe as it is here [64]. In addition, the increase in mobility due to the AlN interlayer will also serve to reduce $R_{DS(on)}$. Concerning the impact on gate charge as seen in Figure 4.9(b), the addition of an insulator material (with a similar dielectric constant to the surrounding material) between the gate and channel will serve to lower the gate capacitance, and thereby the gate charge, by adding a series capacitance. As the AlN layer becomes thicker, this capacitance will be reduced further and gate charge should continue to decrease. However, the simulation data shows a slight increase in gate charge as t_{AlN} increases, which suggests the added series capacitance is not the most significant factor. According to gate charge plots, Q_{GS} and V_T are both reduced with the addition of an interlayer. In addition, adding an interlayer significantly changed the gate charge waveform and nearly eliminates the miller plateau. This is what causes the significant reduction in gate charge.

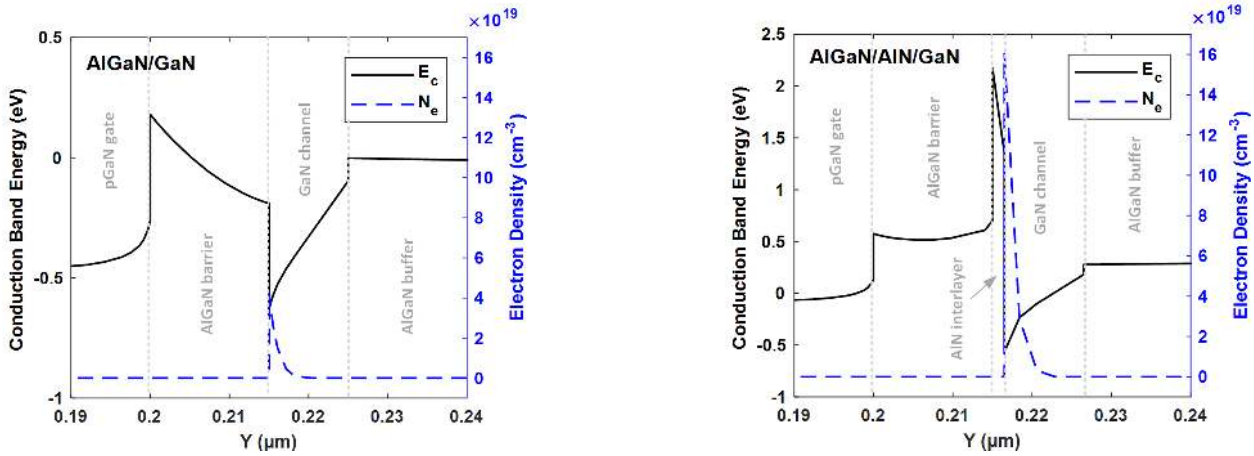


Figure 4.10: Simulation results showing conduction band energy and electron density in the on-state for devices with (a) no AlN interlayer and (b) with a 1.5 nm AlN interlayer.

As seen from this data, it is advantageous from a performance perspective to add an AlN interlayer, and it is crucial to target an interlayer thickness between 0.5-1.5 nm. While an AlN interlayer can reduce interface roughness, a thicker AlN interlayer is undesirable as it will lead to structural degradation due to partial strain relaxation [66]. Lastly, for RF devices, the addition of an AlN interlayer can cause certain reliability issues under RF stress conditions [69].

4.3.4 Buffer Layer Optimization

Buffer layer optimization is critical to obtain high breakdown voltage and device reliability as an increased buffer thickness leads to lower dislocation density in the channel, and higher breakdown voltage due to suppressed vertical leakage and buffer leakage current. Additionally, due to the reduced defect density near the channel and improved surface morphology, the mobility and on-state resistance show improvement as a result of the thicker buffer layer [70]: one causing charged line scattering and the other interface roughness scattering.

However, breakdown voltage optimization for buffer layer thickness comes with a set of challenges as there are many competing factors that influence breakdown trends. For example, high voltage devices are generally known to increase in breakdown voltage as buffer thickness increases, this is generally due to the dominate breakdown mechanism being substrate breakdown. Alternately, low voltage devices can have a negative trend if the dominant breakdown mechanism is due to trapping. As device dimensions scale towards low voltage device design ($<$ 100 V) the dominant influence on breakdown voltage can shift, leading to results contrary to conventional understanding. Conventional understanding of breakdown voltage trends is well detailed in Ref. [38,70] and a detailed discussion on the impact of buffer thickness concerning low voltage design can be found in our work in Ref. [44]. As this topic has been extensively covered in the past, we choose to

present only this brief overview of buffer layer optimization and the underlying challenges as opposed to an in-depth analysis.

4.4 Conclusion

We have presented optimization trends for channel layer thickness, barrier layer thickness and molar fraction, impact of an AlN interlayer, and a brief discussion on buffer layer thickness. This fabless design approach is unique in that it targets a design approach for low voltage (< 100 V) GaN power devices. The optimization of the channel layer thickness showed advantageous properties for low voltage devices. Increasing the channel thickness not only increased breakdown voltage but also lowered the figure of merit. In contrast, the optimization curves for the barrier thickness and molar fraction showed a trade-off between high voltage and low FOM. However, for power electronics design, increasing the barrier thickness is beneficial as it increases the maximum drain current, which will increase the power density. The addition of an AlN interlayer with a targeted thickness between 0.5-1.5 nm results in similar breakdown performance but a vastly improved FOM. Simulations from Sentaurus gave critical insight into the optimization curves, and act as an aid for heterostructure design.

CHAPTER 5: GAN HEMT FABRICATION

A fabrication process flow has been developed for fabricating Schottky-gate, and MIS-HEMT structures at UCF in the CREOL cleanroom. The fabricated devices were designed to validate the simulation work for low voltage GaN devices. The UCF fabrication process is done with a four layer mask, and consists of mesa isolation, ohmic recess etch, an optional gate insulator layer, ohmic metallization, and gate metallization. Following this work, the fabrication process was transferred to the National Nano Device Laboratories (NDL) in Hsinchu, Taiwan, to take advantage of the more advanced facilities there. At NDL the fabrication process was done with an eight layer mask, which allowed for inclusion of a gate field-plate structure, bilayer passivation, and pad metallization. Devices were primarily fabricated on 6" GaN-on-Si wafers procured from Episil.

This chapter outlines the fabrication process at UCF, and summarizes the continued effort at the lab in Taiwan.

5.1 UCF HEMT Fabrication Process

The process for fabricating depletion-mode GaN HEMTs includes the following process steps:

- Mesa isolation
  - Can be done by etching or ion-implantation.
- Gate dielectric

  - Required for MIS-HEMTs. Can be Al_2O_3 or Si_3N_4.

- Ohmic metallization
  - Typically Ti/Al/Ni/Au.
- Gate metallization
  - Typically Ni/Au.
- Passivation
  - Typically Si_3N_4.

Mesa isolation is critical to prevent leakage from source to drain (around the edge of the gate), and is also used to prevent cross-talk when operating multiple devices. For our devices at UCF, the mesa was achieved by Cl_2/Ar etching with ICP-RIE. For proper isolation, the GaN channel is etched completely through; although depending on the conductivity of the channel layer, it may be sufficient to etch through the 2DEG region. This process is shown in Figure 5.1 step 2.

For our devices, an ohmic recess etch was added as an optional step, which was intended to improve $R_{DS(on)}$ performance. This process is shown in Figure 5.1 step 3. Following the ohmic recess etch, ohmic metallization is performed using an E-beam evaporator to deposit Ti/Al metal followed by lift-off to form contacts as seen in Figure 5.1 step 4. Next, gate metallization is performed using the E-beam evaporator to deposit Ni/Au in both the gate and source/drain regions as seen in Figure 5.1 step 5. The ohmic contact metal layers were divided up like this to conserve gold, so that gold would only need to be deposited once. Following the metallization, the contacts were annealed in a rapid thermal annealer (RTA) at 700 °C for 60 sec. in a nitrogen ambient. This is done to make the source/drain contacts ohmic or semi-ohmic.

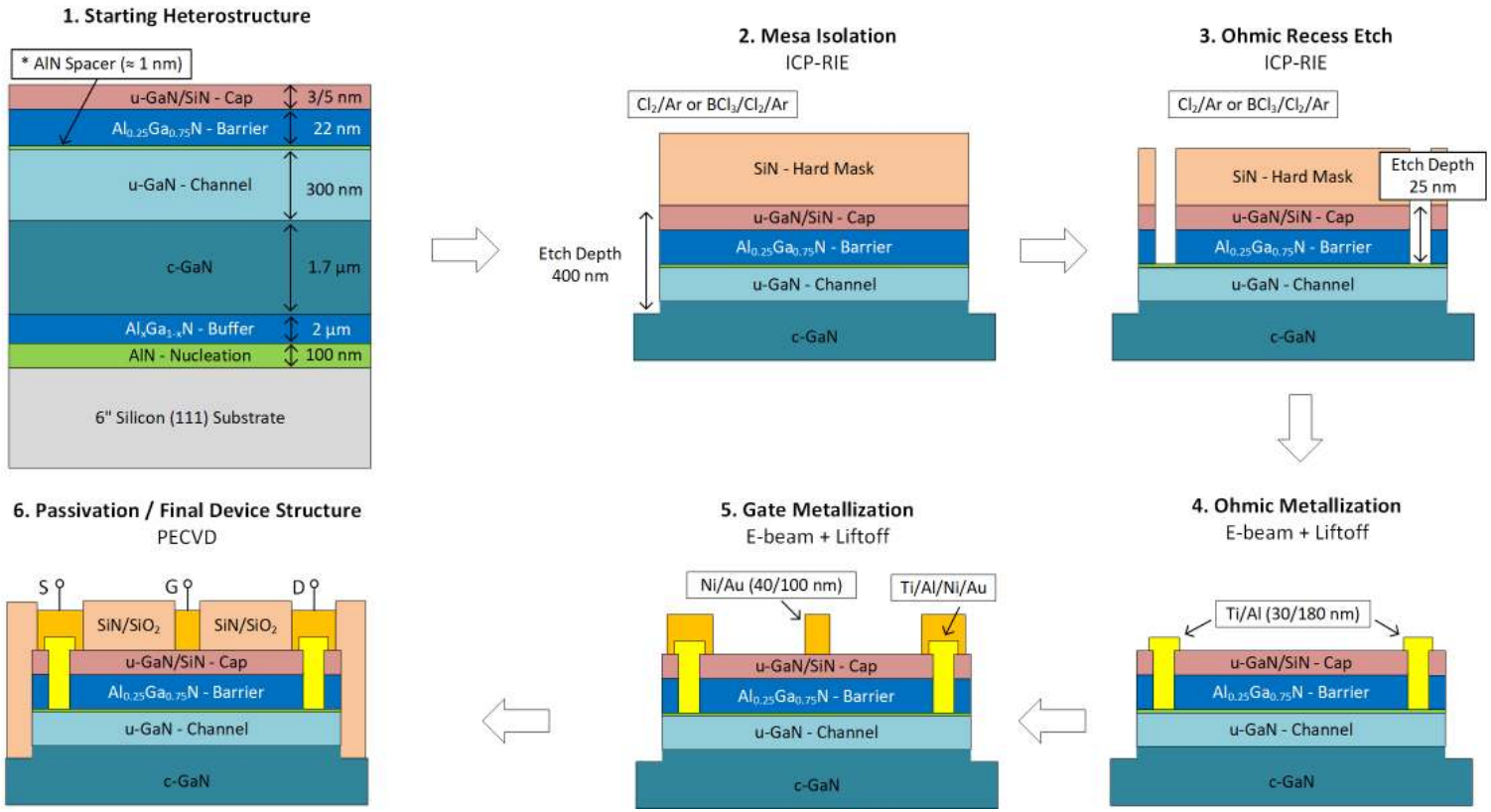
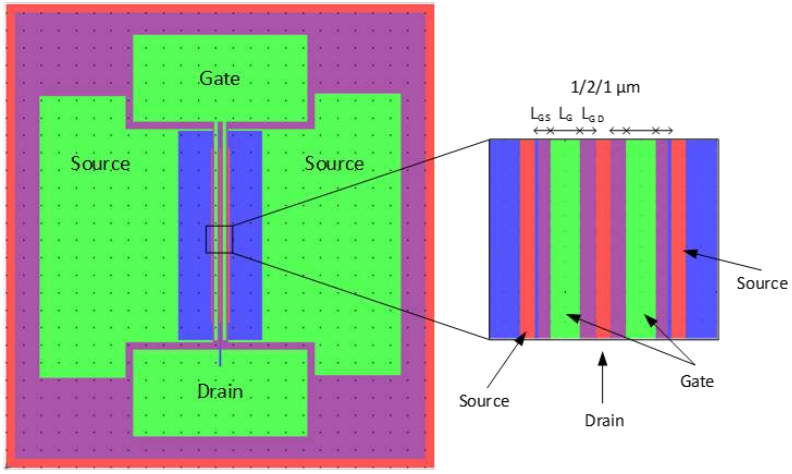


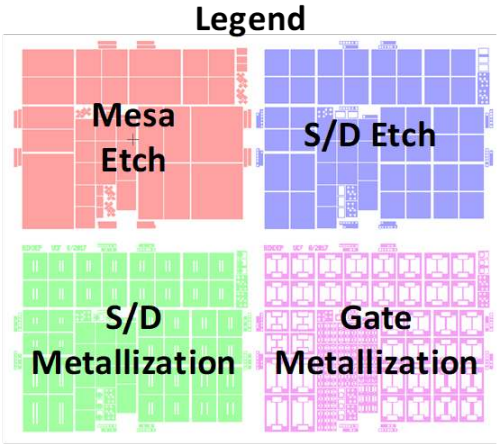
Figure 5.1: A simplified fabrication process flow for the UCF Schottky-gate GaN HEMTs.

The high temperature anneal allows the Ti on the surface to interact with the GaN, forming TiN, which lowers the barrier height giving semi-ohmic performance from the contacts.

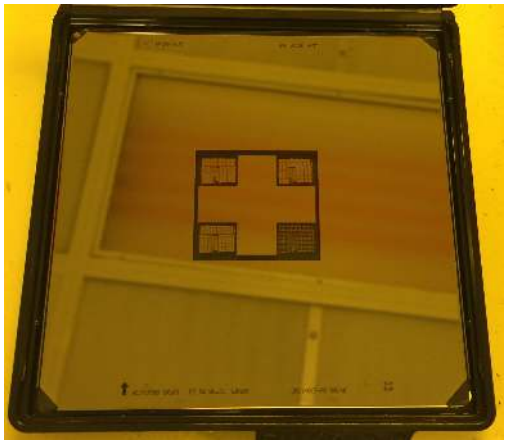
The devices fabricated at UCF employed a double finger design with one drain, two gates, and two source terminals as shown in Figure 5.2(a). This serves two purposes as it doubles the maximum drain current, and also helps with yield as it can be tested as two devices in parallel. The mask legend and physical mask plate for the UCF HEMT design can be seen in Figure 5.2(b) and 5.2(c). The full mask and fabricated devices are shown in Figure 5.3.



(a)

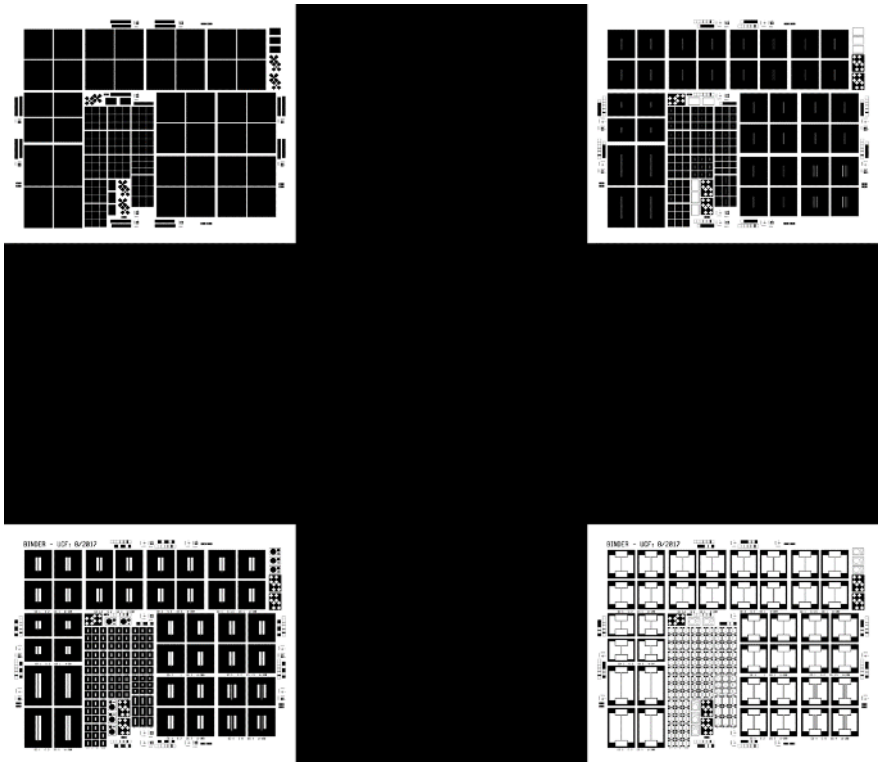


(b)

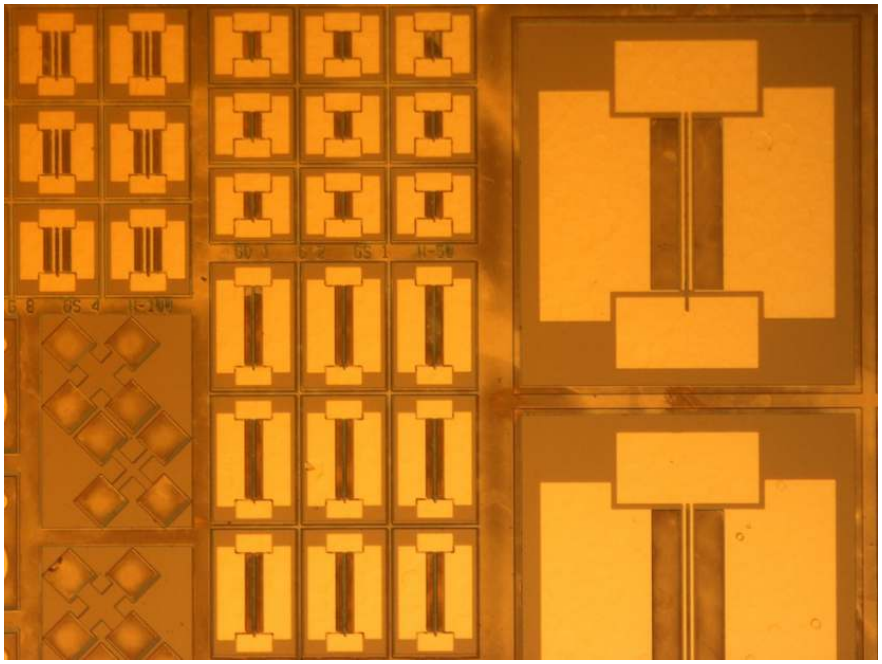


(c)

Figure 5.2: (a) Double finger mask design for UCF HEMTs, (b) mask legend for the UCF HEMT four layer mask, and (c) UCF GaN HEMT photomask on 4" quartz plate.



(a)

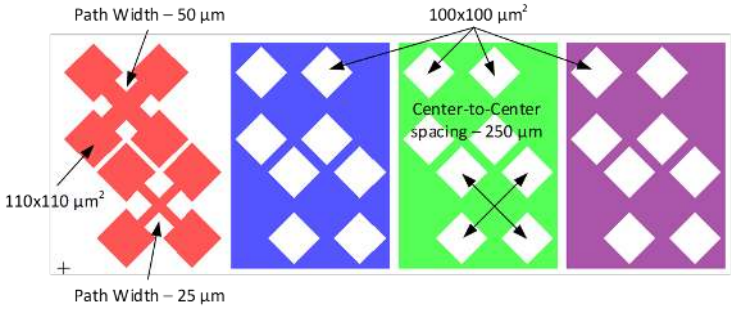


(b)

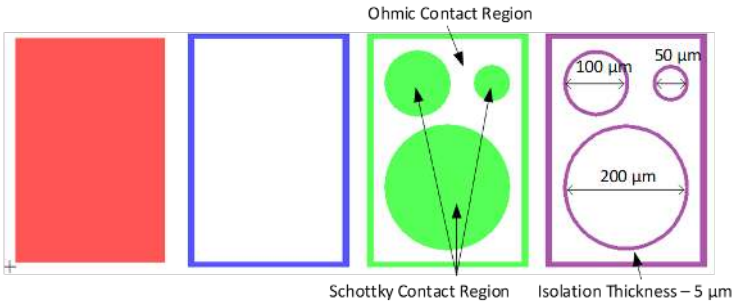
Figure 5.3: (a) Actual four layer mask design image and (b) microscope image of UCF devices after all fabrication steps are complete.

5.1.1 UCF Mask - Test Structures

The UCF mask contains 148 HEMTs, plus 6 types of test and verification structures. These test structures include hall-effect and junction diode test structures (as shown in Figure 5.4), which can be used to determine sheet carrier concentration and carrier mobility. In addition, we have included a transmission line measurement (TLM) test structure for determining sheet resistance, contact resistance, and contact resistivity (as shown in Figure 5.5(a)). For alignment calibration, we have included alignment test structures with vernier marks for quantification of misalignment with 0.25 µm tolerance (Figure 5.5(b)). Finally, we have included profile/height test structures for verifying etch depths and metal heights, and have also included a lithography linewidth test structure to check exposure and also used to qualify the mask design from the manufacturer (Figure 5.5(c) and 5.5(d)).

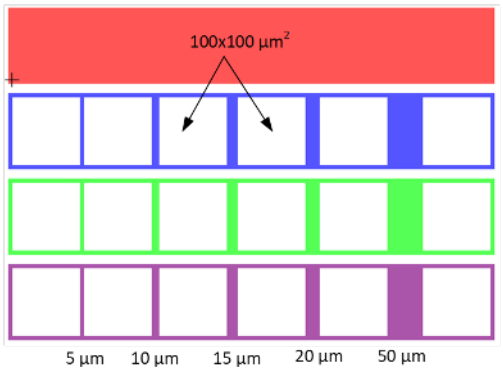


(a)

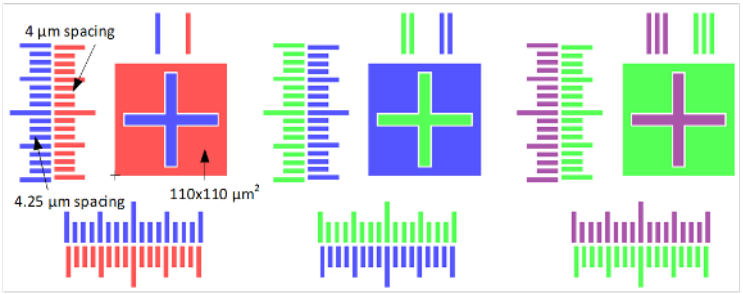


(b)

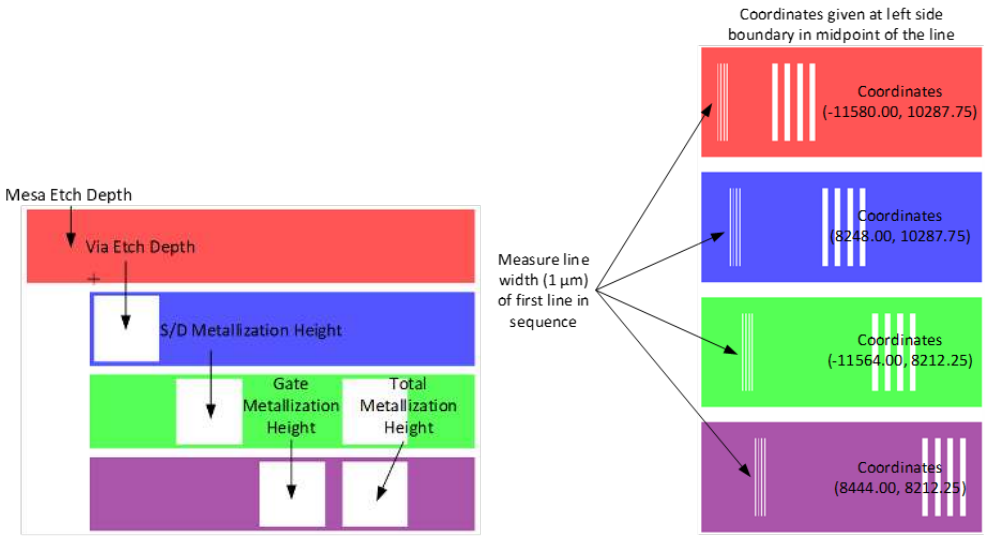
Figure 5.4: (a) Hall-effect test structure and (b) Schottky junction diode test structure.



(a)



(b)



(c) (d)

Figure 5.5: (a) TLM test structure, (b) alignment test structure, (c) profile/height test structure, and (d) linewidth test structure.

The goal of the UCF fabrication was to calibrate the simulation models by providing a comprehensive set of devices with varying features. To do this, there were twelve basic HEMT structures designed. Each of those structures was in a 3x3 cell, to account for yield issues. The minimum feature size was 1 μm, and each mask layer is approximately 1 cm^2 for chip-scale processing. This led to 148 devices per chip, with variations in L_{GD}, L_G, L_{GS}, device width, and L_{drift}. Finally, a set of devices on the mask were scaled 400% to account for lithography processing issues.

Exact processing details are given in APPENDIX: UCF FABRICATION PROCESSING STEPS.

5.2 NDL Fabrication Process

We built off our fabrication experience at UCF to fabricate GaN MIS-HEMTs at the National Nano Device Laboratories in Hsinchu Taiwan. Whereas the UCF process used a 4-layer mask, the NDL process used an 8-layer mask which allowed for bilayer passivation, addition of a gate field-plate structure, and pad metallization. The bilayer passivation was necessary to lower film stress, as stress accumulation on wafer-scale production is a significant issue that is not seen during chip scale production like what is done in the UCF cleanrooms.

The process for fabricating GaN MIS-HEMTs at NDL is as follows:

- Mesa isolation
  - Done by dual-energy Ar ion-implantation.
- Ohmic metallization
  - Ti/Al/Ni/Au.

- Gate recess/gate dielectric/hard mask
  - Gate dielectric is Al_2O_3. Hard mask is Si_3N_4.
- Hard mask opening
  - ICP-RIE etching.
- Gate metal (+Field-plate)
  - Ni/Au metal plus bilayer passivation (Si_3N_4/SiO_2)
- Contact hole #1
  - Etch passivation to create a window for metal contacts.
- Pad metallization
  - Au/Al/Au or similar metal plus passivation.
- Contact hole #2
  - Etch passivation to create a window for metal contacts.

This fabrication process is shown in Figure 5.6, with the red dotted line showing the active process area during each step. The devices shown in Figure 5.6 are single finger MIS-HEMTs; in addition to these devices, the mask contained many of the same test features used on the UCF mask, and also had many different device types including high current designs for 10 A devices.

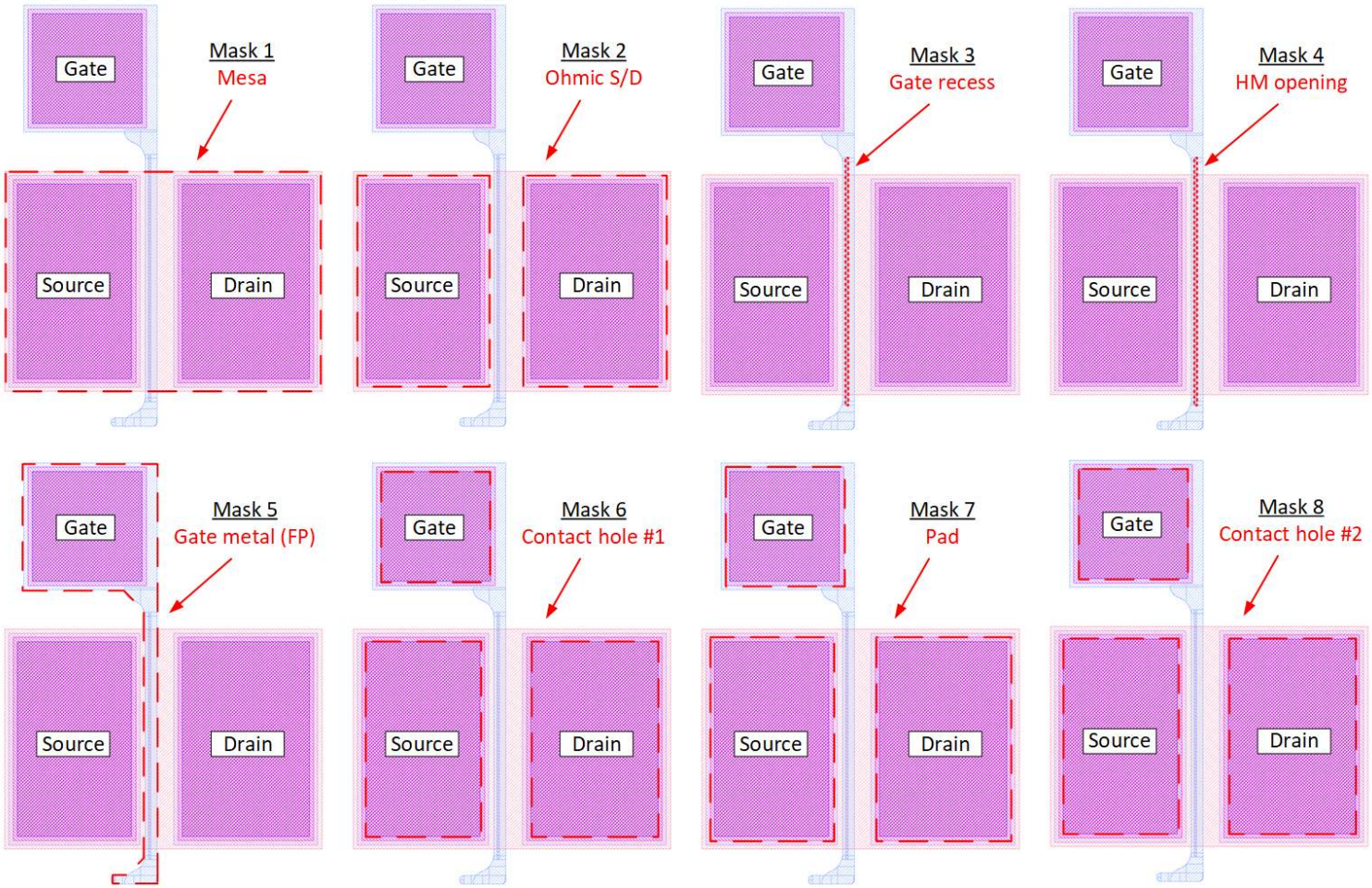


Figure 5.6: The 8-layer mask used at NDL for HEMT fabrication.

For wafer-scale processing, the 6" Si wafer is divided up into 32 dies that are processed using an i-line stepper. Between the individual dies are alignment markers which are placed on mask 0. An example of these alignment markers is depicted on a drawing showing a four die arrangement with alignment markers on a wafer (Figure 5.7)

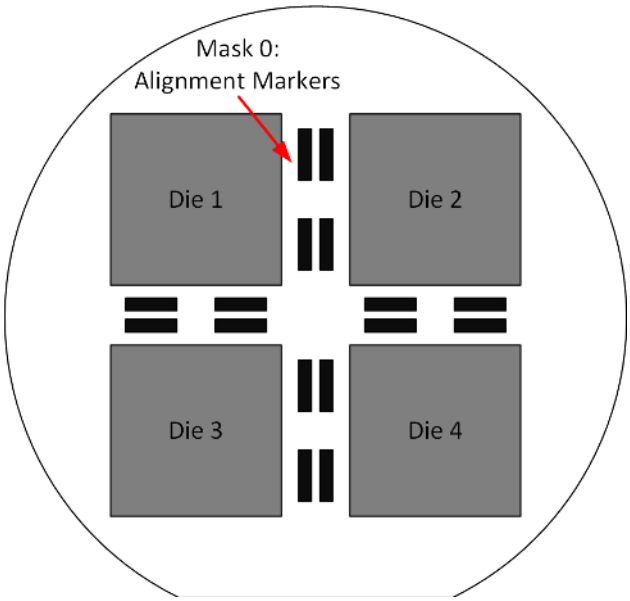
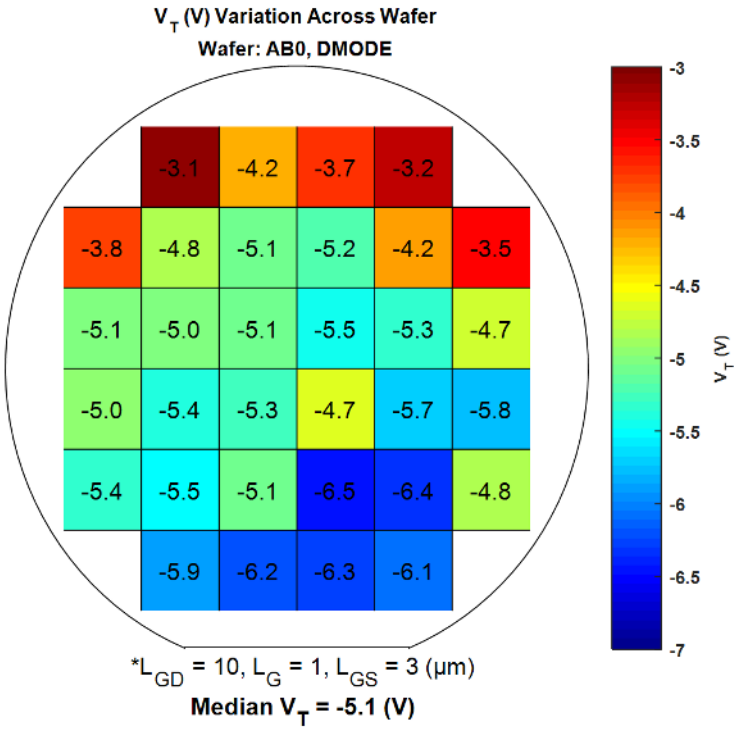
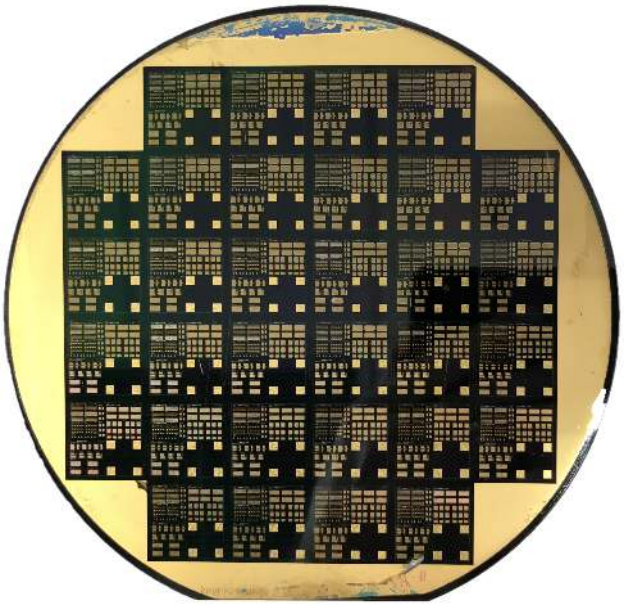


Figure 5.7: Example drawing of mask 0 with sample alignment marker blocks.

One of the advantages of wafer-scale production is that it gives insight into critical aspects of quality control challenges. Wafer mapping allows us to evaluate process uniformity. Typically wafer mapping was done for threshold voltage, transconductance, and on-state resistance after processing. Figure 5.8(a) gives an example of wafer mapping done on NDL wafer AB0. This threshold voltage mapping shows significant variation in threshold voltage at the top and bottom edge of the wafer. This suggests there is some non-uniformity in gate dielectric deposition. Meaning that dielectric deposition for the top row of dies is very thin, and the bottom row deposition is thicker than the nominal value. The median threshold voltage was -5.1 V, and the top row of devices showed a threshold voltage as low as -3.1 V which is indicative of a Schottky-gate HEMT with a very thin dielectric. A wafer image of AB0 is shown in Figure 5.8(b).



(a)



(b)

Figure 5.8: (a) Threshold voltage mapping of NDL wafer "AB0" for d-mode devices and (b) wafer image of AB0.

5.3 Fabrication Results

5.3.1 UCF Devices

The UCF devices were fabricated successfully showing a threshold voltage of -4.7 V for MIS-HEMT devices with a 20 nm SiN insulator, and a threshold voltage of -0.9 V for Schottky-gate HEMT devices with no gate insulator. A device is shown in Figure 5.9 showing the features of each mask layer. Standard I_D-V_D, I_D-V_G, and I_G-V_G curves are shown in Figure 5.10. For these devices, due to the design of the mesa, a drain current leakage path formed causing significant current leakage. This leakage current is normalized and removed from the drain current plots shown in Figure 5.10 and the issue was corrected in the next mask revision by shrinking the mesa isolation to remove the leakage path around the gate.

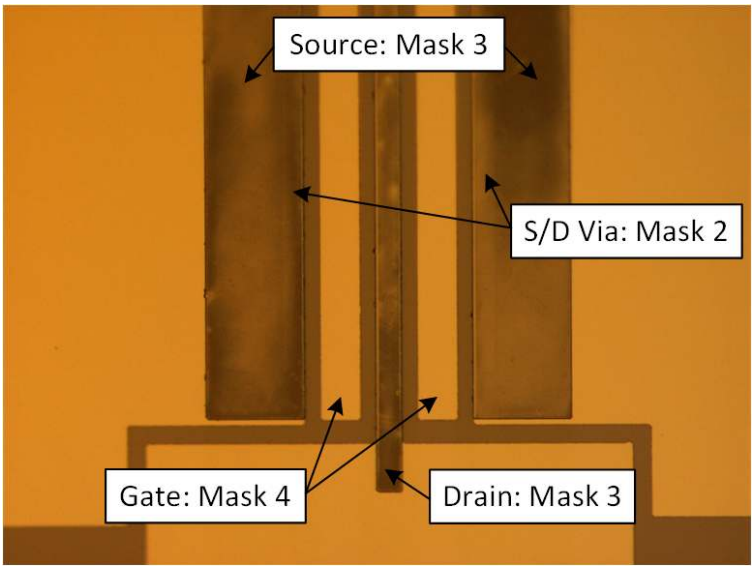
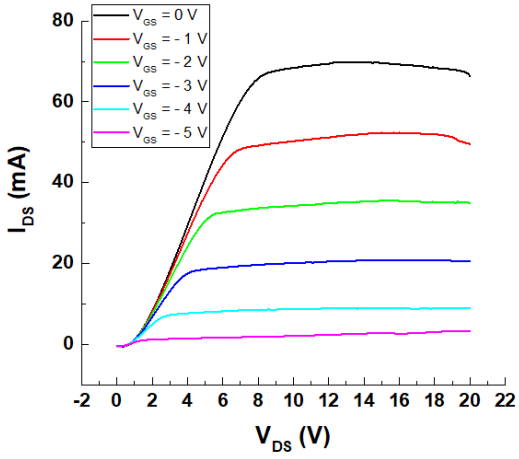
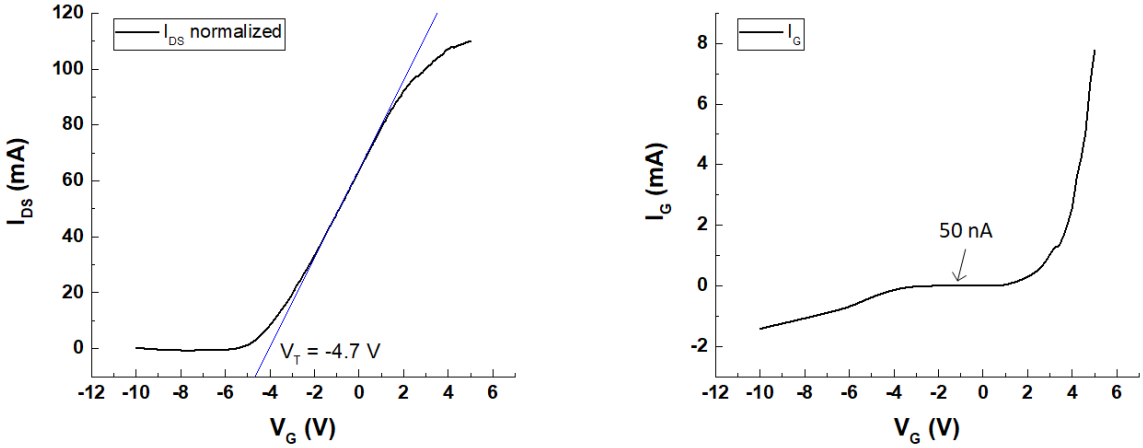


Figure 5.9: UCF GaN HEMT before high temperature annealing, showing features from each mask layer.



(a)



(b) (c)

Figure 5.10: Curves for UCF d-mode MIS-HEMT devices showing (a) normalized drain current versus drain voltage curves, (b) normalized drain current versus gate voltage plot, and (c) gate current versus gate voltage plot.

5.3.2 NDL Devices

Curves for an NDL MIS-HEMT device from wafer AB0 are shown in Figure 5.11: presenting I_D-V_D, I_D-V_G, I_G-V_G, and transconductance plots. The NDL devices have a 15 nm Al_2O_3 dielectric, yielding a median threshold voltage of -5.1 V.

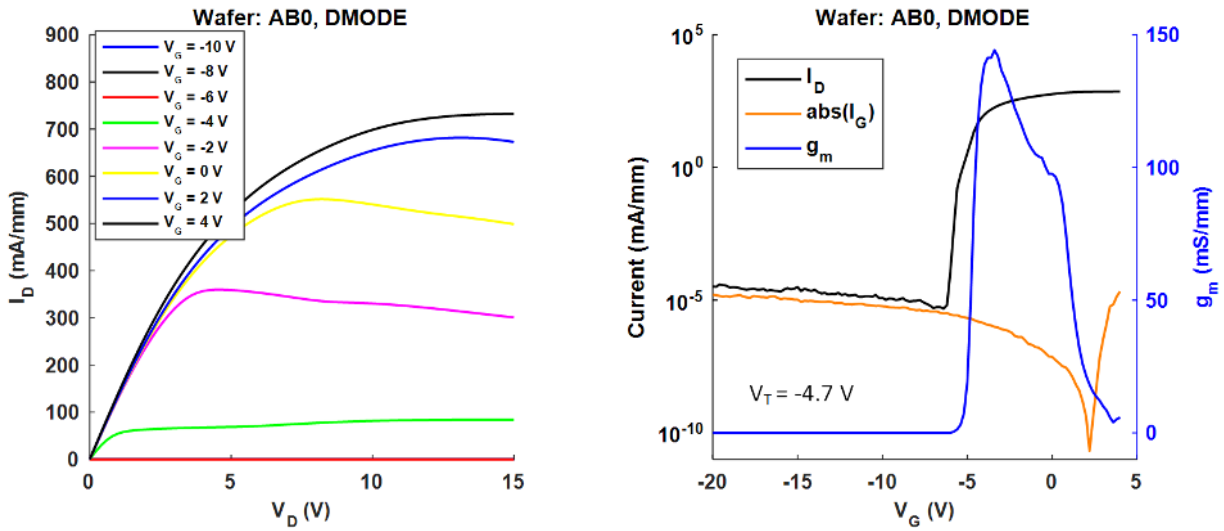
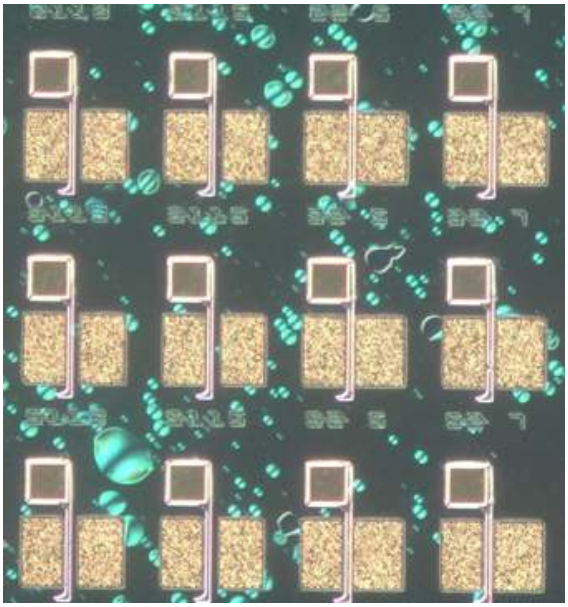
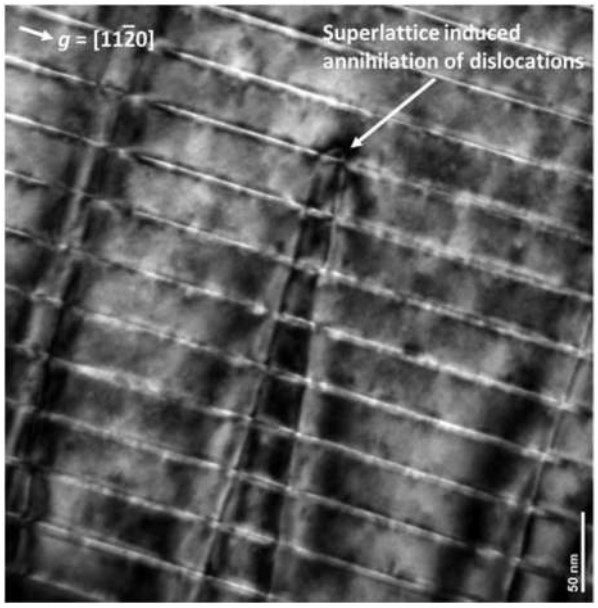


Figure 5.11: Curves for NDL d-mode MIS-HEMT devices showing (a) plot of drain current versus drain voltage, and (b) plot of drain and gate current and transconductance versus gate voltage.

The Taiwan devices showed significant passivation peeling and pitting as a result of stress accumulation on the surface (Figure 5.12(a)). Poor passivation quality results in a high concentration of surface states, leading to current collapse. These wafers were extremely fragile as a result of the high stress growth process. One method to address this issue is to use a superlattice buffer structure which acts as a stress-relief layer and can reduce surface stress by one to two orders of magnitude. Figure 5.12(b) shows how the superlattice buffer structure can also reduce dislocations in the channel by terminating propagating defects in the buffer structure. In addition, a structure with lower stress will also have a lowered defect density. Based on these observations, it is recommended that a superlattice buffer structure should be used for these devices in the future. This would significantly reduce much of the defect-induced performance degradation that is seen with these devices (presented in the next chapter).



(a)



(b)

Figure 5.12: (a) NDL devices showing passivation layer pitting and peeling on the surface and (b) superlattice induced annihilation of dislocations.

5.4 Conclusion

The UCF fabrication effort served as a proof of concept for fabrication in the CREOL cleanroom. Both Schottky-gate HEMTs and MIS-HEMTs were successfully fabricated at UCF using a 4-layer mask. This fabrication process was transferred to the NDL facilities to take advantage of a more mature process-flow. At NDL, an 8-layer mask was used to fabricate MIS-HEMTs on 6" Si wafers. These devices were used to calibrate our simulation models, and it is on these devices that the trap-induced defect study is done; this study is presented in the following chapter.

This extensive fabrication work led to some observations on current fabrication challenges for GaN HEMTs. First, there is a need for Au free contracts, which is a limitation imposed by silicon based cleanrooms. This is because Au serves as a deep level trap for silicon processing. GaN devices many times use Ti/Al/Ni/Au for ohmic contacts to achieve low

contact resistance, and this metallization scheme is especially popular among research institutions. While there is work being done on Au free contacts, the work is not mature enough to be widely adopted, and hence GaN processing (when using Au based contacts) is restricted in silicon fabs. The cost of fabricating GaN devices would be lessened if the need for duplicate dedicated processing equipment could be eliminated.

The second challenge is that GaN heterostructure design shows trade-offs in terms of performance/reliability and thermal conductivity. For high performance devices, the defect density in the heterostructure needs to be reduced, and surface stress needs to be minimized to improve passivation adhesion. One way to do this is by using superlattice stress relief layers, which not only reduces stress but also reduces defect density and can suppress propagating defects. The superlattice structure has reduced thermal performance compared to a graded buffer structure, so while reliability will be improved, power density will be reduced. In order to address the thermal performance issue, it may be prudent to consider switching from silicon wafers to silicon carbide wafers as they have for RF GaN HEMTs. However, SiC wafers cost significantly more than Si wafers, which presents a thermal performance vs. cost trade-off.

Lastly, as some of this research has been done on low voltage GaN devices, it has been seen that to extract the full potential of low voltage design it may be necessary to use higher resolution lithography equipment than is typically used for power devices. Sub-micron lithography is necessary for 30 V breakdown devices to fully reap the benefits of using GaN, possibly requiring features less than 0.5 μm. As an i-line stepper may have a global alignment tolerance of ≤ 0.25 μm this poses a challenge for the fabrication of low voltage power HEMTs.

CHAPTER 6: EXPERIMENTAL RESULTS AND TRAP INDUCED PERFORMANCE ANALYSIS

This chapter covers the experimental results of our fabricated devices, and includes a discussion on trap induced performance analysis for GaN HEMTs.

Negative differential conductance (NDC) seen in the drain current saturation region is typically attributed to self-heating effects in GaN HEMTs. In this chapter, it is demonstrated that NDC is due to trap states in the buffer resulting from poor carrier confinement in the channel during saturation which leads to stray electrons exiting the channel and becoming trapped. Substrate bias testing has been used to confirm that severe current collapse occurs when those electrons are forced to the surface, and that NDC occurs when the carriers are forced to the buffer. In addition to this, pulsed I-V characterization is performed among other tests to isolate the cause of NDC in the saturation region, which effectively eliminated trapping mechanisms that lead to gate- and drain-lag from contributing to NDC. To the best of our knowledge, we are the first to report NDC not as a result of self-heating, but due to trapping within the buffer.

6.1 Introduction

Wide bandgap GaN power devices deliver superior performance in terms of power density and efficiency for power electronics systems due to materials advantages such as higher electron mobility, high critical electric field, and a large bandgap in comparison to conventional silicon based electronics [10,71,72]. Fabrication costs are continually reduced as

GaN-on-Si scales to larger-diameter epi-wafers (now up to 8-inch), which makes GaN integration even more desirable [18,73]. Despite these advantages, GaN high electron mobility transistors (HEMTs) suffer from performance and reliability degradation as a result of trap centers that capture free electrons and have a varying release time. These trap centers are a result of poor structural quality, defects caused by lattice/thermal mismatch, surface states, and buffer dopants. Traps within the device are responsible for current collapse (dynamic $R_{DS(on)}$), knee-walkout, current slump, and other phenomena contributing negatively to device performance and reliability [74,75]. These effects can be mitigated by reducing the trap concentration primarily on the surface and in the buffer. Surface states can be reduced by advanced passivation techniques, such as charge polarized AlN/SiN surface passivation as demonstrated by Chen *et. al* [76]. In addition, field plate techniques can be effective in suppressing surface trapping by reducing the peak electric field at the drain-side gate edge [43,77–79]. Buffer traps can be minimized by using superlattice stress relief layers in the buffer to halt the propagation of defects due to lattice mismatch between the buffer and substrate layers [34,80], however even with this technique there still exists an ample trap concentration in part due to intentionally incorporated compensation dopants in the buffer layer (e.g., C) used to obtain a high resistivity buffer stack [21,81]. To understand the impact on breakdown and reliability, it is crucial to study defect induced performance degradation and to develop ways to further mitigate the effects of carrier traps.

This work focuses primarily on effects seen in the drain saturation current such as the negative differential conductance (NDC) effect, the kink effect (a current collapse phenomena), and substrate biasing effects on trap distribution. A detailed analysis of dc and pulse I-V characteristics is carried out for GaN HEMT devices with a focus on effects resulting from trapping in the device. In addition, substrate biasing, also called back-gating measurement, has been performed to study the influence of trap distributions (surface vs. buffer traps) on current collapse and NDC.

6.2 Device Structure and Fabrication Details

Devices were processed on a commercially available 6″ GaN-on-Si epi-wafer. The epitaxial structure was grown on a p-type Si substrate and consists of an AlN nucleation layer, graded AlGaN buffer layer, GaN channel layer, AlGaN barrier, and a GaN cap. The passivation layer consists of a bilayer SiN/SiO_2 stack to reduce film stress and provide improved isolation. Device isolation is achieved by multi-energy argon ion implantation. Drain and source Ohmic contacts consist of a Ti/Al/Ni/Au metal stack annealed at 875 °C for 30 seconds in a N_2 ambient. The MISHEMT gate structure consists of a 15 nm ALD deposited Al_2O_3 dielectric with a Ni/Au Schottky gate contact. These devices have a single-finger gate layout with a gate width of 100 μm and a gate connected field plate extending 2 μm towards the drain.

Measurements presented in this paper were performed on a device with dimensions of 2-1-13 μm for L_{GS}, L_G, and L_{GD} respectively. All measurements presented in this paper were repeatable both on the same device and also on devices with different lateral dimensions. Additionally, all measurements are conducted at room temperature and in a dark environment, as light irradiation could affect trap behavior within the device [82,83].

6.3 Results and Discussion

Pulse I-V characterization is typically performed to eliminate self-heating effects. Self-heating is commonly known to be responsible for negative differential conductance, a negative drain current slope in the saturation region, which is generally seen in dc I_D-V_D curves for GaN power devices. The decrease in drain current is attributed to a decrease in electron velocity in the channel resulting from the increased lattice temperature [84]. By pulsing the drain current, the built-up heat can be effectively dissipated between pulses

and self-heating effects can be eliminated or significantly reduced given that the duty cycle is sufficiently low [85,86].

In addition, pulse I-V characterization can be used to study gate-lag and drain-lag [87] due to traps within the device which cause reduced drain current and increased knee voltage respectively [88]. Gate- and drain-lag are definied by the response of the drain current to a step change in gate or drain voltage. During a pulse transient, the current does not respond instantaneously to the change in voltage bias, resulting in a lag that is attributed to the presense of traps. By controlling the polarity of the applied pulse (low to high, or high to low), the trapping and de-trapping mechanism can be controlled, allowing for an indirect relationship to be obtained for the relative location and intensity of traps within the device [75,87].

6.3.1 Static versus Pulse I-V Characterization

To investigate these effects, a test bench was setup to evaluate pulse versus dc I-V characteristics. The pulse test is designed to have a pulse width of 5 ms and a pulse period of 500 ms (1% duty cycle). For the pulse tests, the gate voltage (V_{GQ}) is held at a dc value, and the drain is pulsed from a quiescent bias point (V_{DQ}) to the target test voltage. The polarity of the drain pulse determines the state of trapping or de-trapping within the device: a low-to-high pulse ($V_{DQ} = 0V$) causes trapping, and a high-to-low pulse ($V_{DQ} = 20V$) causes de-trapping. For clarity concerning the testing setup, setting the gate voltage input as a dc value or as a pulse had little to no effect on the results.

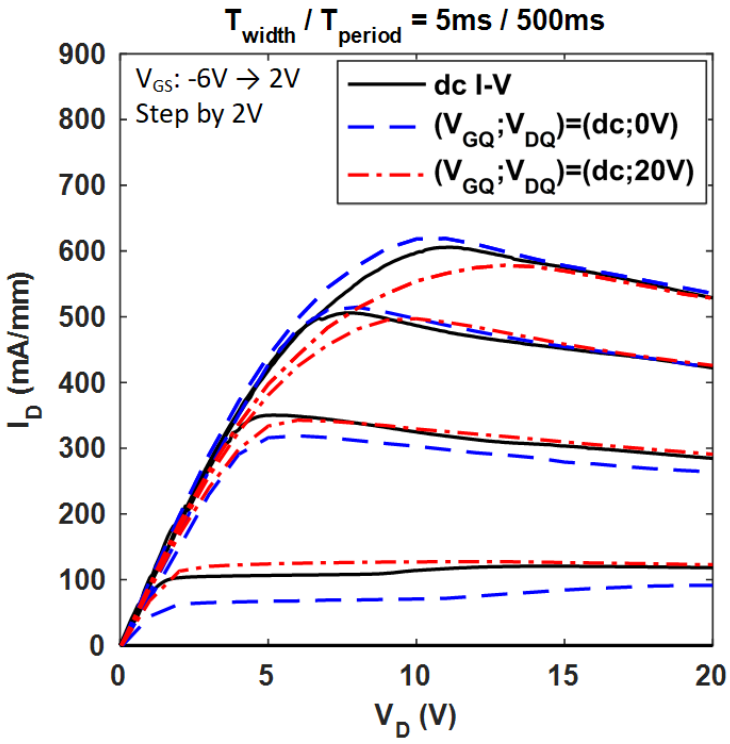


Figure 6.1: Pulse versus dc I-V characteristics for AlGaN/GaN HEMT: showing degradation due to trapping effects.

Comparing the pulse I-V to the dc test characteristics (Fig. 6.1), negative differential conductance is seen in both pulse and dc I-V tests. Pulse I-V testing can eliminate self-heating by giving the device ample time to recover from heating by applying a low duty cycle pulse where the ratio of on to off is low enough that the small amount of heat generated in the on-state is dissipated in the off-state. To reinforce that the self-heating was not present, these tests were also repeated with a duty cycle of 0.1% (10$\times$ lower) with the same results. Since the low duty-cycle pulse test showed no change in NDC compared to dc, the NDC seen in Fig. 6.1 must be caused by some effect other than self-heating. Therefore we can effectively rule out self-heating as the cause for the saturation current degradation since the NDC appears both in pulse and dc curves. Excluding self-heating as the cause for NDC, another mechanisms that could cause the NDC phenomenon is threshold voltage variation due to applied drain bias. To test this, the threshold voltage

is extracted from I_D-V_G curves, and plotted against drain voltage as shown in Fig. 6.2a. However, in reviewing Fig. 6.2a it is apparent that the threshold voltage variation primarily occurs when the device is operating with low drain voltage bias, and not when the device is operating with a drain voltage that would cause saturation. This demonstrates that the NDC is not being caused by threshold voltage variation due to applied drain bias. With the exclusion of self-heating or threshold voltage variation causing the NDC, it follows that the negative slope must be caused either by trapping mechanisms or possibly by field-dependent mobility degradation.

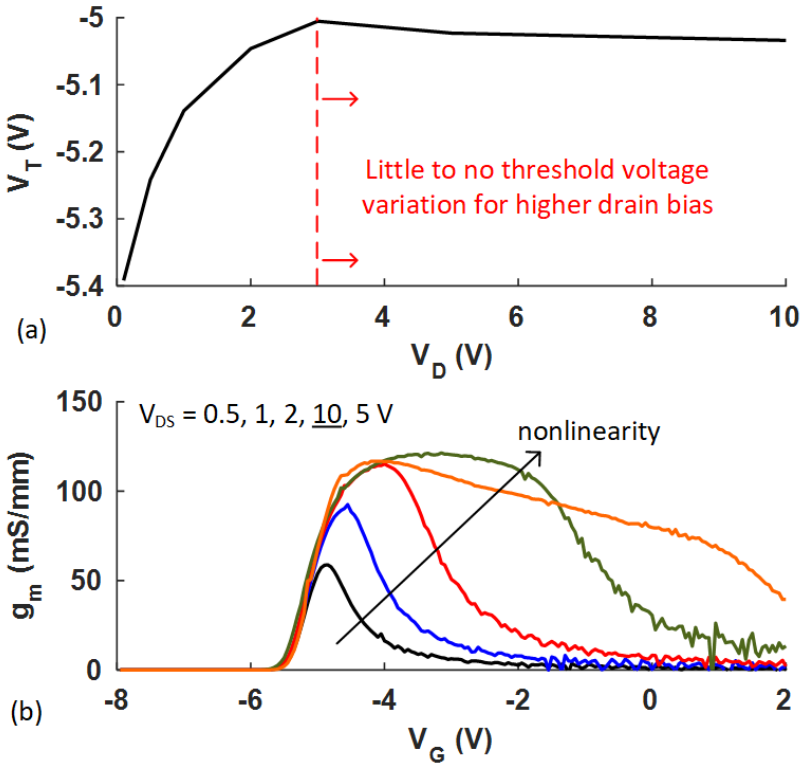


Figure 6.2: (a) Threshold voltage variation due to drain voltage bias. (b) Non-linear transconductance profiles due to velocity reduction in the channel.

Field-dependent mobility degradation can be confirmed by examining transconductance (g_m) profiles as the drain voltage bias is increased [74]. In this case, a highly non-linear profile is observed which is attributed to velocity reduction in the channel as a result of carrier scattering (Fig. 6.2b). This confirms that some amount of mobility degradation is

occurring within this device, however, it does not serve as a way to measure or quantify the degradation. For the purpose of this paper, we wish to focus instead on trapping mechanisms that can be confirmed to be causing NDC in the saturation region.

6.3.2 Trap Characterization via Pulse I-V

Pulse I-V tests can also be used to examine the effect of hot electrons as well as barrier layer and buffer layer traps. Modifying the quiescent drain bias for the pulse test (from 0 V to a positive bias) will incorporate the effects of certain charged trap states. This test is shown in Fig. 6.3a where a significant shift in knee voltage is seen at a given gate voltage bias. The shift in knee voltage, known as drain-lag, is attributed to trapping effects where traps act like a pseudo back gate [75]. Trapped charge located under the metal gate will effectively change the gate bias, thereby changing the pinch-off voltage characteristics. Additionally, applying a quiescent drain bias can induce hot electron injection from the 2DEG into the AlGaN barrier layer which can further increase $R_{DS(on)}$ if the drain bias is sufficiently high [89]. However, when comparing the two pulse conditions in Fig. 6.3a, there is no evident change in degradation in drain current in the saturation region. Therefore we can conclude that the drain bias does not meet the threshold to cause hot electron injection for these devices.

Controlling the polarity of the applied pulse voltage is also a method to study the trapping and de-trapping process. When the pulse voltage is higher than the quiescent bias voltage, the traps capture free charge. Conversely, when the pulse voltage is lower than the quiescent bias voltage, the traps release captured charge [90]. The impact of these phenomena are observed in Fig. 6.3b. When the pulse voltage is higher than the quiescent bias voltage (V_{DQ} = 0 V), the drain current is reduced due to trapping; this is known as gate-lag which is attributed to deep traps beneath the channel [90]. Reversing the polarity of the drain bias pulse serves to release traps, at which point the drain current recovers to the original

pre-trapped value.

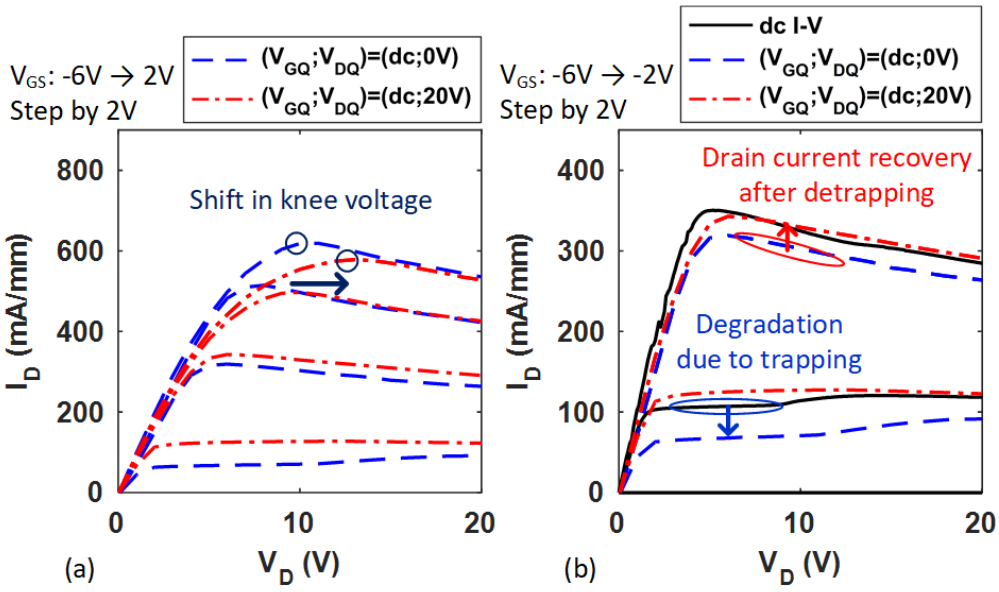


Figure 6.3: (a) Pulse I_D-V_D characterization showing a shift in knee voltage due to starting drain bias. (b) Trapping and recovery phenomena due to drain current pulse polarity.

These measurements give more insight into trapping and de-trapping mechanisms, and into how I-V curves are affected by the ionization of traps, however, saturation region NDC was unaffected by pulse I-V quiescent bias testing. Therefore, the trapping mechanisms leading to drain- and gate-lag can be eliminated from consideration in causing or contributing to the NDC effect. According to the aforementioned understanding of drain- and gate-lag, this rules out certain trapped charges under the metal gate, and certain deep traps beneath the channel from contributing to the NDC phenomena.

6.3.3 Substrate Biasing Effects

Substrate biasing can be used as a tool to understand how traps affect device performance. Under standard operation conditions, in the on-state with the substrate grounded, some electrons will exit the channel and become trapped in the buffer or at the surface (Fig. 6.4a). When V_{BS} is positive, the applied electric field vector will be from substrate to surface,

which will pull these stray channel electrons towards the buffer (Fig. 6.4b). By biasing the device with a positive substrate voltage, trapped charge resulting from carriers exiting the channel should be increased in the buffer region and reduced at the surface due to the presence of the electric field. Conversely, when the applied bias is negative, this will push electrons towards the surface as seen in Fig. 6.4c, resulting in more traps at the surface, and less in the buffer. In short, the location of traps resulting from poor channel confinement can be modified to show the influence due to surface traps (with $V_{BS} \ll 0$) or due to buffer traps (with $V_{BS} \gg 0$). It is important to note that these traps are pulled directly from the 2DEG and occur during dc operation, not after an applied stress, or during a switching transient (as can be observed during the pulse I-V testing).

Both the kink effect and NDC seen in previous I_D-V_D results are heavily impacted by substrate biasing. Applying a positive substrate bias (Fig. 6.5c) increases the NDC effect, and eliminates the kink effect that was seen in Fig. 6.5b. This is due to forcing stray carriers which exit the channel towards the buffer and away from the surface. On the contrary, applying a negative substrate bias serves to eliminate NDC when the drain voltage is swept backwards, however, during a forward sweep, the kink effect is increased significantly (Fig. 6.5d). In this case the stray carriers are forced towards the surface, and away from the buffer. It must be noted that the drain voltage must be swept backwards in this case due to the enormous instability caused by the kink effect. This kink effect is exaggerated by the poor passivation quality as a result of SiN peeling from stress accumulation on the wafer. It is expected that improved passivation would result in minimizing the kink effect and this device would demonstrate no NDC during forwards or backwards sweep with a negative substrate bias.

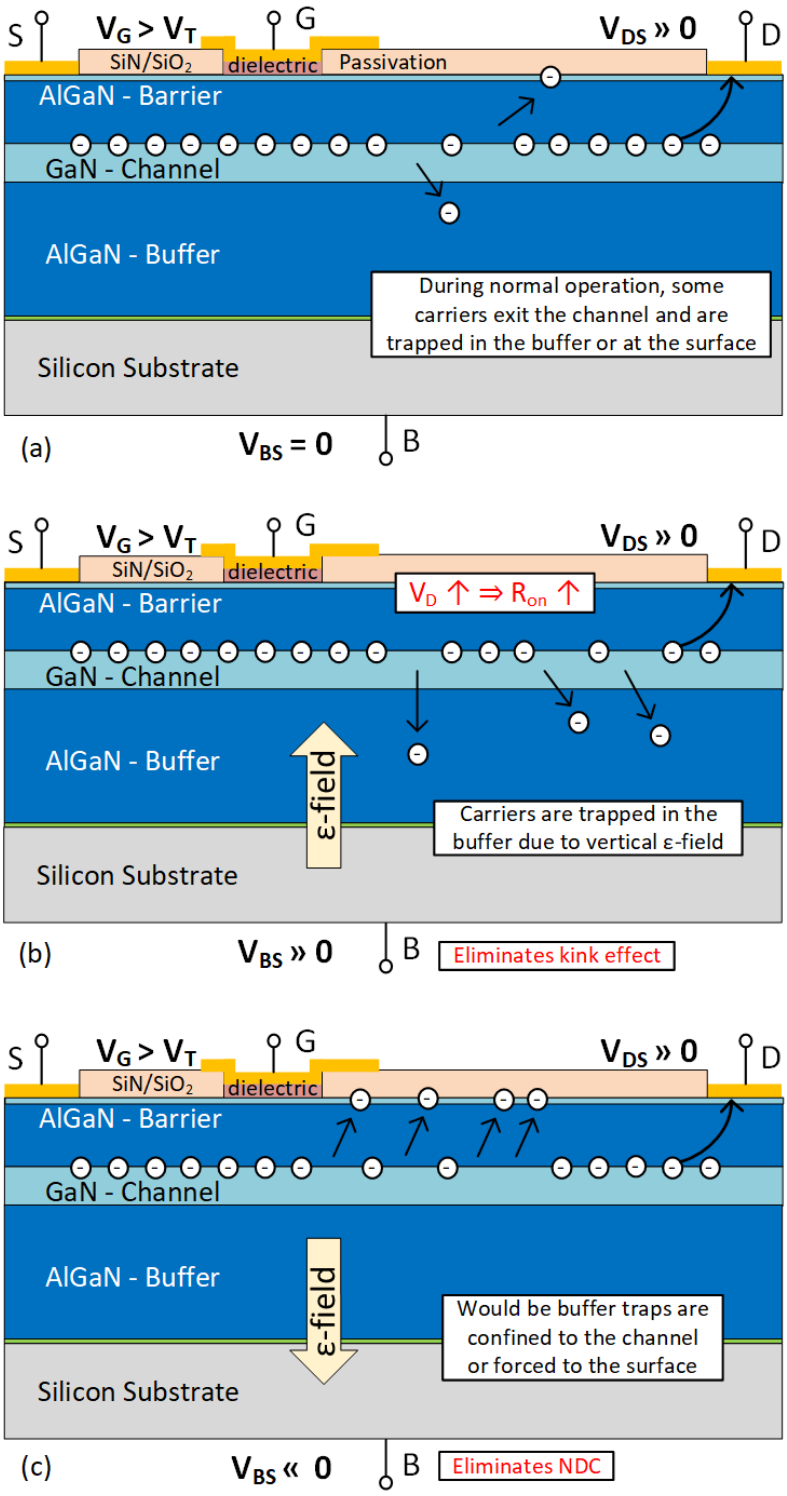


Figure 6.4: Effect of substrate bias on trap distribution within the device at (a) $V_{BS} = 0$ V, (b) $V_{BS} \gg 0$ V, and (c) $V_{BS} \ll 0$ V.

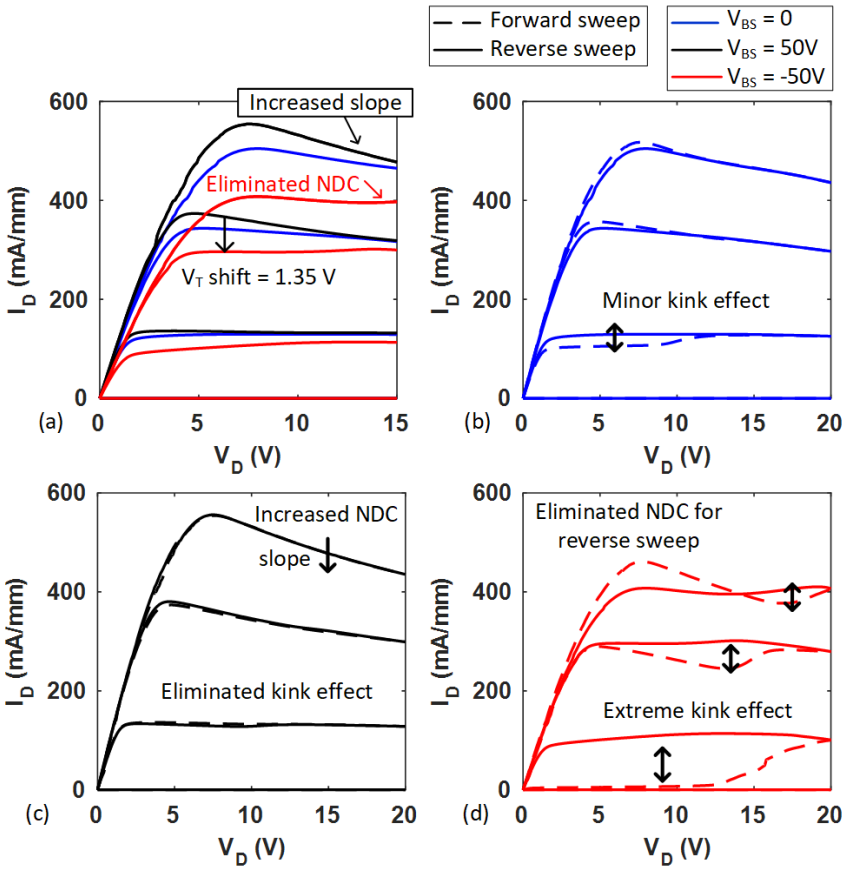


Figure 6.5: (a) Reverse drain voltage sweep showing eliminated NDC with V_{BS} = -50V. Forward and reverse DC I-V characteristics with V_{BS} biased at (b) 0V, (c) 50V, and (d) -50V.

Based on these observations, the kink effect seen in these devices is subject primarily to buffer traps, and surface traps are the cause of NDC. Another thing to note is that a negative substrate bias shifts the threshold voltage more positive, and a positive substrate bias shifts threshold voltage more negative due to charge polarization. This results in a shift in max $I_{D-sat.}$ as shown in Fig. 6.5a. However this shift in threshold voltage remains for some time after the device is tested, suggesting that the charge polarization remains trapped with a long time constant as it requires more than 6 hours of recovery for the threshold voltage to return to the pre-stressed value.

Further examination of substrate biasing can lend insight into the type of traps that are ionized during positive and negative bias conditions. Toward this end, ramped back-

gating measurements are performed to study the effect of sweeping the substrate bias on drain current. For the ramped back-gating measurements, V_{BS} was swept from 0 V to -100 V and back to 0 V at a sweep rate of 1 V/s. Then after a period of 12 hours rest to allow for trap recovery, V_{BS} was swept from 0 V to 100 V and back down to 0 V. Drain current was monitored with the device biased in the saturation region (at $V_{GS} = 0$ V and $V_{DS} = 10$ V). In order to suppress any potential self-heating, low values of V_{GS} and V_{DS} are chosen. Typically the device is biased in the linear region for this type of test to eliminate the possibility of current collapse [91,92], however, to better understand what causes the kink effect and severe NDC seen previously, the device is biased in the saturation region where these effects are most prominent.

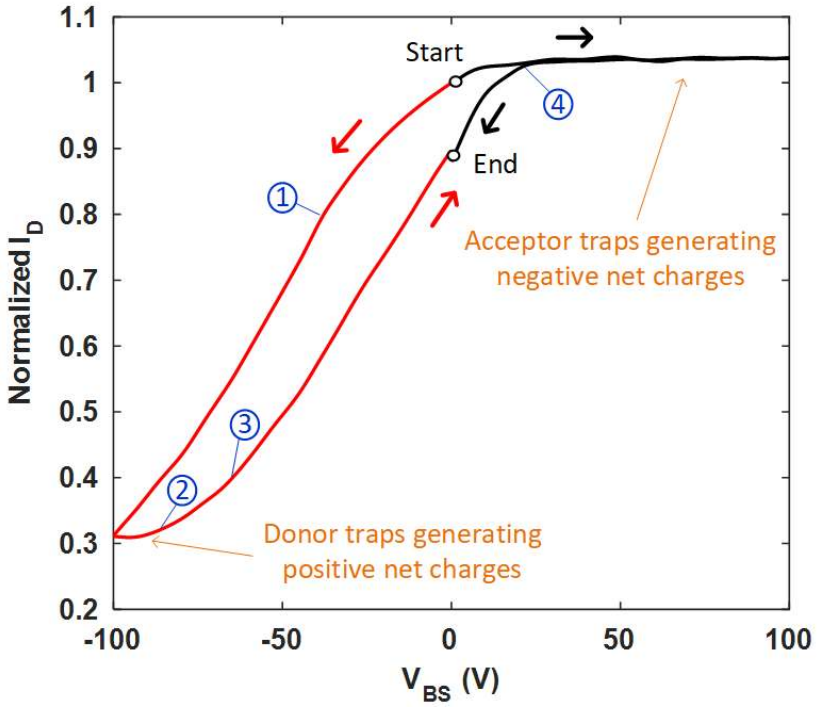


Figure 6.6: Substrate bias sweep with I_D normalized to the value at $V_{GS} = 0V$, $V_{DS} = 10V$, and $V_{BS} = 0V$. Red line represents the reverse bias sweep, followed by 12 hour rest for trap recovery and then the forward sweep shown in black.

Results from the ramped back-gating measurements are shown in Fig. 6.6 where red denotes the negative sweep, and black denotes the positive sweep. The drain current is

normalized to I_D at $V_{GS} = 0V$, $V_{DS} = 10V$, and $V_{BS} = 0V$ and the ramp rate of V_{BS} is set to 1 V/s. It is important to note that it does not matter which sweep direction is done first in this test, so long as the rest period is sufficiently long to allow for full trap recovery. The phenomena leading to the curves in Fig. 6.6 are quite complex, and require a detailed breakdown and analysis of the sweep for better understanding. Starting with the negative sweep, initially the applied negative back-gate bias reduces the 2DEG concentration due to the applied electric field and capacitive coupling. At location 1, the reduction in drain current increases beyond the ideal rate, as carriers are trapped in the surface and the buffer. As acceptor states near the 2DEG are ionized, free holes are created which travel towards the substrate where they are trapped and contribute positive space charge. Stray electrons exiting the channel will of course continue to trap in the surface. This trapping continues until $V_{BS} = -100V$. As V_{BS} is swept back from -100 V to 0 V, positive buffer charging (due to previous ionization of donor traps deep in the buffer) counters the decrease in V_{BS} [92]. This becomes the screening charge which creates the flat portion of the curve on the return sweep leading up to location 2. These ionized donor traps are being released at the same rate as V_{BS} decreases, yielding little to no change in drain current. Between location 2 and 3, the rate of de-trapping decreases, and the drain current begins recovering. As the rate of change of the screening charge decreases, the recovery will start to behave in the ideal manner (as without trapping effects). After location 3, de-trapping is completely halted, and drain current increases due to the change in electric field at the ideal rate. However, after the back-bias, some space charges remain as some traps have a long time constant. At the end of the sweep I_D is degraded by 15% due to reduced 2DEG density from trapped carriers.

For the positive sweep, the drain current initially increases due to the applied electric field, however, at location 4 the increase in drain current saturates. This saturation is due to buffer traps which capture electrons and generate net negative charges which screens the 2DEG from the substrate bias [91]. Electrons furnished from the ohmic contact or the

2DEG are injected into the buffer due to the semi-insulating nature of the buffer stack and the applied voltage polarity [92, 93]. The injected electrons are trapped by acceptor states in the buffer, creating the screening charge which neutralizes the increase in V_{BS}. The flat region suggests that acceptor traps are ionized at the same rate of increase in V_{BS}, resulting in canceling the effect of the applied electric field. During the return sweep, the traps are consequently released at the same rate as the decrease in V_{BS}, however, at location 4, further release of traps is halted and more trapped electrons cannot be effectively released: resulting in the degradation in drain current shown.

The quick saturation of I_D when V_{BS} is forward biased also explains why $|V_T|$ only increases slightly (<2%) at $V_{BS} = 50V$, whereas negative bias has a large impact on threshold voltage ($|V_T| \downarrow \approx 20\%$). In both cases, the trapped carriers contribute to a reduction in threshold voltage that remains after testing. Tests were run at $V_{BS} = 0V$ immediately after negative or positive substrate bias testing to confirm this. Concerning trap recovery, in most cases 90% recovery of threshold voltage (return to the unstressed state) is seen after 1 hour, but 12 hours is required for full recovery back to the original V_T pre-substrate-bias stress. This time interval is consistent with some reported recovery times from other groups. Nakala [75] used a six hour recovery period and reported that this time interval was not sufficient for all V_{DS-MAX} bias points.

6.4 Summary

These results confirm that negative differential conductance observed in I_D-V_D curves is due to trapped charge in the buffer and not due to self-heating effects. This trapped charge is a result of poor carrier confinement in the channel where stray electrons that exit the channel become trapped both at the surface and in the buffer. Substrate biasing tests confirmed that surface trapped charges are responsible for the severe kink effect

(current collapse) seen, and that buffer trapped charges are responsible for the NDC in the saturation region. To the best of our knowledge, we are the first to report NDC due to traps and not as a result of self-heating.

CHAPTER 7: CONCLUSION

This work has addressed a fabless design approach both for high voltage and low voltage GaN power HEMTs. Fabless design is critical to reducing time to market and overall design cost. In addition, these models can improve understanding of device physics, especially when expanding the boundaries of the technology. High voltage design ($>$ 600 V) relies heavily on scaling for L_{GD}, L_{GFP}, and t_{Buffer} when optimizing breakdown voltage and figure of merit. In comparison, low voltage simulations revealed less dependence on vertical leakage current and substrate breakdown compared to high voltage designs, and more reliance on buffer leakage and punch-through as the dominant factors leading to breakdown.

Currently, commercial low voltage GaN power HEMTs are not competitive with silicon devices in terms of figure of merit, even though the materials advantage still exists at low voltage. This is thought to be partially due to inability to scale power devices given that the standard equipment used to fabricate high voltage power HEMTs is not well suited for submicron scale devices. In addition, some structures and advanced features will not scale to submicron resolution and thus cannot be used for low voltage devices (one example being the HD-GIT). This presents challenges for low voltage design especially concerning heterostructure quality, as some reliability concerns can be overcome with advanced field-plate designs, or a hybrid drain structure, both of which may not be feasible at submicron scale. Aggressive scaling for low voltage design suggests that GaN HEMTs can achieve half the current FOM of state-of-the-art silicon devices.

A portion of this work was dedicated to analysis of defect-induced performance degrada-

tion, and to the effects of trapping on performance. In this regard, heterostructure quality is critically important. It was found that devices on wafers with high stress growth had significant issues with buffer traps, and also poor passivation adhesion, which in turn produced a high density of surface states leading to current collapse. Substrate bias testing revealed that buffer traps are responsible for the negative differential conductance seen in testing, and that in this case it was not due to self-heating. These issues are in part due to the high stress growth, and as such can potentially be mitigated by using a superlattice stress relief layer.

To push the boundaries of low voltage fabrication further, it is likely that GaN power devices will need equipment similar to that used for GaN RF devices such as E-beam lithography to produce smaller features with an acceptable alignment tolerance. In addition, as these devices become smaller, thermal performance becomes a critical issue as the power density increases and the thermal interface becomes smaller. In this way, every thermal advantage needs to be taken, such as switching from Si to SiC substrates, and considering the impact a superlattice buffer structure has on thermal performance. It is likely that improved packaging for thermal performance will become critical to the adoption of low voltage GaN power HEMTs.

APPENDIX : UCF FABRICATION PROCESSING STEPS

Mask 1: Mesa isolation					
Step	Item	Tool	Recipe/Condition	Spec	Note
1	Wafer cleaning	Wet Bench	AMD bath		
2	Hard mask deposition	Plasma-Therm 790 PECVD/ICP Etcher (Upstairs)	Recipe: SiN_Diff Rate: 9 nm/min Time: 27:16 min:sec SiN THK: 300 nm		recipe in folder: Dep0/up/SiN_Diff
3	PR coating	Spin Coater	Recipe: 14 (1) PR: S1813, i-line (2) SB: 130 °C/ 60 sec		
4	Photolithography	MJB4 (i-line)	Mask: Layer 1 (clear) Dose: 1mW/cm^2 Exposure: 15 sec		
5	Development & baking	Wet Bench/Hotplate	(1) PEB: 115 °C/ 60 sec (2) Dev: 45 sec (CD26)		
6	SiN HM etching	Plasma-Therm 790 PECVD/ICP Etcher (Upstairs)	Recipe: EtchSiN1 Time: 10 min		
7	PR Strip	Wet Bench	AMD bath		
8	Dry etching	Unaxis Shuttleline ICP-RIE III-V etcher	Recipe: Gas/flow: Cl_2/ 7 sccm N_2/ 43 sccm Pressure: 5.3 mTorr Power/bias: 500/100 W Time: 11:30 min:sec	Depth: 400 nm	$Rate_{GaN}$: 35 nm/min $Rate_{SiN}$: 16 nm/min Selectivity = 2.17:1 (GaN:SiN)
9	HM removal	Wet Bench	(1) Wet Etch: 50% HCL Time: 4 min Rate: 50 nm/min (2) AMD bath		
Mask 2: Ohmic Recess Etch					
10	Hard mask deposition	Plasma-Therm 790 PECVD/ICP Etcher (Upstairs)	Recipe: SiN_Diff Rate: 9 nm/min Time: 11 min SiN THK: 100 nm		recipe in folder: Dep0/up/SiN_Diff
11	PR coating	Spin Coater	Recipe: 14 (1) PR: S1813, i-line (2) SB: 130 °C/ 60 sec		
12	Photolithography	MJB4 (i-line)	Mask: Layer 2 (clear) Dose: 1mW/cm^2 Exposure: 15 sec		
13	Development & baking	Wet Bench/Hotplate	(1) PEB: 115 °C/ 60 sec (2) Dev: 45 sec (CD26)		
14	SiN HM etching	Plasma-Therm 790 PECVD/ICP Etcher (Upstairs)	Recipe: EtchSiN1 Time: 5 min		
15	PR Strip	Wet Bench	AMD bath		
16	Dry etching	Unaxis Shuttleline ICP-RIE III-V etcher	Recipe: Gas/flow: Cl_2/ 7 sccm N_2/ 43 sccm Pressure: 5.3 mTorr Power/bias: 500/100 W Time: 30? sec	Depth: 15 nm	$Rate_{GaN}$: 35 nm/min $Rate_{SiN}$: 16 nm/min Selectivity = 2.17:1 (GaN:SiN)
17	HM removal	Wet Bench	(1) Wet Etch: 50% HCL Time: 2 min Rate: 50 nm/min (2) AMD bath		

Mask 3: Ohmic S/D Metallization					
18	PR coating	Spin Coater	Recipe: 14 (1) PR: S1813, i-line (2) SB: 130 °C/ 60 sec		
19	Photolithography	MJB4 (i-line)	Mask: Layer 3 (clear) Dose: 1mW/cm^2 Exposure: 15 sec		
20	Development & baking	Wet Bench/Hotplate	(1) PEB: 115 °C/ 60 sec (2) Dev: 45 sec (CD26)		
21	PR descum	Apex SLR Etcher	Recipe: Gas/flow: O_2/ 10 sccm Ar/ 20 sccm Pressure: 60? mTorr Power/bias: 100/50 W Time: 30 sec		Might be better to do with 0 W bias and higher RF power (300 W?)
23	Metal deposition	Temescal E-beam evaporator	Ti/Al/Ni/Au: 30/180/40/100 nm		NDL uses: Ti/Al/Ni/Au: 25/125/45/75 nm
24	Lift-off	Wet Bench	(1) ACE + sonication: 10 min (2) AMD + N_2 dry		
26	RTA	RTP-600S	(1) Pre-run test: 700 °C/30 sec (2) 700 °C/60 sec	NDL uses: 875 °C/30 sec	For pre-run use 15 sec N2 purge. For standard run use 300-600 sec N2 purge.
27	TLM measurement	Probe station	TLM measurement	Au-free standard: ρ_c = 1E-3 Ω-cm^2	NDL's standard: ρ_c = 5E-5 Ω-cm^2
Mask 4: Gate Metallization					
28	PR coating	Spin Coater	Recipe: 14 (1) PR: S1813, i-line (2) SB: 130 °C/ 60 sec		
29	Photolithography	MJB4 (i-line)	Mask: Layer 4 (clear) Dose: 1mW/cm^2 Exposure: 15 sec		
30	Development & baking	Wet Bench/Hotplate	(1) PEB: 115 °C/ 60 sec (2) Dev: 45 sec (CD26)		
31	PR descum	Apex SLR Etcher	Recipe: Gas/flow: O_2/ 10 sccm Ar/ 20 sccm Pressure: 60? mTorr Power/bias: 100/50 W Time: 30 sec		Might be better to do with 0 W bias and higher RF power (300 W?)
33	Metal deposition	Temescal E-beam evaporator	Ni/Au: 40/100 nm		NDL uses: Ni/Au: 50/300 nm
34	Lift-off	Wet Bench	(1) ACE + sonication: 10 min (2) AMD + N_2 dry		

LIST OF REFERENCES

[1] H. A. Mantooth, M. D. Glover, and P. Shepherd, "Wide Bandgap Technologies and Their Implications on Miniaturizing Power Electronic Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 3, pp. 374–385, Sep. 2014.

[2] P&S Market Research, "Global Power Electronics Market Size, Share, Development, Growth and Demand Forecast to 2022 - Industry Insights by Device (Power Discrete, Power Modules, Power IC), by End-User (Consumer Electronics, Automotive, Industrial, Power & Energy, ICT, Aerospace & Defense, Others), By Voltage (Low Voltage, Medium Voltage, High Voltage, Very High Voltage)," Tech. Rep., Mar. 2017.

[3] D. Visalli *et al.*, "Limitations of Field Plate Effect Due to the Silicon Substrate in AlGaN/GaN/AlGaN DHFETs," *IEEE Transactions on Electron Devices*, vol. 57, no. 12, pp. 3333–3339, Dec. 2010.

[4] O. Hilt, A. Knauer, F. Brunner, E. Bahat-Treidel, and J. Wrfl, "Normally-off AlGaN/GaN HFET with p-type Ga Gate and AlGaN buffer," Jun. 2010, pp. 347–350.

[5] D. Visalli, M. Van Hove, P. Srivastava, J. Derluyn, J. Das, M. Leys, S. Degroote, K. Cheng, M. Germain, and G. Borghs, "Experimental and simulation study of breakdown voltage enhancement of AlGaN/GaN heterostructures by Si substrate removal," *Applied Physics Letters*, vol. 97, no. 11, p. 113501, Sep. 2010.

[6] "Sentaurus Device User Guide."

[7] Y. Zhang, "Simulation and fabrication of GaN-based vertical and lateral normally-off power transistors," Ph.D. dissertation, 2013.

[8] A. Hinoki, J. Kikawa, T. Yamada, T. Tsuchiya, S. Kamiya, M. Kurouchi, K. Kosaka, T. Araki, A. Suzuki, and Y. Nanishi, "Effects of Traps Formed by Threading Dislocations on Off-State Breakdown Characteristics in GaN Buffer Layer in AlGaN/GaN Heterostructure Field-Effect Transistors," *Applied Physics Express*, vol. 1, no. 1, p. 011103, Dec. 2007.

[9] "EPC2023 Enhancement Mode Power Transistor Datasheet," 2017.

[10] H. Amano *et al.*, "The 2018 GaN power electronics roadmap," *Journal of Physics D: Applied Physics*, vol. 51, no. 16, p. 163001, Apr. 2018.

[11] S. K. Saha, "Cost-Benefit Analysis of Computer-Aided Technology Customization Projects," *Open Journal of Business and Management*, vol. 05, no. 02, p. 272, Apr. 2017.

[12] H. Hahn, F. Benkhelifa, O. Ambacher, F. Brunner, A. Noculak, H. Kalisch, and A. Vescan, "Threshold Voltage Engineering in GaN-Based HFETs: A Systematic Study With the Threshold Voltage Reaching More Than 2 V," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 538–545, Feb. 2015.

[13] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, and I. Omura, "Recessed-gate structure approach toward normally off high-Voltage AlGaN/GaN HEMT for power electronics applications," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 356–362, Feb. 2006.

[14] M. Van Hove, X. Kang, S. Stoffels, D. Wellekens, N. Ronchi, R. Venegas, K. Geens, and S. Decoutere, "Fabrication and Performance of Au-Free AlGaN/GaN-on-Silicon Power Devices With Al2o3 and Si3n4/Al2o3 Gate Dielectrics," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3071–3078, Oct. 2013.

[15] M. Meneghini, O. Hilt, J. Wuerfl, and G. Meneghesso, "Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate," *Energies*, vol. 10, no. 2, p. 153, Jan. 2017.

[16] L. Efthymiou, G. Longobardi, G. Camuso, T. Chien, M. Chen, and F. Udrea, "On the physical operation and optimization of the p-GaN gate in normally-off GaN HEMT devices," *Applied Physics Letters*, vol. 110, no. 12, p. 123502, Mar. 2017.

[17] M. Meneghini *et al.*, "Gate Stability of GaN-Based HEMTs with P-Type Gate," *Electronics*, vol. 5, no. 4, p. 14, Mar. 2016.

[18] J. Wurfl, "GaN High-Voltage Power Devices," F. Medjdoub and K. Iniewski, Eds. Boca Raton, FL, USA: CRC Press, 2016.

[19] M. Xu, Y. Weng, and H. Wang, "Reduction of leakage current in GaN-based high-electron mobility transistor employing carbon-doped GaN superlattice buffer layers," Nov. 2016, pp. 62–63.

[20] P. Xu, Y. Jiang, Y. Chen, Z. Ma, X. Wang, Z. Deng, Y. Li, H. Jia, W. Wang, and H. Chen, "Analyses of 2-DEG characteristics in GaN HEMT with AlN/GaN super-lattice as barrier layer grown by MOCVD," *Nanoscale Research Letters*, vol. 7, no. 1, p. 141, Feb. 2012.

[21] A.-J. Tzou, D.-H. Hsieh, S.-H. Chen, Y.-K. Liao, Z.-Y. Li, C.-Y. Chang, and H.-C. Kuo, "An Investigation of Carbon-Doping-Induced Current Collapse in GaN-on-Si High Electron Mobility Transistors," *Electronics*, vol. 5, no. 2, p. 28, Jun. 2016.

[22] De Brida Christian, "Gallium Nitride simulations using Sentaurus Software," Ph.D. dissertation, 2010.

[23] J.-J. Zhu, X.-H. Ma, B. Hou, W.-W. Chen, and Y. Hao, "Investigation of trap states in high Al content AlGaN/GaN high electron mobility transistors by frequency dependent capacitance and conductance analysis," *AIP Advances*, vol. 4, no. 3, p. 037108, Mar. 2014.

[24] Y. Shi, Q. Zhou, Y. Jin, B. Chen, W. Chen, W. Huang, and B. Zhang, "Impact of interface traps on switching behavior of normally-OFF AlGaN/GaN MOS-HEMTs: Impact of interface traps on switching behavior of normally-OFF AlGaN/GaN MOS-HEMTs," *physica status solidi (c)*, vol. 13, no. 5-6, pp. 328–331, May 2016.

[25] V. Joshi, A. Soni, S. P. Tiwari, and M. Shrivastava, "A Comprehensive Computational Modeling Approach for AlGaN/GaN HEMTs," *IEEE Transactions on Nanotechnology*, vol. 15, no. 6, pp. 947–955, Nov. 2016.

[26] D. A. Deen, R. Miller, A. Osinsky, B. P. Downey, D. F. Storm, D. J. Meyer, D. S. Katzer, and N. Nepal, "Polarization-mediated Debye-screening of surface potential fluctuations in dual-channel AlN/GaN high electron mobility transistors," *Journal of Applied Physics*, vol. 120, no. 23, p. 235704, Dec. 2016, arXiv: 1610.03921.

[27] I.R. Gatabi, "Tunnel MOS Heterstructure Field Effect Transistors for RF Switching Applications," Ph.D. dissertation, 2013.

[28] E. Bahat-Treidel, "GaN-Based HEMTs for High Voltage Operation," Ph.D. dissertation, 2012.

[29] V. Barkhordarian, "Power MOSFET Basics."

[30] Alpha & Omega Semiconductor, "Power MOSFET Basics."

[31] N. Herbecq, I. Roch-Jeune, A. Linge, M. Zegaoui, P.-O. Jeannin, N. Rouger, and F. Medjdoub, "Above 2000 V breakdown voltage at 600 K GaN-on-silicon high electron mobility transistors: Above 2000 V breakdown voltage at 600 K," *physica status solidi (a)*, vol. 213, no. 4, pp. 873–877, Apr. 2016.

[32] H. Jiang *et al.*, "Source-Drain Punch-Through Analysis of High Voltage Off-State AlGaN/GaN HEMT Breakdown," *Journal of Physics: Conference Series*, vol. 864, no. 1, p. 012023, 2017.

[33] A. Binder and J. S. Yuan, "Optimization of an enhancement-mode AlGaN/GaN/AlGaN DHFET towards a high breakdown voltage and low figure of merit," Oct. 2017, pp. 122–126.

[34] B. Krishnan, A. Kumar, A. Velaga, A. Binder, J.-S. Yuan, J. Su, and A. Paranjpe, "TEM Microstructural Analysis of 8 AlxGa1-xN based Enhancement Mode HEMTs and Correlation of Device Reliability Issues with Lattice Defects," Miami, FL, 2018.

[35] B. Lu and T. Palacios, "High Breakdown ($> \hbox{1500\ V}$) AlGaN/GaN HEMTs by Substrate-Transfer Technology," *IEEE Electron Device Letters*, vol. 31, no. 9, pp. 951–953, Sep. 2010.

[36] S. Tanabe, N. Watanabe, M. Uchida, and H. Matsuzaki, "Effects of surface morphology and C concentration in C-doped GaN buffer on breakdown voltage of AlGaN/GaN HEMTs on free-standing GaN substrate: Breakdown voltage of AlGaN/GaN HEMTs on free-standing GaN substrate," *physica status solidi (a)*, vol. 213, no. 5, pp. 1236–1240, May 2016.

[37] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura, and H. Ohashi, "High breakdown voltage AlGaN-GaN power-HEMT design and high current density switching behavior," *IEEE Transactions on Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.

[38] G. Meneghesso, M. Meneghini, and E. Zanoni, "Breakdown mechanisms in AlGaN/GaN HEMTs: An overview," *Japanese Journal of Applied Physics*, vol. 53, no. 10, p. 100211, Oct. 2014.

[39] E. Bahat-Treidel, O. Hilt, F. Brunner, J. Wurfl, and G. Trankle, "Punchthrough-Voltage Enhancement of AlGaN/GaN HEMTs Using AlGaN Double-Heterojunction Confinement," *IEEE Transactions on Electron Devices*, vol. 55, no. 12, pp. 3354–3359, Dec. 2008.

[40] H. T. Henderson and K. L. Ashley, "Space-Charge-Limited Current in Neutron-Irradiated Silicon, with Evidence of the Complete Lampert Triangle," *Physical Review*, vol. 186, no. 3, p. 811, 1969.

[41] M. Uren, K. Nash, R. Balmer, T. Martin, E. Morvan, N. Caillas, S. Delage, D. Ducatteau, B. Grimbert, and J. De Jaeger, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 2, pp. 395–398, Feb. 2006.

[42] J. Luo, S.-L. Zhao, M.-H. Mi, W.-W. Chen, B. Hou, J.-C. Zhang, X.-H. Ma, and Y. Hao, "Effect of gate length on breakdown voltage in AlGaN/GaN high-electron-mobility transistor," *Chinese Physics B*, vol. 25, no. 2, p. 027303, 2016.

[43] W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, "Suppression of Dynamic On-Resistance Increase and Gate Charge Measurements in High-Voltage GaN-HEMTs With Optimized Field-Plate Structure," *IEEE Transactions on Electron Devices*, vol. 54, no. 8, pp. 1825–1830, Aug. 2007.

[44] A. Binder, J.-S. Yuan, B. Krishnan, and P. M. Shea, "Fabless design approach for lateral optimization of low voltage GaN power HEMTs," *Superlattices and Microstructures*, vol. 121, pp. 92–106, Sep. 2018.

[45] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, T. Ueda, T. Tanaka, and D. Ueda, "Gate Injection Transistor (GIT)A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Transactions on Electron Devices*, vol. 54, no. 12, pp. 3393–3399, 2007.

[46] T. Ueda *et al.*, "GaN-based Gate Injection Transistors for power switching applications," Dec. 2014, pp. 11.3.1–11.3.4.

[47] S. Kaneko *et al.*, "Current-collapse-free operations up to 850 V by GaN-GIT utilizing hole injection from drain," May 2015, pp. 41–44.

[48] K. Tanaka *et al.*, "Suppression of current collapse by hole injection from drain in a normally-off GaN-based hybrid-drain-embedded gate injection transistor," *Applied Physics Letters*, vol. 107, no. 16, p. 163502, Oct. 2015.

[49] Xinhua Wang, Sen Huang, Yingkui Zheng, Ke Wei, Xiaojuan Chen, Haoxiang Zhang, and Xinyu Liu, "Effect of GaN Channel Layer Thickness on DC and RF Performance of GaN HEMTs With Composite AlGaN/GaN Buffer," *IEEE Transactions on Electron Devices*, vol. 61, no. 5, pp. 1341–1346, May 2014.

[50] X.-H. Ma, Y.-M. Zhang, X.-H. Wang, T.-T. Yuan, L. Pang, W.-W. Chen, and X.-Y. Liu, "Breakdown mechanisms in AlGaN/GaN high electron mobility transistors with different GaN channel thickness values," *Chinese Physics B*, vol. 24, no. 2, p. 027101, Feb. 2015.

[51] S. Ahmed, M. I. B. Taher, M. T. Hasan, and M. S. Islam, "GaN-based Double Gate MOSFETs: Effect of gate length." IEEE, 2016, pp. 2334–2337.

[52] X.-J. Zhang, Y.-T. Yang, B.-X. Duan, C.-C. Chai, K. Song, and B. Chen, "Drain-induced barrier lowering effect for short channel dual material gate 4h silicon carbide metalsemiconductor field-effect transistor," *Chinese Physics B*, vol. 21, no. 9, p. 097302, Sep. 2012.

[53] U. G. Lee and J. Jang, "Drain-Induced Barrier Lowering in Short-Channel Poly-Si TFT After Off-Bias Stress Using Metal-Induced Crystallization of Amorphous Silicon," *IEEE Electron Device Letters*, vol. 32, no. 9, pp. 1233–1235, Sep. 2011.

[54] K.-H. Cho, Y.-S. Kim, J. Lim, Y.-H. Choi, and M.-K. Han, "Design of AlGaN/GaN HEMTs employing mesa field plate for breakdown voltage enhancement," *Solid-State Electronics*, vol. 54, no. 4, pp. 405–409, Apr. 2010.

[55] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and T. Ogura, "600v AlGaN/GaN power-HEMT: design, fabrication and demonstration on high voltage DC-DC converter." IEEE, 2003, pp. 23–7.

[56] P. Ivo, A. Glowacki, E. Bahat-Treidel, R. Lossy, J. Wrfl, C. Boit, and G. Trnkle, "Comparative study of AlGaN/GaN HEMTs robustness versus buffer design variations by applying Electroluminescence and electrical measurements," *Microelectronics Reliability*, vol. 51, no. 2, pp. 217–223, Feb. 2011.

[57] M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, and F. Fantini, "Investigation of High-Electric-Field Degradation Effects in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 55, no. 7, pp. 1592–1602, Jul. 2008.

[58] A. G. Gudkov, V. D. Shashurin, V. N. Vyuginov, V. G. Tikhomirov, S. I. Vidyakin, S. V. Agasieva, E. N. Gorlacheva, and S. V. Chizhikov, "The Influence of AlGaN Barrier-Layer Thickness on the GaN HEMT Parameters for Space Applications," K. V. Anisimov, A. V. Dub, S. K. Kolpakov, A. V. Lisitsa, A. N. Petrov, V. P. Polukarov, O. S. Popel, and V. A. Vinokurov, Eds. Cham: Springer International Publishing, 2018, pp. 273–280.

[59] S. Majumdar, S. Das, and D. Biswas, "Barrier layer engineering: Performance evaluation of E-mode InGaN/AlGaN/GaN HEMT," 2015, p. 020021.

[60] S. Turuvekere, A. DasGupta, and N. DasGupta, "Effect of Barrier Layer Thickness on Gate Leakage Current in AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 62, no. 10, pp. 3449–3452, Oct. 2015.

[61] F. Medjdoub, M. Alomari, J.-F. Carlin, M. Gonschorek, E. Feltin, M. Py, N. Grandjean, and E. Kohn, "Barrier-Layer Scaling of InAlN/GaN HEMTs," *IEEE Electron Device Letters*, vol. 29, no. 5, pp. 422–425, May 2008.

[62] J. P. Ibbetson, P. T. Fini, K. D. Ness, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors," *Applied Physics Letters*, vol. 77, no. 2, pp. 250–252, Jul. 2000.

[63] S. Sque, "High-voltage GaN-HEMT devices, simulation and modelling," 2013.

[64] L. Guo, "The influence of 1 nm AlN interlayer on properties of the Al0.3ga0.7n/AlN/GaN HEMT structure," *Microelectronics Journal*, vol. 39, pp. 777–781, 2008.

[65] H. Huang, Y. C. Liang, and G. S. Samudra, "Theoretical calculation and efficient simulations of power semiconductor AlGaN/GaN HEMTs," Dec. 2012, pp. 1–4.

[66] A. Teke, S. Gkden, R. Tlek, J. H. Leach, Q. Fan, J. Xie, u. Ozgur, H. Morko, S. B. Lisesivdin, and E. Ozbay, "The effect of AlN interlayer thicknesses on scattering processes in lattice-matched AlInN/GaN two-dimensional electron gas heterostructures," *New Journal of Physics*, vol. 11, no. 6, p. 063031, Jun. 2009.

[67] S. Kolluri, S. Keller, D. Brown, G. Gupta, S. Rajan, S. P. DenBaars, and U. K. Mishra, "Influence of AlN interlayer on the anisotropic electron mobility and the device characteristics of N-polar AlGaN/GaN metal-insulator-semiconductor-high electron mobility transistors grown on vicinal substrates," *Journal of Applied Physics*, vol. 108, no. 7, p. 074502, Oct. 2010.

[68] F. Medjdoub, M. Zegaoui, D. Ducatteau, N. Rolland, and P. A. Rolland, "High-Performance Low-Leakage-Current AlN/GaN HEMTs Grown on Silicon Substrate," *IEEE Electron Device Letters*, vol. 32, no. 7, pp. 874–876, Jul. 2011.

[69] R. Coffie, Y. C. Chen, I. Smorchkova, M. Wojtowicz, Y. C. Chou, B. Heying, and A. Oki, "IMPACT OF AlN INTERALAYER ON RELIABILITY OF AlGaN/GaN HEMTS," p. 4.

[70] S. L. Selvaraj, A. Watanabe, A. Wakejima, and T. Egawa, "1.4-kV Breakdown Voltage for AlGaN/GaN High-Electron-Mobility Transistors on Silicon Substrate," *IEEE Electron Device Letters*, vol. 33, no. 10, pp. 1375–1377, Oct. 2012.

[71] K. J. Chen, O. Haberlen, A. Lidow, C. l. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Transactions on Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017.

[72] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si Technologies for Power Switching Devices," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013.

[73] D. Marcon, Y. N. Saripalli, and S. Decoutere, "200mm GaN-on-Si epitaxy and e-mode device technology," Dec. 2015, pp. 16.2.1–16.2.4.

[74] A. Zhang, "e-HEMT: An Engineering Model for GaN-Based High Electron Mobility Transistors," Ph.D. dissertation, Aug. 2014.

[75] P. Nakkala, "Pulsed I-V and RF characterization and modeling of AIGaN HEMTs and Graphene FETs," Ph.D. dissertation, 2015.

[76] Z. Tang, S. Huang, Q. Jiang, S. Liu, C. Liu, and K. J. Chen, "High-Voltage (600-V) Low-Leakage Low-Current-Collapse AlGaN/GaN HEMTs with AlN/SiNxPassivation," *IEEE Electron Device Letters*, vol. 34, no. 3, pp. 366–368, Mar. 2013.

[77] K. Horio, H. Onodera, and A. Nakajima, "Analysis of backside-electrode and gate-field-plate effects on buffer-related current collapse in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics*, vol. 109, no. 11, p. 114508, Jun. 2011.

[78] H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller, and U. K. Mishra, "High breakdown voltage AlGaN-GaN HEMTs achieved by multiple field plates," *IEEE Electron Device Letters*, vol. 25, no. 4, pp. 161–163, Apr. 2004.

[79] R. Chu, A. Corrion, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes, and K. Boutros, "1200-V Normally Off GaN-on-Si Field-Effect Transistors With Low Dynamic on -Resistance," *IEEE Electron Device Letters*, vol. 32, no. 5, pp. 632–634, May 2011.

[80] L. Zhe, W. Xiao-Liang, W. Jun-Xi, H. Guo-Xin, G. Lun-Chun, and L. Jin-Min, "The influence of AlN/GaN superlattice intermediate layer on the properties of GaN grown on Si (111) substrates," *Chinese Physics*, vol. 16, no. 5, pp. 1467–1471, May 2007.

[81] P. Moens *et al.*, "On the impact of carbon-doping on the dynamic Ron and off-state leakage current of 650v GaN power devices," May 2015, pp. 37–40.

[82] S. C. Binari, P. B. Klein, and T. E. Kazior, "Trapping effects in GaN and SiC microwave FETs," *Proceedings of the IEEE*, vol. 90, no. 6, pp. 1048–1058, Jun. 2002.

[83] Q. Jiang, Z. Tang, C. Zhou, S. Yang, and K. J. Chen, "Substrate-Coupled Cross-Talk Effects on an AlGaN/GaN-on-Si Smart Power IC Platform," *IEEE Transactions on Electron Devices*, vol. 61, no. 11, pp. 3808–3813, Nov. 2014.

[84] J. D. Albrecht, R. P. Wang, P. P. Ruden, M. Farahmand, and K. F. Brennan, "Electron transport characteristics of GaN for high temperature device modeling," *Journal of Applied Physics*, vol. 83, no. 9, pp. 4777–4781, May 1998.

[85] N. Gao, Y. L. Fang, J. Y. Yin, B. Wang, Y. M. Guo, Z. Z. He, G. D. Gu, H. Y. Guo, Z. H. Feng, and S. J. Cai, "Comparison of AlGaN/GaN HEMTs grown and fabricated on sapphire substrate with AIN and GaN nucleation layers," Nov. 2017, pp. 195–199.

[86] M. Chaibi, T. Fernandez, A. Mimouni, J. Rodriguez-Tellez, A. Tazon, and A. M. Sanchez, "NONLINEAR MODELING OF TRAPPING AND THERMAL EFFECTS ON GaAs AND GaN MESFET/HEMT DEVICES," *Progress In Electromagnetics Research*, vol. 124, pp. 163–186, 2012.

[87] D. Niessen, "Nonlinear Characterization and Modelling of GaN HEMTs for Microwave Power Amplifier Applications," Ph.D. dissertation, May 2013.

[88] M. Gassoumi, B. Grimbert, C. Gaquiere, and H. Maaref, "Evidence of surface states for AlGaN/GaN/SiC HEMTs passivated Si3n4 by CDLTS," *Semiconductors*, vol. 46, no. 3, pp. 382–385, Mar. 2012.

[89] X. Zheng, S. Feng, Y. Zhang, X. He, and Y. Wang, "A New Differential Amplitude Spectrum for Analyzing the Trapping Effect in GaN HEMTs Based on the Drain Current Transient," *IEEE Transactions on Electron Devices*, vol. 64, no. 4, pp. 1498–1504, Apr. 2017.

[90] O. Jardel, F. D. Groote, C. Charbonniaud, T. Reveyrand, J. P. Teyssier, R. Quere, and D. Floriot, "A Drain-Lag Model for AlGaN/GaN Power HEMTs," Jun. 2007, pp. 601–604.

[91] A. Pooth, M. J. Uren, M. Csar, T. Martin, and M. Kuball, "Charge movement in a GaN-based hetero-structure field effect transistor structure with carbon doped buffer under applied substrate bias," *Journal of Applied Physics*, vol. 118, no. 21, p. 215701, Dec. 2015.

[92] S. Yang, C. Zhou, S. Han, J. Wei, K. Sheng, and K. J. Chen, "Impact of Substrate Bias Polarity on Buffer-Related Current Collapse in AlGaN/GaN-on-Si Power Devices," *IEEE Transactions on Electron Devices*, vol. 64, no. 12, pp. 5048–5056, Dec. 2017.

[93] C. Zhou, Q. Jiang, S. Huang, and K. J. Chen, "Vertical Leakage/Breakdown Mechanisms in AlGaN/GaN-on-Si Devices," *IEEE Electron Device Letters*, vol. 33, no. 8, pp. 1132–1134, Aug. 2012.