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GaN Substrates for III-Nitride Devices

Bulk gallium nitride substrates for optoelectronic devices have been under intense development, and availability of this crystalline material has been increasing in size, doping, and orientation.

By Tanya Paskova, Drew A. Hanser, and Keith R. Evans

ABSTRACT | Despite the rapid commercialization of III-nitride semiconductor devices for applications in visible and ultra-violet optoelectronics and in high-power and high-frequency electronics, their full potential is limited by two primary obstacles: i) a high defect density and biaxial strain due to the heteroepitaxial growth on foreign substrates, which result in lower performance and shortened device lifetime, and ii) a strong built-in electric field due to spontaneous and piezoelectric polarization in the wurtzite structures along the well-established [0001] growth direction for nitrides. Recent advances in the research, development, and commercial production of native GaN substrates with low defect density and high structural and optical quality have opened opportunities to overcome both of these obstacles and have led to significant progress in the development of several opto-electronic and high-power devices. In this paper, the recent achievements in bulk GaN growth development using different approaches are reviewed; comparison of the bulk materials grown in different directions is made; and the current achievements in device performance utilizing native GaN substrate material are summarized.

KEYWORDS | Ammonothermal growth; doping; gallium nitride (GaN); heterostructure field-effect transistor (HFET); hydride vapor phase epitaxy; laser diode (LD); light-emitting diode (LED); native substrates; point defects; Schottky diodes; solution growth; structural defects; surface orientation; thermal conductivity

I. INTRODUCTION

Nitride-based devices such as ultraviolet (UV)-blue-green emitters, high-power transistors, detectors, etc., have

became commercial realities relying completely on heteroepitaxial approaches by employing a variety of foreign substrates including, sapphire, silicon carbide, and silicon. However, their performance is significantly limited by the structural quality of these materials as a result of the well-known disadvantages of the heteroepitaxy, such as lattice mismatch, thermal expansion coefficient mismatch and chemical incompatibility leading to high-dislocation density, mosaic crystal structure, biaxial induced stress, and wafer bowing. In order to reduce these structural defects, special approaches have been developed such as low-temperature buffer technologies or epitaxial lateral overgrowth (ELOG) techniques, which complicate and extend the device growth process. Additional drawbacks are related to the lower electrical and/or thermal conductivity of most foreign substrates, which require more complicated and expensive device designs.

Availability of lattice matched GaN substrates can bring not only a new quality in GaN-based devices by improved device performance through eliminating the structural defects and providing better vertical electrical and thermal conductivity; moreover, it will lead to cost-efficient device processing through simplification of the epitaxial growth process by eliminating the need for low-temperature buffer layers. In this paper, we summarize the major efforts in GaN substrate development and present the current achievements in producing large-scale high-quality native GaN substrates with different surface orientations. We discuss the advantages of using the native GaN substrates with respect to the current heteroepitaxial nitride-based devices. Some specific devices with improved performance are described before a short summary is given.

II. MAJOR EFFORTS IN GaN SUBSTRATE GROWTH

In contrast to classical semiconductors like silicon and gallium arsenide, for which the development of substrates and thin-film device structure went hand-by-hand, the

III-nitride thin-film device technology is by far advanced over the development of native substrate crystal growth. However, recently there has been considerable interest and widespread ongoing research and development efforts to change this situation. Several methods, considered with high potential to deliver high quality and/or cost-effective and scalable native GaN crystals, are currently under intensive development. In this paper, however, we only focus on the techniques that demonstrated ability to produce relatively large bulk crystals, in shape of boules with diameter of 2 in and thickness up to several millimeters, which allow producing of substrates with different surface orientations.

A. Hydride Vapor Phase Epitaxy

Currently, hydride vapor phase epitaxy (HVPE) is considered to be a highly practical method to obtain GaN thick layers that can serve as quasi-bulk substrates after delaminating from the foreign substrates or to obtain GaN boules that can be sliced to fabricate native bulk substrates. The biggest advantage of the technique is its ability to produce high-quality material at high growth rates due to a high surface migration of the halide species, motivating the versatility of HVPE as a growth method for both device applications and substrate application. Among all the bulk growth techniques under investigation today for nitrides, HVPE is the most promising technique since it utilizes a process at more favorable conditions, namely, low pressure and relatively low growth temperature. Combined with the high growth rate, it determines the growth process to be also cost effective.

Nowadays, the fundamental growth physics and chemistry of HVPE growth of GaN are well understood. The available models [1], [2] of the kinetics of the process and growth mechanisms occurring at the solid/vapor interface during HVPE growth of GaN assume a surface process involving several steps and allow simulation of the growth rates. Based on a quasi-thermodynamic growth model, simulations of gas dynamics, temperature distribution, and partial pressures can be simulated for any specific reactor design [3], [4]. Commonly the HVPE process for growing III-nitrides consists of two main reactions: i) forming chloride gas of the group III metal at relatively lower growth temperature and ii) growth reaction between the chloride metal and ammonia to form the nitride film at higher growth temperature, typically in the range of 1050 °C–1100 °C. Basically, two temperature zone reactors are needed in horizontal or vertical design, but often more temperature zone reactors are employed with a higher flexibility for temperature control and particularly in case of doping varieties.

The HVPE technique was proven capable to produce n-type, p-type, and semi-insulating material. The HVPE-GaN material always exhibits unintentional n-type conductivity, related to background doping by silicon and oxygen, introduced from the quartz parts within the reactor and/or from the process gases. For intentional n-type doping, silicon and oxygen are mostly used, but doping by Ge and Sn has also been explored. The Si doping can be achieved either by introducing gas [5], silane (SiH_4), disilane (Si_2H_6), or dichlorsilane (SiH_2Cl_2) or by exposing solid Si to HCl to form $SiCl_x$ [6]. The latter was reported to ensure the highest intentional free carrier concentration of 8×10^{18} cm^{-3} [6]. The p-type doping in HVPE GaN growth can be achieved by using Zn [7], Cd [8], Be [9], or Mg [10], [11]. Today Mg doping, shown to be relatively more efficient, is mostly used by adding pure metal or powder Mg in a separate boat or mixed with Ga metal and exposed to the HCl. The use of H_2 carrier gas and its effect on the efficacy of p-type doping with Mg is a point of controversy in the reports due to the formation of Mg-H complexes and the need for thermal annealing that is usually performed in situ directly after the growth. The semi-insulating type of HVPE-GaN was reported by using Fe compensating doping [12], [13], achieving free carrier concentration as low as 5×10^{13} cm^{-3} [13].

The optimization of the HVPE-GaN growth is impeded by the typical complications of crystal growth technology like the multidisciplinary nature and complex multiparameter character of the process. In addition, the nucleation optimization was of significant importance. Several techniques resulted in significant improvements, such as different single buffers of ZnO [14], [15], metal-organic chemical vapor deposition (MOCVD) grown GaN thin layers [16], [17], reactively sputtered AlN [16], [18], or TiN [19], and also different modifications of growth forced in lateral in-plane directions, as ELOG around masks of different materials and shapes [20]–[22] or grooved substrates. The selection of the nucleation scheme determines the type of HVPE GaN layers usually produced with different thicknesses and different characteristics.

B. Ammonothermal Growth

The ammonothermal process is a solvothermal process that allows the solubilization of polycrystalline III-nitride nutrient or feedstock in supercritical ammonia under high pressure by utilizing a solubilizing agent or mineralizer. The dissolved nutrient is then transported to the region of crystallization, where it recrystallizes on seed crystals or through self-seeding. The type of the mineralizer used determines the main type of the ammonothermal approach, with respective advantages and disadvantages. The mineralizers are generally divided into three groups: i) basic mineralizer, which introduces NH_2^- ions to the solution; ii) acidic, which introduces NH_4^+ ions; and iii) neutral, which does not introduce either of them. Dissolution of III-nitrides using potassium azide (KN_3) or potassium amide (KNH_2) ammonothermal-basic solutions [23]–[26] has been suggested by several groups to occur through formation of soluble intermediate compounds, which subsequently decompose with temperature. Other crystallization mechanisms, which involve forward solubility of

nitride species, have been reported for ammonothermal-acidic [27]–[29] solutions, which utilize ammonium halide mineralizers. The ammonothermal-basic growth is conducted by transporting the mass from high- to low-temperature zones and has been reported to possess several advantages, including lower dissolution density due to solubilizing in the higher temperature zone; lower contamination probability due to recrystallization in the lower temperature zone; lower probability for cubic formation; and absence of disastrous effect of the basic solution on the autoclave materials, which results in safety improvements and cost effectiveness. In contrast, the acidic approach requires special, usually costly, Au or Pt liners, and still the safety operation remains problematic. Nevertheless, the approach is expected to be capable of handling higher growth rates at higher pressures [29].

In general, the ammonothermal technique is characterized with relatively low growth rate capacity; however, it requires relatively low temperature and reasonable pressure, which allow controllable recrystallization at close to equilibrium conditions, which in turn allows production of high-quality material. In addition, the technique allows large-scale wafer growth and scalable production approach by conducting multiple seeded growths in a single run.

The quality of this type of material is still in the beginning of detailed evaluation. Given the fact that a reasonable large cystal is a result of a very long process, optimization of the growth conditions and producing a systematic series for thorough analysis will take more time. Nevertheless, the first experimental results indicate that the properties of the ammonothermal GaN material are very strongly influenced by the quality and surface preparation of the seeds used. The best results from the crystallinity point of view were reported for self-prepared seed and multiple regrowth processes [30]. Dislocation presence was not revealed by standard etch pit density and cathodoluminescence techniques, and the curvature of samples with diameter up to 2 in has been measured to be more than 1000 m. The free carrier concentration of undoped samples was reported to be usually in the range of 10^{19} cm^{-3} [24]–[26] but can go down to 2×10^{18} cm^{-3} [30].

C. Solution Growth at Lower Pressure, Lower Temperatures

An alternative solution growth approach by using Na flux instead of nitrogen solution was proposed by Yamane *et al.* [31] several years ago. The advantages of this approach are mostly related to the more favorable growth conditions of typically 800 °C and 5 MPa. The results for self-nucleation growth so far are quite similar to that obtained by high-pressure solution growth approach. In the absence of a GaN seed, two growth habits were demonstrated—prisms or platelets—with length and lateral sizes of a few millimeters. Kawamura *et al.* [32] have modified the Na-flax method for growth on 2-in

templates. In the case of using GaN film grown by MOCVD, growth rates up to 20 μm/h were attained, and a boule with a thickness of 3 mm was shown. Another advantage of this liquid epitaxial method is its ability to reduce some structural defect density, consistent with reports for other material systems such as SiC. A decrease of dislocation density from 10^8 cm^{-2} in the seed to 10^4 cm^{-2} in the regrown material was reported and explained in terms of a change in the dominating growth mode from vertical in the seed to lateral in the Na-flux solution growth [33].

Similar results of reducing the dislocation density have been reported for alternative low-pressure solution growth (LPSG) at growth temperature in the range of 900 °C–1020 °C [34] by employing a different chemical solution. A growth rate of 1 μm/h was reported for growth on metalorganic vapor phase epitaxy (MOVPE) GaN templated sapphire up to 3-in in diameter. Also, at nearly atmospheric pressure and temperature of about 800 °C, employing another chemical solvent, seeded growth on an HVPE-GaN seed was demonstrated [35]. Up to now, the reported growth rates of a few micrometers per hour are not suited for bulk crystal growth. In addition, since in these approaches nitrogen has to be dissolved and then diffused through the Ga melt to the growth front, maintaining homogeneous growth over large areas remains a challenge.

A short comparative summary of the current achievements in producing largest GaN crystals by the three techniques is shown in Table 1.

III. CURRENT ACHIEVEMENTS IN GaN SUBSTRATE DEVELOPMENT

Since HVPE is the method that dominates the GaN substrate market today, we will focus further in this paper on the different approaches used by this technique only. The specific characteristics of the material available on the market are not included in this paper. There are several thorough reviews in the literature [36]–[43] discussing the properties of the HVPE grown GaN in detail, which we recommend to interested readers. It is important to note that the growth process (including nucleation scheme, the growth rate, and growth recipes), as well as the material properties resulting from using different foreign substrates and optimizations, are completely different for growth of thin films with thickness up to 50 μm (often called templates), for thick films in the range of 100–2000 μm, and for boule growth with thickness more than several millimeters, the latter two being of interest for substrate applications after removing the foreign substrate.

A. Single Substrate Development

Crack-free thick HVPE GaN layers with thicknesses of about 300–500 μm have been demonstrated by using the ELOG technique on 2-in sapphire and on GaAs substrates.

Table 1 Summary of Current Bulk GaN Growth Methods and Material Best Characteristics and Crystals Size Achieved

	HVPE	Ammono-thermal	Na-flux LPE
Largest wafer size	3 inch *	2 inch [30]	2 inch [33]
Largest boule size	2in/10 mm [13,49]	2in/2 mm [30] 10x10 mm^2 [26]	2 in / 3 mm [33]
Dislocation density	$10^5 - 10^6$ cm^{-2} [13,49]	Not observed	$10^2 - 10^4$ cm^{-2} [33]
Lowest unintentional doping	1×10^{16} cm^{-3} [13,49]	2×10^{18} cm^{-3} [30]	1×10^{16} cm^{-3} [31]
Curvature	c-plane: 10 m [13] m-, a-: no [13,49], semipolar: no [49]	1000 m [30]	

*http://www.hitachi-cable.co.jp/en/products/news/20030213t.html

The growth procedure developed by Usui *et al.* [21] consists principally of an HVPE selective homoepitaxial growth on a thin MOCVD grown GaN layer. The MOCVD growth was performed using the conventional two-step procedure, consisting of a 20-nm-thick buffer layer and high-temperature main overlayer. A SiO$_2$ layer was deposited by chemical vapor deposition and then fabricated into mask/window stripes with a period of about 7 μm, using conventional photolithographic techniques. Alternatives of using W [22] and SiN [44] masks instead of SiO$_2$, or using GaAs [45], LiGaO$_2$ [46], LiAlO$_2$ [47] substrates instead of sapphire, have also been demonstrated. In addition, in order to further reduce the dislocation density, the ELOG approach can be performed by the so-called two-step (2S) approach, which can employ either a second layer of mask usually with shifted period with respect to the first mask or a change of the growth parameters, usually a reduced growth temperature [40].

These thick layers can be separated from the substrates they were grown on by different approaches depending on the type of the substrate used and the nucleation scheme. The easiest way for substrate removal is a chemical etching in case of using GaAs or LiGaO$_2$ as a substrate. This approach was particularly developed on GaAs substrate and successfully manufactured by Sumitomo Electric Industries Ltd.[1] In the case of using sapphire as a substrate, a laser-induced liftoff process was developed to separate GaN from the sapphire by using different pulsed UV lasers. The process works by irradiating the sapphire/GaN interface with intense laser pulses just at the absorption edge of GaN. It leads to a fast and strong heating, which causes thermal decomposition in the interface regions of the film, yielding metallic Ga and nitrogen gas effusion. This approach was particularly developed for 2S-ELOG nucleation and successfully manufactured by Lumilog Ltd.[2]

In contrast to the MOCVD nitride technology, the early work on low-temperature GaN buffers in the same chamber was not successful in the HVPE technology. Alternatively, buffers of different nature deposited by different techniques, mostly reactive sputtering, have been proposed and demonstrated to ensure significant improvement of the crystal quality of the layers with thickness up to several hundred micrometers and, in some instances, up to millimeters. The ZnO buffer has been suggested as a buffer for HVPE growth of thick GaN films (up to 300 μm thickness) by Detchprohm *et al.* [14] and has been used for substrate delamination due to its easy chemical etching. The ZnO buffer has been developed and optimized at Lincoln laboratory and is known to be one of the best working buffers for growth of thick GaN layers of good quality [36], but large-area free-standing substrates have not been demonstrated by utilizing this buffer. In order to serve as a good buffer for HVPE-GaN substrate applications, a specific requirement needs to be fulfilled. Namely, a weak interface region close to the substrate is needed, which could ensure so-called void-assisted separation. Such a buffer is reactively sputtered TiN, as suggested by NEC Corp. in 2002 [21]. This approach was developed and successfully manufactured by Hitachi Cable, which recently announced production of a crack-free 3-in free-standing GaN wafer [Fig. 1(a)].[3] Another high-temperature reactively sputtered AlN buffer was also found to be effective in suppressing defect formation in the GaN nucleation region [48]. This buffer approach also permits reducing of tensile stress during GaN growth by forming a weak interface, which leads to optimized structural properties [48] of films with thickness up to ~1–2 mm. In addition, the weak interface allows a self-separation of the films. This approach was developed and successfully manufactured by Kyma Technologies, which announced a production of free-standing GaN wafers of different size [Fig. 1(b)].[4]
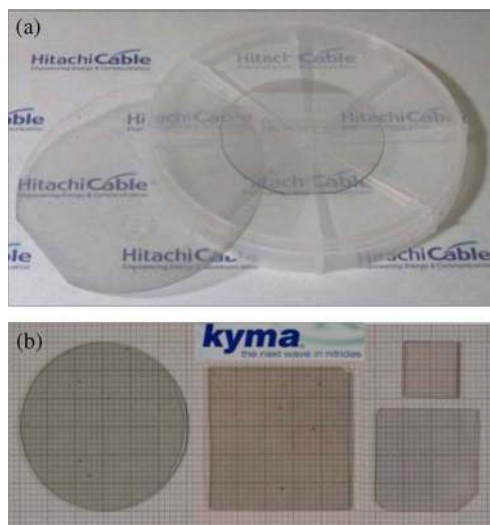
[1]http://www.sei.co.jp/.
[2]http://www.lumilog.com/.

[3]http://www.hitachi-cable.co.jp/en/products/news/20030213t.html.
[4]http://www.kymatech.com/.

B. Boule Growth Development

The use of MOCVD templates for GaN growth on sapphire was first shown in molecular beam epitaxy (MBE) growth of thin GaN layers. Later, it was successfully employed in HVPE-GaN growth [17] and is currently used by many research groups. The reports consistently showed that the MOCVD-GaN templates can provide good buffers for growth of thick HVPE GaN layers with very good structural and optical characteristics, although it is difficult to grow films with sufficient thickness without cracks. However, in the case of the growth of a boule several millimeters thick, the cracks predominantly occur in the sapphire while the boule remains intact. Mitsubishi Chemical Co. reported growth of 2-in boules up to 5–6 mm thick [Fig. 2(a)] using such a buffer approach [49], [50]. Two-inch boule growth ranging from 2.5 and 3.5 mm up to 10 mm has been reported also by ATMI Inc, [51], Ferdinand-Braun-Institute [52], and Kyma Technologies, Inc. [Fig. 2(b)] [53], [54], respectively. Different buffers and higher growth rates up to 300 μm/h are likely to be used by the different groups. When fully developed, the boule growth is the most preferable and economical pathway to achieve GaN substrates with the necessary quality, size, and cost. At this time, GaN boule growth is still in the early stages of development, and no mature technology is available yet due to several challenges.

C. Nonpolar and Semipolar Substrate Development

The boule growth approach is also the technique of choice for producing substrates with surface orientation different from the (0001) for devices benefiting from the absence or reduced polarization induced electric fields. This is accomplished by slicing nonpolar substrates perpendicularly or by slicing semipolar substrates inclined to the boule growth surface [Fig. 3(a)].

There has been intensive research during the last few years in developing growth of nitride structures with active device layers aligned along planes tilted with respect to the hexagonal basal plane of the crystallographic unit cell. The spontaneous polarization is an intrinsic material property of wurtzite semiconductors as a result of the ionic nature of the bonds in III-nitrides, which after summarizing overall do not compensate due to differences in the bond lengths. In a quantum well (QW), the differences between the spontaneous polarization vectors of the barrier and the well lead to electrostatic field. However, when the growth direction is inclined with respect to the [0001] direction, the remaining field strength in the quantization direction is a projection of this vector on the off-axis growth direction, as shown in Fig. 3(b) for a representative In composition of 10% in a InGaN/GaN QW [55] with spontaneous polarization coefficients published in [56]. The piezoelectric polarization field, being a result of strain situation of pseudomorphically grown active layers, is also very sensitive to the tilt of the active region to the [0001] direction. The two polarization contributions are minimized for devices grown in nonpolar directions with tilt $\Theta = 90°$. Some planes having a tilt angle Θ between 0 and 90°, called semipolar, have been found stable during growth and are expected to have reduced polarization field, although even theoretically their exact dependences are yet not exactly
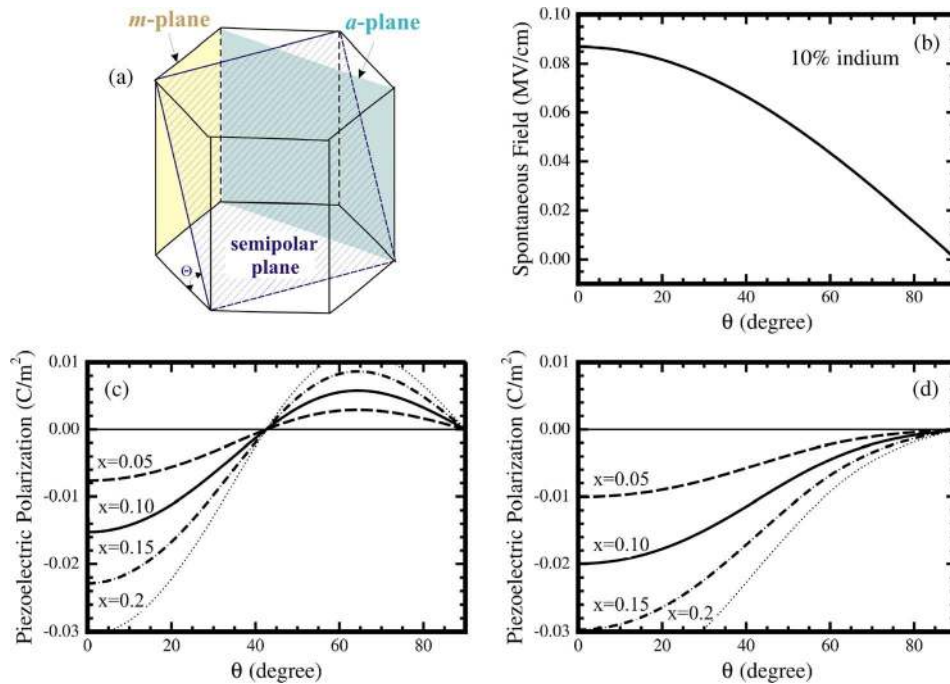
Fig. 3. *(a) Schematic view of the polar (0001) c-plane, nonpolar (11-20) a-plane and (10-10) m-plane, and (11-22) semipolar plane. (b) Calculated spontaneous polarization field as a function of the growth direction tilt with respect to the basal plane for InGaN/GaN structure with 10% indium using spontaneous polarization coefficients published in [56]. (c), (d) Calculated tilt dependences for piezoelectric field for InGaN/GaN structure with different indium compositions using piezoelectric tensor elements published in (c) [57] and (d) [58]. (Adapted with permission from [55].)*

known due to uncertainty in the piezoelectric tensor elements as clearly demonstrated in [55] for different sets of tensor elements (Fig. 3(c) and (d) with tensor elements from [57] and [58], respectively).

The development of substrates with both nonpolar and semipolar surfaces was initiated by utilizing foreign substrates, such as (1-102) sapphire or (11-20) SiC for a-plane GaN, (100) LiAlO₂ or (1-100) SiC for m-plane GaN, and (100) MgAl₂O₄ for (10-11)-plane GaN, or (110) MgAl₂O₄ for (10-13)-plane GaN [59]. The HVPE growth of thick layers GaN has also benefited from the ability for self-separation from some of the above substrates [60]. However, it was consistently found that in all these cases, in addition to the dislocation density, a high density of stacking faults was always generated. The biggest obstacle in these cases is that the stacking faults do not decrease along the sample thickness contrary to the dislocation density along the *c*-growth axis and are inherited in the subsequent epitaxial device structures. Furthermore, several optimizations have been suggested and elaborated mostly by using ELOG techniques, yet the device performance remained insufficient [61]. Recently, researchers from different groups consistently focused their attention on using nonpolar and semipolar substrates sliced from boules, which allowed growth of device structure with no stacking faults.

IV. ADVANTAGES OF GaN SUBSTRATE FOR III-NITRIDE EPITAXIAL GROWTH

Despite the fact that the current heteroepitaxial nitride industry works quite well for most of the LED devices, especially considering the wide availability of cheap substrates such as sapphire, a potential availability of native GaN substrates is expected to have significant impact on the industry in two major ways: by reducing device production cost and by improving the device performance. Even assuming the GaN substrates are not likely to compete with the sapphire cost in the near future, the overall device cost may still be significantly reduced by shortening the real epitaxial time and by circumventing the low-temperature buffer and/or lateral epitaxial steps required in the current nitride production. In this section, we will focus on the impact of the native GaN substrates on the device performance for some of the devices by enabling i) low defect density and smooth morphology homoepitaxy, ii) good thermal conductivity and lower operation temperature, and iii) good electrical conductivity and simplified device architecture.

A. Low Defect Density and Smooth Morphology

In contrast to many material systems for which even a low defect density leads to a dramatic deterioration of the device performance, many of the nitride-based devices can

successfully operate even at presence of dislocations with density in the range of 10^8–10^9 cm^{-2}. It is particularly valid for the blue light-emitting diodes (LEDs), which, combined with phosphors to produce the majority of white-light LEDs produced today, perform at the highest efficiency level of GaN-based LEDs. For devices operating at shorter (UV) or longer (green) wavelengths, which are characterized with relatively low operating efficiencies, there is still ongoing debate on what mechanisms lead to the changing of internal quantum efficiency (IQE). There are several proposed mechanisms to explain the decrease in LED efficiency with increasing current, including carrier injection and confinement effects [62], [63], piezoelectric polarization effects [64], and Auger loss [65]. There is also evidence that the material quality of the device plays a large role in governing the LED performance. Compositional changes and associated material quality differences in the InGaN for green-wavelength LEDs are believed to contribute to the efficiency drop seen at longer wavelengths [66]. InGaN is a notoriously difficult material to grow due to its low decomposition temperature, a reported miscibility gap [67], and increasing lattice mismatch with GaN as the indium content is increased. Material quality tends to decrease with increasing indium content, and compositional uniformity in quantum wells tends to decrease as well. Indium-rich regions form in quantum wells and result in carrier localization, which enhances efficiency at blue wavelengths, but at longer wavelengths the effective localization is reduced, allowing higher indium content LEDs to be more susceptible to nonradiative recombination at dislocations in InGaN [68]. V-defect formation in the growth of InGaN has also been shown to be associated with threading dislocations [69], and it is believed that reducing the density of such defects will improve the performance of green LEDs [70]. Growth of InGaN on low-defect density bulk substrate can improve its material quality and the LED performance. Nonradiative recombination is also an issue for UV LEDs, where the IQE is lower than in visible-wavelength LEDs due to the lack of carrier localization and the typically high number of dislocations.

The high dislocation density is even more critical for laser diode (LD) performance. The dislocations cause deterioration of the LD performance by providing fast diffusion paths along their lines, thus smearing out the quantum well and shorting the p-n junctions, as well as by serving as nonradiative recombination centers, thus leading to heat generation instead of optical emission [71]. The latter leads to an increase of the threshold current density and to limitation of the lifetime of the devices.

The power electronic devices also suffer from the high dislocation densities in the heteroepitaxial nitride structures. For example, pure screw dislocations have been identified as a path for reverse-bias leakage currents in high-power Schottky barrier diodes (see also the next section). The dislocations also have negative impact on de-
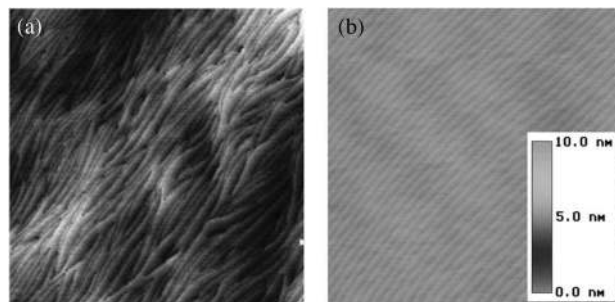

Fig. 4. *AFM images* (2×2 μm^2) *of surface morphology of MOVPE grown GaN epilayers on (a) HVPE-GaN template/sapphire and (b) HVPE GaN substrate (after [48]).*

vices, such as UV-blind avalanche photodetectors and solar cells by influencing the dark current and photoresponse [72].

Representative atomic force microscopy (AFM) images taken from GaN epitaxial layers grown on GaN template/sapphire and on polished HVPE-GaN substrate are shown in Fig. 4(a) and (b), respectively. Apparently, the epitaxial structure grown on the GaN substrates [Fig. 4(b)] reveals very good uniformity with low surface roughness root mean square (rms) typically of about 0.5 nm (over an area of 2×2 μm^2) with monolayer atomic steps and with no step terminations, contrary to the heteroepitaxial surface [Fig. 4(a)], due to much lower dislocation density intersecting the surface. We also note that the surface smoothness of bulk GaN substrates with nonpolar surface orientations is typically even better (rms below 0.1 nm), due to easier chemical mechanical polishing, thus ensuring the high-quality device epitaxy.

B. Thermal Conductivity

An additional drawback of most of the foreign substrates used for nitride-based devices is their low thermal conductivity. This is especially true for the sapphire substrates. High-power devices often require high output power and high current density, leading to high temperatures in the devices via self-heating, which reduce the device performance. A proper thermal management considers a substrate with high thermal conductivity such as SiC and AlN, but the need of a buffer and misfit dislocation generation may compromise their benefits.

There are several reports in the literature presenting finite-element calculations of the heat dissipation in nitride devices grown on thermal insulating and thermal conductive GaN substrates [73]–[75]. The thermal resistance was shown to be four to five times higher in case of using sapphire. As shown in a schematic graph of typical device structure on insulating substrate [Fig. 5(a)], the current is spread over much smaller area, leading to even more heating in the active region, which deteriorates the device performance over time as shown in Fig. 5(b) [74]. In the case of using GaN substrate, the wider area over which the
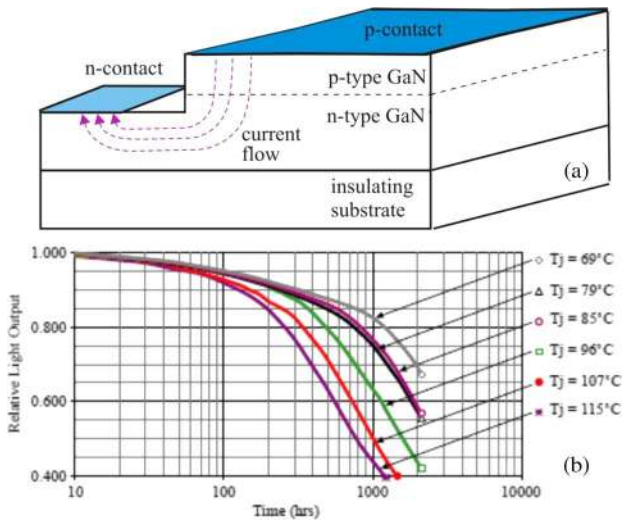
Fig. 5. *(a) Typical device structure on insulating sapphire substrate. (b) Light output variation as a function of time for a LED array. (Adapted with permission from [74].)*

current is spread additionally allows better heat extraction and leads to a reduction of the thermal resistance [76].

C. Electrical Conductivity

The advantage of the GaN substrates with good electrical conductivity over insulating substrates is multi-

faceted. Apparently the use of GaN substrates allows simplified device design, as shown in Figs. 6(b), 7(a) and (b), and 9(b), which reduces the device production cost. The vertical design also allows larger contact area and larger area for spreading the current. In addition, some devices can benefit from anisotropic characteristics of some material parameters being higher along the *c*-axis, as will be discussed in the next section.

V. DEVICES ON BULK GaN SUBSTRATES

A. Light Emitters

During the last few years, GaN-based LEDs grown on low-dislocation density substrates have been demonstrated by many groups. Compared to the same devices grown on sapphire, these LEDs show enhanced optical and electrical properties, such as reduction in current–voltage differential resistance, reduction in turn-on voltage, and increase in output power slope efficiency. As for the LDs, practically all the GaN-based lasers have been demonstrated on bulk substrates. With improvement of the substrate and epitaxial quality as well as the device optimizations, the green range was approached. The longest wavelength achieved recently is 500–514 nm at 5 mW by Nichia [77].

Conventional *c*-plane quantum-well structures, in both cases grown on sapphire [Fig. 6(a)] and on GaN substrate [Fig. 6(b)], suffer from the undesirable quantum-confined
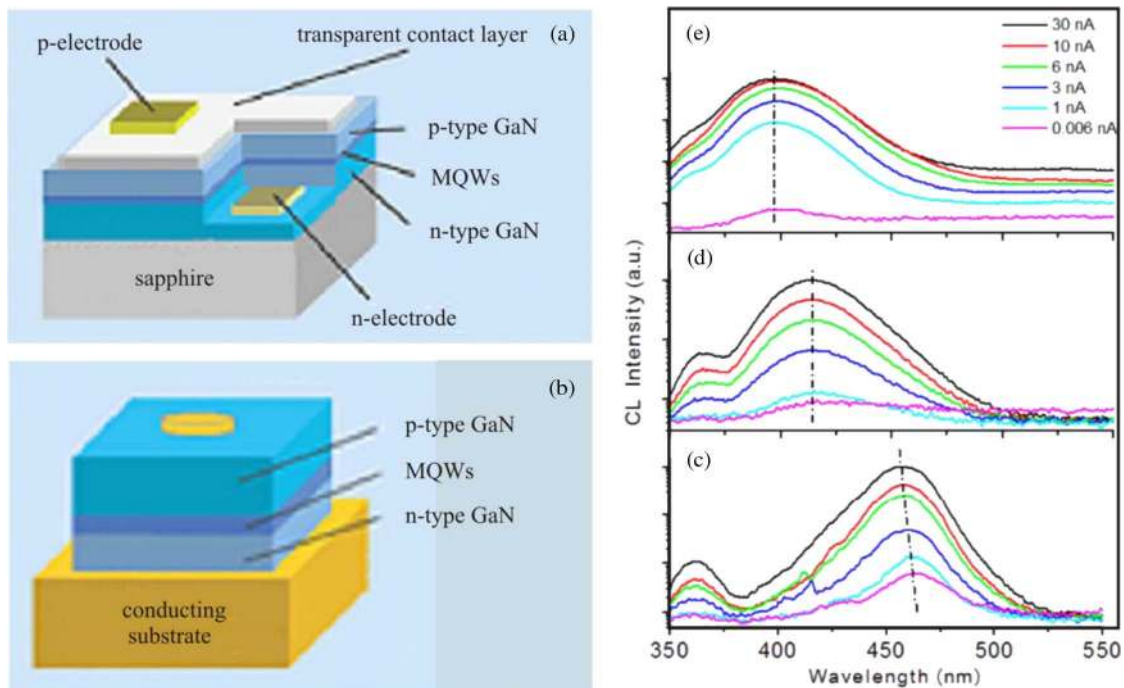

Fig. 6. *Typical LED structure on (a) insulating sapphire substrate and (b) conducting substrate (compoundsemiconductor.net). CL spectra of LED grown on (c) sapphire substrates, (d) c-plane GaN, and (e) m-plane GaN (after [78]).*

Table 2 Development of LD on Nonpolar and Semipolar Bulk GaN Substrates

Wavelength	Characteristic	Substrate	Reported
400 nm	cw	(1-100)	Feb. 2007 [90]
405 nm	pulse	(1-100)	Feb. 2007 [91]
411 nm	Clad. layer free	(1-100)	March 2007 [92]
406 nm	pulse	(10-11)	May 2007 [93]
403 nm	cw	(1-100)	Aug. 2007 [94]
452 nm	pulse	(1-100)	Sept. 2007 [95]
405-474 nm	pulse	(11-22)	Dec. 2007 [96]
460 nm	cw	(1-100)	Dec. 2007 [97]
463 nm	pulse	(1-100)	Jan 2008 [98]
481 nm	cw	(1-100)	June 2008 [99]
499.8	cw	(1-100)	March 2009 [100]

Stark effect (QCSE), due to the existence of strong piezo-electric and spontaneous polarizations. The strong built-in electric fields along the **c**-direction cause spatial separation of electron and holes that in turn gives rise to lower carrier recombination efficiency, reduced oscillator strength, and blue-shifted emission. The QCSE becomes more pronounced with increasing indium composition in InGaN QWs needed for longer wavelength LEDs, and a noticeable blue shift of the emission occurs with increasing current [Fig. 6(c)], while the effect is less pronounced at shorter wavelength [Fig. 6(d)] with less In amount in the QW [78].

The LED and LD devices can ultimately benefit from the use of designs that enable the active region to be parallel to nonpolar planes and thereby reduce the build-in electric fields as discussed above. However, the use of foreign substrates for the heteroepitaxial growth of GaN in direction different from the [0001] axis favors the generation of stacking faults in addition to high dislocation density, which act as self-formed quantum wells at certain wavelengths and thus prevent emission from intentionally formed QW at shorter wavelengths. LEDs at different wavelengths have been produced during the last several years with different surface orientations, showing no emission shift with increasing current and confirming the absence of polarization induced field in nonpolar QWs for violet [79], [80], blue [81], [82], and green LEDs [83]–[85]. However, the external quantum efficiency in these devices was disappointingly low. Only recently, with the availability of bulk GaN nonpolar and semipolar substrates sliced form boules, the performance of the LEDs devices grown on them was significantly improved. With the current increased efficiencies and output power levels [86]–[89], LEDs are now considered more promising for SSL due to reduced power consumption, high durability, and lower maintenance cost, not to mention reduced carbon footprint on the environment. There are still unresolved questions like In incorporation efficiency in layers grown on GaN substrates with different surface orientations, resulting in different emission wavelength [as in Fig. 6(d) and (e)] in

simultaneously grown samples in the [0001], [1–100] and [11–20] directions [78], [84], [85] on GaN substrates. Further knowledge gained on this issue as well as a further increase of the substrate size will allow better control of In incorporation for achieving the desired wavelengths.

In addition, the availability of low-defect-density bulk GaN substrates sliced from boules with nonpolar and semipolar orientations allowed production of laser diodes at longer wavelengths approaching the "green gap" during last few years [90]–[100]. Table 2 summarizes the recent development of nitride-based LD emitting in the range of 400–500 nm.

B. Schottky Diodes and Power Switches

High-power diodes and switching devices based on GaN substrates, such as GaN Schottky diodes and power heterostructure field-effect transistors (HFETs), show performance dependent on defect density and therefore should benefit from the lowest possible defect density. Pure screw dislocations have been identified as a path for reverse-bias leakage current in GaN [101], [102]. Growing on a GaN substrate with reduced total dislocation density and, therefore, the screw dislocation density at the surface reduces the gate leakage current. Schottky barrier diodes have been fabricated that have shown some benefits of using bulk GaN [Fig. 7(a)] over sapphire as the substrate material, where improvements in the reverse recover time, on-resistance, reverse breakdown, and reverse leakage current were reported [103]–[105]. By using a free-standing GaN substrate, a vertical geometry Schottky diode with a full backside ohmic contact [Fig. 7(b)] can be fabricated, which enables higher current conduction than lateral devices [Fig. 7(a)]. Recent research shows that vertical mobility in GaN Schottky diodes is about six times higher than the lateral mobility [104]. Improved reverse breakdown voltage performance, manifested by high breakdown field [Fig. 7(c)] and its relatively low slope versus diode diameter [inset in
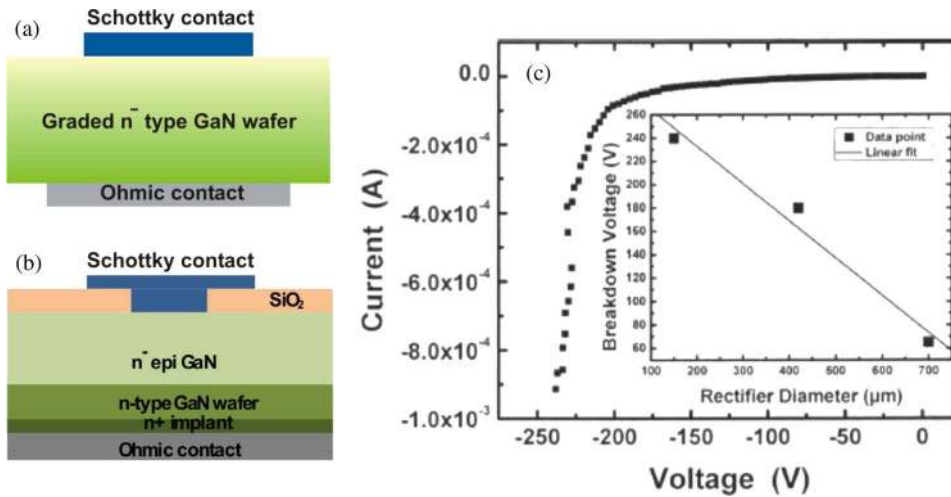
Fig. 7. *(a), (b) Two vertical structures of Schottky diode fabricated on GaN bulk material. (c) Reverse breakdown characteristics of a diode with structure shown on (a). The inset shows a plot versus diode diameter (after [104]).*

Fig. 7(c)], for vertical device geometries indicates that the vertical depletion mode has a more uniform field distribution than lateral mode, which minimizes premature breakdown caused by field crowding at contact edges. The reverse recovery characteristics of the Schottky rectifier, when the diode was switched from forward to reverse bias, showed an ultrafast switching time of less than 20 ns, similar for both types of device structure. Although the vertical device is expected to display better reverse recovery characteristics than the lateral one due to the "dislocation-blind" vertical transport and further research is needed to clarify this point, the vertical transport mode appears to be superior and promising in high-frequency device application.

In several research publications over the past two years on GaN-based HFETs for power switching, a move to develop bulk GaN based power switching devices was suggested [106], [107]. While SiC and GaN are both excellent candidate materials for Schottky diodes and MOSFETs, GaN is expected to surpass the SiC due to its superior materials properties. Fig. 8 shows a summary of the published experimental results for the on-resistance (Ron) versus the breakdown voltage (BV) for GaN FETs and diodes. The theoretical limits for devices made from Si, SiC, and GaN are also shown in the figure [108]. For current devices, the performance of GaN devices exceeds the Si limit and is approaching the SiC limit, with much additional progress to be made via further improvements in material quality and optimization of device layer design and fabrication approach. Improved GaN device performance relative to SiC is expected to extend to devices such as HFETs and MOSFETs, which can be used as the transistor in converter and inverter circuits. Higher channel mobilities for GaN MOSFETs relative to SiC have been demonstrated and are expected to even further increase with decreasing defect density. As a

result, the channel component of the on-resistance is expected to be even lower for GaN MOSFETs, and the drift component to be lower due to the higher breakdown electric field. Thus, even higher efficiency switching GaN MOSFET is expected due to lower switching losses when compared to SiC.

C. RF HFETs

At present the high-frequency high-power electronics relies on wide-bandgap material and particularly on AlGaN/GaN material system. The unique properties of nitride-based high electron mobility transistors (HEMTs) result from polarization phenomena at the heterostructure QWs and from the nitrides' robust physical parameters, which lead to high output power density, high operation
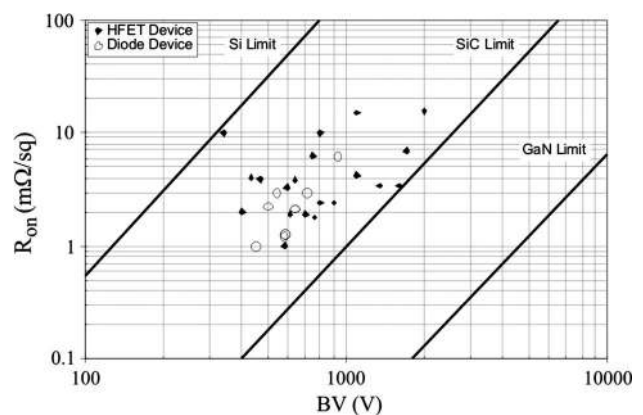

Fig. 8. *On-resistance versus breakdown voltage for GaN FET and diodes. The performance limits for Si, SiC, and GaN devices are shown by the solid lines (after [108]).*
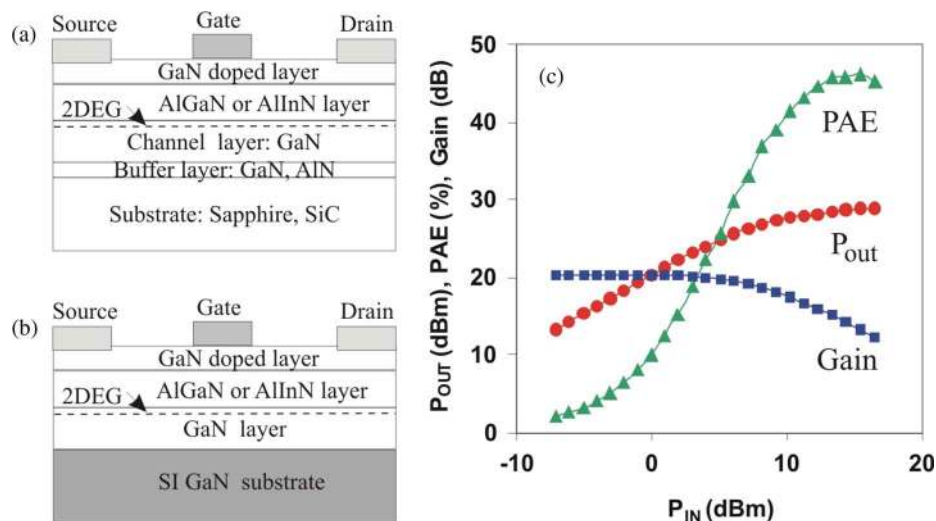
Fig. 9. *Typical structure of HEMT grown on (a) foreign substrate and (b) semi-insulating GaN substrate. Output power, gain, and power-added efficiency at 4 GHz of device with 150-μm-wide gate (after [115]).*

voltage, and high input impedance due to unique properties of GaN, such as high breakdown voltage and large bandgap. Owing to the piezoelectric and spontaneous polarization, AlGaN/GaN HFETs grown on *c*-plane sapphire or SiC have two-dimensional electron gas (2DEG) densities of $\sim 1 \times 10^{13}$ cm^{-2}, even without doping the barriers [109]. Moreover, by increasing the Al composition in the barrier, the sheet carrier density can be increased further, which is desirable for high-power high-frequency applications [110]. When a thin (of about 7 nm) AlN barrier is used, 2DEG densities could be as high as 5×10^{13} cm^{-2}, which is near the polarization limit [111]. However, for Al compositions larger than 40%, due to the large lattice mismatch between GaN and AlGaN, inferior barrier quality significantly reduces the mobility [112] and therefore the device performance. To address this issue, Kuzmík proposed using a nearly lattice-matched AlInN/GaN material system to improve the performance of HFETs with high sheet carrier densities provided by spontaneous polarization only [113], [114]. So far, the growth on lattice-mismatched substrates (sapphire, SiC) was unavoidable [Fig. 9(a)], and the resulting layers contain a large number of threading dislocations. To address this issue, use of high-quality substrates with a low dislocation density is needed. The large-scale semi-insulating GaN templates with reduced dislocation density may be one solution to the material quality problem, but not necessarily sufficient due to the remaining strain-induced defects in growth on foreign sapphire, as well as remaining sapphire with very low thermal conductivity. Therefore, eliminating the foreign substrate is needed, so that higher quality native bulk substrate material with high thermal conductivity can be used to enhance the device performance [Fig. 9(c)].

There is a small but growing number of studies investigating the use of semi-insulating GaN substrates for radio-frequency (RF) HEMT applications [114]–[118]. Researchers at the U.S. Naval Research Laboratories have grown via MBE AlGaN/GaN HEMTs on semi-insulating GaN substrates [116], [117]. Comparative analysis revealed that for all device metrics examined, the performance of HEMTs on GaN substrates relative to those on SiC was improved. Fig. 9(c) shows device performance characteristics, including an off-state breakdown voltage in excess of 200 V, low gate leakage, and an output power density over 5 W/mm at 4 GHz and 4.8 W/mm at 10 GHz. Microwave measurements on 0.45 mm gate-length devices yielded f_T and f_{MAX} of 36 and 56 GHz, respectively, demonstrating excellent device performance attainable by RFplasma-assisted MBE grown HEMTs on low dislocation density HVPE-GaN substrates. Another study showed 9.4 W/mm at 10 GHz for HEMTs on GaN substrates with improved reliability when compared to similar devices on SiC substrates [118]. The improved performance of nitride-based HEMTs is promising for their potential wide application in satellite broadcast equipment, mobile phones, GPS navigation systems, broadband wireless access systems, and other core technologies fundamental to our information-driven society.

VI. SUMMARY

Native bulk GaN substrates have been intensively developed by several growth techniques. Availability of this material is constantly increasing in amount, size, doping, and orientation alternatives. Their use in device growth is proven as beneficial for improvement of the performance of all devices under consideration and for

device production cost reduction for some devices. Further improvement of the substrate quality, along with increasing size and decreasing cost, is expected in the near future, which will in turn influence the device quality and cost. ∎

Acknowledgment

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