Materials Science Forum
ISSN: 1662-9752, Vol. 1062, pp 463-467
doi:10.4028/p-4b1mb3
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Submitted: 2021-09-30
Revised: 2022-02-08
Accepted: 2022-02-09
Online: 2022-05-31

Gate Bias Effects on SiC MOSFET Terrestrial-Neutron Single-Event Burnout

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Keywords: Silicon Carbide, MOSFET, oxide reliability, TDDB

Abstract. Power devices are susceptible to failure by terrestrial neutron single-event burnout (SEB) while in the high-voltage blocking state and above a V_{DS} threshold for that device. Typically, the SEB failure rate is measured at a high blocking voltage, with the source and gate at ground potential. Here the effect of a negative gate bias, commonly applied during MOSFET switching to the blocking state, on the SEB failure rate is examined. It is observed that the SEB failure rate is only weakly dependent on the negative gate bias, because it does not significantly affect the peak field in the drift region where avalanche breakdown is initiated. A negative gate bias of -8V_{GS} in the device blocking state at 1100V_{DS} only results in a 6% increase in the MOSFET SEB failure rate.

Introduction

All power devices are susceptible to failure by terrestrial neutron single-event burnout (SEB) in the high drain bias (V_{DS}) blocking state, above a V_{DS} threshold for that device. This had been discovered initially for Si-based power devices [1,2], and more recently shown for SiC diodes and MOSFETs [3-7]. Typically, the SEB failure rate is measured at a high blocking voltage with the source and gate at ground potential. In this study the effects of a negative gate bias, while at high V_{DS}, on the SEB failure rate are examined, to better match conditions of MOSFETs switched to the off-state using a negative gate bias.

Experimental and Results

Neutron SEB testing of MOSFETs has been performed at Los Alamos National Laboratory (LANL) using their spallation neutron source, as described in [6]. Groups of 12 devices are tested at given V_{GS} and V_{DS} bias conditions (all at 25°C), run until some or all the devices fail, and the failure time is correlated with the neutron fluence to determine a neutron fluence per fail. Fresh sets of 12 parts are mounted for each test at given V_{DS} and V_{GS} values. At very low V_{DS}, only a few devices may fail because the test time needed is very long if the FIT rate is low; while at V_{DS} closer to the rated voltage the test is typically run until all devices in the group fail. The failure rate is converted to the sea level neutron flux level, and the overall FIT rate is obtained for each group using the failure data for all the failed parts in the group, as described in JEP151 [8], and modeled with a trend line as presented in [9]. TCAD simulations of the MOSFET gate field under the various device bias conditions have also been performed to demonstrate electric field effects of the applied bias conditions. The TCAD model has Fowler-Nordheim tunneling enabled, and both hole and electron carriers. The TCAD modeling is not meant to describe the SEB event, but only to show the oxide and SiC fields under the SEB test conditions.

Presented here are results from Wolfspeed 1200V 16mohm SiC MOSFETs (C3M0016120K, Gen3), measured under neutron irradiation at LANL. Figure 1 shows the mean failure in time (FIT, fails per billion device hours) scaled to the NY city sea level average flux value, from groups of 12 devices tested to failure at each V_{DS} condition, at V_{GS} = 0V and room temperature. The points on the graph are the FIT rate obtained from all the failures in each V_{DS} group [8]. The SEB failure for

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these devices follows trends with V_{DS} typically observed for vertical power devices [5, 7, 9], indicating that below a given V_{DS} value failure rates are exceedingly small.

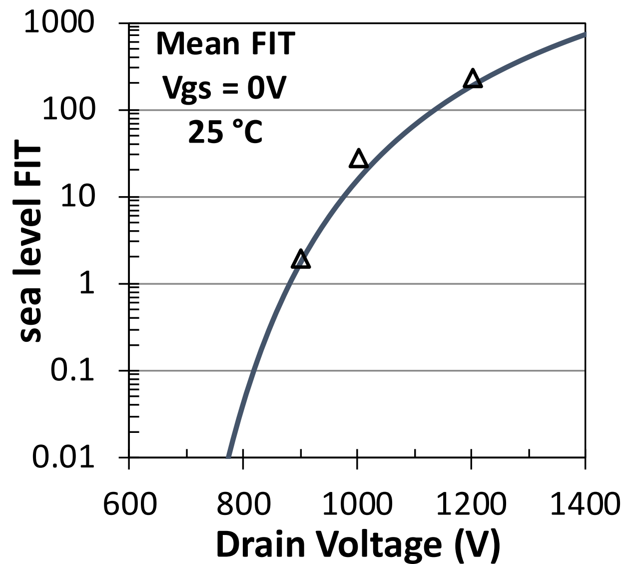

Fig. 1. Mean FIT versus V_{DS} for Wolfspeed G3 1200V 16mohm SiC MOSFETs, with V_{GS} = 0V. FIT rate is strongly dependent on the V_{DS} value.

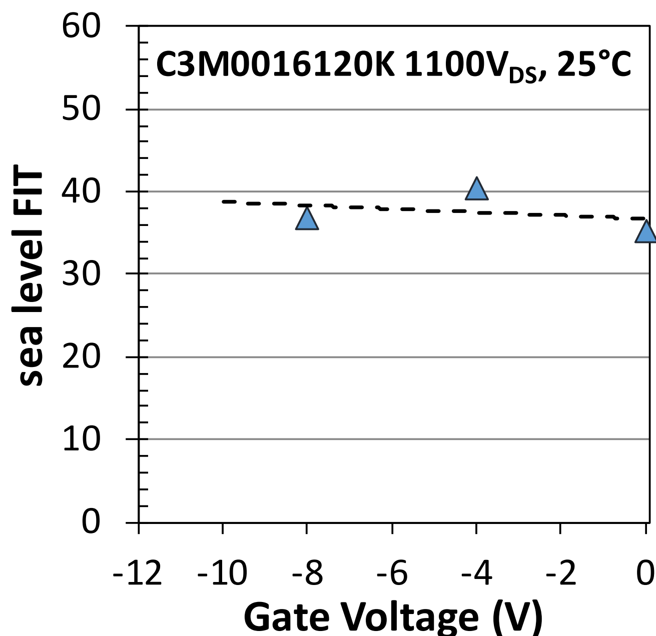

Fig. 2. Mean FIT versus V_{GS} for Wolfspeed G3 1200V 16m SiC MOSFETs, with V_{DS} = 1100V. FIT rate is weakly dependent on the V_{GS} value.

The effects of negative gate bias on the mean failure rate are shown in Fig. 2 for the Gen3 1200V 16mohm devces. The recommended gate turn-off voltage for this device is -4V, while the minimum rated gate bias is -8V. The result of decreasing the V_{GS} from 0V to -8V on the mean FIT rate at 1100V_{DS} reveals there is overall a small increase in the failure rate as the negative gate bias increases, but the effect is small. The SEB failure rate on average appears to increase about 1% per volt of -V_{GS} applied.

To understand better the effect of the negative gate bias on the device, TCAD MOSFET simulations of these planar devices (half-cells shown) have been used to compare the SiC and gate oxide fields under 1200V V_{DS} conditions, and at V_{GS} of either 0V or -8V. As shown in Figs. 3 and 4, the effects of applying the negative gate bias on the electric fields in the MOSFET are confined

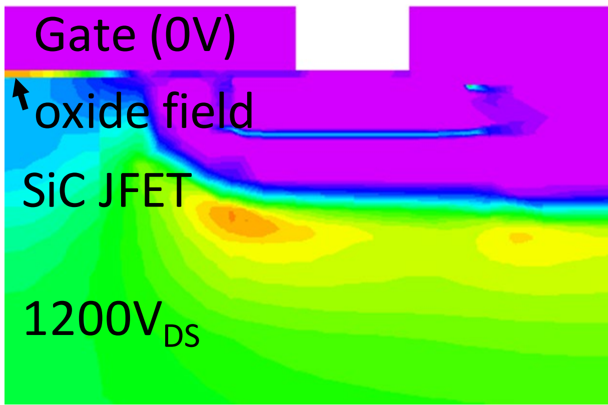

Fig. 3. TCAD MOSFET simulation at $1200V_{DS}$ and V_{GS} = 0V showing E-field distributions.

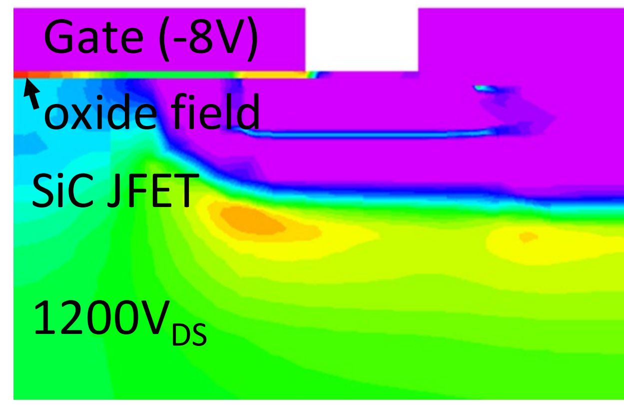

Fig. 4. TCAD MOSFET simulation at $1200V_{DS}$ and V_{GS} = -8V. Note the increased gate oxide field.

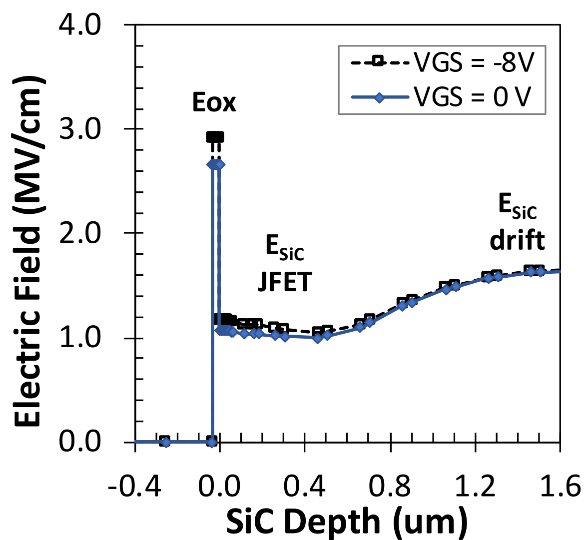

Fig. 5. TCAD electric field cutline along the JFET center (left edge of Figs. 3 & 4). Note the higher oxide and JFET fields for V_{GS} = -8V.

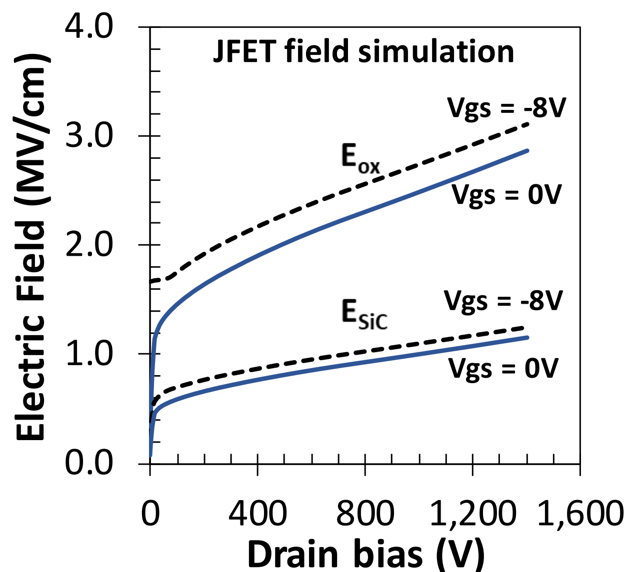

Fig. 6. TCAD derived oxide field and peak SiC field at the top center of the JFET region of the MOSFET, as V_{DS} and V_{GS} bias levels change.

to the gate oxide region and the SiC JFET region. Note in Fig. 4 that the gate oxide in the left edge of the image near the arrow (the center of the JFET region in the full device cell) has reached a higher field, but the field in the drift itself is relatively unchanged. To demonstrate this more clearly, Fig. 5 shows the E-field versus depth through a cutline along the JFET center (left edges of Figs. 3 and 4), from the gate down through the SiC drift. The fields in both the oxide and SiC at the JFET center increase as V_{GS} increases in the negative bias direction. The peak oxide field and SiC peak JFET field just under the oxide increase ~9% when V_{GS} is decreased from 0V to -8V. The fact that this closely matches the observed SEB failure rate increase with V_{GS} indicates a correlation between the gate bias and the SEB failure rate. Fig. 5 shows that the field in most of the SiC drift layer, below the JFET region, is unaffected by the applied gate bias, and is higher than the JFET field, due to the P-well shielding of the JFET region. Note that the gate oxide field under $1200V_{DS}$ blocking and $-8V_{GS}$ obtained in these TCAD simulations is lower than the typical MOSFET on-state gate oxide field, which is about 4MV/cm for a $15V_{GS}$ bias.

To better understand the effects of the V_{DS} and V_{GS} bias, the simulated JFET peak SiC field (just under the oxide at the JFET center) and peak oxide fields in the center of the JFET gap are shown in Fig. 6 as a function of the V_{DS} value, for V_{GS} values of either 0V or -8V. The negative gate bias increases the oxide field and the SiC field at the JFET center, for all V_{DS} values. The results in Fig. 6 show that the electric fields in the JFET region with V_{DS} of 1100V and V_{GS} of -8V are equal to the electric fields obtained with V_{DS} of 1360V with V_{GS} = 0V. If the SEB failure were controlled by the JFET fields alone, then at 1100V_{DS}, applying -8V_{GS} would result in a similar SEB rate to that at 1360V_{DS} with V_{GS} = 0V. From Fig. 1 that would indicate that the SEB rate should increase ~8X when -8V_{GS} is applied; but from the results in Fig. 2 this is clearly not the case. Only a 6% increase in SEB is observed when increasing the V_{GS} from 0 to -8V at 1100V_{DS}.

Considering the rate of SEB failure observed from V_{DS} and V_{GS} changes in Figs. 1 and 2, and the electric field simulations, the SEB failure rate is clearly more strongly dependent on V_{DS} than V_{GS}, in the valid ranges of device operation. The drain field effects of the applied V_{DS} dominate the SEB failure rate overall because the locations of the device going into avalanche breakdown are controlled primarily by the drain bias. The effect on avalanche voltage of field changes at the top of the JFET region due to V_{GS} effects are very small. Note that the peak SiC fields where avalanche breakdown would be initiated are below the P-shielding region (in Figs. 3 and 4), which is not significantly affected by the applied V_{GS}. The electric field in the JFET region due to applied gate bias would only affect the SEB rate if it changes the electric field where the field peaks occur (making avalanche breakdown more likely), which it does not.

These results, which indicate that the JFET region is not a significant contributor to SEB failure, is in general agreement with other results [5, 6] which show that the failure rates of SiC diodes and SiC MOSFETs are similar when the data are properly scaled to device active area and drift field, using avalanche breakdown field as a normalization factor. Device turn-off with negative V_{GS} poses no significant SEB risk, because the SEB failure rate is dominated by the applied drain bias.

Summary

The measured SEB failure data shows that applying -8V V_{GS} at 1100V V_{DS} only results in a 6% increase in the SEB failure rate. This generally agrees with the TCAD simulations showing that the oxide field and peak SiC field in the JFET center only slightly increase with negative V_{GS} applied. The effects of the applied V_{DS} on SEB failure rate are much larger than the effect of applying a small negative V_{GS}. The peak SiC fields, which determine the avalanche voltage, are in the drift region below the JFET region (in the P-shielding region), and these are not significantly affected by the applied V_{GS}. Thus, the SEB failure is dominated by the effects of the drain bias, and gate bias effects are minimal.

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