Gate dielectric surface modification in organic field-effect transistors

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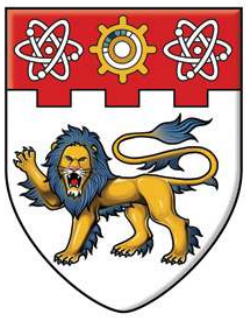

NANYANG TECHNOLOGICAL UNIVERSITY

GATE DIELECTRIC SURFACE MODIFICATION IN ORGANIC FIELD-EFFECT TRANSISTORS

FENG CHENGANG

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2012

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
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2012

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research and has not been submitted for a higher degree to any other University or Institution.

_____ _____

Date Feng Chengang

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EXECUTIVE SUMMARY

Organic semiconductors attract intensive research interest because of their unique properties, such easy fabrication, mechanically flexibility, and low cost. They are now widely used as active elements in optoelectronic devices including light-emitting diodes, thin-film field-effect transistors, solar cells and memories, among which organic field-effect transistors (OFETs) offer a suitable building block for many flexible, large-area applications such as display backplanes, electronic textiles, and robotic skin. Interestingly enough, OFETs grew in parallel with another device, the organic light-emitting diode (OLED). However, the development of OLEDs has been much faster than that of OFETs, so that commercial products based on OLEDs are now available on the market, which is not yet the case for OFETs.

In the past few years, much research effect has been directed at improving the charge-carrier mobility by better materials and device architectures, subsequently, OFETs are able to match, and in some cases even exceed, the basic transistor performance of amorphous silicon (a-Si) thin-film transistors (TFTs). As OFETs are now moving closer to applications, their operational stability and the control of threshold voltage becomes more crucial than ever. In this thesis, we primarily focus on engineering the interface between organic semiconductor and gate dielectric by dielectric surface modification, which play a decisive role in the functioning of OFET devices, in a top contact bottom gate structure that avoids the influence of the interaction metal contact and the active layer.

The work contained in this thesis is firstly directed toward studying the effect of buried traps at dielectric-dielectric interface on the device stability. Hysteresis-negligible pentacene FET devices were demonstrated in the dark condition by using PVP-*co*-PMMA to modify the surface of SiO_2 gate insulator. However, the threshold voltage of such devices still can be greatly shifted due to the charge trapping mechanism (minority carrier) by the application of a gate bias under illumination. It suggested that the negligible hysteresis might originate from the dynamic balance of trapping/detrapping charge carriers in our devices. Therefore, it can be concluded that only the demonstration of hysteresis-free FET devices is not nearly enough, one still needs trying to reduce the possibility of charge trapping, or even eliminate it. In order to minimize the charge trapping at the interface between semiconductor and gate dielectric, highly purified PMMA was utilized to substitute PVP-*co*-PMMA as buffer dielectric because of the absence of hydroxyl groups acting as traps. When a thin PMMA buffer dielectric (10 nm) was used, the photo-generated non-equilibrium electrons (holes) in pentacene (C_{60}) active layer near the dielectric surface can also be injected into the buried

traps at the surface of SiO_2 passivated by thin PMMA layer, inducing the shift in threshold voltage. By understanding the charge trapping mechanism, such photo-induced charge transfer can be effectively suppressed with optimized thickness of PMMA ($45\,\mathrm{nm}$) buffer dielectric, thus, stabilize the threshold voltage. This work also shows that besides the device encapsulation and the development of new organic semiconductors (OSCs) combining high mobility with excellent stability, data presented in this work brings out an alternative approach to enhance the stability of OFET devices using dual gate dielectric and a guide about how to select a proper buffer dielectric. From a scientific perspective, it is also very interesting to study the mechanism of charge transfer across a buffer dielectric.

For the low-voltage FET devices (operating at $1\,\mathrm{V}$), 12 nm high-κ materials hafnium oxide (HfO_2) was used as gate insulator, which was grown on silicon substrate by atomic layer deposition at a temperature of $250\,℃$. In this work, the effect of oxygen plasma treatment at the HfO_2 surface upon the device performance was thoroughly investigated under atmospheric dark condition. With proper exposure time (t_e), not only mobility but also the stability of devices was improved, attributing to the ultraclean surface of HfO_2 with lower concentration of oxygen vacancies and increased grain size of pentacene film. A mobility of $0.056\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ with a threshold voltage of $-0.23\,\mathrm{V}$ was achieved at $t_e = 15\,\mathrm{s}$. The subthreshold slope decreased with increasing t_e and a minimum value of $157\,\mathrm{mV\,decade^{-1}}$ was obtained. However, pentacene film on plasma-treated HfO_2 was more fragile due to the surface stress enhanced weathering effect. Moreover, oxygen plasma treatment also offers the good tunability of the threshold voltage, as compared to other surface modifications using HMDS, OTS and cross-linked PVP as buffer dielectric that would increase the threshold voltage by lowering the gate capacitance, as the thickness of used low dielectric OTS and cross-linked PVP is comparable to, even larger than that of ALD grown HfO_2.

This thesis also demonstrates the heterostructure FET devices with a polymeric light-emitting material, crystallized PFO or amorphous PVK, buffer layer. These hole-transport polymers were chosen to form a type I hetero-junction (straddling gap) with pentacene in a FET structure, to study the electronic structure of their interface as well as the charge transport along and charge transfer across such interface, which also can be considered as a complement to the semiconductor-dielectric system such as PVA/P3AT and/or Parylene/rubrene. The heterostructure devices exhibit a typical p-channel operation: for low negative V_g, both field induced charges and photo-generated charges could be confined in the channel layer due to the large ΔE_{HOMO}; for high negative V_g, holes were expected to be distributed in both layers. Interestingly, the threshold voltage of such devices can be controlled through varying the positive starting source-gate voltage V_{g_start} under illumination due

to the trapping of photogenerated electrons in PFO (or PVK) layer and the interface, e.g. by varying V_{g_start} from 60 to 200 V in the off-to-on transfer curve, a total shift in V_{th} of ca. 137 V was obtained in PFO-FETs, namely, V_{th} varied from -14.6 to 122.5 V. The trapping of photogenerated charge is also studied in terms of hysteresis behavior. It is found that the hysteresis window ΔV_{th} was mainly determined by V_g in PFO-FETs, while it was strongly correlated with the value of V_g & V_{ds} and the sweeping direction of V_g in PVK-FETs, indicating a different charge injection mechanism. However, the maximum ΔV_{th} exceeded the half of the total sweep range of V_g in both devices, showing their great charge storage ability. Such light-programmable feature might motivate the development of a new type of organic memory devices.

SYMBOLS AND ABBREVIATIONS

C_i	Capacitance per unit area of the gate dielectric
F	Transverse electrical field
I_{ds}, V_{ds}	Source drain current, Source drain voltage
L, W	Channel length, Channel width
κ	Kappa
S	Subthreshold slope
t_e	Plasma exposure time
V_g, V_{th}	Source gate Voltage, Threshold voltage
μ	Field-effect mobility

a-Si	Amorphous silicon
AFM	Atomic Force Microscope
ALD	Atomic Layer Deposition
BSC/FSC	Back/Forward sweep current
GB	Grain boundary
HMDS, OTS	Hexamethyldisilazane, Octadecyltrichlorosilane
HOMO	Highest Occupied Molecular Orbital
LUMO	Lowest Unoccupied Molecular Orbital
MNOS	Metal-Nitride-Oxide-Silicon
MOS	Metal-Oxide-Semiconductor
OFET	Organic Field-Effect Transistor
OLED	Organic Light-Emitting Diode
OSCs	Organic Semiconductors
OTFT	Organic Thin-Film Transistor
PFO, PVK	Poly(9,9-dioctylfluorene), Poly(*N*-vinylcarbazole)
PMMA	Poly(methyl methacrylate)
PVD	Physical Vapor Deposition
PVP-*co*-PMMA	Poly(4-vinylphenol-co-methyl methacrylate)
SAM	Self-assembly monolayer
TC	Top Contact
UV	Ultraviolet
XPS	X-ray Photoelectron Spectroscopy
XRD	X-ray Diffraction

CHAPTER 1: INTRODUCTION

1.1 MOTIVATION

Interest in organic electronics stems from the ability to deposit organic films on a variety of very-low-cost substrates and the relative ease of processing of the organic compounds that are currently being engineered by hundreds of chemists. The field known as "organic" or "plastic" electronics is centered on field effect transistor (FET)-based circuits mounted on these large-area and/or flexible substrates, such as glass, plastic or metal foils.

FET devices fabricated using organic materials with semiconductor-like properties have garnered tremendous interest for use in applications requiring relatively limited electronic function and performance. The applications where organic FETs may best find use are those exploiting the unique capabilities offered by organic materials, notably their "soft" properties, which permit circuit fabrication on cheap flexible plastic substrates and the use of high-throughput roll-to-roll processing. Typical examples of such applications include (i) switching devices for active matrix flat panel displays (AMFPDs) based on liquid crystal pixels (AMLCDs), organic light emitting diodes (AMOLEDs), or "electronic paper" displays[1] based on pixels comprising either electrophoretic ink-containing microcapsules[2] or "twisting balls",[3] (ii) sensor arrays,[4] (iii) smart cards (addressable ID and vending cards) and (iv) radio-frequency identification tags (RFIDs).[5] Together these applications represent a

large and growing macroelectronics market, which has proved to be surprisingly challenging for organic electronics to tackle.

One bottleneck is the device geometry result from the limited methods of patterning the organic semiconductor layer. Organic material is not suitable for photolithography, therefore we have to use shadow mask, spin coater and sputter. Limited methods means undesired effects might dominate the characteristics, such as increased leakage and subthreshold slope stem from less control of the charge induced by the gate metal. Bottom contact structure affects the grain size and the crystal disordering due to the surface energy of the contact metal and interface issue between metal and organic material.[6] Pentacene molecules, for example, prefer to "stand up" with the long axis of the molecule perpendicular to the plane of the substrate when deposited on the commonly used insulator SiO_2.[7] When deposited on top of gold contacts, however, strong interactions between the pentacene π-clouds and the metal surface lead to tiny grains at the contact and, in some cases, voids are observed.[6]

Process condition is another significant issue of organic material. Low cost and large scale fabrication can be performed by spin-coating, stamping, and printing. These easy processes make the fabrication cost lower than inorganic material, but the organic must be soluble during these processes. However, most of the organic materials are not soluble unless side chains are added to the molecules of the polymer material. But the side chains could alter the chain arrangement of polymer and affect the performance of the current characteristic. Vacuum deposition which requires more expensive processes but provides a high degree of control over variables such as time, sublimation

temperature, temperature of the substrate during deposition and base pressure, has better performance and is a very powerful tool to study the device physics (e.g. charge transport mechanism), nevertheless, less compatible with plastic substrates.

One of more significant than above issues is the mobility problem. Even operating at large voltage ($10\sim50\,\mathrm{V}$), organic transistor render only several $\mu\mathrm{A}\,\mu\mathrm{m}^{-1}$. The power consumption results from the high operating voltage and could cause the devices unreliable. Mobility is mainly dependent on the semiconductor materials, the semiconductor-dielectric interface and device architectures, and different combinations of materials result in different mobility. Among the OFET devices reported, pentacene is typically employed as the channel layer due to its superior carrier mobility, which results from the high degree of molecular ordering seen during its film growth.[6,8-10]

Another major problem that hinders the development of practical OFET devices is that current devices require rather high voltage to operate, while in a typical low-end application, the available voltage will be very low. The key to low voltage operation is the reduction of the threshold voltage and the inverse subthreshold slope. The transistor parameters are largely controlled by the gate insulator rather than the semiconductor. Consequently, the search for gate dielectrics with low leakage current, low interface trap density, high breakdown strength, and high capacitance that are consistent with cheap, basic manufacturing methods is one of the current challenges of organic electronics. Typically, low-voltage devices can be achieved through increasing the unit capacitance of gate dielectric C_i by (i) increasing the dielectric constant, and (ii) reducing its physical thickness, according to $C_i = \frac{\varepsilon_0 \varepsilon_r}{d}$. Therefore, a number of

materials have been investigated, such as metal oxide (e.g. Al_2O_3,[11] Ta_2O_5,[12-15] TiO_2,[16,17] ZrO_2,[18,19] HfO_2[20-22] etc) , ultrathin cross-linked polymeric dielectric (e.g. P4VP and PMMA etc),[23-26] and self-assembled molecular dielectric.[27,28]

As OFETs are moving closer to applications, their stability under realistic atmospheric as well as electrical operating conditions has come under more intense scrutiny. In order to improve the device stability, much effort in the past few years has been devoted to (i) developing materials that combine high field-effect mobility with excellent environmental stability,[29-32] (ii) engineering the interface (e.g. metal contact-semiconductor and/or dielectric, and semiconductor-dielectric),[33,34] and (iii) encapsulating the device with a suitable permeation barrier, such as polymeric layers, hybrid organic-metallic layers, nitrides and inorganic oxides.[35-37]

From the issues mentioned above, we know that there is still a long way to go to significantly reduce the cost of manufacturing OFETs as compared to mainstream thin film transistors while delivering similar performance, but, we believe, now it is not too much away.

1.2 OBJECTIVES

This thesis is primarily focusing on engineering the interface through the surface modification to tune the chemical properties of gate insulator. Work is directed first towards designing and setting up of a powerful physical vapor deposition system. Subsequently, it studies the effect of wet and dry treatment methods to modify the semiconductor-dielectric interface, thus, minimize the trapping of charge and improve the device stability. Finally, it targets at

realizing the control of threshold voltage in the heterojunction FET devices. As such this PhD project has the following main objectives:

- *Set up a high-vacuum deposition system.* To perform a straight forward fabrication of various organic semiconductors and/or metals on various substrates without exposure to air.
- *Investigate the influence of buried trapping states at dielectric-dielectric interface on the device stability.* Studies will be conducted by taking into account the nature of buffer dielectrics for improving the device stability.
- *Study the effect of oxygen plasma treatment on the gate insulator, subsequently, the device performance.* The advantages of this method will be manifested by the improvement of field-effect mobility as well as the control of threshold voltage etc in low-voltage FET devices.
- *Explore novel FET devices by employing organic heterojunctions.* To study the electronic structure of the interface between two OSCs as well as the charge transport along and charge transfer across such interface.

In general, the study on the device stability in this thesis, which suggests an easy-to-realize fabrication method to produce high-performance reliable devices, is expected to be useful in applications beyond the scope of this project.

1.3 SIGNIFICANCE AND MAJOR CONTRIBUTIONS

This thesis demonstrates that employing a FET structure with dual dielectric is an efficient way to enhance the device stability, where they would compensate both dielectrics' drawbacks, for example, the buffer dielectric

forms few defects at the interface but has a low electrical strength/dielectric constant, while high-κ gate insulator uses low voltage but has poor interface. It also brings out a general method to realize stable OFETs with fairly good mobility, even under illuminated condition, which is important for the applications of OFET devices as switchers for flat panel displays.

Secondly, oxygen plasma treatment is proved to be very effective to improve the quality of 12 nm low-temperature ALD grown HfO_2 and its interface, subsequently, the electrical performance and the stability of low-voltage pentacene FETs. More interestingly, the study on aging of pentacene film grown at the surface of plasma-treated HfO_2 gives us a direct insight into how these devices degrade in atmospheric condition.

This thesis also describes molecular orbital energy level engineering by using heterojunction FET structure. Benefitting from the discontinuities in energy levels at the heterointerface, it demonstrates that devices with pentacene /PFO (or PVK) heterojunctions exhibit typical p-channel operation, while possess light-programmable threshold voltage due to the charge transfer across the heterointerface.

These contributions have been published in internationally recognized journals, details of the publications can be found at the end of this thesis. Presentations were also made at 3 international conferences which provided the opportunity to share the work with the community.

1.4 THESIS ORGANIZATION

This thesis is organized as follows after introducing motivations and objectives of this project in Chapter 1.

Chapter 2 presents the literature review. It provides the background knowledge of OFETs, charge transport mechanism in organic semiconductors and the brief overview of recent development of OFETs.

Chapter 3 introduces the main equipment used for the fabrication of OFET devices and presents some factors that affect the molecular orientation and packing of organic semiconductors during the deposition, subsequently the charge transport along the channel layer.

Chapter 4 describes how to improve the device stability by using dual dielectric structure, and probes into the underlying physics. It is carried out by the application of both electrical and optical signals to trigger the response of interface states at the surface of buffer dielectric and buried traps at the dielectric-dielectric interface, which is manifested by the shift of threshold voltage.

Chapter 5 presents a detailed study on the effect of plasma treatment on the electrical performance of pentacene FETs with 12 nm ALD grown HfO_2. And the comparison to other chemical modifications is made to show the advantages of oxygen plasma treatment.

Chapter 6 covers the experimental demonstration of heterojunction FET devices and discusses possible working principle in dark and illumination condition. The charge transfer across the heterointerface (e.g. PFO/pentacene) is studied in terms of the control of threshold voltage and hysteresis behavior.

Chapter 7 concludes the thesis. It presents several recommendations for improvements and possible further research directions.

CHAPTER 2: LITERATURE REVIEW

2.1 CHAPTER INTRODUCTION

The basic idea that guides the insulated-gate field-effect transistor (FET) traces back to the mid-1920s,[38] but it was not until 1960 that this early concept could be successfully demonstrated, with the invention of the metal-oxide-semiconductor FET (MOSFET).[39] Field-effect measurements on copper phthalocyanine (CuPc) films were reported as early as 1964.[40] However, organic field-effect transistors (OFETs) that could indeed be used in practical electronic circuits only appeared in the late 1980s.[41,42] Since then, great effort has been devoted to optimizing the device structures and the processing conditions, understanding the charge transport mechanisms, and developing various novel materials, subsequently, the performance of OFETs has continuously improved. In terms of the key figures of merit, namely, the on/off current ratio, the field effect mobility and the threshold voltage, some OFETs[43] now compete with amorphous silicon (a-Si) FETs, which are preferred to conventional crystalline silicon FETs in applications, where large areas are needed, for example, AMFPDs.

To better understand what are OFETs and how they works, the basic structures and working principles, their current-voltage characteristics, and how to extract information from them, will be introduced. Organic semiconductors (OSCs) that are widely used as channel layer (p- and n-channel) and the most common charge transport models will be also briefly introduced.

2.2 DEVICE ARCHITECTURE

OFETs adopt the architecture of the thin film transistor (TFT), which has proven its adaptability with low conductivity materials. A typical FET is constructed with the basic components: a thin semiconducting film, an insulating layer and three electrodes. Two of them, the source and the drain, are in contact with the semiconductor film at a short distance from one another. The third electrode, the gate, is separated from the semiconductor film by the insulating layer.

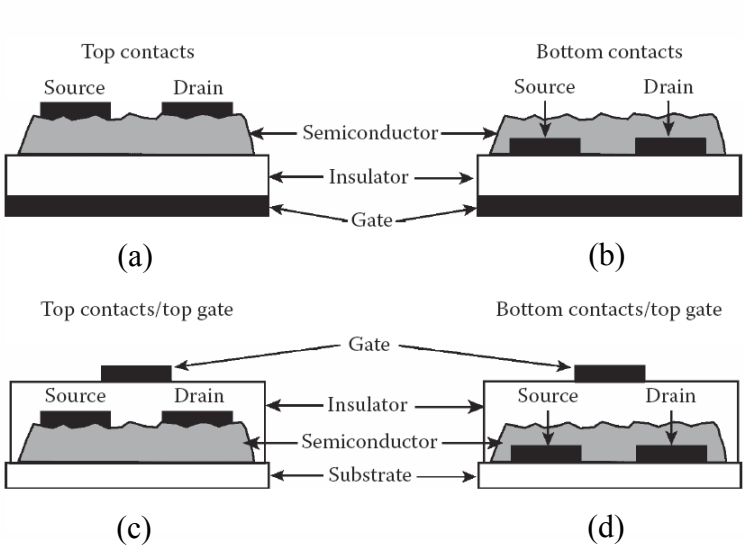


Figure 2-1. Four possible OFET architectures (in cross-section), including (a) top contacts (TC), (b) bottom contacts (BC), (c) top contacts with a top gate (TCTG), (d) bottom contacts with a top gate (BCTG). Figure from [44]

There are two main architectures to choose from in OFET fabrication: the top contact and the bottom contact configurations. The physical difference between the two is the order of fabrication steps. That is, the source/drain contacts are either deposited before or after the semiconductor layer is deposited to create a bottom contact or top contact device, respectively. One can also build the entire transistor on top of the semiconductor layer (the so-

called top gate architectures), in which the insulator and gate contact are sequentially deposited on top of either of the two contact configurations. All four of these OFET architectures are shown schematically in Fig. 2-1.

Top contact OFETs (Fig. 2-1a) generally exhibit the lowest contact resistances. This is likely because of the increased metal–semiconductor contact area in this configuration. A major contribution to contact resistance in the top contact configuration is *access resistance*. Access resistance results from the requirement that charge carriers injected from the source contact first have to travel through several tens of nanometers of undoped semiconductor before reaching the channel and then back up to the drain contact. However, some researchers have proposed that access resistance is less than might be expected for top contact OFETs because the contact metal penetrates the film down to the accumulation layer (perhaps due to large peak-to-valley roughness of the semiconductor film or the nature of the metal deposition process).[45]

With the bottom contact architecture, access resistance is not an issue because the contacts are in the same plane as the OFET channel, however, it usually suffers from greater contact resistance. It mainly ascribes to the fact that film morphology in the vicinity of the contacts is often nonideal. A number of researchers have demonstrated that the organic semiconductor grain sizes are very small near the contacts, presumably due to heterogeneous nucleation phenomena.[6]

For both top gate architectures, it should be noted that they face the additional concerns of semiconductor top surface roughness (since this is where the channel will form) and forming a stable interface between the insulator and the top of the semiconductor film. And attentions shall be paid to

the deposition of the top insulator that might damage the underlying semiconductor film. However, a proper top insulator also can provide an encapsulation effect against environmental exposure, subsequently, improving the device stability.

2.3 WORKING PRINCIPLE OF OFETS

The voltage applied between the source and drain is referred to as the source drain voltage, V_{ds}. For a given V_{ds}, the amount of current that flows through the semiconductor film from source to drain is a strong function of the voltage, V_g, applied to the gate electrode. The semiconductor film and the gate electrode are capacitively coupled such that application of a bias on the gate induces charge in the semiconductor film. Much of this charge is mobile and moves in response to the applied source drain voltage V_{ds}. Ideally, when no gate voltage is applied, the conductance of the semiconductor film is extremely low because there are no mobile charge carriers; i.e., the device is "off". When the gate voltage is applied, mobile charges are induced, and the transistor is on.

The origin of the gate-induced charging (also known as the "field effect") is clarified in the simplified electronic energy level diagrams shown in Fig. 2-2. Fig. 2-2a shows the positions of the highest occupied molecular orbitals (HOMOs) and lowest unoccupied molecular orbitals (LUMOs) of the organic semiconductor relative to the Fermi levels of the source and drain contacts. In this case, the gate bias is zero. If a small source-drain bias were applied, there would be no conduction because there are no mobile charges in the semiconductor.

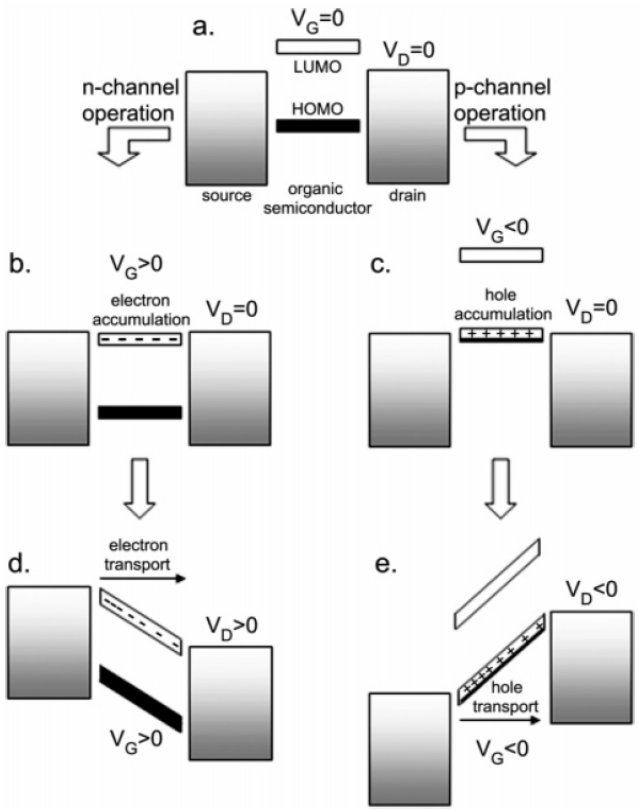


Figure 2-2. (a) Idealized energy level diagram of an organic TFT at $V_g = 0$ *and* $V_{ds} = 0$. *(b-e) demonstrate the principle of field effect transistor operation for the case of electron accumulation (b) and transport (d) and hole accumulation (c) and transport (e). Figure from [46]*

Parts b and d of Fig. 2-2 show the situation when a positive gate voltage is applied with $V_{ds} = 0$ and $V_{ds} > 0$, respectively. Application of a positive gate voltage produces a large electric field at the organic/insulator interface. This field causes the HOMO and LUMO levels in the semiconductor to shift down (lower in energy) with respect to the Fermi levels of the metal contacts, which remain fixed as their potentials are externally controlled. If the gate field is large enough, the LUMO will become resonant with the Fermi levels of the contacts, and electrons can then flow from the contacts into the LUMO, Fig. 2-2b. Now there are mobile electrons at the semiconductor-insulator interface, which upon application of a drain voltage, Fig. 2-2d, result in electric current between the source and drain.

This same reasoning applies with negative gate bias, Fig. 2-2c,e. Negative gate bias causes the HOMO and LUMO levels to shift up such that the HOMO becomes resonant with the contact Fermi levels and electrons spill out of the semiconductor and into the contacts, leaving positively charged holes. These holes are now the mobile charges that move in response to an applied drain voltage, Fig. 2-2e. Note that in Fig. 2-2d,e the source electrode is always the charge-injecting contact regardless of the sign of the gate voltage.

The above diagrams are a useful way to visualize the mechanism by which conduction in OFETs is modulated by the gate electrode. Now we move closer to see how the field-induced charge carriers are distributed along the channel and flows from the source to the drain. When no source-drain bias is applied, the charge carrier concentration in the transistor channel is uniform. A linear gradient of charge density from the carrier injecting source to the extracting drain forms when a small source-drain voltage is applied ($V_{ds} \ll V_g$, Fig. 2-3b). This is the linear regime, in which the current flowing through the channel is directly proportional to V_{ds}. The potential $V(x)$ within the channel increases linearly from the source $[x = 0, V(x) = 0]$ to V_{ds} at the drain electrode $[x = L, V(x) = V_{ds}]$.

When the source-drain voltage is further increased, a point $V_{ds} = V_g - V_{th}$ is reached, at which the channel is "pinched off" (Fig. 2-3c). That means a depletion region forms next to the drain because the difference between the local potential $V(x)$ and the gate voltage is now below the threshold voltage. A space-charge-limited saturation current $I_{ds,sat}$ can flow across this narrow depletion zone as carriers are swept from the pinch-off point to the drain by the comparatively high electric field in the depletion region. Further increasing the

source-drain voltage will not substantially increase the current but leads to an expansion of the depletion region and thus a slight shortening of the channel. Since the potential at the pinch-off point remains $V_g - V_{th}$ and thus the potential drop between that point and the source electrode stays approximately the same, the current saturates at a level $I_{ds,sat}$ (Fig. 2-3d).

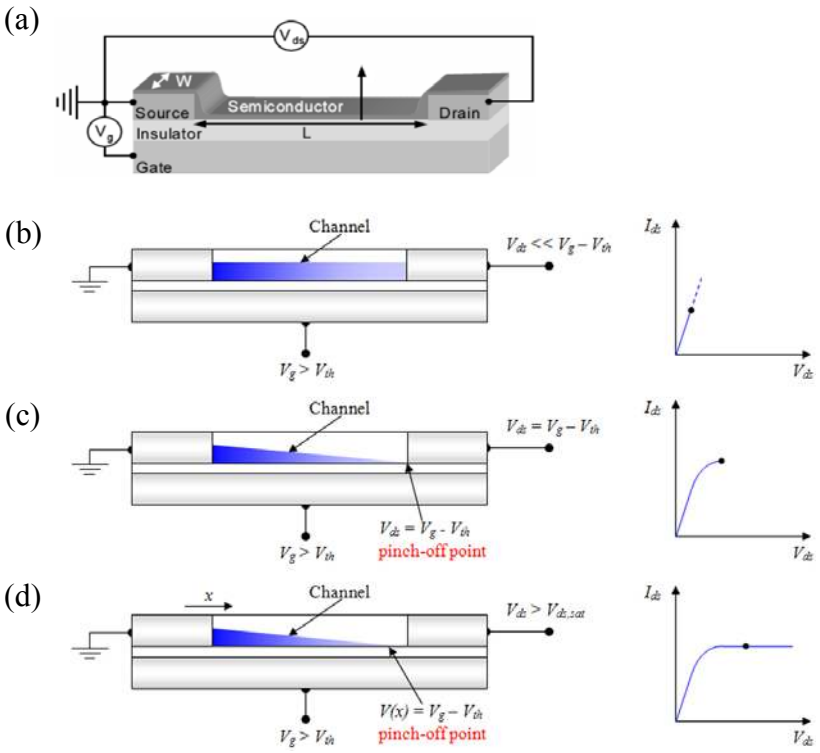


Figure 2-3. Schematic structure of a field-effect transistor and applied voltages: L = channel length; W = channel width; V_{ds} = drain voltage; V_g = gate voltage; V_{th} = threshold voltage; I_{ds} = drain current. (b-d) Illustrations of operating regimes of field-effect transistors: (a) linear regime; (b) start of saturation regime at pinch-off; (c) saturation regime and corresponding current- voltage characteristics.

Note that transistors with short channel lengths require thin gate dielectrics, typically $L > 10d_{dielectric}$,[47,48] in order to ensure that the field created by the gate voltage determines the charge distribution within the channel (gradual channel approximation) and is not dominated by the lateral field due to the source-drain voltage. Otherwise, a space-charge limited bulk

current will prevent saturation and the gate voltage will not determine the "on" or "off" state of the transistor.[49-54]

2.4 MODELING OF THE CHARACTERISTICS OF OFETS

The current-voltage characteristics in the different operating regimes of field-effect transistors can be described analytically assuming the gradual channel approximation. That is, the field perpendicular to the current flow generated by the gate voltage is much larger than the electric field parallel to the current flow created by the drain voltage. This is valid for long channel transistors but starts to fail for very short channel lengths.

At a given gate potential higher than the threshold voltage V_{th}, the induced mobile charges Q per unit area at the source contact are related to V_g via

$$Q = C_i(V_g - V_{th}) \tag{2.1}$$

where C_i is the capacitance per unit area of the gate dielectric. In eq 2.1 the channel potential is assumed to be zero. However, the induced charge density depends on the position along the channel (x), which is accounted for in the following equation:

$$Q = C_i(V_g - V_{th} - V(x)) \tag{2.2}$$

Neglecting diffusion, the source-drain current (I_{ds}) induced by carriers is

$$I_{ds} = W\mu QE_x \tag{2.3}$$

where μ is the charge mobility, and E_x is the electric field at x. By substituting $E_x = \frac{dV}{dx}$ and eq 2.2 into eq 2.3, we find

$$I_{ds}dx = W\mu C_i(V_g - V_{th} - V(x))dV \tag{2.4}$$

The gradual channel expression for the drain current can then be obtained by integration of the current increment from $x = 0$ to L, that is from $V(x) = 0$ to V_{ds}, assuming that the mobility is independent of the carrier density and hence the gate voltage:

$$I_{ds} = \frac{W}{L}\mu C_i\left[(V_g - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (2.5)$$

In the linear regime with $V_{ds} \ll V_g$, this can be simplified to

$$I_{ds} = \frac{W}{L}\mu_{lin} C_i (V_g - V_{th})V_{ds} \quad (2.6)$$

Two important technological parameters are the channel conductance g_d and the trans-conductance g_m, which are given by eq 2.7 and eq 2.8, respectively.

$$g_d = \left|\frac{\partial I_{ds}}{\partial V_{ds}}\right|_{V_g=const} = \frac{W}{L}\mu_{lin} C_i (V_g - V_{th}) \quad (2.7)$$

$$g_m = \left|\frac{\partial I_{ds}}{\partial V_g}\right|_{V_{ds}=const} = \frac{W}{L}\mu_{lin} C_i V_{ds} \quad (2.8)$$

The field effect mobility in the linear regime (μ_{lin}) can thus be extracted from eq 2.8, this is, the gradient of I_{ds} versus V_g at constant V_{ds} (also applicable for gate voltage dependent mobilities).

When $V_{ds} = V_g - V_{th}$, the channel is pinched off. The current cannot increase substantially anymore and saturates ($I_{ds,sat}$). Thus, eq 2.5 is no longer valid. Neglecting channel shortening due to the depletion region at the drain, the saturation current can be obtained by substituting V_{ds} with $V_g - V_{th}$, yielding

$$I_{ds} = \frac{W}{2L}\mu_{sat} C_i (V_g - V_{th})^2 \quad (2.9)$$

In the saturation regime, the square root of the saturation current is directly proportional to the gate voltage. This equation assumes that the mobility is gate

voltage independent. If this is not the case, a gate voltage dependent saturation mobility (μ_{sat}) can be extracted using

$$g_m = \frac{W}{L}\mu_{sat}C_i(V_g - V_{th}) \quad (2.10)$$

Fig. 2-4c shows a transfer curve in the saturation regime. Here the square root of the drain current should be linearly dependent on the gate voltage, and its gradient is proportional to the mobility according to eq 2.9. Extrapolating the linear fit to zero yields the threshold voltage V_{th}.

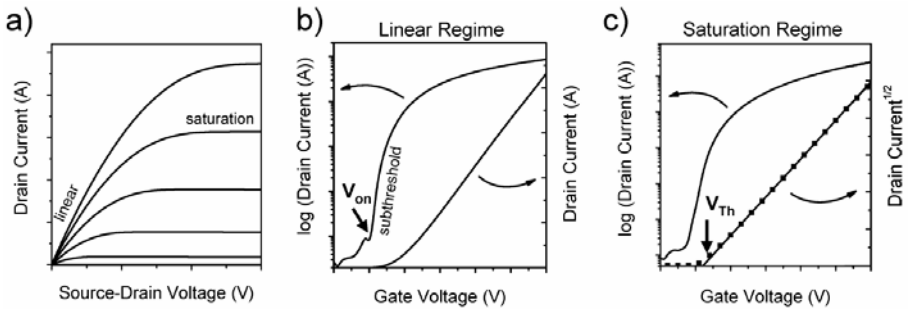


Figure 2-4. Representative current-voltage characteristics of an n-channel organic field-effect transistor: (a) output characteristics indicating the linear and saturation regimes; (b) transfer characteristics in the linear regime ($V_{ds} \ll V_g$), indicating the onset voltage (V_{on}) when the drain current increases abruptly; (c) transfer characteristics in the saturation regime ($V_{ds} > V_g - V_{th}$), indicating the threshold voltage V_{th}, where the linear fit to the square root of the drain current intersects with the x-axis. Figure from [55]

Threshold voltages can originate from several effects and depend strongly on the semiconductor and dielectric used. Built-in dipoles, impurities, interface states, and, in particular, charge traps contribute to the threshold voltage.[56] Note that, independent of the cause of V_{th}, it can be reduced by increasing the gate capacitance and thus inducing more charges at lower applied voltages. The threshold voltage is not necessarily constant for a given device. When organic transistors are operated for an extended time, V_{th} tends to increase. This bias stress behavior has a significant effect on the

applicability of organic transistors in circuits and is presently under intense investigation.[57-62] A shift of the threshold voltage on the time scale of current-voltage measurements causes current hysteresis (usually the forward scan shows higher currents than the reverse scan). Large, stable threshold shifts, e.g., induced by polarization of a ferroelectric gate dielectric, can be used in organic memory devices.[63,64]

2.5 ORGANIC SEMICONDUCTORS

The study of organic thin-film field-effect transistors has expanded from its original objectives in developing organic semiconductors. Common organic semiconductors are relatively wide band gap semiconductors with band gaps in the range of $2 - 3$ eV. Methods for controlled doping of these materials are not well established, as compared to that of silicon technology, mainly because doping often requires the mixing of a redox active small molecular dopant into the organic semiconductor host, which can be mobile under applied electrical fields during device operation.[65-67] Therefore, in most applications, organic semiconductors are not intentionally doped and are used in their as-synthesized form. State-of-the-art methods for the synthesis and purification of polymer semiconductors are capable of controlling the concentration of impurities left over from the synthesis to ppm levels.[68,69] For small molecules, high chemical purity can be achieved using techniques such as vacuum sublimation.[70] Therefore, for many materials, even unintentional extrinsic doping levels are low enough to consider these materials as intrinsic semiconductors.

When incorporating these intrinsic organic semiconductors into field-effect transistor configurations to evaluate their charge transport characteristics in combination with a particular gate dielectric such as SiO_2, most of FETs (e.g. pentacene FETs) conduct holes and achieve their high conductivity "on" state with *negative* gate voltage, whereas some FETs are n-channel devices (i.e. they conduct electrons) and turn on with *positive* gate voltage. The diagrams in Fig. 2-2 might lead one to believe that any organic semiconductor can be made to conduct holes or electrons, depending on the sign of the gate voltage. This is not true; for many organic semiconductor-based FETs, only p-channel operation seems possible due to the presence of charge traps and residual dopants. For this reason, such materials have been called "p-type" organic semiconductors. Over the last 10 years, many groups have aimed to realize n-channel organic FETs, subsequently, to enable complementary circuit design that utilize both negative and positive gate voltage to turn transistors on and off. This usually involved the synthesis of special organic semiconductors with high electron affinities, comprising specific electron withdrawing groups. These were then called "n-type" organic semiconductors.

2.5.1 POPULAR P-TYPE SEMICONDUCTORS

Molecules involving π-conjugation have high HOMO levels and exhibit electron-donating properties. Those molecules are good candidates for p-type semiconductors, such as oligomers, pentacene, phthalocyanine, etc. Small molecules such as pentacene possess the best electronic characteristics to date.

Pentacene consists of five aligned condensed benzene rings. It belongs to the family of polyacenes, which were extensively studied as organic

semiconductors during the 1960s and the 1970s. The highest field-effect mobilities so far have been recorded for pentacene ($0.3 - 0.7\ cm^2V^{-1}s^{-1}$ on SiO_2/Si substrates,[43] $1.5\ cm^2V^{-1}s^{-1}$ on chemically modified SiO_2/Si substrates,[71] and $\geq 3\ cm^2V^{-1}s^{-1}$ on polymer gate dielectrics[72,73]). However, pentacene has disadvantages such as instability in air and low solubility in solvents. Good solubility is crucial for device fabrication using solution methods such as inkjet printing. To overcome those disadvantages, various pentacene derivatives and analogues have been developed and the FETs based on them have been fabricated.[74-78]

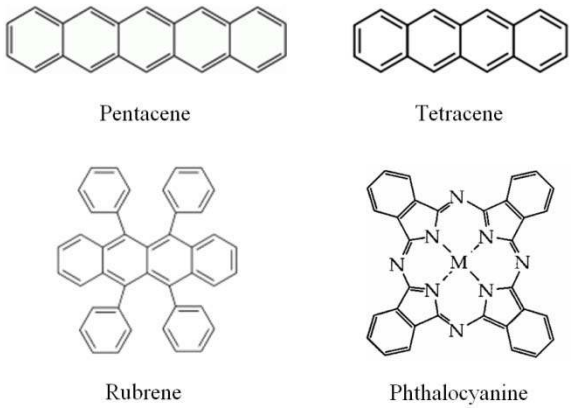


Figure 2-5. Chemical structure of several widely used p-type small molecules. In metal phthalocyanine (Pc), the central hydrogen atom (M = H_2) is changed to metal atom.

Tetracene, the next one being pentacene, also exhibits high hole FET mobility (up to $0.1\ cm^2V^{-1}s^{-1}$, and the maximum mobility achieved so far is $0.4\ cm^2V^{-1}s^{-1}$)[79-81] and reasonably high fluorescence quantum yield, which is promising for nanoscale light source with the planar geometry.[82] Rubrene holds the distinction of being the organic semiconductor with the highest carrier mobility, which reaches $40\ cm^2V^{-1}s^{-1}$ for holes.[83] This value was measured

in OFETs prepared by peeling a thin layer of single-crystalline rubrene and transferring to a Si/SiO_2 substrate.

Phthalocyanines (Pcs) were probably the first reported organic semiconductors,[84] and the ones that have been studied the most. They are thermally stable up to 400 ℃, and easy to evaporate under vacuum. The field effect was reported in a Pc as early as 1970[85] and OFETs were made in 1988.[86] Their field-effect mobility ranges between 0.0001 and 0.01 $cm^2V^{-1}s^{-1}$.[86-88] Although Pcs have been reported to behave as both n- and p-type semiconductors, Pc-based OFETs are all p-type. The leading problem with Pcs remains their extreme sensitivity to oxygen.

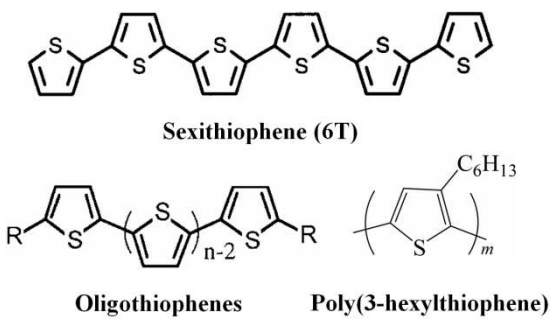


Figure 2-6. Chemical structure of typical thiophene and its derivatives. In oligothiophene, R = H (unsubstituted) and R = C_nH_{2n+1} (alkyl end-substituted).

The use of polythiophene as a semiconductor in FET device dated back to 1986,[41] and followed by the demonstration a 6T-based (Fig. 2-6) OFET in 1989.[42] This was also the first report of an OFET made with polymeric and small conjugated molecules. Thiophene can be considered to be the building block of choice that has proven itself to be most successful in generating good packing and FET performance. The most prominent example is regioregular poly(3-hexylthiophene) (P3HT). When solution deposited, either by drop-

casting or spin-coating, a polycrystalline layer is generated, with the best hole mobility being around $\mu = 0.1\ cm^2V^{-1}s^{-1}$.[89,90] To date, P3HT is still the state of the art semiconducting polymer for prospective commercialization of OFETs owing to its good solubility and high performance.

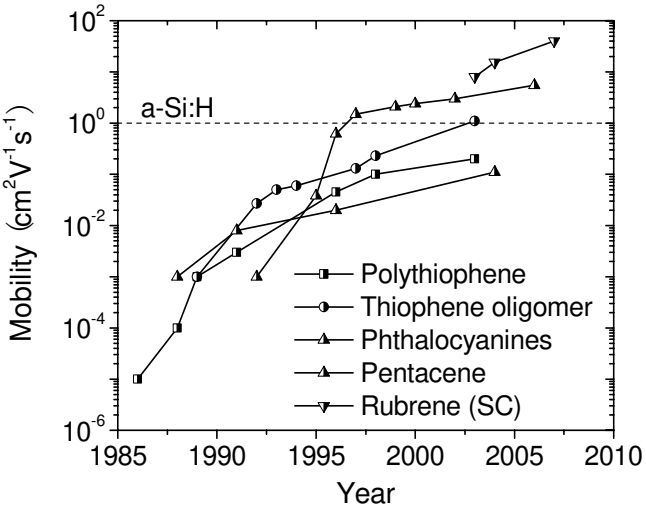


Figure 2-7. Evolution of OFET hole mobility for the several common p-type organic semiconductors. The various p-type materials are grouped together into families of similar molecules taking into account only the core part of each molecule. For reference, a representative range of electron mobilities for a-Si:H TFT is shown. The hole mobility in a-Si:H TFT is much lower than the electron mobility.SC = 'single crystal'.

As shown in Fig. 2-7, the used organic semiconductors seem to have reached "maturity" as far as their performance is concerned. Their individual performance versus time curves are about to saturate (re: when a new, higher value is not reported in the years following the last entry for a material, it means that there was no improvement in mobility during those years), however, what one still can do is to improve their device environmental and operational stability by engineering the semiconductor-dielectric interface and/or device encapsulation etc, for the practical applications, as their performance is now comparable to that of amorphous silicon TFTs.

2.5.2 POPULAR N-TYPE SEMICONDUCTORS

Compared to p-type organic semiconductors, n-type semiconductors are not fully developed, and their FET performance has lagged behind that of p-channel OFETs. The majority of work in this area has been to design molecules with increased electron affinity through substitution with electronegative elements (e.g. –F, –CN, $–NO_2$ *etc*) to allow efficient electron injection into the LUMO by high work function stable metals (e.g. Al and Au etc) and to increase hydrophobicity, which can decrease the environmental sensitivity of these materials by repelling moisture.[46,91] Over the last two decades, great progress has been achieved with n-type OTFTs. Mobilities ranging from 0.001 to $1.0\ \mathrm{cm^2V^{-1}s^{-1}}$ and current on/off ratio $> 10^5$ have been achieved and in some cases air stable devices have been realized, a list of which is given in Fig. 2-8 and Table 2-1.

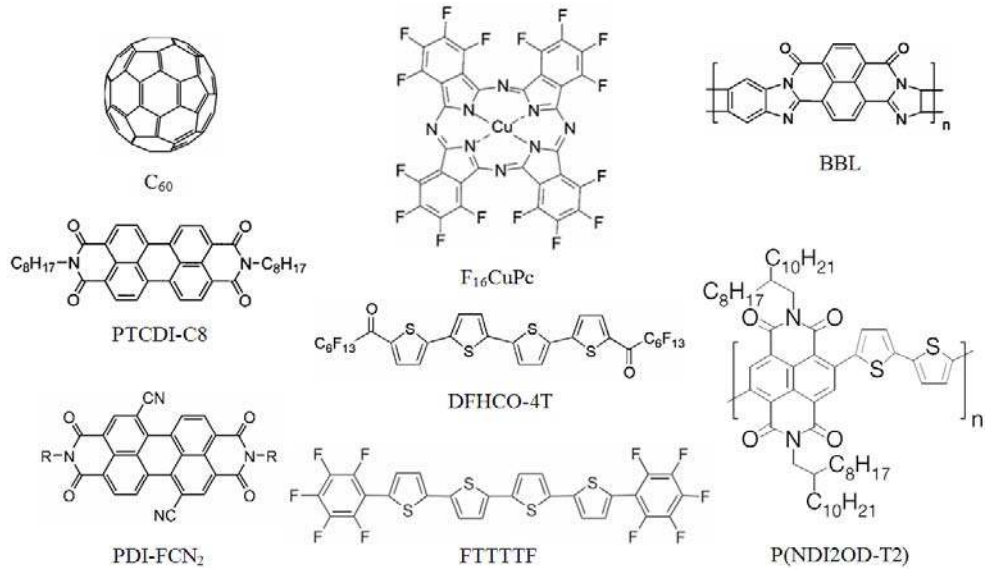


Figure 2-8. Chemical structures of representative n-channel organic semiconductors with known FET characteristics.

Table 2-1. Field-effect mobility ($cm^2V^{-1}s^{-1}$) of n-type semiconductors.

Year	Material	T_{dep} [℃]	μ	I_{on}/I_{off}	Substrate (Structure, SD contacts)	Ref.
1995	C_{60}	RT	0.08	10^6	SiO_2/Si (BC, Cr/Au)	[92]
			0.3	22	TDAE/SiO_2/Si (BC, Cr/Au)	
1996	NTCDA	55	0.003	10^3	SiO_2/Si (BC, Au)	[93]
1998	F_{16}CuPc	125	0.03	10^4	SiO_2/Si (BC, Au)	[94]
2000	NTCDI-C8F	70	0.1	10^5	SiO_2/Si (BC, Au)	[95]
	DHF-6T	80	0.02	10^5	HMDS/SiO_2/Si (TC, Au)	[96]
2002	PTCDI-C8	50	0.6	10^5	SiO_2/Si (BC, Au)	[97]
2003	C_{60}	130	0.56	10^8	SiO_2/Si (BC, Ti/Au)	[98]
	BBL [(s)]	NA	0.1	10^3	HMDS SiO_2/Si (BC, Ti/W/Au)	[99]
2004	PTCDI-C8	75	1.7	10^7	PS/SiO_2/Si (TC, Ag)	[100]
	PDI-FCN_2	NA	0.64	10^4	HMDS/ SiO_2/Si (TC, Au)	[101]
	DFH-4T	100	0.22	10^6	HMDS/ SiO_2/Si (TC, Au)	[102]
2005	DFHCO-4T	70	0.6	10^7	HMDS/ SiO_2/Si (TC, Au)	[103]
	Bithiazole	RT	1.83	10^4	OTS/SiO_2/Si (TC, Au)	[104]
2006	FTTTTF	60	0.5	10^8	HMDS/ SiO_2/Si (TC, Au)	[105]
	Perfluoropentacene	50	0.22	10^5	OTS/SiO_2/Si (TC, Au)	[106]
	C_{60}	50	2-4.9	10^3	Pentacene/Al_2O_3/Al (TC, Mg)	[107]
		250	6	NA	BCB/ITO (TC, LiF/Ai)	[108]
2007	Thiazolothiazole	RT	1.2	10^7	TDTS/SiO_2/Si (TC, Au)	[109]
	TC-PTCDI	125	0.18	10^6	OTS/SiO_2/Si (TC)	[30]
	F_{16}CuPc	180	0.11	NA	*p*-6P/ SiO_2/Si (TC, Au)	[110]
	NDI-$8CN_2$	110	0.15	10^3	SiO_2/Si (TC, Au)	[29]
	PBI-F2	125	0.35	10^7	OTS/SiO_2/Si (TC, Au)	[111]
2008	Functional acenes	60	0.37	10^5	OTS/SiO_2/Si (TC, Au)	[112]
	C60PC12F25[(s)]	NA	0.25	10^5	HMDS/ SiO_2/Si (TC, Au)	[113]
	NTCDIs	140	0.57	10^7	OTS/SiO_2/Si (TC, Au)	[114]
2009	DFHCO-4T	70	4.6	NA	*P*αMS/ SiO_2/Si (TC, Au)	[115]
	P(NDI2OD-T2)[(s)]	NA	0.85	10^6	Glass or PET (BCTG, Au)	[116]
	PBI derivatives	125	1.42	10^6	OTS/SiO_2/Si (TC, Au)	[117]
2010	Cl_8-PTCDI	125	0.91	10^7	OTS/SiO_2/Si (TC, Au)	[118]
	NDIs[(s)]	RT	0.51	10^5	OTS/SiO_2/Si (TC, Ag)	[119]
	PNDTBT-16[(s)]	RT	0.54	10^7	HMDS/ SiO_2/Si (TC, Au)	[120]

[(s)]Thin films were fabricated by spin-coating and/or printing.

2.6 CHARGE TRANSPORT MECHANISM IN OSCs

The high mobility found in conventional inorganic semiconductors rests on the fact that charges in crystalline materials move freely in delocalized bands. These bands result from the coalescing of discrete levels; when a large number of individual atoms are gathered together in a three dimensional lattice, the discrete atomic levels widen into bands. By contrast, the lower mobility found in organic semiconductors is because the molecular levels, which become the building blocks for the solid, do not interact with each other so

easily. Localization of the states in organic semiconductors may have various origins.

- In molecular crystals, the cohesion between individual units is ensured by weak van der Waals forces rather than strong covalent bonding. This leads to narrow bands, which in turn reduces the delocalization of the energy levels.
- Conjugated molecules tend to change their geometry upon charging, showing a strong electron–phonon coupling. The association of the charge with the geometrical deformation is termed *polaron*. When the charge moves in the solid, the associated deformation follows it like its shadow. In other words, a polaron is a *self-localized* charge.
- A last source of charge localization, which mainly occurs in polymer, is *disorder*.

The main consequence of localization is the reduction of charge mobility. It also has a decisive effect on the temperature dependence of the mobility. When charges move in delocalized levels, their mean free path is much larger than the de Broglie's wavelength, so transport is only limited by scattering by phonons. In this case, the mobility increases when temperature decreases; however, in materials with localized levels, charge transport is thermally activated, so the mobility *decreases* as the temperature is lowered.

2.6.1 SMALL POLARON MODELS

A polaron results from the coupling of a charge with the deformation of the lattice associated with this charge. When the deformation compares with the distance between lattice elements (which is the case in molecular solids,

where the deformation is localized on the individual molecules), the polaron is termed *small*. [sometimes referred to as *radical cations* (or *radical anions*)]. Fig. 2-9 described the mechanism of self-trapping through the creation of localized states in the gap between the valence and the conduction bands.[121]

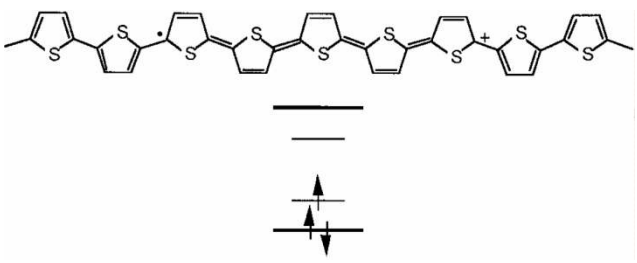


Figure 2-9. A polaron in polythiophene. Top: Change in the chemical structure. Bottom: Corresponding energy diagram. Figure from [122]

A useful model to describe the charge transport in organic materials is that of the small polaron, developed by Holstein.[123] It is a one dimensional, one-electron model (that is, the electron-electron interactions are neglected). The total energy of the system is the sum of three terms. The lattice energy E_L (eq 2.11) is given by a sum of N harmonic oscillators that vibrate at a unique frequency ω_0.

$$E_L = \sum_{n=1}^{N} \frac{1}{2M} \left(\frac{\hbar}{i} \frac{\partial}{\partial u_n}\right)^2 + \frac{1}{2} M \omega_0^2 u_n^2 \qquad (2.11)$$

Here, u_n is the displacement of the nth molecule from its equilibrium position, and M the reduced mass of each molecular site. The electrons are described within the frame of the tight-binding approximation, where it is assumed that the effect of the potential at a given site of the one-dimensional chain is limited to its nearest neighbors. In that case, the energy dispersion of the electron is given by eq 2.12, where J is the electron transfer energy and a is

the lattice constant. Finally, the electron-lattice coupling is accounted for by a term of the form given in eq 2.13, where A is a constant.

$$E_k = E_0 - 2j\cos(ka) \tag{2.12}$$

$$\varepsilon_n = -Au_n \tag{2.13}$$

An important parameter is the polaron binding energy E_b, which is defined as the energy gain of an infinitely slow carrier due to the polarization and deformation of the lattice. In Holstein's model, $E_b = A^2/(2M\omega_0^2)$. The limit of the small polaron turns up when the electronic bandwidth, $2J$, is small compared to the polaron binding energy. In that case, the electronic term of the total Hamiltonian can be treated as a perturbation. The mobility of the small polaron is calculated by solving the time-dependent Schrödinger equation. Its high-temperature limit ($T > \Theta$, where the Debye temperature Θ is defined by $k\Theta = \hbar\omega_0$) is given by eq 2-14. It is worth pointing out that the term $ea^2/\hbar$ has the dimension of a mobility, and is close to $1\,cm^2V^{-1}s^{-1}$ in most molecular crystals.

$$\mu = \sqrt{\frac{\pi}{2}}\frac{ea^2}{\hbar}\frac{J^2}{\sqrt{E_b}}(kT)^{-\frac{3}{2}}\exp\left(-\frac{E_b}{2kT}\right) \tag{2.14}$$

2.6.2 DISORDER MODELS

So far, the situation where chemical and physical defects are absent has been considered and charge transport is limited by the dynamic disorder arising from electron-phonon coupling. A description of charge transport in the presence of static disorder will be provided; this transport mechanism is expected to be operative in many organic materials since they usually present a highly amorphous character. In 3D materials, when disorder is weak, only the states at the band edge are truly localized. Increasing the amount of disorder

localizes more and more of the states in the band, until all states become localized in the case of strong disorder. Transport then operates in the hopping regime with charges jumping between interacting molecules. In the case of amorphous conjugated polymer films, diagonal disorder is induced both by electrostatic effects and a distribution in effective conjugation lengths while off-diagonal disorder comes from a distribution in the relative positions /separations between adjacent units.

Field Dependence. The impact of an external electric field is to lower the barrier for upward energy hops; this allows the charges to leave the states in the tail of the density of (localized) states (DOS), which would otherwise act as traps.

A general feature of charge transport in organic materials is that the mobility becomes field dependent at high electric field (namely, at fields in excess of $\sim 10^5$ V cm^{-1}). [124] This phenomenon occurs through a Poole–Frenkel mechanism,[125] in which the coulombic potential near the localized levels is modified by the applied field in such a way as to increase the tunnel transfer rate between sites. The general dependence of the mobility is given by eq 2.15. Here, $\mu(0)$ is the mobility at zero field, $\beta = (e/\pi\varepsilon\varepsilon_0)^{1/2}$ the Poole–Frenkel factor, and F the magnitude of the electric field.

$$\mu(F) = \mu(0)\exp\left(\frac{q}{kT}\beta\sqrt{F}\right) \tag{2.15}$$

Temperature Dependence. When the mobility is extrapolated at the zero-field limit, the fit of the Monte Carlo results leads to the following expression:

$$\mu(T) = \mu_0 \exp\left[-\left(\frac{2\sigma}{3k_B T}\right)^2\right] = \mu_0 \exp\left[-\left(\frac{T_0}{T}\right)^2\right] \tag{2.16}$$

with σ representing the width of the *diagonal disorder*, which reflects the fluctuations in site energies (i.e., the energies of the HOMO or LUMO levels of individual molecules or chain segments) within the material.[126] The temperature helps in overcoming the barriers introduced by the energetic disorder in the system and the temperature evolution here only depends on the amplitude of σ.

2.7 CHAPTER SUMMARY

This chapter introduces the fundamentals of organic field-effect transistors and the recent state development for organic semiconductors. There are now a large number of vacuum-sublimed as well as solution-processed organic semiconductor materials that have been demonstrated to exhibit field-effect mobilities on the order of $0.1 - 1\ \mathrm{cm^2V^{-1}s^{-1}}$, and it is clear that OFETs are able to match, and in some cases even exceed that of a-Si TFTs, indicating that OFETs are moving closer to applications. Therefore, the reliability of OFET devices becomes critical for stepping into this area. While exploring materials that combine high field-effect mobility with good environmental stability and state-of-art encapsulation techniques, these comparably less stable molecules (e.g. pentacene) can also be utilized to fabricate OFET devices with reasonable reliability through engineering the semiconductor-dielectric interface that comprises the main research work found in the subsequent chapters of this thesis.

CHAPTER 3: SETUP OF PHYSICAL VAPOR DEPOSITION SYSTEM

3.1 CHAPTER INTRODUCTION

Physical vapor deposition (PVD) is a variety of vacuum deposition and is a general term used to describe any of a variety of methods to deposit thin films by the condensation of a vaporized form of the material onto various surfaces (e.g., silicon substrate with thermally grown SiO_2). The material to be deposited is placed in an energetic, entropic environment, so that particles of material escape its surface. Facing this source is a cooler surface which draws energy from these particles as they arrive, allowing them to form a solid layer. The whole system is kept in a vacuum deposition chamber, to allow the particles to travel as freely as possible.

Usually, vacuum based thin film deposition methods for OFET fabrication include: vacuum thermal evaporation, organic vapor phase deposition (OVPD),[268] organic molecular beam deposition (OMBD)[7] and laser evaporation. Among them, vacuum thermal evaporation is used in our PVD system, which will be discussed in detail as follows.

3.2 SETUP OF PVD SYSTEM

Vacuum thermal evaporation involves heating OSCs using a resistive heating source under a vacuum environment with a pressure in the range of 10^{-8} to 10^{-6} Torr. For organic small molecules and oligomers that are

solution insoluble, vacuum thermal evaporation is an ideal deposition method. A number of organic semiconductors have been deposited using this method. Examples are oligothiophene and oligofluorene derivatives,[127,128] metallo-phthalocyanines,[88,129] and acenes (pentacene and tetracene).[43,71,79] Currently, the best mobility for organic semiconductors has been reported for vacuum-deposited pentacene films.[43,71-73,130] Vacuum thermal evaporation has the advantages of forming films with high film uniformity and good "run-to-run" reproducibility. However, this method has a relatively high material consumption and also a high initial cost for equipment setup. Nevertheless, this method has already been used for the manufacturing of organic small molecule based light emitting displays by several companies.

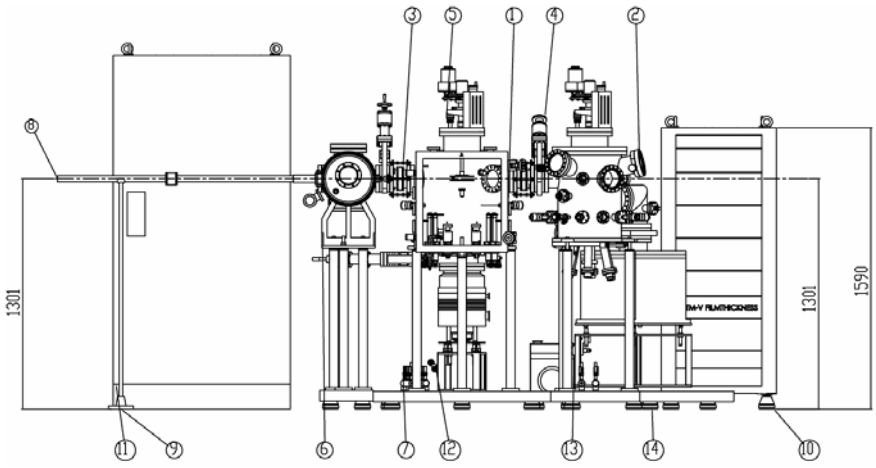


Figure 3-1. Schematic diagram of our PVD system.

Our multi-purpose system for research and development application is used for depositing metal, dielectric and organic films. From the left to the right hand side, this system (Fig. 3-1) consists of 3 chambers: (i) Chamber I (Pretreatment Chamber) with gloves for transferring substrates and O_2/H_2 plasma treatment, (ii) Chamber II (Metal Chamber) for metal and dielectric

deposition, (iii) Chamber III (Organic Chamber) for the deposition of organic semiconductors.

3.2.1 PRETREATMENT CHAMBER

Pretreatment chamber ($\Phi 200 \times 300$ mm, Fig. 3-2) can be pumped to vacuum and filled with N_2. A mechanical pump is connected, the limit pressure better than 8×10^{-3} Pa can be achieved. One plasma treatment apparatus generating O_2/H_2 plasma is installed inside, which is used to clean the sample substrate and/or modify its surface, by controlling the input amount of O_2/H_2 and current, various energies and densities of ionized gas can be obtained for different purposes. Maximum 4 substrates (20×20 mm^2) can be loaded in one time and transported among three chambers by a mechanical hand without breaking the vacuum chamber. When the chamber is filled with N_2, it functions like a simple glove box, where the shadow masks can be changed by a pair of gloves fixed inside the chamber through glass view windows.

Figure 3-2.(a) Front, (b) Inside and (c) Back view of pretreatment chamber.

3.2.2 METAL CHAMBER

Metal Chamber ($450 \times 450 \times 500$ mm, Fig. 3-3) is one of two main chambers for thin film deposition, which is double layered with cooling water.

This chamber is connected with a mechanical pump and a molecular pump, where the limit pressure better than 8×10^{-5} Pa can easily be achieved. There are three types of evaporators installed for various metal depositions: (i) High temperature Boron Nitride (BN) crucible-based thermal evaporator, (ii) High temperature Ta/Mo boat-based thermal evaporator, (iii) E-beam evaporator. All these evaporators have each substrate shutter to control the arrival of evaporating vapor at the substrates. The average distance between the evaporator and the sample substrate is more than 300 mm and the sample can rotate automatically $5-30$ rpm, which would make the resulting thin film more uniform. Under high vacuum condition, the evaporating rate and relative thickness of thin film can be accurately monitored by a water-cooling detector and a frequency counter, therefore, high quality of metal thin films can be fabricated.

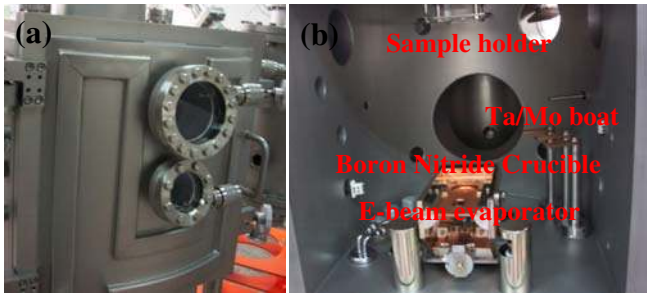


Figure 3-3. (a) Front and (b) Inside view of metal chamber.

Another advantage of metal chamber is that it can be open when the molecular pump is working, which greatly attributes to the side-pumping pipe from the mechanical pump. For example, one might want to add new material during the process. Without this side pumping function, much time (nearly 20 min each time) has to be wasted for switching on/off the molecular pump.

Obviously, this side-pumping function makes the work more efficiently.

3.2.3 ORGANIC CHAMBER

Organic chamber ($\Phi 350 \times 500$ mm) is equipped with an ion pump, whose limit pressure better than 8×10^{-6} Pa can be achieved. 6 slightly tilted sets of organic thermal evaporator (operating below 600 °C) are installed, converging properly at the center of sample holder (can rotate automatically $5 - 30$ rpm). 2 sets of power supply of controlling temperature to control the 6 sets organic thermal evaporators with a control accuracy of 3‰. 3 sets of water-cooling film detectors and 3 sets of frequency counters are employed to monitor evaporating rates. The temperature of thermal evaporators is governed by computer-assistant PID controller, which can control the crucible temperature more accurately and efficiently. The schematic diagram of its work principle is shown in Fig. 3-4.

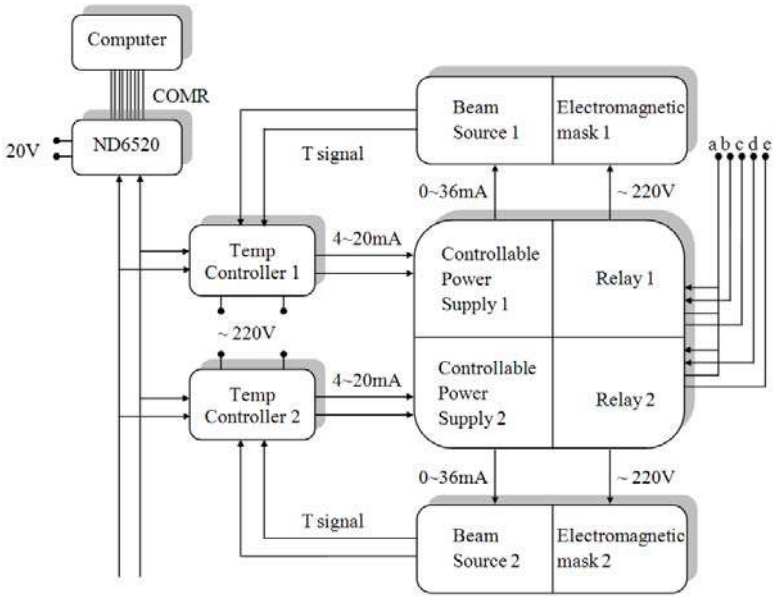


Figure 3-4. Flow chart of computer-assistant PID controller.

3.3 EFFECT OF DEPOSITION CONDITIONS

Device performance is greatly influenced by various deposition conditions due to the different resulting molecular structure and thin film morphology. Organic materials tend to pack into either a herringbone or a π-π stacking structure, governed by intermolecular interactions. Better overlap between the π molecular orbitals generally results in a higher mobility. To achieve high field effect mobility, several factors should be considered when selecting vacuum deposition, including

1. *Base pressure*

   It should be noted that, in any vacuum deposition chamber, zero pressure is never achieved. This fact has significant implications because, at any pressure, there exists a mixture of residue molecules such as N_2, O_2, H_2O, and CO_2 that impinges on the substrate and possibly interacts with the growing film. The mean free path or average distance between collisions for gas molecules is influenced by vacuum pressure. In order to fabricate best quality films (e.g. large grain size and small number of charge traps), high vacuum is needed to minimize the collisions among gas molecules.[131]

2. *Deposition rate*[7,71,132 -134]

   It affects the nucleation density of a given organic semiconductor on a given substrate surface. In general, a faster deposition rate leads to higher nucleation density and smaller average grain sizes. An additional energy is required for charge carriers to hop from one grain to another.[135] In addition, impurities and trapping molecules absorbed from the ambient environment tend to accumulate at grain boundaries

and further increase the energy barrier for hopping. Therefore, high mobility is generally obtained for films with large and interconnected grains.

3. *Substrate temperature*[7,43,133,134]

It affects the diffusion length of the molecules on the substrate, which normally increase with the increase of temperature, and also affects the packing of the molecules [e.g. large π-conjugation length along the long axis of the molecule and close molecular packing of the molecules along at least one of the short molecular axes (π-stacking)], therefore, the mobility of resulting film.

4. *The purity of organic source materials*

Purity of the organic source material is also important and together with substrate cleanliness they can determine in large part the quality of an OFET. Impurities can affect the mobility, the on/off ratio and in some cases even the polarity of the OFET.[136,137]

5. *Substrate surface*

Substrate surface properties have significant impact on the molecular orientation and thin film morphology of the semiconductor being deposited upon. In most cases, this substrate surface is also the dielectric surface (sometimes patterned metal contacts & dielectric surface). It is known that the current flow in an OFET is mainly confined within the first 5 nm of semiconductor away from the dielectric/semiconductor interface.[138-141] Therefore, the morphology and molecular orientation of this first 5 nm film is most critical to the performance of OFETs. The properties of such surface also can be

tuned by surface modification: (i) wet method, e.g. self-assembly monolayers (SAMs) and/or an spin-on polymer;[6,14,71,89,130,141-146] (ii) dry processing, e.g. ion beam, UV ozone and plasma treatment.[115,146-152]

3.4 CHAPTER SUMMARY

This chapter introduces the setup of our custom-made PVD system and its relative functions. With this system, we are able to (i) optimize the fabrication process of OFETs by considering deposition conditions and surface treatment; (ii) study the basic charge transport mechanism and band alignment for various organic material and/or organic-metal interface; (iii) explore designs and device structures alternative to the existing metal oxide field-effect transistor design.

CHAPTER 4: THE EFFECT OF BURIED TRAPS ON THE DEVICE STABILITY

4.1 CHAPTER INTRODUCTION

The interfacial interactions of organic semiconductor layer with gate dielectric are often very specific and play a decisive role in the functioning of OFET devices. Optimum device performance, e.g. high mobility, generally requires synergistic interactions at the semiconductor-dielectric interface. For example, while the silane coupling agents, e.g. OTS,[6,71] on the thermal SiO_2 surface enhances the packing order of pentacene molecules, utilization of an untreated native SiO_2 has led to the reductions in mobility and on/off ratio and the increment in subthreshold slope. A great variety of other alkyl silylating agents have also been explored with the objective of optimizing the dielectric-semiconductor interactions, often with satisfactory performance results.[43,56,89] Specifically, HMDS surface treatment has been employed to promote segregation of regioregular polythiophenes for improved mobility,[89] while perfluorosilane modification has been used for manipulating threshold voltages of OFETs.[141,153,154] More recently, alkylphosphonic acid SAM on alumina has been demonstrated to be effective in achieving one of the best FET performances of evaporated pentacene semiconductor.[130] However, all of these modifications have two limiting characteristics. Firstly, the creation of a synergistic dielectric surface requires appropriate chemical reactions between the modification agent and the dielectric surface. Secondly, if SAMs are

utilized, their qualities, which depend critically on the dielectric surface chemistry and the methods through which they are formed, would greatly affect the final FET performance. These modification approaches may thus be difficult to implement reproducibly in high-throughput manufacturing processes, particularly on such chemically inert surfaces as those of common plastic substrates for electronic design.

An attractive alternative approach is to insert an additional layer between the gate insulator and the active layer, for instance, a spin-on polymer. The chemical properties of the gate dielectric, e.g. roughness and surface energy *etc*, can then be effectively tuned via the choice of the buffer dielectric, [13,14,144-146,155-157] which would strongly influence the semiconductor film microstructure and subsequently the charge transport along the channel. A proper buffer dielectric is able to passivate the trapping states (e.g. hydroxyl groups), giving rise to a clear n-type field-effect behavior in OSCs, and reduce energy disorder and carrier localization at the interface between the active layer and the gate dielectric which is caused by the local polarization effects of high-κ gate dielectric.[145,157,158] Given its many advantages, this approach is widely used to fabricate low voltage, high performance organic FETs.[13,14]

To make useful devices, the electrical stability/reliability of organic FETs is another important parameter, which has not yet reached the stage of the practical use. After a much dedicated research, it has been found that employing a FET structure with dual dielectric is also an efficient way to enhance the device stability, where they would compensate both dielectrics' drawbacks, for example, the buffer dielectric forms few defects at the interface but has a low electrical strength/dielectric constant, while high-κ gate insulator

uses low voltage but has poor interface.[14] A proper buffer dielectric also can depress the absorption of moisture at the dielectric interface and the penetration of oxygen into OSCs, thus further retarding device characteristics decay throughout its shelf-life and operating life. In order to characterize its significance, application of a gate bias is normally utilized. Zhang et al.[159] showed that FET devices of polycrystalline pentacene with polystyrene (PS) buffer dielectric and Al_2O_3 gate insulator exhibited an almost steady current output ($I_{ds}(t)/I_{ds0} > 95\%$) and little threshold voltage shift ($\Delta V_{th} < 0.1\ V$) upon gate-bias stress at $V_g = V_{ds} = -10$ V for 1 h in a N_2-filled glove box ($O_2, H_2O < 1\ ppm$). It is comparable to or even better than that of a-Si TFTs, ascribing to the excellent interface of PS and its lack of dipole moments. Good device stability now can be achieved, but not to the point of having no degradation for a more prolonged period of time, e.g. more than a year. Usually, the shift of the threshold voltage is one of manifestations of device degradation, which was proposed to arise from the following factors: (i) charging/ polarization of gate dielectric and changes in dielectric constant over time; (ii) the presence of oxygen, moisture, chemical impurities and light irradiation etc; and (iii) intrinsic structural and energetic disorder of OSCs and/or specific structural defects.[63,160-168] Despite the wide range of possible dielectric-dielectric combinations, it should be pointed out that trapping states at the surface of gate insulator actually still exist but are simply shielded from carriers' access, when a polymeric buffer dielectric is used for surface passivation. Previously, Ng et al.[168] investigated the influence of different gate insulators by the charge injection from the gate electrode, and water ion movement on the stability of PQT-based FETs with pMSSQ buffer dielectric.

However, the effect of buried trapping states on the device stability, especially under applied extrinsic stimulus, is still lack of in-depth study.

In this chapter, we studied the electrical stability of both p- and n-channel FET devices, in which the gate insulator SiO_2 is modified by Poly(4-vinylphenol-co-methyl methacrylate) (PVP-*co*-PMMA) or poly(methyl methacrylate) (PMMA). The bottom layer of the bilayer dielectrics investigated in this study is thermally oxidized SiO_2 grown on n^{++}-Si due to the material's high chemical stability and excellent insulating properties with extremely low current leakage, which would minimize the effect of charge injection from the gate electrode. More importantly, a large amount of Si–OH silanol groups tend to be present on the SiO_2 surface, leading to electrochemical trapping of electrons, when thermal SiO_2 is grown at $800-1000\,℃$.[158] On the other hand, the selection of the two polymeric buffer dielectrics is because of the demonstration of hysteresis-free FET devices.[169,170] PVP-*co*-PMMA can also be cross-linked via exposure to UV light, without any other agents that can minimize the unintentional residuals, and thus becomes robust and very resistant to common organic solvents (e.g. alcohol, toluene, chloroform and chlorobenzene etc), which would be of great use for the fabrication of all solution-processed OFET circuits on flexible substrates.[171] The use of trap-free PMMA is motivated by its hydrophobic methyl radical groups that can serve as moisture inhibitors and the absence of hydroxyl groups, providing a defect-free high-quality interface.[13,14,169] In the present study, both electrical and optical signals are utilized to trigger the response of these buried trapping states in ambient condition, which can be manifested by the shift of threshold voltage. It was reported that although moisture causes

charge trapping, trap formation was only observed after negative bias stress in pentacene flip-crystal FETs[166], and thus would have little impact on studying how these buried traps were approached by minority carriers in our devices shown below.

4.2 EXPERIMENTAL DETAILS

Organic FET devices were fabricated with a top-contact configuration (Fig. 4-1c). A heavily doped n-type silicon wafer ($\leq 0.01\ \Omega\cdot$cm) and 500 nm (or 200 nm) thermally oxidized SiO_2 were used as a gate electrode and gate dielectric layer, respectively. Before being processed, the substrates were cleaned by acetone and IPA in an ultrasonic bath and rinsed in deionized-water. The substrates were then dried using a nitrogen gun. The PVP-*co*-PMMA and PMMA buffer dielectric were spin-coated from the solution in propylene glycol monomethyl ether acetate (PGMEA) and anisole, and annealed on a hot plate to remove the residual solvents at 150 ℃ and 120 ℃ for 1 h, respectively. Their thicknesses were evaluated by a Dektak surface profilometer. $50-60$ nm thick Pentacene and/or C_{60} were deposited in a vacuum system by thermal evaporation at a background pressure of 10^{-5} Pa. The deposition rate was controlled at 0.5 Å s^{-1} for pentacene and 1 Å s^{-1} for C_{60}, respectively, and the substrates were maintained at room temperature. Finally, 30 nm gold (Au) and aluminium (Al) used as the source-drain contacts for pentacene and C_{60} FETs, respectively, were thermally evaporated through a shadow mask. For a typical FET device reported here, the channel length (L) and width (W) were 0.1 and 2 mm, respectively.

In the bilayer insulators, the buffer dielectric acts as part of the dielectric layer during the device operation. The capacitance (C_i) of the devices can be calculated using the following equation:

$$\frac{1}{C_i} = \frac{1}{C_s} + \frac{1}{C_p} = \frac{t_s}{\varepsilon_0 \varepsilon_s} + \frac{t_p}{\varepsilon_0 \varepsilon_p} \quad (4.1)$$

where t_s and t_p are the thickness of SiO_2 dielectric layer and polymeric buffer dielectric, respectively; ε_s and ε_p are the dielectric constants of SiO_2 dielectric layer and polymeric buffer dielectric, respectively.

The electrical characterization of the devices was measured using a Keithley 4200 SCS semiconductor parameter analyzer under ambient condition at room temperature on a standard probe station with or without light illumination. The visible light illumination was used for the study of photo-induced charge transfer, shining at the top surface of the device from a halogen lamp and focused to a spot size approximately equal to the area of the device to cover the entire channel with an estimated light intensity of 1 mW cm^{-2}. AFM images were obtained using a Nanoscope IIIa AFM (digital instrument) in tapping mode.

4.3 RESULTS AND DISCUSSION

4.3.1 PVP-*co*-PMMA BUFFER DIELECTRIC

The pentacene FET with PVP-*co*-PMMA gate insulator and buffer dielectric (see Fig. 4-1b,c) exhibits unipolar p-channel field-effect behavior, i.e. hole accumulation in the channel, as seen from the output characteristics in Fig. 4-2a and Fig. 4-3a. The output characteristics show two distinct regions of device operation: linear and saturation. In the linear region (also known as the ohmic mode), the FETs operate like a resistor, controlled by the gate voltage

related to both the source and drain voltage. At higher V_{ds}, the accumulated layer in the channel is pinched off, as indicated by the lack of channel region near the drain, and the drain current is weakly dependent on drain voltage and controlled primarily by V_g. It agrees well with the model discussed in chapter 2.

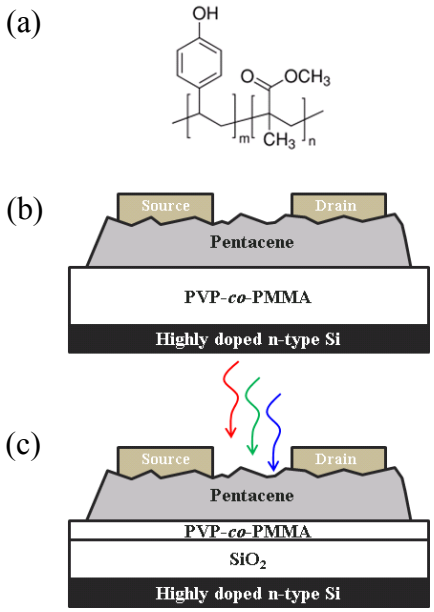


Figure 4-1. (a) Chemical structure of Poly(4-vinylphenol-co-methyl methacrylate) [PVP-co-PMMA], and PVP-co-PMMA used as gate insulator in (b) and buffer dielectric in (c).

Fig. 4-2b shows $I_{ds} - V_g$ curves of pentacene FETs with 340 nm PVP-*co*-PMMA as gate insulator, where a little difference in I_{ds} was observed upon the sweep direction of V_g, normally said to show a "*hysteresis*". Obviously, the back sweep current (BSC) was higher than the forward sweep current (FSC), which might be caused by mobile ions in PVP-*co*-PMMA, or by its polarization due to the exposure to air (e.g. moisture).[163,164,166,167] This higher BSC hysteresis is a bistability in the operational transistor current, resulting in two different threshold voltage V_{th}. As such, it is not an unwanted feature per

se—it could be useful in nonvolatile memory devices—but it must be avoided in standard integrated circuits.

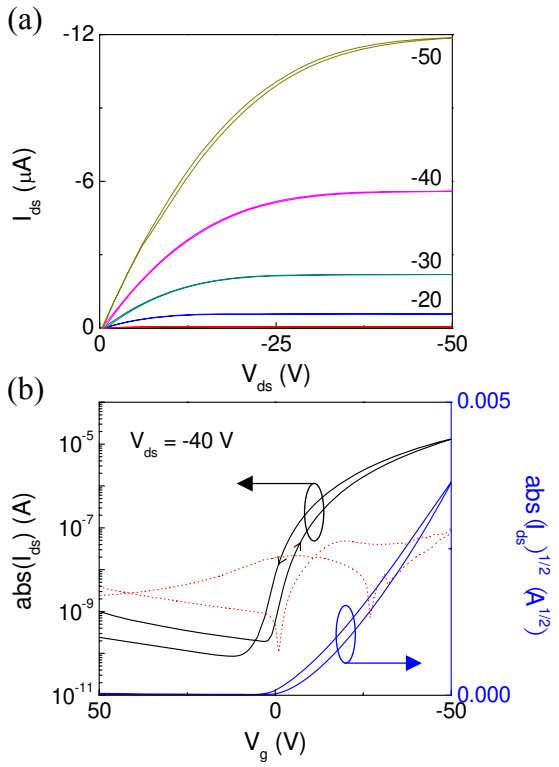


Figure 4-2. (a) The output curves and (b) transfer characteristics of pentacene FETs using 340 *nm PVP-co-PMMA as gate insulator (red dot line: the leakage current* I_g*). The arrows indicate the sweep direction of* V_g*.*

When the thinner PVP-*co*-PMMA was employed to modify the surface of SiO_2, the magnitude of hysteresis was reduced and exhibited a lower BSC (Fig. 4-3b), as compared to that in Fig. 4-2b. Such lower BSC hysteresis was attributed to the charge trapping close to the channel, primarily at the dielectric surface (rather than the polarization effect),[165] and the suppressed gate leakage current I_g(ca. $2-3$ order lower) due to the excellent insulating property of SiO_2. Now we use this hysteresis-negligible pentacene FET to study the effect of bias stress under illumination on its electrical performance.

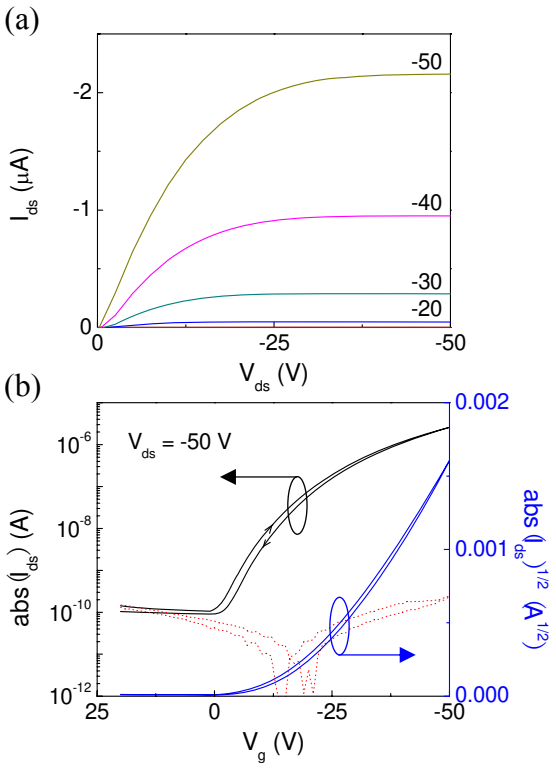


Figure 4-3. (a) The output and (b) transfer characteristics of pentacene FETs using 500 *nm* SiO_2 *as gate insulator modified by* 20 *nm PVP-co-PMMA buffer dielectric (red dot line: the leakage current* I_g*). The arrows indicate the sweep direction of* V_g.

By the application of a gate bias of 200 V for 20 s under illumination, the entire transfer curve of pentacene FETs with 20 nm PVP-co-PMMA buffer dielectric was greatly shifted to the positive side due to the tapping of a large amount of photogenerated electrons, as shown in Fig. 4-4a, giving rise to a total shift in threshold voltage (ΔV_{th}) of larger than 90 V. These electrons might be trapped in the bulk of PVP-*co*-PMMA and at its interface due to the hydroxyl groups, and in the grain boundaries and other structural defects. The time evolution of I_{ds} recorded at $V_{ds} = -50$ V & $V_g = 0$ V was shown in Fig. 4-4b, indicating that the trapped electrons can survive for a long time. It suggested that the negligible hysteresis might originate from: (i) the dynamic balance of trapping/detrapping charge carriers and (ii) almost no charge

trapping due to the unaccessible trapping states (e.g. deeply buried traps) or the absence of trapping states. Therefore, it can be concluded that only the demonstration of hysteresis-free FET devices is not nearly enough in our devices and/or most other practical FET devices, one still needs trying to reduce the possibility of charge trapping, or even eliminate it.

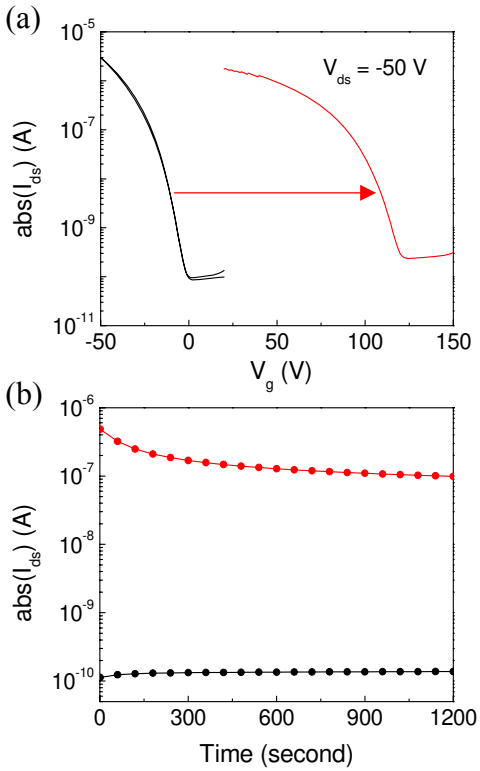


Figure 4-4. (a) Transfer curves of pentacene FETs with $500\ nm$ *SiO_2 and* $20\ nm$ *PVP-co-PMMA buffer dielectric at* $V_{ds} = -50\ V$ *before and after programing with a gate bias of* $200\ V$ *for* $20\ s$ *at* $V_{ds} = 0\ V$ *under illumination. (b) Time evolution of* I_{ds} *measured in the dark at* $V_{ds} = -50\ V$ *&* $V_g = 0\ V$ *after programing with a gate bias of* $200\ V$ *for* $20\ s$ *under illumination (red line) and then* $-200\ V$ *for* $5\ s$ *(black line) at* $V_{ds} = 0\ V$ *in the dark.*

In order to study the effect of buried traps at dielectric-dielectric interface, highly purified PMMA was used to substitute PVP-*co*-PMMA as buffer dielectric to minimize the charge trapping at the interface between the

semiconductor and the gate dielectric, because of the absence of hydroxyl groups. The details of the experimental results are discussed as follows.

4.3.2 PMMA BUFFER DIELECTRIC

4.3.2a IN DARK CONDITION

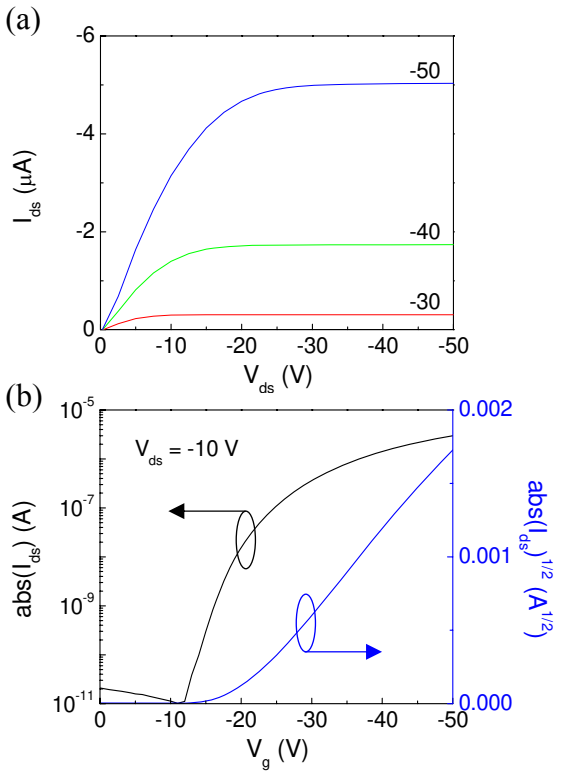


Figure 4-5. (a) The output and (b) transfer characteristics of pentacene FETs with 500 *nm* SiO_2 *and* 10 *nm PMMA buffer dielectric.*

The electrical characteristics of pentacene FETs with thin PMMA buffer dielectric were presented in Fig. 4-5. Compared to that of devices with PVP-*co*-PMMA, this batch of devices exhibited higher driving current density and charge carrier mobility (Fig. 4-6) at the same bias condition because of the excellent dielectric surface provided by PMMA. In both cases, the mobility increases quasi-linearly with gate voltage, when $V_g > V_{th}$. Such gate-bias dependence comes from the fact that, as the gate bias is increased, the Fermi

level at the semiconductor-insulator interface moves closer to band-edge, so that more traps are filled. This leads to an increase of mobile charges in the delocalized levels, and an enhancement of the effective mobility, which has been previously studied in other OFET devices.[172,173]

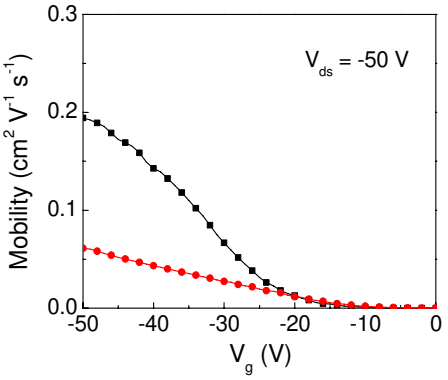


Figure 4-6. Gate-voltage dependent mobility of Pentacene FET devices with $10\ nm$ *PMMA (black square line) and* $20\ nm$ *PVP-co-PMMA (red circle line) buffer dielectric measured at room temperature.*

By simply assuming that the evaporated pentacene thin film in devices consists of grains (bulk) where single crystal properties hold, and grain boundaries (GBs) where high concentration of traps exists, the effective mobility is then given by[174]

$$\frac{1}{\mu} = \frac{1}{\mu_g} + \frac{1}{\mu_b} \tag{4.2}$$

where μ_g and μ_b are the mobility in the grain and in the grain boundary, respectively. If $\mu_g \gg \mu_b$, the overall mobility will only mirror charge transport limitations at grain boundaries, this is, the mobility of OFETs is controlled by the rate of thermionic carrier jumps across the grain boundary.

$$\mu \approx \mu_b = \mu_0 \exp\left(-\frac{E_b}{k_B T}\right) \tag{4.3}$$

Here, $E_b = q\phi_b$, and the barrier height is described by[174]

$$\phi_b = \frac{q^2 n_t^2 d_m}{8\varepsilon_{se} C_i V_g} \tag{4.4}$$

where ε_{se} is the permittivity of the semiconductor, k_B is Boltzmann's constant, T is the absolute temperature, q is the electron charge, n_t is the density of trapped charges and d_m is the thickness of the conducting channel. Obviously, these defects in GBs, acting as charge traps, play an important role in the gate voltage dependence of hole mobility in our devices. On the other hands, when a certain amount of mobile charge carriers (holes and/or electrons) are captured in GBs during the device operation, the threshold voltage V_{th} would be also affected and described as follows:

$$V_{th} = V_{fb} + 2\psi_b + \frac{\sqrt{2\varepsilon_s q N_a (2\psi_b)}}{C_i} \tag{4.5}$$

$$V_{fb} = \phi_{ms} - \frac{Q_f}{C_i} \tag{4.6}$$

where ψ_b is the potential difference between the Fermi level E_f and the intrinsic Fermi level E_i of the semiconductor, N_a is the density of the acceptor, ϕ_{ms} is the potential difference the metal gate and semiconductor bulk at zero gate bias, and Q_f is the interface charge that contains the charge trapped in GBs of a polycrystalline thin film, e.g. pentacene.

Based on eq 4.5 and eq 4.6, the value of V_{th} can be tuned through varying the density of charge at the semiconductor-dielectric interface. In order to investigate this effect, the device characteristics were measured after programing with a gate bias at $V_{ds} = 0$ V for various durations. When a negative bias was applied to the gate, the shift in transfer curves increased with increasing bias time, as shown in Fig. 4-7a. The value of ΔV_{th} as large as 8 V was obtained after programing with a gate bias of $V_g = -200$ V for 500 ms, indicating that a great number of field-induced holes were trapped. It suggested

that device failure would occur when the device operates successively at "ON" state. This phenomenon is generally observed when SiO_2 is employed as the gate dielectric, which is proposed to result from structural defects present in polycrystalline pentacene film and/or hole trapping states due to absorbed water molecules on the SiO_2 surface.[165,175]

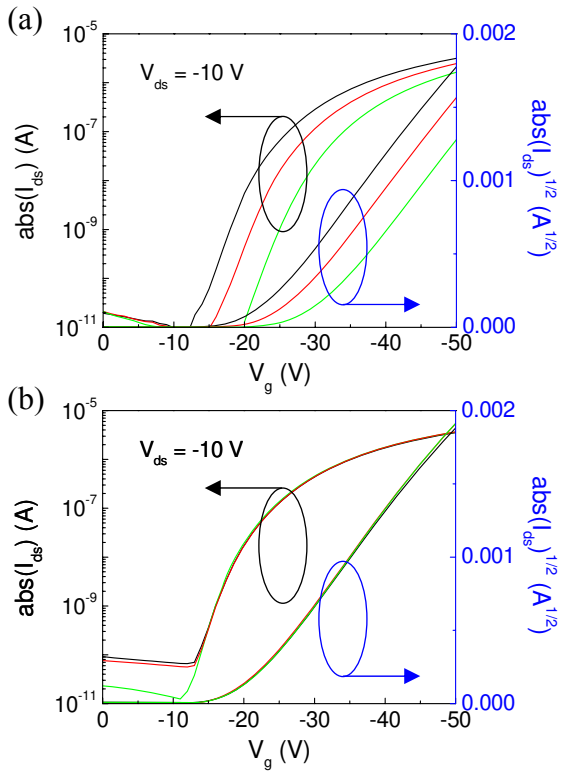


Figure 4-7. Transfer characteristics of pentacene FETs with $500\ nm$ *SiO_2 and* $10\ nm$ *PMMA buffer dielectric at* $V_{ds} = -10\ V$ *before (black line) and after programing with a gate bias of (a)* $-200\ V$ *and (b)* $200\ V$ *at* $V_{ds} = 0\ V$ *for* $100\ ms$ *(red line) and* $500\ ms$ *(green line).*

When the device was programed with positive gate bias, the shift in transfer curves was hardly observed as shown in Fig. 4-7b and the inset of Fig. 4-9b. Compared with the devices with bare SiO_2,[158,176] our devices appeared to be more immune to V_{th} shift caused by positive bias, which actually is a preferred feature for practical application of organic integrated circuits (ICs). It can be proposed that such a feature results from: (i) the charge injection barrier

provided by the 10 nm-thick PMMA layer, which hinders the field-induced minority carriers (electrons) from being captured by the surface silanol groups; (ii) the large electron injection barrier between Au and pentacene; (iii) the low electron carrier density in the p-channel pentacene active layer. The above hypotheses were also applicable for the n-channel FETs with C_{60} as active layer, but these devices exhibited the opposite trend as compared to that of pentacene FETs, as shown in Fig. 4-8.

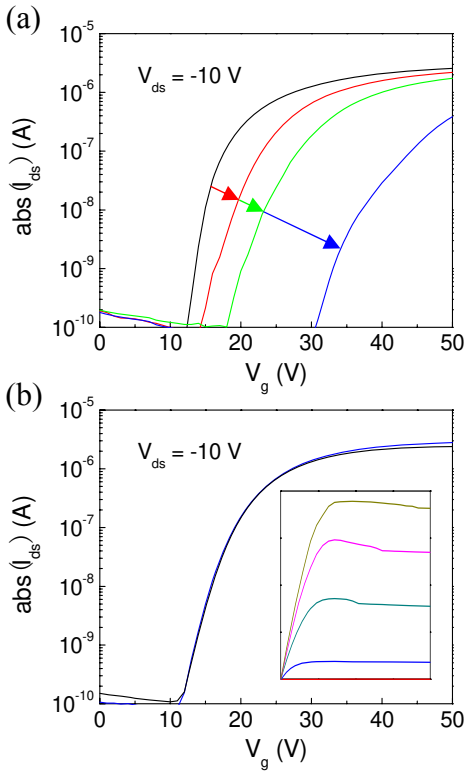


Figure 4-8. Transfer characteristics of C_{60} FETs with 500 nm SiO_2 and 10 nm PMMA buffer dielectric with $V_{ds} = -10$ V before (black line) and after programing with a gate bias of (a) 200 V and (b) -200 V at $V_{ds} = 0$ V for 10 ms (red line), 100 ms (green line) and 1s (blue line). The inset shows its output characteristics.

The inset in Fig. 4-8b showed that the drain current I_{ds} of C_{60} FETs began to decrease due to the oxygen molecules acting as electron traps,[92] when V_{ds} swept to the saturation region. The trapping of electrons appeared even

more significant at higher gate voltage, e.g. with threshold voltage shift $\Delta V_{th} = 18\,V$ for biasing at $V_g = 200\,V$ and $V_{ds} = 0\,V$ for $1\,s$. The $I_{ds} - V_g$ curves would return to the initial state when the device was left unbiased for around 1 h due to the release of trapped electrons (data not shown here). The trapping of holes was hardly observed, i.e. almost no shift in the subsequent $I_{ds} - V_g$ curves, although a gate bias of $-200\,V$ for 1 s was applied.

The above results indicated that the silanol group-related electron traps for p-channel devices and the water-related hole traps for n-channel devices at the interface of SiO_2 almost cannot be accessed, which was primarily attributed to the charge injection barriers, originating from the large mismatch between the work functions of source/drain contacts and LUMO/HOMO levels of used active layers, and from the additional buffer dielectric. Given that $\Phi Au = -5.1\,eV$ and $LUMO_{pen} = -3.2\,eV$ and $HOMO_{pen} = -5\,eV$, $\Phi Al = -4.2\,eV$ and $LUMO_{Ful} = -3.8\,eV$ and $HOMO_{Ful} = -7.1\,eV$, the charge injection barrier of electrons (holes) for pentacene (C_{60}) FETs is as large as $1.9\,(2.9)\,eV$, without taking PMMA into account, which is already too large to be surmounted.[177,178] This is slightly different from that of memory devices based on the FET structure employing floating gate (FG) and/or the metal-nitride-oxide-silicon (MNOS) transistor.[49,127,179] In the case of devices with FG, electrons are easily induced and injected through a thin insulator at high transverse electrical field, even though high work-function metal is used as the source-drain contact in p-channel FETs. The average electrical field during writing/erasing in flash memory is about $10\,MV\,cm^{-1}$, we might need to increase the applied voltage to verify our results. But due to the voltage limitation of our equipment, a thinner gate insulator shall be employed. The

exact mechanism for preventing charge carriers from being captured in pentacene (C_{60}) FETs would be investigated in future. On the other hands, the trapping of majority carriers occurred in pentacene (C_{60}) FETs when devices operated under working state. We assumed that the amount of trapped charge Q_{trap} at their initial state was zero. When negative (positive) gate bias was applied, the amount of trapped charges, Q_{trap}, can be evaluated through the following equation:

$$Q_{trap} = \pm C_i \Delta V_{th} \quad (4.7)$$

By applying a gate bias of ± 200 V with 1 (0.5) s bias time for C_{60} (pentacene) FETs, respectively, the calculated value of Q_{trap} was around $\pm 1\ (0.5) \times 10^{-7}$ C cm^{-2}. Obviously, Q_{trap} increases when the bias time was extended and long time biasing would completely turn the device off leading to the failure of switching function. A similar phenomenon was also observed in the devices using SAMs as buffer dielectric when these devices were repeatedly stressed by measuring transfer characteristics in the saturation regime, because surface silanol groups cannot be fully passivated by SAMs.[158,180]

4.3.2b UNDER ILLUMINATION

It is important to understand light illumination effects on electrical performance of these devices, as well as the underlying physics of these effects in applications such as switches for flat panel displays (FPDs). Light absorption generates electrons and holes, and these electrons and holes may be paired in form of excitons that diffuse like neutral particles. The bound electron-hole pairs can be dissociated by applying an appropriate gate-to-source bias in the FET devices, and the separated electrons (holes) begin to

move under the influence of the electrical field. It was expected that the shift of V_{th} toward the positive (negative) side in pentacene (C_{60}) FETs would be brought out due to the involvement of non-equilibrium charge carriers, when a positive (negative) gate bias was applied under illumination.[180] When investigating the effect of steady-state broadband illumination on the electrical performance of our devices, the illumination power was controlled at a low level to minimize the degradation of OSCs under light irradiation and the programming time was not more than 30 s to minimize the charge trapping in the grain boundaries of our polycrystalline films. Before programming by a gate bias, the incident light was stabilized for 5 s. This was done by shining the top of the entire channel region.

As expected, the entire transfer curve of pentacene FETs with 10 nm PMMA buffer dielectric was greatly shifted toward the positive direction by applying a gate bias of 200 V for 20 s under illumination, as shown in Fig. 4-9a. As a result, the value of V_{th} was changed by more than 125 V, as seen from Fig. 4-9b. In contrast, there was little change in V_{th} when the device was merely illuminated for 20 s without gate bias, shown by the solid blue circle in Fig. 4-9b, or programmed by a positive gate bias without illumination, shown in the inset of Fig. 4-9b. Usually, the drain current in the "OFF" state is slightly affected, which is attributed to the enhancement of carrier density in the channel of the device and thus the conductivity. The change in V_{th} was attributed to the generation of non-equilibrium charge carriers, which were transferred under the electrical field and trapped by buried trapping states at the PMMA-SiO_2 interface. It showed a good agreement with published results observed in p-channel FETs with 10 nm PS (or PMMA) buffer dielectric.[181]

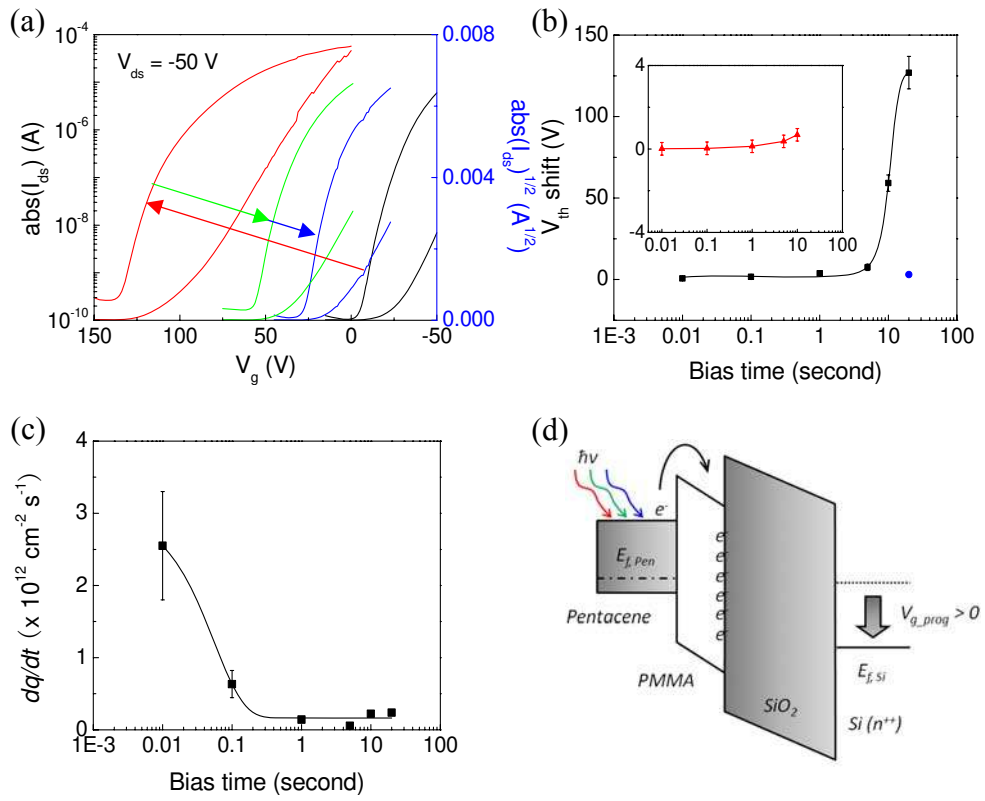


Figure 4-9. (a) Transfer curves of pentacene FETs with 500 *nm* SiO_2 *and* 10 *nm PMMA buffer dielectric: initial characteristics (black line), measured in the dark after programing (*$V_g = 200\ V$, $V_{ds} = 0\ V$ *for* 20 *s under illumination) immediately (red line),* 1 *h later (green line), and* 10.5 *h later (blue line); (b)* V_{th} *shift versus programing duration under illumination (black square line) and in dark condition (red triangle line, shown in the inset), and blue circle represents the* V_{th} *shift was induced by the illumination for 20 s without application of gate bias; (c) the transfer rate of electrons versus programing time; (d) schematic illustration of electron generation under illumination, transfer across PMMA buffer dielectric, and trapping at the PMMA/*SiO_2 *interface, where* $E_{f,Si}$ *and* $E_{f,pen}$ *are the Fermi energy of pentacene and silicon, respectively.*

However, the time of positive gate bias needed for inducing the shift in V_{th} was much shorter than ours, which might result from the variation of conductivity of polymers because of different processing conditions, e.g. the effect of solvent.[183] The charge transport can either tunnel between localized states, depending on the density of defect states in polymers, or hop via extended electronic states, though clearly one mechanism would dominate. In the case of transport via extended states, carrier motion is repeatedly

interrupted by trapping of carriers in localized states and then re-emission into the extended states. The drift mobility in such situations is greatly reduced from the free carrier mobility due to the time the carriers spend in traps. Although it is still far away from the well understanding of the exact mechanism in OFET memory devices, a potential mechanism was proposed, in which the charge transfer was greatly related with the applied electrical field.[181-183] An electrical field F of ca. $4.6\ \mathrm{MV\ cm^{-1}}$ (according to $= \mathrm{V_g}/\left[\mathrm{t_p} + \mathrm{t_s}(\varepsilon_\mathrm{p}/\varepsilon_\mathrm{s})\right]$), much larger than the dielectric strength of PMMA (ca. $0.2\ \mathrm{MV\ cm^{-1}}$), was applied to facilitate the charge injection. Fig. 4-9b shows the resulting shift in $\mathrm{V_{th}}$ of our pentacene FETs as a function of bias time. Clearly, there was a turning point. For $\mathrm{t} < 1\ s$, the change in threshold voltage $\Delta\mathrm{V_{th}}$ was less than 4 V. For $1 \leq \mathrm{t} \leq 20$ s, the value of $\Delta\mathrm{V_{th}}$ increased sharply. This was ascribed to a response time τ, which the photogenerated electrons needed to be transferred through PMMA and trapped at the interface of SiO_2. It seemed that this was a slow process, as a long bias time was indispensable to achieve the considerable shift in $\mathrm{V_{th}}$ under a constant transverse electrical field F. Given that the mobility of PMMA at room temperature is ca. $1.0 \times 10^{-11}\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$,[184] it took nearly 0.02 s for electrons to transport through 10 nm PMMA), which was reasonable compared to the observed response time τ. It is believed that the observed photoinduced shift in $\mathrm{V_{th}}$ is caused by the charging of the bilayer gate dielectric with non-equilibrium carriers that are photogenerated in pentacene near the interface and transferred/trapped in these buried trapping states at the surface of SiO_2, schematically shown in Fig. 4-9d. The variation of the surface density of charges transferred/trapped at the PMMA-SiO_2 interface, $\Delta\mathrm{n} = \mathrm{Q_{trap}}/\mathrm{q}$, is related to the observed shift of

threshold voltage V_{th} according to eq (4.7). The charge transfer rate can be roughly estimated from the shift ΔV_{th} after applying a V_g at $V_{ds} = 0$ V for a (short) time interval Δt under illumination:

$$dn/dt = \frac{C_i \Delta V_{th}}{q \Delta t} \quad (4.8)$$

Interestingly, the electron transfer rate decreased quickly ($t < 1\,s$) and gradually reached a constant level ($1 \leq t \leq 20$ s), as shown in Fig. 4-9c. This indicated that the average charge transfer rate across 10 nm PMMA under illumination was ca. 1.6×10^{11} cm^{-2} s^{-1}. It was because a surface potential created by charge trapped in the buried states decelerated the injecting electrons and reduced the electron penetration range, resulting in a saturation of trapped charges. An electron transfer rate of ca. 5×10^{9} cm^{-2} s^{-1} under short wavelength light illumination ($400 < \lambda < 500\,nm$) was reported in the single crystal rubrene FETs with parylene as the gate dielectric, which was much smaller than our results.[181] This was mainly ascribed to (i) the different flux of photons, (ii) the injection barrier provided by the bulk material of parylene, and (iii) the transverse electrical field F, which determined the extent of the charge injection and transport.

When a charge is injected and trapped, the de-trapping also occurs simultaneously to restore the neutral state by transferring the excessive charges to the ground, which was characterized by the retention time in dark condition. After programming, a decay process of I_{ds} (measured at $V_{ds} = -50$ V and $V_g = 0$ V) in the "ON" state in dark condition was recorded and plotted in Fig. 4-10, where the time required for the "ON" state current to decrease to 10% of its initial value was estimated to be around 10^4 s.

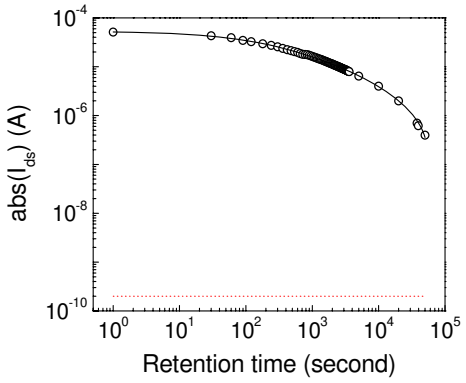


Figure 4-10. Time evolution of I_{ds} measured in the dark at $V_{ds} = -50\ V$ and $V_g = 0\ V$ after programing ($V_g = 200\ V$, $V_{ds} = 0\ V$, for $20\ s$ under illumination). The off current (dot line) is shown for reference.

In Fig. 4-9a, it was more obvious that the shift in V_{th} toward negative side was very fast in the first hour and became very slow in the next 10 hours, indicating that there were two distinguishable decay rates: (i) an initial rapid relaxation due to the recombination of closely packed holes and electrons and (ii) a subsequent slower relaxation that originated from deeply trapped carriers, depending on the quality and conductivity of the PMMA buffer dielectric. Our results indicated that a charge storage lifetime in the dark can be estimated to be several days long. On the other hand, based upon our discussion in section 3.1, the trapped electrons can also be swept out and/or recombined with field-induced holes by applying a negative gate bias in the dark. Consequently, the shifted transfer curve can restore to its initial state, completing a cycle of turning "ON" and "OFF".

The photo-induced charge transfer was also studied in the n-channel FETs. However, when programming the device, only a short time period of gate bias was used in order to minimize the degradation of C_{60} due to the exposure to the ambient air and light irradiation.[92,185,186] Two mechanisms of degradation had been described as following: (i) the absorbed oxygen molecule

acts as electron traps within the lattice of C_{60} molecule and epoxidation reaction might take place on C_{60},[92] and (ii) the fragmentation of C_{60} caused by ultraviolet (UV) light.[185-187] When a gate bias of -200 V with a period of 1 s was applied, the transfer curve was greatly shifted toward the negative direction, as shown in Fig. 4-11. However, it quickly went back to the original state within a few minutes in the dark, attributing to the rapid release of trapped holes. This suggested that the trapping of electrons was much more supportive in this device due to the presence of oxygen dopants and accessible hydroxyl groups, as compared to that of holes.

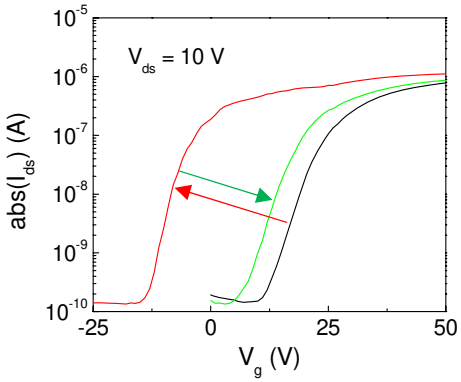


Figure 4-11. Transfer curves of C_{60} FETs with $500\,nm$ SiO_2 and $10\,nm$ PMMA buffer dielectric at $V_{ds} = -10\,V$: initial characteristics (black line), measured in the dark after programing ($V_g = -200\,V$, $V_{ds} = 0\,V$ for $1\,s$ under illumination) immediately (red line) and $1\,min$ later (green line).

To further verify our previous hypothesis that the charge trapping primarily took place at the dielectric-dielectric interface, 45 nm thick PMMA was used as the buffer dielectric to minimize the pinhole defects and increase the barrier width, and 200 nm thick SiO_2 was used as the gate insulator. To compare with the previous results, the effect of light illumination on inducing the shift in V_{th} was carried out by applying a gate bias of ± 100 V in order to

equalize the value of F (ca. 4.7 MV cm^{-1}) across the dual dielectric. When programmed by a gate bias of 100 V with a period of 30 s under illumination, the transfer curve only shifted slightly toward the positive direction (see Fig. 4-12a), giving rise to a ΔV_{th} of less than 2 V.

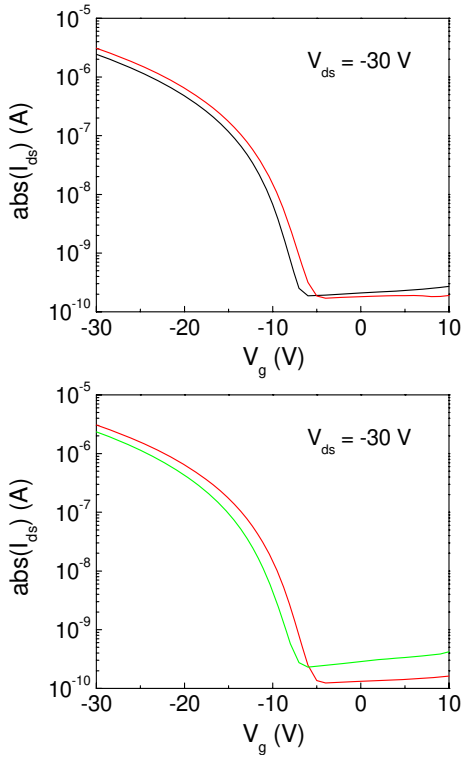


Figure 4-12. Transfer curves of pentacene FETs with $200\ nm$ *SiO_2 and* $45\ nm$ *PMMA buffer dielectric with* $V_{ds} = -30\ V$ *before (black line) and after (red line) programing, where a programing gate bias of (a)* $100\ V$ *and (b)* $-100\ V$ *for* $30\ s$ *at* $V_{ds} = 0\ V$ *was applied under illumination.*

This was ascribed to a small quantity of electrons trapped in the structural defects of polycrystalline pentacene thin films, i.e. grain boundaries, and at the interface between pentacene and PMMA. The transfer of electrons from the active layer into these buried trapping states at SiO_2 surface was greatly depressed as the thick PMMA film effectively shielded the underneath hydroxyl groups. At the same time, a gate bias of -100 V with a period of 30 s

was also applied under illumination, the shifted transfer curves due to the application of the positive gate bias was almost restored to the initial state (see Fig. 4-12b), showing only a little shift (ca. 0.5 V) to the negative direction. This indicated that the trapping of holes was suppressed because the reduction of absorbed water molecules thanking to the hydrophobic surface of PMMA. By utilizing the thickness-optimized PMMA, our devices were very resistive to the high transverse electric field and light illumination, resulting in excellent device stability. This differed from that of devices with ≥ 60 nm styrenic polymers (or PMMA), who exhibited considerable shift in V_{th} after programming.[161,182] To further improve the device stability, the purification of active materials as well as the buffer dielectrics is needed to cut down the unintentional doping acting as the charge trapping centers.

4.4 CHAPTER SUMMARY

In conclusion, the shift of threshold voltage due to the charge trapping (both electron and hole) in the buried states between PMMA and SiO_2 was evaluated in p- and n-channel OFETs, respectively. The trapping of electrons (compared to holes) in p-channel devices and the trapping of holes (compared to electrons) in n-channel devices are more difficult in the dark condition due to the large injection barrier between the contact and the active layer. Although the 10 nm-thick PMMA layer also provides an additional charge injection barrier, when the device is programmed under illumination, the photo-generated non-equilibrium charge carriers in the active layer can be easily injected through 10 nm PMMA into these buried states and trapped under the high electrical field. The trapped electrons in p-channel FETs can retain for

several days while the release of trapped holes in n-channel FETs is much faster. However, such photo-induced charge transfer can be effectively suppressed by an optimized thickness of PMMA buffer dielectric (45 nm) at the same characterization condition, and thus stabilize the threshold voltage. Besides the device encapsulation and the development of new OSC combining high mobility with excellent stability, data presented in this work brings out an alternative approach to enhance the stability and reliability of organic transistors using bilayer gate dielectric. In order to selecting a proper buffer dielectric, attention must be paid to the following: (i) nonpolar buffer dielectrics with excellent film-forming and low surface/bulk states are preferred, such as low-k polymeric dielectric BCB and Cytop,[158,188] and (ii) its thickness should also be optimized when it is applied in FET structures (both bottom- and top-gate architectures). Our findings should also be relevant to other cases, for example, in an OFET-based memory device where the charge dissociation/trapping process under light irradiation is involved.

CHAPTER 5: LOW-VOLTAGE PENTACENE FIELD-EFFECT TRANSISTORS

5.1 CHAPTER INTRODUCTION

With the demonstration of high-performance and reliable organic field-effect transistors (OFETs),[43,188,189] comparable to that of amorphous silicon TFTs, it seems likely that they will find use in current and future macroelectronic applications. All these applications require devices with suitable performances, among them a low operating voltage, a high on/off ratio and a high stability are of prime importance. For portable devices that could be driven by low-voltage power sources such as batteries, high capacitance density with low tunneling current in a transistor is essential to reduce the operation voltage and power consumption, which is proportional to the dielectric constant but inversely proportional to the thickness of the insulator. Common dielectric materials for low-voltage devices include ultrathin cross-lined polymer films,[23-26,48] polyelectrolytes,[190,191] inorganic oxides,[11-22] and hybrid organic/inorganic dielectrics.[22,192,193] Since the "high-κ metal gate" technology was introduced by several semiconductor companies such as Texas Instruments Inc and IBM in the (sub) 45 nm microprocessor, attentions to the need for high-κ gate insulators was widely disseminated. A great number of these materials have been investigated as gate dielectrics that are also applicable in the OFET structure, such as BST,[194-196] Ta_2O_5,[12-15] TiO_2[17] and, particularly, HfO_2 as well as their silicates.[20-22,197,198] For perovskite crystals,

e.g. BST, Ti ions in unit cells throughout the crystal can be uniformly displaced in response to an applied electrical field. This displacement of Ti ions causes an enormous polarization in the materials, which is normally utilized for ferro-electric non-volatile memory devices. In the case of Ta_2O_5 and TiO_2, both have small band gaps, i.e. small E_g values, which directly correlate with high leakage current. This shortcoming makes the pure Ta_2O_5 and TiO_2 unreliable as gate dielectric. On the contrary, HfO_2 offers relatively high values for both κ, nominally close to that of Ta_2O_5, and $E_g(\text{ca. } 5.68 \text{ eV})$, and also exhibits high temperature stability. For these reasons, HfO_2 has been frequently used to fabricate low-voltage OFETs.

Unfortunately, for high-κ oxide such as HfO_2, there is a hysteresis phenomenon in its capacitance-voltage ($C-V$) characteristics.[199] This hysteresis will induce a flatband voltage shift, consequently a threshold voltage instability when it is applied to MOSFETs and/or OFETs. Therefore, in the case of MOS devices, some methods, such as cosputtering of silicon and aluminum with hafnium to deposit hafnium silicate and aluminate dielectrics,[200,201] and the use of nitric gas for CVD[202] or oxidizing sputtered metal nitride like HfN[203] to form hafnium oxynitride (HfON) films, are used to improve it. Moreover, pre- and post-deposition annealing ($400-900\,℃$) and/or plasma treatment are usually employed to form high quality HfO_2 thin film with improved thermal stability, reduced leakage current for the same equivalent oxide thickness (EOT), and enhanced reliability.[204-206] Wang et al.[205] reported that post-deposition NH_3 plasma treatment can successfully introduce nitrogen atoms into the dielectric to form Hf−N bonding and suppress Hf−Si bonding, leading to removal of the dielectric vacancies and

subsequently a reduction of some trapping levels. Lai et al.[206] demonstrated that the fluorine atoms were distributed at the interface between the HfO_2 thin film and silicon substrate after pre-CF_4 plasma treatment on Si, effectively inhibiting the formation of an interfacial layer between the HfO_2 thin film and Si substrate. The fluorine passivation also plays a role in blocking oxygen diffusion into the Si, resulting in an EOT reduction for the HfO_2 gate dielectrics. In these two cases, the deposition of HfO_2 gate dielectric will not affect the morphology of the channel layer, subsequently the device performance, because the rigidness of silicon substrate. However, it is quite different for OFETs, because OFETs adopt the architecture of the thin film transistor. For example, in the top-contact structure, the organic active layer is grown after the deposition of HfO_2 gate dielectric, apart from forming high quality HfO_2 thin film with low bulky defect and leakage current, its surface nature (e.g. roughness and organic contaminations) also has a great impact on the FET performance, such as affecting the growth mode of organic molecules (i.e. the molecular ordering and packaging). In order to improve the surface condition of HfO_2, surface modifications are widely investigated by using the experiences of other systems for reference, such as (PMMA) OTS-modified SiO_2 and other dry gaseous processing techniques.[6,71,141-152] Acton et al.[22] showed that high capacitance ($690\ \mathrm{nF\ cm^{-2}}$) and low leakage current density are achieved by $HfO_2(3.1\ \mathrm{nm})/SiO_2(1.7\ \mathrm{nm})$ modified by anthryl-terminated phosphonic acid (PA) SAMs while simultaneously improving pentacene OFETs performance including low subthreshold slopes ($100\ \mathrm{mV\ dec^{-1}}$), high I_{on}/I_{off} $(10^5 - 10^6)$ and hole mobility ($0.22\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$). Later, the same group found that using spin-coated n-octylphosphonic acid (OPA) on Ag

bottom-contact electrodes and ultra-thin HfO_2 dielectric, C_{60} and pentacene based OFETs can operate under 3 V with low contact resistance (down to $700\ \Omega \cdot \mathrm{cm}$), low subthreshold swing (down to $75\ \mathrm{mV\ dec^{-1}}$), high on-off current ratios of 10^7, and charge carrier mobilities as high as 4.6 and $0.8\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$, for C_{60} and pentacene, respectively.[207] Zhang et al.[208] reported that pentacene FETs showed excellent bias stress stability ($V_g = -3$ V and $V_{ds} = -0.5$ V) in N_2-filled glove box ($O_2, H_2O < 0.1\ ppm$) with extremely low I_{ds} decay of ~10% with ODPA and ~15% without ODPA at HfO_2 surface (50 nm) after two hours respectively. On the other hand, a thin low-k polymeric buffer dielectric has also been used as a simple and effective way to modify the surface properties of HfO_2, which retains the advantages from the both organic and inorganic dielectrics.[209-212] Wang et al.[210] found that a thin PS layer (17 nm) annealed at 120 ℃ can be utilized to enhance the mobility by optimizing the quality of HfO_2 (5 nm) by inducing flatter phenyl group orientation and better matched surface energy with pentacene. Additionally, PS can also be used to passivate the surface of HfO_2 such as hydroxyl groups and suppress the absorption of moisture to eliminate the hysteresis behavior due to the trapping of charges.[211] Besides the above two modification methods, a low temperature gaseous processing technique provides another easy and economical way to improve the surface quality of HfO_2 chemically and physically, such as UV ozone, ion beam and plasma treatment.[213-215] It is referred to as a dry process, because there is not any organic solvent involved during the treatment. For instance, UV ozone has been used to eliminate the defects such as oxygen vacancies in the oxide film and increase the work function of the bare Au SD contact, resulting in better

hole injection into organic active layer.[214] It also can be employed to grow a passivating interlayer (Al_2O_3) on Al gate electrode to restrict the charge injection from the metal gate.[215,216] Nitridation techniques used to treat MOS devices are also applicable to OFETs.[217] Excellent interface quality between HfO_2 and pentacene is achievable by annealing the deposited HfO_2 film in N_2O or NH_3 at $200\,℃$, giving rise to a mobility of $0.655\,cm^2\,V^{-1}\,s^{-1}$ at the operating voltage of less than 3 V. Meena et al. also reported that the number of traps can be minimized within the low temperature deposited HfO_2 film after oxygen plasma treatment in a metal-insulator-metal (MIM) structure by completely oxidizing the film surface to $–(O–Hf–O)_n–$ and removing the residual organic parts.[218] This process allows high-performance electronic devices to be fabricated on plastic substrates. However, the effects of oxygen plasma treatment on the surface of HfO_2 film on the performance of pentacene-based OFETs and aging effect of the oxygen plasma modified pentacene polycrystalline film have been rarely reported in the literature.

In this work, low-voltage pentacene FETs were fabricated with ultrathin HfO_2 gate dielectric grown by atomic layer deposition (ALD). Compared to other processing routes such as sol-gel,[21,22,207,210,212] sputtering[209,211,214,215,217] and anodization,[21] ALD offers many advantages because of its self limiting chemical reaction: (i) accurate film thickness control (in subnanometer); (ii) good uniformity over large area (up to many inches size) and reproducibility; and (iii) high film quality at low deposition temperature that is well compatible with plastic substrates.[208,213,218] The study on the influence of oxygen plasma on device performance will be carried out through various exposure times for plasma treatment and a series of (negative and

positive) gate bias stress measurement. It is found that using plasma-treated HfO_2 realized not only higher mobility but also improved resistance to gate bias stress, as well as the tunability of threshold voltage. Finally, taking the plasma-induced increase of surface energy into account, a potential degradation mechanism for polycrystalline pentacene film on plasma-treated HfO_2 due to the exposure to the air and light was proposed.

5.2 EXPERIMENTAL DETAILS

Pentacene FETs were fabricated on a heavily doped n-type silicon substrate (resistivity $= 0.01\ \Omega \cdot \mathrm{cm}$, also serves as gate electrodes). A schematic of the device is given in Fig. 5-1a. After standard Radio Corporation of America (RCA) clean, $12\ \mathrm{nm}$ thick HfO_2 was deposited by alternating exposures of tetrakis(dimethylamido)hafnium (TDMAH) and water vapor using a Savannah100 ALD system (Cambridge Nanotech Inc.) with a substrate temperature of $250\ ^\circ\mathrm{C}$, which is close to the upper limit of the working temperature of a plastic substrate.[219] To ensure sufficient vapor pressure, both TDMAH vessel and water vessel were maintained at $150\ ^\circ\mathrm{C}$. The growth rate is 1.0 Å per cycle. Before the deposition of pentacene, the surface of HfO_2 was treated by oxygen plasma treatment using Advanced System Technology (AST) Clen 100 with a fixed power of $30\ \mathrm{W}$ and a constant oxygen flow of $20\ \mathrm{sccm}$ at a base pressure of $160 - 170\ \mathrm{mTorr}$. Prior to processing the substrates, the plasma-treatment chamber was pre-cleaned for $10\ \mathrm{min}$ in order not to recontaminate the surface during cleaning. The device was completed by the deposition of Au source-drain contacts through a shadow mask. The details of the fabrication of pentacene FETs can be found elsewhere.[220] Typical device

dimensions were 100 um channel length (L) and 2 mm channel width (W). For comparison, devices using HMDS (OTS and poly(4-vinyl phenol) (P4VP)) modified HfO_2 as gate dielectric with the same thickness of pentacene active layer and channel length and width were fabricated. The HMDS treatment was performed in a vapor prime system (Yield Engineering System, Inc.) at 150 °C with a base pressure of 760 Torr for 20 min. The silane SAM was laid on HfO_2 by first cleaning the wafer surface with oxygen plasma, followed by immersion in a 0.1 M OTS solution in toluene at 60 °C for 20 min, subsequently rinsed by isopropanol, and then dried using a nitrogen gun before use. P4VP buffer dielectric was prepared from a solution of P4VP and poly(melamine-co-formaldehyde) methylated (weight ratio of 1:1) in propylene glycol monomethyl ether acetate (PGMEA), deposited by spin coating, and cross-linked at 180 °C for 1 h under a vacuum atmosphere. The final thickness of cross-linked P4VP films was $20 - 30$ nm, measured by the surface profiler.

The electrical characteristics of individual device were measured using a Keithley 4200 SCS Semiconductor Parameter Analyzer and Agilent 4294A Precision Impedance Analyzer in a standard probe station under ambient dark condition at room temperature. Unless specified, the gate sweep direction in transfer characteristics was from positive to negative, with 100 ms hold time and 100 ms delay time at 10 mV steps. The thickness of HfO_2 was measured using fixed-angle (70°) spectroscopic ellipsometry VB-250 at $300 - 1000$ nm, and the values reported represent the mean of five measurements over a 4 inch wafer. The chemical bonding of the elements of interest was analyzed by XPS. The topographies of HfO_2/Si substrate and pentacene film grown on HfO_2/Si

substrates with/without plasma treatment were evaluated by atomic force microscopy (AFM) using a Digital Instruments Nanoscope IIIa Multimode scanning probe microscope operating in tapping mode. The X-ray diffraction (XRD) analysis of pentacene film on HfO_2/Si substrates with/without plasma treatment were carried out with a Bruker D8–Advanced X-Ray Diffracto-meter (Cu Kα radiation, $\lambda = 1.5406$ Å).

5.3 RESULTS AND DISCUSSION

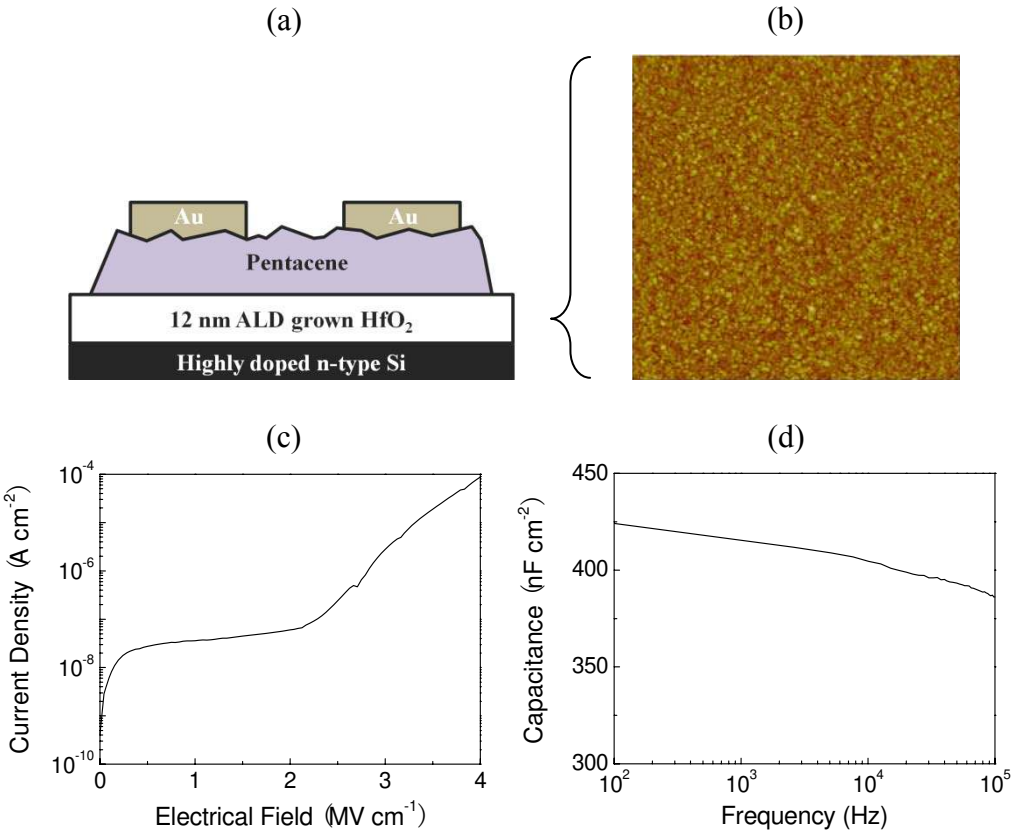


Figure 5-1. (a) Schematic of a top-contact OFET. (b) Topography of the surface of ALD grown HfO_2 ($1 \times 1\ um^2$). (c) Leakage current density versus electrical field. (d) Frequency-dependent capacitance for $12\ nm$ ALD grown HfO_2 sandwiched between Au dots and highly doped n-type Si substrate.

Good surface uniformity of the gate dielectric is crucial for fabricating high-performance and reliable devices over large areas. The AFM image

shown in Fig. 5-1b indicated that the as-deposit ALD grown HfO_2 film on silicon substrate was pin-hole free and smooth with a root-mean-square (RMS) roughness of 0.3 nm. In order to evaluate the insulating properties of the ALD grown HfO_2 film, metal-insulator-metal devices composed of heavily doped Si-HfO_2-Au were characterized. The density of leakage current (D_L) presented in Fig. 5-1c was well below 1×10^{-7} A cm^{-2} at 2 M cm^{-1}. It increased rapidly to 1×10^{-4} A cm^{-2} with further increasing applied voltage, suggesting that the injection of electrons from Au to the heavily doped silicon would be greatly enhanced through the HfO_2. The capacitance density of 415 nF cm^{-2} was achieved at a frequency of 1 kHz with slightly smaller values at higher frequency, as shown in Fig. 5-1d. As compared to other fabrication method,[21] the lower value of the capacitance may be attributed to the loose structure. However, these data presented here suggested that our ALD grown HfO_2 is already fit for the fabrication of low-voltage OFETs.

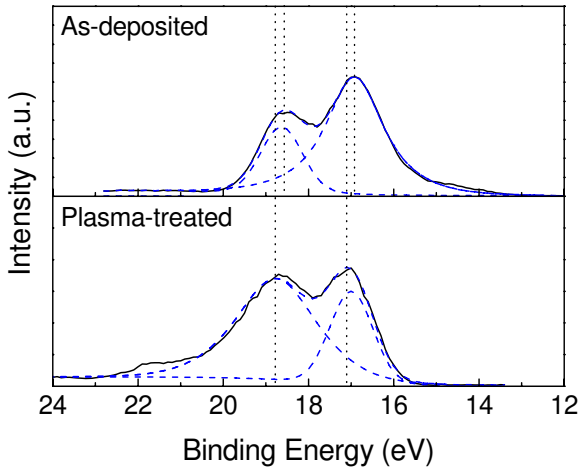


Figure 5-2. High resolution XPS spectra of the Hf 4f energy levels for 12 nm as-deposited and plasma-treated HfO_2 films on silicon. The solid curve represents the experimental data; dash curves represent the fitted peaks and the summarized results of the fitted data.

Prior to carrying out the study on the influence of the O_2 plasma on the electrical performance of pentacene FET devices, we firstly examined the difference of the chemical composition of the HfO_2 film before/after plasma treatment by using XPS analysis. Fig. 5-2 displays high-resolution spectra of the Hf 4f energy levels of the two samples. The spectra were deconvoluted into two spin–orbit doublet peaks for the Hf $4f^{7/2}$ and Hf $4f^{5/2}$ energy levels at different binding energies of the Hf−O bonds. For as-deposited HfO_2 film, the peaks for the $4f^{7/2}$ and $4f^{5/2}$ binding energies were detected at 16.8 and 18.5 eV, respectively. After O_2 plasma treatment, the binding energies of the $4f^{7/2}$ and $4f^{5/2}$ were raised to 17.0 and 18.7 eV, respectively, which was shifted roughly 0.2 eV to the higher binding energy (BE) as compared to that of as-deposited HfO_2 film. The shift toward higher BE for the Hf–O bonds suggested that oxygen plasma treatment introduced some bonding structures for the complete oxidation of the Hf atoms.[218] It implied that O_2 molecules reacted with the Hf dangling bonds (or traps, such as oxygen vacancies) to form stronger Hf–O bonds. In addition, the low-resolution XPS for the Hf 4f bonds for HfO_2 film with/without plasma treatment was also recorded to examine its chemical composition. Fig. 5-3 reveals that the sample consisted of hafnium, oxygen, and a small amount of contaminating carbon; no other impurities were present on the film surface. It shows the spectrum of the as-deposited film with an O(1s) peak at around 530.3 eV and two O(1s) peaks for a plasma-treated sample at 530.7 and 532.1 eV, respectively. The presence of two peaks implied that oxygen were present as HfO_2 and Hf–Si–O, indicating the formation of a thin interfacial layer. In the plasma-treated film, the C(1s) peak at around 285 eV band intensity significantly decreased than the as-

deposited film. The existence of low intense C(1s) peak can be attributed to a partially oxidized carbon species with a slight peak broadening, since the oxygen atoms bond to a portion of carbon. This spectroscopic result revealed that the content of defects was much reduced after subjecting the sample to the plasma treatment. However, the integrity of our ALD grown dielectrics can be further improved by annealing at higher temperature.

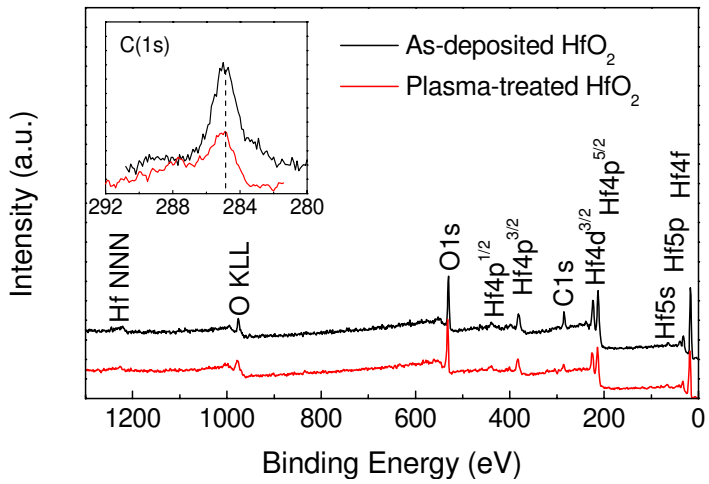


Figure 5-3. Low resolution XPS spectra of 12 *nm ALD deposited* HfO_2 *film on Si substrate for as-deposited and plasma-treated samples. Inset: XPS spectra in the BE regions of O (1s).*

Typical output and transfer characteristics of a pentacene FET with as-deposited HfO_2 were shown in Fig. 5-4a,b, respectively. Good saturation behavior was obtained, demonstrating desirable FET characteristics with an operation voltage of -1 V. The field-effect mobility μ_{sat} and the threshold voltage V_{th} were estimated in the saturation regime defined by standard MOSFET models through fitting the data of $\sqrt{I_{ds}}$ versus V_g to a square law model. Also the subthreshold slope (S), which determined the change in gate voltage V_g needed to turn the device on and off, can be extracted. For low-

power circuits, small S and V_{th} are demanded, which would be influenced by the gate capacitance and the density of interface traps N_{tr}:[49,122]

$$S = \frac{kT}{q}\ln 10 \cdot \left(1 + \frac{C_d + C_{it}}{C_i}\right) \tag{5.1}$$

$$V_{th} = \frac{qN_{tr}d}{C_i} \tag{5.2}$$

where kT is the product of the Boltzmann constant k and the temperature T, q is the charge of electron, C_d is the depletion-layer capacitance, C_{it} results from interface traps and d is the thickness of conducting channel. The calculated values of μ_{sat}, S and V_{th} were $0.01\ cm^2\ V^{-1}\ s^{-1}$, $252\ mV\ dec^{-1}$ and $-0.4\ V$, respectively.

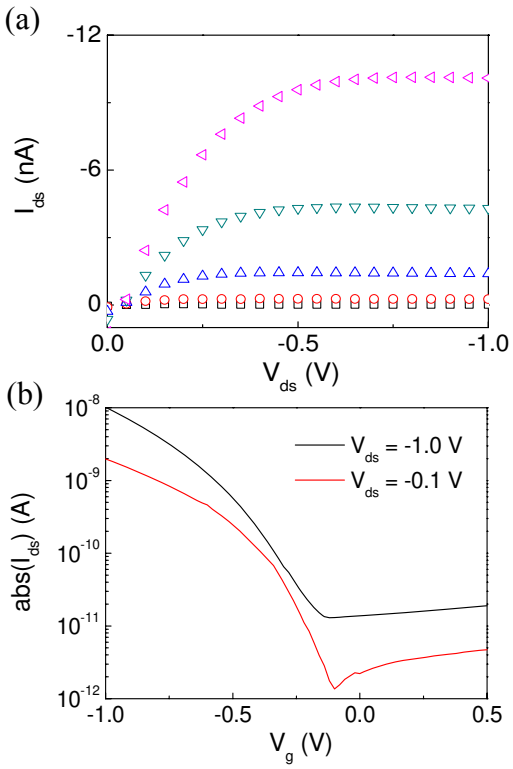


Figure 5-4. (a) Output characteristics (V_g ranges from -0.2 to $-1\ V$ in a step of $-0.2\ V$). (b) Transfer characteristics of pentacene FETs using HfO_2 as gate dielectric without the plasma treatment.

The obtained value of μ_{sat} in our devices was similar to that of devices with as-deposit HfO_2, shown in Table 5.1. Usually, a low mobility ranging

from 10^{-3} to 0.1 $cm^2\ V^{-1}\ s^{-1}$ was observed when pentacene active layer was directly deposited on top of the bare HfO_2 film. It is known that the device performance, e.g. field-effect mobility, was proposed to be strongly correlated with the growth mode of pentacene film, which is influenced by the surface roughness and its hydrophobicity (i.e. the surface energy) of beneath gate dielectric,[222,223] sometimes SD contacts and gate dielectric. Best mobility is measured when pentacene molecules are closely packed in a 3D growth mode with improved the interconnection and contact between grains on the smooth and slightly hydrophobic surface. According to the previous work, the surface energy theoretical value derived from the orthorhombic-phase pentacene grown was estimated to be 38 $mJ\ m^{-2}$.[224] Wei et al.,[225] fabricated a low surface-energy bare HfO_2 film (34.24 $mJ\ m^{-2}$), matchable to 38 $mJ\ m^{-2}$, giving rise to a hole mobility of as high as 3.8 $cm^2\ V^{-1}\ s^{-1}$ in pentacene film directly deposited on such HfO_2 film. However, the surface energy of deposited HfO_2 film is normally much larger than 38 $mJ\ m^{-2}$, resulting in a 2D growth mode of pentacene film (containing the large voids in the first layer of pentacene film and incomplete growth of subsequent layers), which can limit the transport of charge carriers and cause lower carrier mobility.[223] In order to achieve a proper surface to provide a better growth environment for OSCs, dielectric surface modification, as mentioned before, is widely used.[22,225] Apart from tuning the morphology of OSCs, modification of HfO_2 film can also passivate trap sites at the dielectric surface (e.g. –OH groups), reduce the polaron formation between the charge carriers in the OSC and the induced ion polarization of the underlying high-κ lattice, and in the BC structure, tune the work function of the metal to match the energy level of OSC to achieve ohmic

contact. Therefore, the mobility of OFETs with surface treated HfO_2 film was generally one order of magnitude larger than ours.[22,207,210]

Table 5.1. Summary of OFET characterization (Thickness of HfO_2 thin film, D; Operation voltage, V_{op}; Threshold voltage, V_{th}; Field-effect mobility, μ) with pentacene active layer grown on HfO_2 surface.

Dielectric	Method*	D (nm)	V_{op} (V)	V_{th} (V)	μ ($cm^2\ V^{-1}\ s^{-1}$)	Ref.
HfO_2	Anodiz.	40.1	-1.5	-0.75	0.022	[21]
HfO_2	Sol-gel	20	-2.5	-0.3	0.13	[21]
HfO_2/SiO_2	Sol-gel	3.1/1.7	-1.5	-0.72	0.08	[22]
HfO_2	Sol-gel	40	-5	-3.7	0.035	[212]
HfO_2	Sol-gel	190	-15	-7.46	3.8	[225]
HfO_2	ALD	50	-3	-0.87	0.23	[208]
HfO_2/Al_2O_3	ALD	10/10	-5	-1.89	0.0011	[213]
HfO_2	ALD	40	-2	-1.2	0.02	[221]
HfO_2	ALD	12	-1	-0.4	0.01	Ours
HfO_2	Sputt.	400	-12	0	0.02	[209]
HfO_2	Sputt.	300	-5	-1.62	0.09	[211]

* Dielectric deposition method. Abbreviations: sputt., sputtering; anodiz., anodization; ALD, atomic layer deposition.

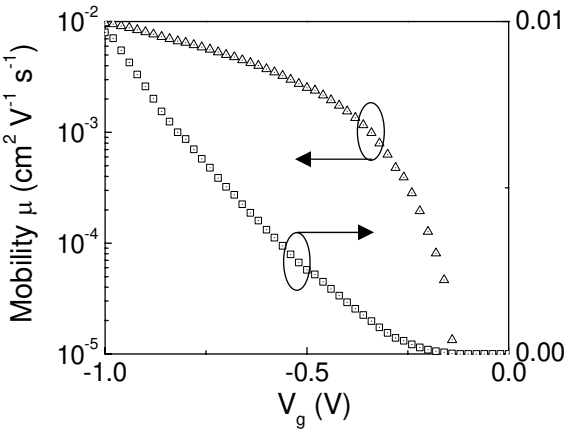


Figure 5-5. Gate voltage dependent mobility of pentacene FETs using HfO_2 as gate dielectric without the plasma treatment, calculated from the transfer characteristics in Fig. 5-2b at $V_{ds} = -1\ V$.

As shown in Fig. 5-5, the mobility of our pentacene FETs with bare HfO_2 presented a pronounced gate voltage dependence, which has already been reported in various OSCs and can be analyzed in the frame of a multiple

trapping and release (MTR) model.[122] A striking feature revealed by Fig. 5-5 was a nonsaturation behavior of mobility at $V_g = -1\,V$. Therefore, it was expected that the carrier mobility can be further improved by increasing V_g.

Fig. 5-6a shows a series of $I_{ds} - V_g$ curves of pentacene FETs using plasma-treated HfO_2 with various exposure time t_e. A dramatic improvement of I_{ds} by about one order of magnitude was observed in plasma-treated devices. This increase would be ascribed to: (i) a shift in threshold voltage, presented in Fig. 5-6b; (ii) an enhancement of field-effect mobility; or (iii) a change in pentacene growth mode on HfO_2, resulting in different molecule orientation and morphologies, as shown in Fig. 5-8 and Fig. 5-13.

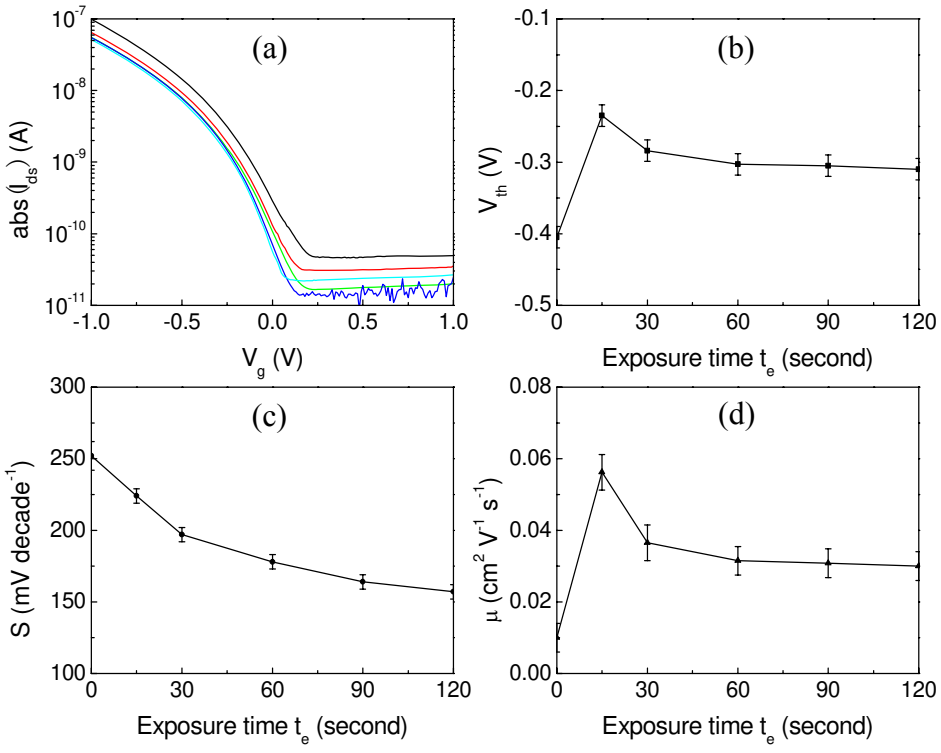


Figure 5-6. (a) $I_{ds} - V_g$ curves of pentacene FETs using oxygen plasma-treated HfO_2 with various exposure time: 15 s (black line), 30 s (red line), 60 s (green line), 90 s (blue line) and 120 s (cyan line). (b) Dependence of threshold voltage V_{th}, sub-threshold swings S, and field-effect mobility μ on the exposure time t_e.

As we can see, $I_{ds} - V_g$ curve moved toward the positive direction with a very short exposure time (e.g. $t_e = 15\ s$) and then shifted back to the negative side gradually, indicating that V_{th} was dynamically tuned. According to eq 5-2, it can be known that the density of interface traps was being changed during the exposure to oxygen plasma. This feature can be originated from: (i) plasma-induced fixed negative charges trapped at the surface of HfO_2 film, neutralizing positively charged states that contributed to the large initial negative threshold voltage;[148] and (ii) elimination/re-creation of the interface defects (e.g. the reduction of organic contaminating carbon, shown in the inset of Fig. 5-3) by oxygen radicals. At $t_e = 15\ s$, the value of V_{th} was minimized. An estimated value of $N_{tr} (= C_i V_{th}/q)$ was around $6.1 \times 10^{11}\ cm^{-2}$. When the exposure time t_e increased, additional trapping states would be induced, giving rise to an increase in V_{th}, as shown in Fig. 5-6b. However, the RMS roughness of HfO_2 was hardly affected up to 240 s indicated by the AFM images (data not shown). With $t_e = 240\ s$, a V_{th} of $-0.47\ V$ can be obtained (data not shown), which was even more negative than that of devices with as-deposit HfO_2. A similar trend was also observed in the behavior of μ_{sat}. It was maximized at $t_e = 15\ s$ with a value of $0.056\ cm^2\ V^{-1}\ s^{-1}$ and sustained at $0.03\ cm^2\ V^{-1}\ s^{-1}$ up to several minutes. We ascribed the enhanced mobility to the ultraclean HfO_2 surface with increased surface energy. As mentioned before, the surface energy of gate dielectric played an important role in influencing the morphology and molecular orientation of OSCs and thus the electrical properties of OFETs.[223] The ultraclean surface of HfO_2 with increased surface energy would increase the mean diffusion length of pentacene molecules, resulting in micron-size dendritic grains that contributed

to the improved carrier mobility because of the effect of grain boundaries.[226] Interestingly, pillar-like grains occurred indicated by dotted ovals on plasma-treated substrates, as shown in Fig. 5-13b-d. The density of these pillar-like grains would slightly increase with the increase of exposure time, which gave rise to a more pronounced RMS roughness of pentacene film. Their effect on the electrical performance will be studied through the contact resistance in future. Another critical feature was that subthreshold slope S decreased gradually with increasing t_e. The lowest S of 157 mV decade^{-1} was achieved at $t_e = 120$ s, which was comparable to that of amorphous silicon FETs.

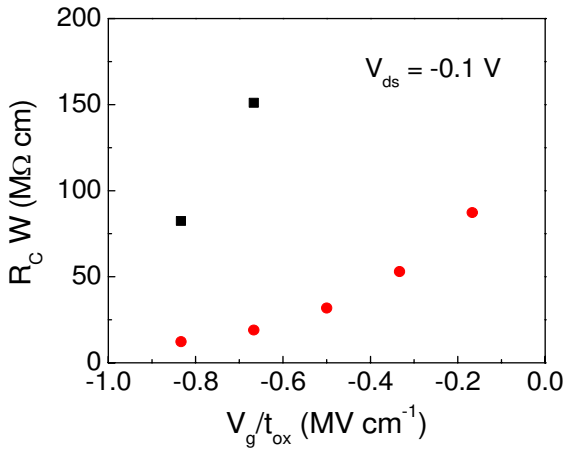


Figure 5-7. Contact resistance ($R_C W$) versus V_g/t_{ox} for pentacene FET devices with (black square) as-deposited and (red circle) 15 s plasma-treated HfO_2. Device resistances are calculated in the linear regime from the slope of the $I_{ds} - V_{ds}$ characteristics.

However, our devices suffered from an unusually high contact resistance R_C, shown in Fig. 5-7, which was also significant for such low gate voltage. Normally, it was observed in nanoscale OFETs, resulting in a nonideal I – V characteristics (e.g. a superlinear behavior).[227,228] This has also been seen in micron scale devices at low source-drain voltages and is known as current crowding.[229] As mentioned previously, the value of μ_{sat} determined from our

pentacene crystal were 10 times smaller than that of pentacene films deposited on SiO_2.[43,71] Such low μ_{sat} value may result from highly resistive contacts associated with Au-pentacene junctions, hindering the charge injection from the source, but also probably reflected a relatively high concentration of trap states in our pentacene film that can decrease the average mobility of free carriers by serving as scattering centers. Despite of the high contact resistance, it would not conceal the effect of oxygen plasma treatment on the other electrical parameters. Improvements in these characteristics can be expected from the use of purified materials as well as the deposition condition. Our future work will examine this possibility. On the other hand, the off-state current of pentacene FET devices (at $V_{ds} = -1$ V and $V_g < V_{th}$) slightly varied by almost an order of magnitude between different oxygen plasma treatment, but was well below 100 pA, as shown in Fig. 5-6a. The off-state current shall be contributed by FN tunneling from source to drain through the channel and FN tunneling from drain to gate through the oxide. The change of off-state current with exposure time seemed to be related to the variation of FN tunneling promoted by oxide traps generated during plasma exposure. The overall performance has been improved by plasma treatment on the gate surface.

Fig. 5-8 presented the X-ray diffraction pattern of a 500 Å pentacene film deposited onto HfO_2 with/without plasma treatment, revealing the crystal type and molecule orientation. All films were found to be highly ordered showing sharp diffraction peaks. On any growth conditions, a 5.73° diffraction peak was the strongest, which indicated that the major component of pentacene film is the thin film phase with a 15.4 Å interplanar spacing of (001).

However, two additional peaks emerged when pentacene deposited on plasma-treat HfO_2, indicating the presence of another phase, shown by the dash line. The stronger peak sat at $19.2°$, suggesting that a significant fraction of pentacene molecules are lying flat with an interplanar spacing of 3 Å. Such phase was also not detected by XRD for pentacene deposited on HMDS-treated HfO_2 (Fig. 5-9) and PS-treated HfO_2.[210] Wang et al. reported that the presence of more than one phase in pentacene can cause highly defective films[7] leading to the lower μ_{sat} for OFETs using bare HfO_x compared to those using PS/HfO_x,[210] whereas Shtein et al. found that such flat-lying pentacene molecules implied the improved adhesion of pentacene to the substrate, which was observed for pentacene grown on the surface of bare and OTS-treated SiO_2 under various substrate temperatures and depositing rates.[133] In view of the changes in pentacene molecular orientation accompanying the increase in μ_{sat}, it seems unclear what role the in-plane π-system overlap plays in the field-effect transistor behavior.

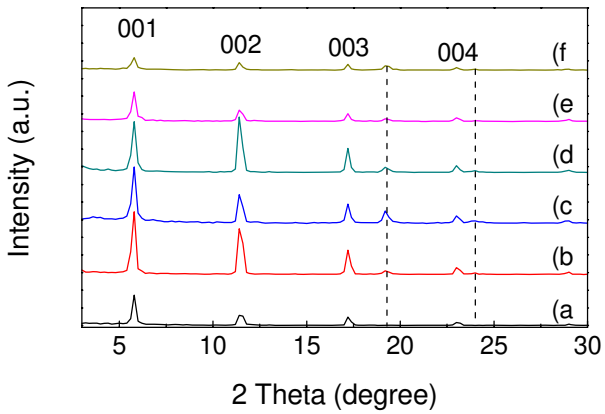


Figure 5-8. X-ray diffraction patterns of pentacene films deposited on plasma-treated HfO_2/Si substrates with different exposure time t_e: (a) 0 s, (b) 15 s, (c) 30 s, (d) 60 s, (e) 90 s, and (f) 120 s.

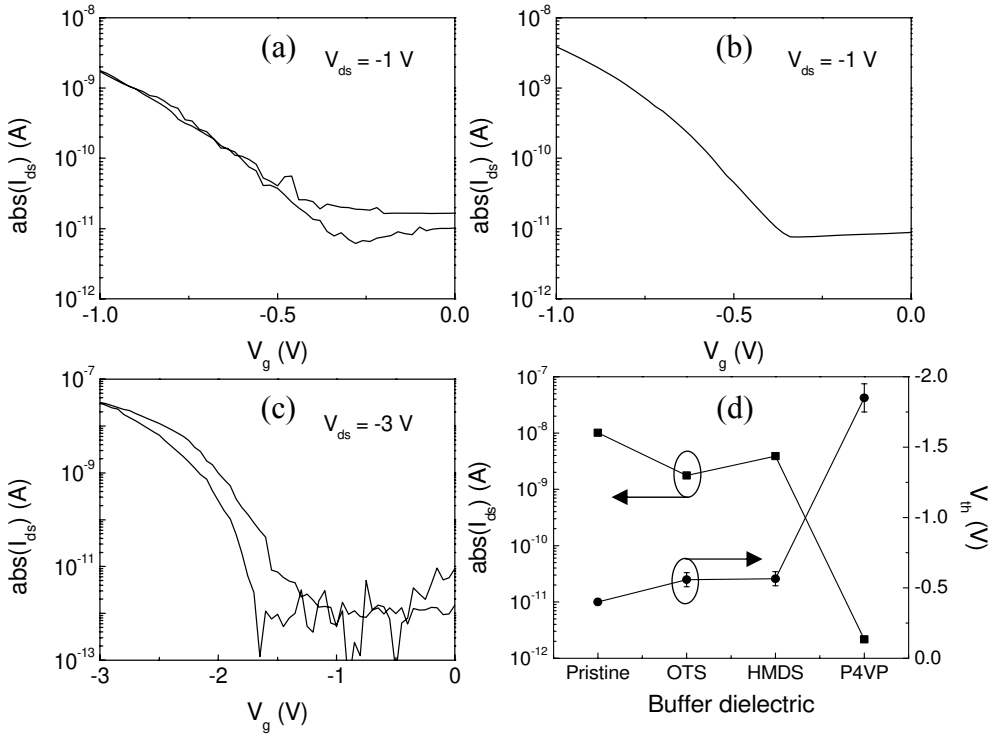


Figure 5-9. $I_{ds} - V_g$ curves of pentacene FETs with HfO_2 gate dielectric treated by (a) OTS, (b) HMDS, (c) cross-linked P4VP. (d) Summary of extracted output current I_{ds} at $V_g = V_{ds} = -1\ V$ and the threshold voltage V_{th} of pentacene FET devices for different SiO_2 treatments.

Pentacene FET devices fabricated on chemically modified HfO_2 were also investigated, shown in Fig. 5-9. In the case of devices with SAM-modified HfO_2 gate dielectric, the threshold voltage V_{th} of these devices was slightly increased, as compared to that of devices with bare HfO_2. Taking no account of the density of interface traps N_{tr}, the value of V_{th} is inversely proportional to C_i according to eq 5-2. Because of the low dielectric constant (despite of the ultrathin thickness of SAMs), the series total capacitance would be lowered, therefore, a larger gate voltage (i.e. larger V_{th}) was needed to turn the device on. It was more remarkable by the use of thick polymeric P4VP, giving rise to a V_{th} of as large as -1.85 V, as the thickness of low-κ P4VP buffer dielectric already exceeded that of HfO_2. On the other hand, the output current I_{ds} was not enhanced, even lowered by using SAMs modification, ascribing to the

reduced ordering of pentacene molecules on SAMs-treated HfO_2, suggested by the lowered diffraction peaks shown in Fig. 5-10. Therefore, it suggested that the use of plasma treatment on our ultrathin ALD grown HfO_2 is an effective method to improve the electrical performance of pentacene FET devices.

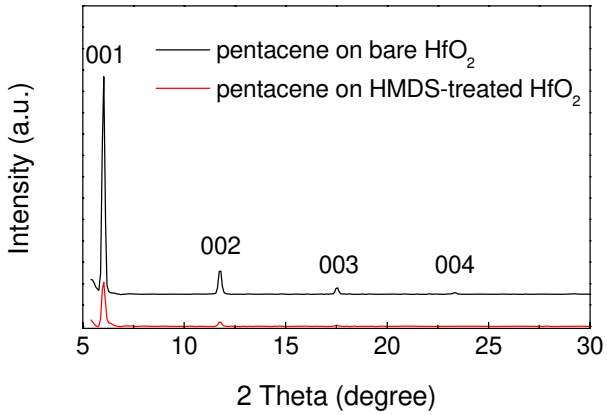


Figure 5-10. X-ray diffraction patterns of pentacene films deposited on (black line) bare and (red line) HMDS-treated HfO_2/Si substrates.

Here the reliability/stability of pentacene FET devices with plasma-treated HfO_2 was also investigated through applying a gate voltage bias stress continuously. Fig. 5-11a shows the time-dependent decay of the on-current I_{ds} under a dc bias stress ($V_{ds} = -0.5$ V and $V_g = -1$ V), which could measure the mobile hole concentration in the accumulation layer. For all devices, I_{ds} decreased rapidly at first few seconds and then continued to decrease at a slower rate, whereas the device with as-deposited HfO_2 suffered from the most severe degradation of I_{ds} after 1000 s bias stress measurement, as shown in Fig. 5-11b. It was mainly due to the trapping of holes, shifting the threshold voltage to a more negative value. For devices with as-deposited HfO_2, the trapping of holes was ascribed to the following factors: (i) organic residues and other contaminants acting as trapping states near the surface of the dielectric, (ii)

water molecules-related hole traps,[167] and (iii) structural defects (e.g. oxygen vacancies) and grain boundaries of the semiconductor. Plasma treatment can effectively reduce the amount of organic residuals, nevertheless residual carbon species (inset of Fig. 5-3) was still found over the film, and also diminished the oxygen vacancies in the HfO_2 film that would cause the charge trapping and render remote Coulomb scattering of carriers in the channel,[230,231] leading to a better bias stress stability and higher mobilites (Fig. 5-6d).

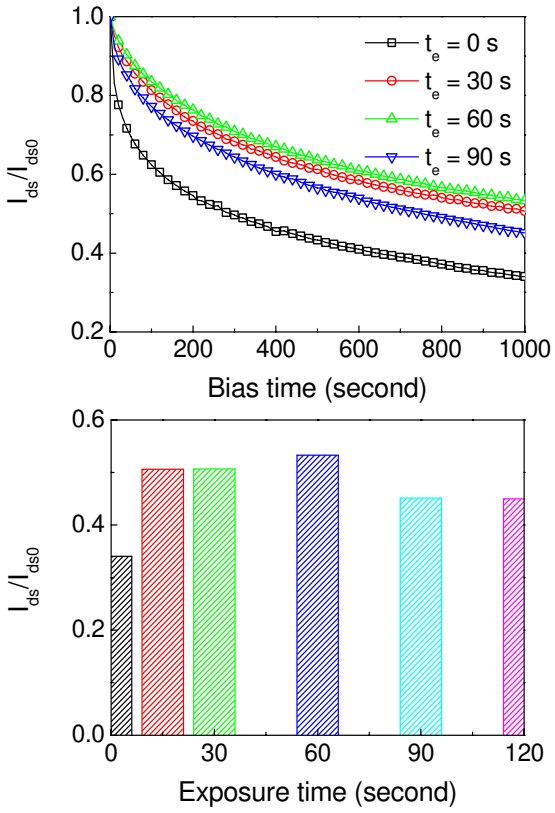


Figure 5-11. (a) Time-dependent decay of I_{ds} of pentacene FETs with as-deposite HfO_2 (black square) and plasma-treated HfO_2 for 30 s (red circle), 60 s (green triangle) and 90 s (blue down triangle) under continuous dc voltage biases of $V_{ds} = -0.5\ V$ and $V_g = -1\ V$. (b) Dependence of I_{ds}/I_{ds0} after 1000 s bias stress on the exposure time t_e.

However, devices with plasma-treated HfO_2 still exhibited 50% decay of I_{ds} after 1000 s bias stress measurement. In these devices, mechanism (ii)

would dominate due to the presence of polar functional groups (e.g. –OH) that rendered the surface super hydrophilic, although the access of moisture to grain boundaries at the interface of gate dielectric in the channel would be slightly reduced due to the increased grain size. Improvement in stability was expected when devices operated in N_2-filled environment avoiding oxygen and moisture. Recovery of the bias stress at room temperature normally took several days, but illumination due to the generation of mobile electron-hole pairs was proved to speed up the recovery, indicating that a fraction of holes were deeply trapped in the semiconductor (bulk or interface).

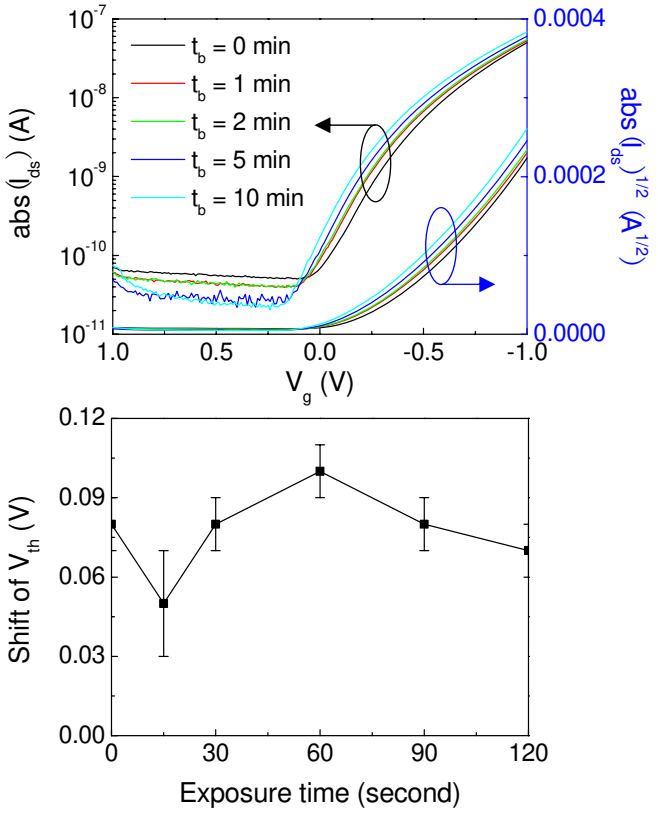


Figure 5-12. (a) $I_{ds} - V_g$ curves of pentacene with $60\ s$ plasma-treated HfO_2 after $0\ min$ (black line), $1\ min$ (red line), $2\ min$ (green line), $5\ min$ (blue line) and $10\ min$ (cyan line) dc voltage bias biases of $V_{ds} = -0.5\ V$ and $V_g = 1\ V$. (b) Dependence of V_{th} shift after $10\ min$ dc voltage biases of $V_{ds} = -0.5\ V$ and $V_g = 1\ V$ on the exposure time t_e.

A positive gate bias ($V_{ds} = -0.5$ V and $V_g = 1$ V) was also applied to induce a positive shift in threshold voltage and bias stress time t_b spanned from 1 to 10 min, as shown in Fig. 5-12a. An interesting feature was that the off-current in the depletion region gradually decreased and threshold voltage shifted to more positive value with the increase of t_b, indicating the trapping of electrons due to the presence of a large amount of surface hydroxyl groups[158] and oxygen vacancies in plasma-treated HfO_2 film.[230] A shift of as large as 0.1 V in the devices with 60 s plasma-treated HfO_2 was observed at $t_b = 10$ min, corresponding to transferred electron density of 2.6×10^{11} cm^{-2}. However, the mobility, the on/off ratio, and the subthreshold slope are minimally affected by the gate bias stress. Fig. 5-12b presents the shift of V_{th} after 10 min bias stress as a function of exposure time t_e. Obviously, there were two turning points at 15 s and 60 s, respectively. The device with 15 s plasma-treated HfO_2 appeared most resistive to the positive gate bias with a minimum ΔV_{th} of $\sim$0.05 V. It can be said that the residues and other contaminants can be effectively removed and possibly partial oxygen vacancies can also be compensated by oxygen molecules within 15 s, when the pentacene film presented the strongest diffraction peak shown in Fig. 5-8, contributing to lower threshold voltage and improved field-effect mobility, and at the mean time the density of hydroxyl groups created during plasma treatement that captured electrons was still low. Interestingly, the shift in threshold voltage decreased again at $t_e \geq 90$ s, which was analogous to that of devices using as-deposit HfO_2. We believed that it was correlated with the density of surface hydroxyl groups and re-induced fixed positive charges on the surface and/or in the bulk of HfO_2 film.

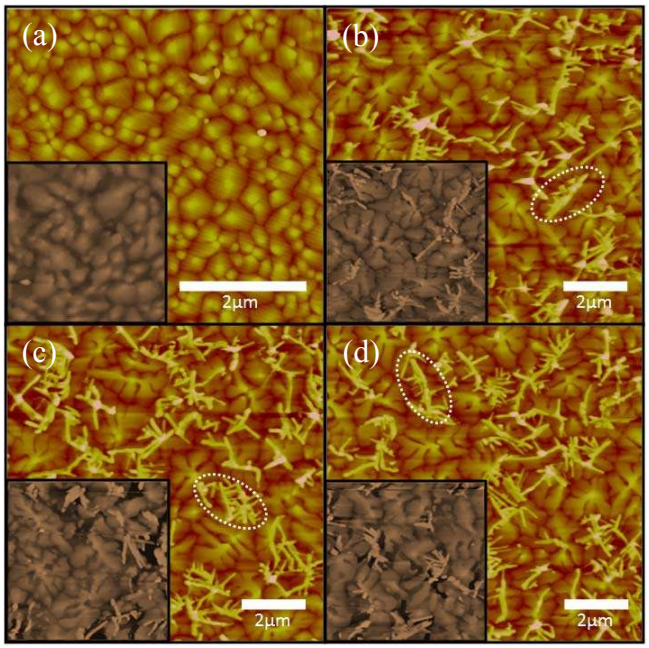


Figure 5-13. Topography of pentacene films deposited on (a) 0 *s, (b)* 30 *s , (c)* 60 *s and (d)* 90 *s plasma-treated HfO_2. The inset shows the corresponding morphologies after* 10 *months' storage in dry box.*

Beyond characterizing the effect of oxygen plasma on grain size and subsequent electrical properties, study on the aging of pentacene films was also carried out in this work. Obviously, the polycrystalline pentacene films became more disintegrated with increasing exposure time for oxygen plasma after 10 months storage in the air, as shown in the inset of Fig. 5-13. It is known that long time exposure to oxygen plasma resulted in a very large surface energy of HfO_2, increasing the mean diffusion length of pentacene molecules. However, the nucleation of pentacene islands was also restricted by the evaporation rate and substrate temperature. A larger surface stress was believed to act on pentacene crystals, especially at the edge between the tilted pentacene molecules and the flat-lying molecules, when pentacene was deposited on plasma-treated HfO_2 film. A schematic diagram for the degradation process of pentacene crystals under atmospheric condition was shown in Fig. 5-14. We believed that this degradation process of pentacene film was enhanced by the

participation of oxygen and moisture due to the hydrophilic HfO_2 surface. Post-thermal treatment $(45-60\,℃)$[232,233] is thus of use to rearrange the pentacene molecules to release the surface stress and thus can minimize such weathering effect. Besides, precaution, e.g. encapsulation,[35-37] shall also be helpful to ensure the environmental stability of semiconductor films as well as the operational stability of devices.

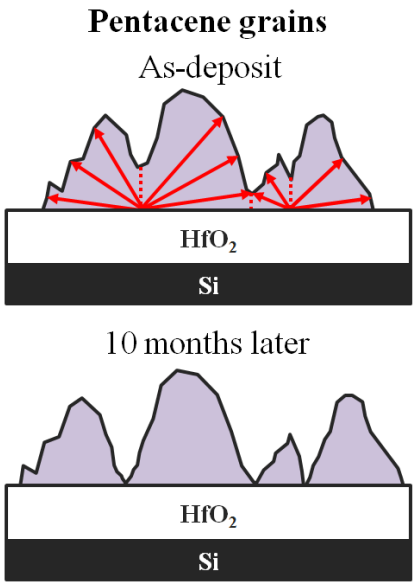


Figure 5-14. Schematic illustration of the degradation process of micron-size polycrystalline pentacene grains. The dash line and arrows indicate the disintegrating region and surface stress, respectively.

5.4 CHAPTER SUMMARY

In conclusion, we have fabricated pentacene FETs operated at a low voltage of -1 V using high-κ HfO_2 gate dielectric grown by ALD at a temperature of 250 °C. The unit capacitance of 12 nm-thick HfO_2 was 415 nF cm^{-2} at a frequency of 1 kHz. The influence of oxygen plasma treatment on the electrical properties of pentacene FETs, such as threshold voltage (V_{th}), sub-threshold slope (S) and field-effect mobility (μ_{sat}), was thoroughly

investigated. The maximum μ_{sat} of 0.056 $cm^2\ V^{-1}\ s^{-1}$, minimum V_{th} of -0.23 V and on/off ratio of $> 10^3$ was achieved at $t_e = 15$ s. S decreased with the increase of t_e, and a minimum value of 157 $mV\ decade^{-1}$ can be obtained. Negative gate bias stress measurement indicated that the operational stability of devices using plasma-treated HfO_2 was improved within 120 s exposure time in this work due to the removal of organic residues at the HfO_2 surface and oxygen vacancies in the HfO_2 film. However, the device with $t_e = 15$ s showed best immunity to positive gate bias and the worst at $t_e = 60$ s, which we thought depended on the quantity of hydroxyl groups and re-induced fixed positive charges presented on the surface of HfO_2. Finally, we have suggested that the aging of pentacene crystals on plasma-treated HfO_2 under atmospheric condition could be related to surface stress enhanced weathering. In order to improve the environmental and operational stability of devices, post-thermal treatment and/or encapsulation shall be a great choice.

CHAPTER 6: HETEROSTRUCTURE FET DEVICES

6.1 CHAPTER INTRODUCTION

The highest occupied and lowest unoccupied molecular orbital (HOMO and LUMO) energy levels in a semiconducting molecular solid are, in some respects, analogous to the valence and conduction band extrema energy levels in inorganic semiconductors. Several heterostructure devices with inorganic semiconductors have been demonstrated which exploit the differences in such energy levels in different materials in very creative and technologically important ways.[234] Heterostructure lasers, transistors, and light emitting diodes are examples of devices where "Bandgap Engineering" has been proven to be enormously successful. Indeed, the innovative combination of heterostructure and quantum confinement effects has led to new structures and devices which sometimes possess unusual and often superior technological characteristics.[235]

Devices with two or more organic and/or polymeric active materials (possessing different HOMO/LUMO levels) have also been made in the hope of benefiting from the discontinuities in energy levels at the heterointerface. In OLEDs, for example, a heterostructure architecture is often used to control the charge balance and confine the injected carriers near the heterointerface (and away from the contacts) to improve light emission efficiency.[236] In organic photovoltaic cells (OPVCs), an optimized heterointerface can make the exciton dissociation effectively into free charge carriers and hinder their recombination, subsequently enhance the power conversion efficiency.[237] By contrast, charge

transport is slightly different in OFETs, which occurs parallel to the active interfaces. However, the application of heterostructure concepts to OFETs also can be very useful and have been able to realize some novel device effects in heterostructure FETs.[55,178] For example, two active materials that transport opposite carrier types (i.e. p-channel and n-channel semiconducting materials) have been used in the same device to achieve ambipolar (sometimes also referred to as bipolar) behavior, because the complementary approach to fabricate integrated circuits (ICs) offers low power dissipation, wide noise margins and high robustness, as compared to the unipolar approach (either holes or electrons as dominate charge carriers in OFETs). From a scientific perspective, the ability to realize ambipolar transistors also enables new ways to improve the understanding of the physics of these organic devices. Dodabalapur and co-workers firstly proposed and demonstrated bilayer FETs by employing the known hole-conducting α-hexathienylene (α-6T) and the electron-conducting C_{60}, and both hole and electron transport was observed in these devices, although with lower mobilities than those for each material on its own.[178,238] Moreover, direct comparison of hole and electron transport within the same device is important as well, and the recombination of opposite charge carriers and light emission within the transistor channel are expected to take place. By carefully choosing the materials according to the relative position of their HOMO and LUMO levels as well as the deposition order, Dinelli et al. achieved a balanced electron/hole mobility (ca. 0.03 $cm^2\ V^{-1}\ s^{-1}$) and observed the light emission from the combination of α,ω-dihexylquarter-thiophene (DH4T) and PTCDI-$C_{13}H_{27}$.[239]

On the other hand, the first layer (close to the gate dielectric) in the heterostructure devices can also influence the interaction between the molecules in the second layer and the substrate (sometime acting as an alignment layer), therefore promote the packing mode of the second layer and enhance the device performance (unipolar transport). Itaka et al. showed that the use of a substrate covered with an atomically flat pentacene monomolecular layer can drastically increase the crystallinity of C_{60} film and increase the field-effect mobility of C_{60} FETs to 4.9 $cm^2\ V^{-1}\ s^{-1}$,[107] while similar crystallization effect in rubrene films grown on pentacene buffers was observed.[240] Later, Hu et al. further studied the effect of pentacene buffer layer grown at the surface of a pre-rubbed polyvinylalcohol (PVA) on the electrical performance of rubrene FETs. It was found that the highest hole mobility of rubrene FETs was measured at 45° off the rubbing direction, indicating a favourable C–H π interaction between an oriented pentacene layer and the rubrene layer.[241] At the meantime, Song et al. demonstrated that by inserting 3.5 nm vacuum deposited film of *para*-sexiphenyl (*p*-6P) between phthalocyanato tin(IV) dichloride ($SnCl_2Pc$) film and SiO_2/Si substrate, not only high mobility of $SnCl_2Pc$ FETs (0.3 $cm^2\ V^{-1}\ s^{-1}$) but also the good device stability in air can be achieved.[242] In addition, FET devices with low pinch-off voltage ($V_{po} = \sim 5\ V$) was demonstrated by introducing acceptor layers (e.g. 3 nm TCNE) on thick thermal silicon oxide (ca. 500 nm) as gate insulator due to charge transfer between pentacene and TCNE.[243] At the same time, the same group reported that by using the bilayer structure of PVK and pentacene, the control of threshold voltage V_{th} of a device can be realized because of the charge trapping mechanism in PVK layer, which would be critical for the reliability of

enhanced ICs.[246] In the case of silicon metal-oxide-semiconductor field-effect transistors, V_{th} can be adjusted by doping the channel region and/or a second gate bias to tune the electrostatic potential and the carrier density in the channel.[49] The same techniques have not yet been well developed for OFETs, whereas great efforts have been made to develop a few methods to achieve the control of threshold voltage.[141,154,244-247] Nevertheless, little research has been done on employing light illumination as a control apparatus to V_{th}, which will bring about light-controlled OFETs. Although a shift in V_{th} upon light illumination was observed, it was very difficult to strictly control V_{th} in a wide range for a single OFET device.

Previously, chargeable gate dielectrics (sometimes referred to as "electrets") were employed to study the effect of photo-induced charge transfer on the shift of the field effect onset.[181,248] The memory effect in the FET structure due to the photo-induced charge transfer was firstly studied by Dutta and Narayan.[248] It was found that the negative charges are severely trapped and lie in the deep energy states in the depletion mode after being generated under illumination. Later, the rate of the charge transfer (both holes and electrons) was investigated in detail by Podzorov and Gershenson,[181] which was determined by (i) the flux of photons with energies greater than the LUMO-HOMO gap of an organic semiconductor and (ii) the magnitude of the transverse electrical field applied at the semiconductor-dielectric interface. However, both works focuses on the charge transfer from an active layer to a gate dielectric. In this work, two conjugated polymer, poly(9,9-dioctylfluorene) (PFO) and Poly(*N*-vinylcarbazole) (PVK), shown in Fig. 6-1a, were selected to form type I heterojunction (straddling gap) with pentacene to study the charge

transfer effect, which have been widely investigated as a hole-transport material in the fabrication of blue LEDs,[249-252] and the diagram of energy levels of PFO/ pentacene (or PVK/pentacene) was similar to that of PVA/P3AT or Parylene/rubrene. The use of PFO was due to the presence of the deep electron trapping states and its high room-temperature hole mobility with weak field dependence.[249] Besides, PFO will emit polarized light if they can be oriented, as it is an emissive liquid-crystal polymer.[253] Such a polarized emitter is of great interest for use as a backlight in a liquid-crystal display since it provides the replacement for the normal backlight and polarizer combination. For PVK, bistable resistance switching based on trapping and detrapping of majority carriers using PVK films was demonstrated, which revealed their nonvolatile memory nature.[254] PVK was also used to tune the flat-band voltage (V_{fb}) in pentacene FETs due to the charge trapping mechanism.[246] For these reasons, high performance OFET devices with a pentacene active layer and nanostructured PFO (or PVK thin film) were fabricated to study charge transport along and charge transfer across the heterointerface. Under negative gate bias ($|V_g| > |V_{th}|$) in the dark condition, these FETs presented conventional p-channel behavior and operate in the enhancement mode, as the field-induced carriers are expected to be confined in the pentacene layer due to the HOMO offset between PFO or PVK ($\mathrm{LUMO} = -2.3$ eV and $\mathrm{HOMO} = -5.8$ eV)[249] and pentacene ($\mathrm{LUMO} = -3.2$ eV and $\mathrm{HOMO} = -5.1$ eV, see Fig. 6-1b).[177,255] When it is under illumination, non-equilibrium charge carriers (holes and electrons) are generated and separated under the influence of the electric field. By applying proper positive gate bias, i.e. operating in the depletion mode, electron carriers can be trapped by the nanostructured PFO (or

PVK) and the interface, causing a shift in the threshold voltage. As we will show hereinafter, by varying the starting source-gate voltage V_{g_start} in the off-to-on transfer characteristics, V_{th} can be tuned through the effect of photo-induced charge transfer. After that, the hysteresis behavior in such hetero-junction FET devices was also systematically investigated at various bias conditions under light illumination. It was found that the hysteresis phenomenon presented strong bias-dependence and a maximum hysteresis window ΔV_{th} larger than $80\,V$ was obtained from the cyclic transfer characteristics, on which both electron and hole trapping have an impact. Detailed analysis for these results and a possible mechanism are discussed.

6.2 EXPERIMENTAL DETAILS

For the fabrication of heterostructure FET devices using pentacene and polymeric light-emitting materials, a heavily doped silicon wafer with a 200 or 500 nm thermally grown oxide layer was used as the common gate and supporting substrate. PFO (see Fig. 6-2a) was deposited on the wafer after a wafer-cleaning process. It consisted of $10-15$ nm nano-structured PFO dispersed in PMMA, referred as PFO&PMMA (PFO-FETs1), and for PFO-FETs2, another 10 nm PMMA film was used to planarize the surface of PFO&PMMA film, while 10 nm pure PFO covered by 10 nm PMMA was employed in PFO-FETs3. PFO&PMMA (or pure PFO) film was spin-coated from 0.2wt% solution in toluene (the ratio of PFO to PMMA is 1) and the nano-structured PFO was formed during the annealing process at 105 ℃ for 10 min on a hotplate under the air ambient. PMMA planarizing layer was spin-coated from chlorobenzene solution and annealed at 105 ℃ for 10 min on the

hotplate to remove the residual solvent. For the fabrication of PVK-FETs, 10 nm PVK (see Fig. 6-2a) was spin-coated from 0.2wt% solution in chlorobenzene and annealed at 120 ℃ for 30 min . The devices were completed by the deposition of 30 nm gold as source-drain contact through the shadow mask after the evaporation of 50 nm pentacene active layer, as shown in Fig. 6-1. For a typical device, the channel length (L) and width (W) of organic transistors were 100 um and 2 mm, respectively. For comparison, the control devices with the same thickness of organic semiconductor and the same L and W were fabricated on bare SiO_2/Si substrates without a PVK (PFO) layer. To characterize absorption spectra, PFO&PMMA (or PFO) film with the same thickness was prepared on the quartz substrate.

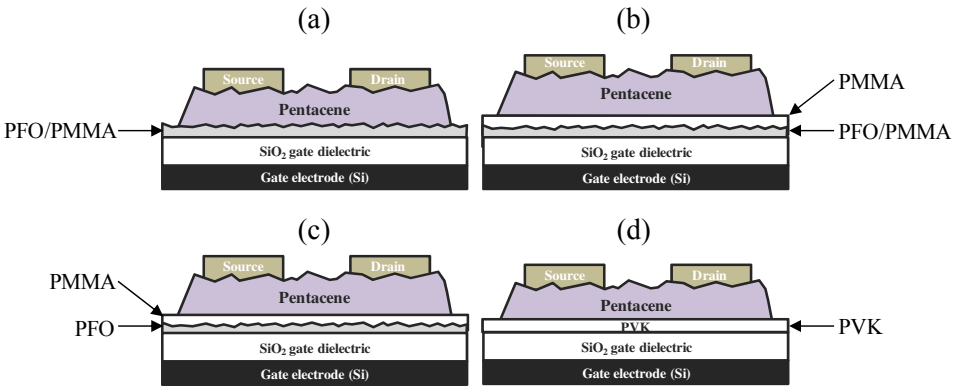


Figure 6-1. Schematic of top-contact OFETs: (a) PFO-FETs1, (b) PFO-FETs2, (c) PFO-FETs3, and (d) PVK-FETs.

To investigate the effect of light illumination on the electrical performance of our devices, the devices were illuminated from the top from a halogen lamp. The characterization of the devices was carried out on a standard probe station with or without light illumination. The light intensity was preset using a neutral density filter. To clarify the charge transfer and trapping mechanism in these devices, a Dongwoo Optron TH3 arc lamp together with a

Dongwoo Optron DM150i monochromator was used to conduct red light illumination at a wavelength of 628 nm. The light was focused to a spot size approximately equal to the area of the device to cover the entire channel with an estimated light intensity of $1\ \mathrm{mW\ cm^{-2}}$. Electrical characteristics were measured using a Keithley 4200 SCS semiconductor parameter analyzer with 100 ms hold time and 100 ms delay time under ambient condition at room temperature. Unless other specified, the gate bias sweep direction was from positive to negative at 1 V steps (and back to positive in the part of studying the hysteresis behavior). AFM images were obtained using a Nanoscope IIIa AFM (digital instrument) in tapping mode. Absorption spectrum was measured at room temperature using a Shimadzu UV-VIS spectrometer.

6.3 RESULTS AND DISCUSSION

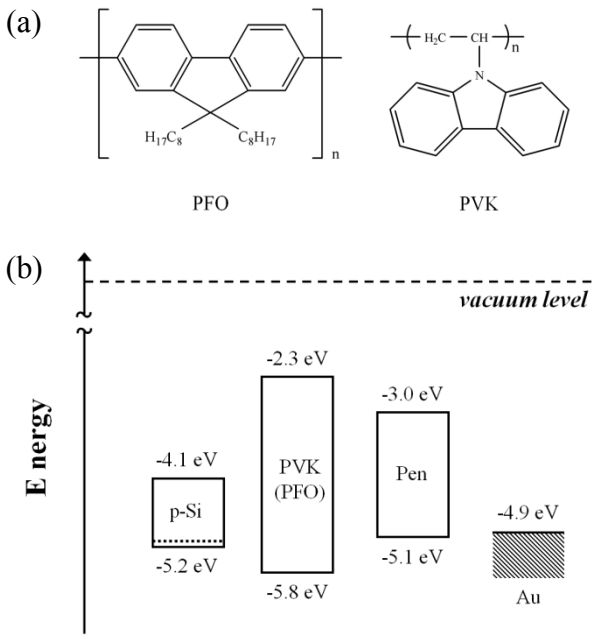


Figure 6-2. (a) The chemical structures of PFO and PVK; (b) Energy levels (HOMO and LUMO) of PVK (PFO) and the work function of heavily p-doped silicon and Au.

Fig. 6-3 shows the output and transfer characteristics of p-type pentacene FETs, where the source-drain currents $|I_{ds}|$ are plotted against the gate voltage V_g in a logarithmic scale, at a constant source-drain voltage of $V_{ds} = -100$ V for PFO-FETs1. I_{ds} does not begin to rise until V_g exceeds 100 V, indicating an extremely large threshold voltage due to the presence of a large amount of trapping states. At $V_g = -150$ V, the value of I_{ds} was smaller than 40 nA and gradually decreased with the increase of V_{ds}. It means that the field-induced holes can be transferred from pentacene into PFO and some would be trapped under such high transverse electrical field, although there is a large band-gap offset ($\Delta E_{HOMO} = 0.7$ eV) between PFO and pentacene, shown in Fig. 6-2b.

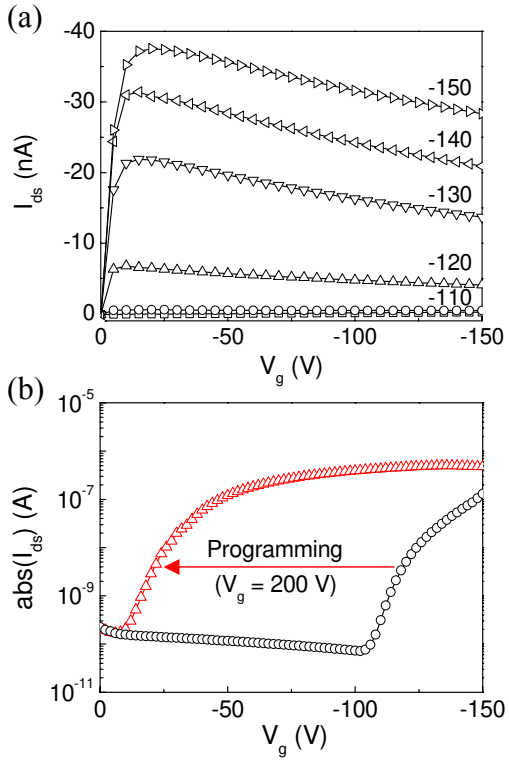


Figure 6-3. (a) Output characteristics in dark condition. (b) Transfer characteristics of PFO-FETs1 with 500 nm SiO_2 at $V_{ds} = -100\,V$, where $V_g = 200\,V$ for 30 s was applied at $V_{ds} = 0\,V$ under visible light illumination for inducing the shift in V_{th}.

From linear curve fitting to the data of $\sqrt{I_{ds}}$ versus V_g in the saturation region (not shown here), V_{th} is obtained as the intercept to the X-axis of the linear fitting curve, whereas field-effect mobility μ_{sat} is derived from the slope. The evaluated values of the mobility μ_{sat} V_{th} and on/off current ratio are 0.028 $cm^2\ V^{-1}\ s^{-1}$, -110 V and 10^3, respectively. By applying light illumination on the device at $V_g = 200$ V for 30 s, the entire transfer curve was shifted to the positive side. The shift of the threshold voltage can be attributed to the trapping of photo-generated electrons and neutralize the positively charged states that contribute to the large initial negative threshold voltage. Therefore, the transferred carrier density Δn can be estimated by the follows:

$$\Delta n = \frac{Q_{trap}}{q} = \frac{C_i \Delta V_{th}}{q} \tag{6.1}$$

where Q_{trap} is the amount of trapped charges and q is the charge of electron. The calculated Δn was ca. 3.75×10^{12} cm^{-2}. It seems that the nanostructured PFO played as charge-trapping centers like silicon nanoparticles (NPs) distributed in the gate oxide.[256] In our case, the effect of field-induced electrons on inducing the shift of V_{th} under positive gate bias was suppressed because of (i) the low electron carrier density in the p-type pentacene layer and the large electron injection barriers (ii) between pentacene and Au and (iii) between pentacene and PFO, shown in Fig. 6-2b. However, by applying visible light illumination, the photo-generation process produced excess high-energy electron carriers, which was an important mechanism of boosting the amount of trapped electrons in nanostructured PFO and the interface, resulting in a significant shift of V_{th}. The calculated mobility was 0.026 $cm^2\ V^{-1}\ s^{-1}$, which was in good consistence with that obtained in the dark condition.

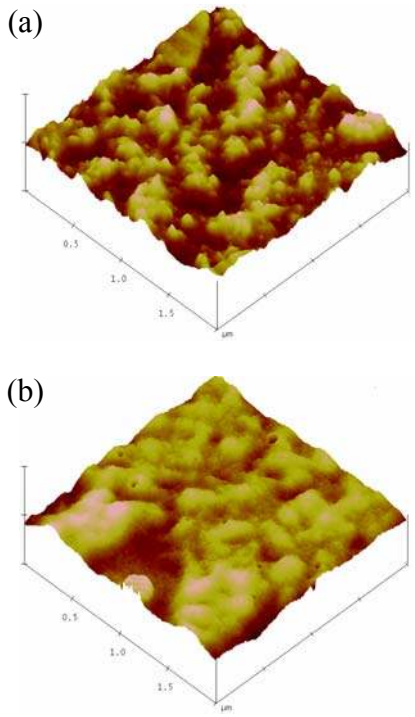


Figure 6-4. Atomic force microscope images of surfaces of polymer: (a) PFO&PMMA spin-coated on SiO_2 surface ($R_q = 4\ nm$), (b) PMMA film planarizing PFO&PMMA ($R_q = 1.5\ nm$). Data scale is $50\ nm$ and R_q represents RMS roughness.

Obviously, the obtained performance of PFO-FETs1 was not satisfying, e.g. low mobility and terribly large threshold voltage. This might be due to the rough interface between the pentacene and the PFO&PMMA film, as shown in Fig. 6-4a, since PFO tends to crystallize to form nanostructures during annealing process. This rough interface brings a large amount of interfacial states that trap charge carriers, contributing to the large negative threshold voltage. Besides, the charge transport in the accumulation region became worse due to the charge scattering effect, thereby deteriorating the field-effect mobility. In order to improve the surface condition, a 10 nm-thick thin PMMA layer was employed for planarization, shown in Fig. 6-4b. The electrical characteristics of PFO-FETs2 in the dark condition were presented in Fig. 6-5a. The device performance was greatly improved by the introduction of a 10 nm

PMMA buffer layer, giving rise to a mobility of 0.35 $cm^2\,V^{-1}\,s^{-1}$, V_{th} of -15 V and an on/off ratio of $> 10^5$.

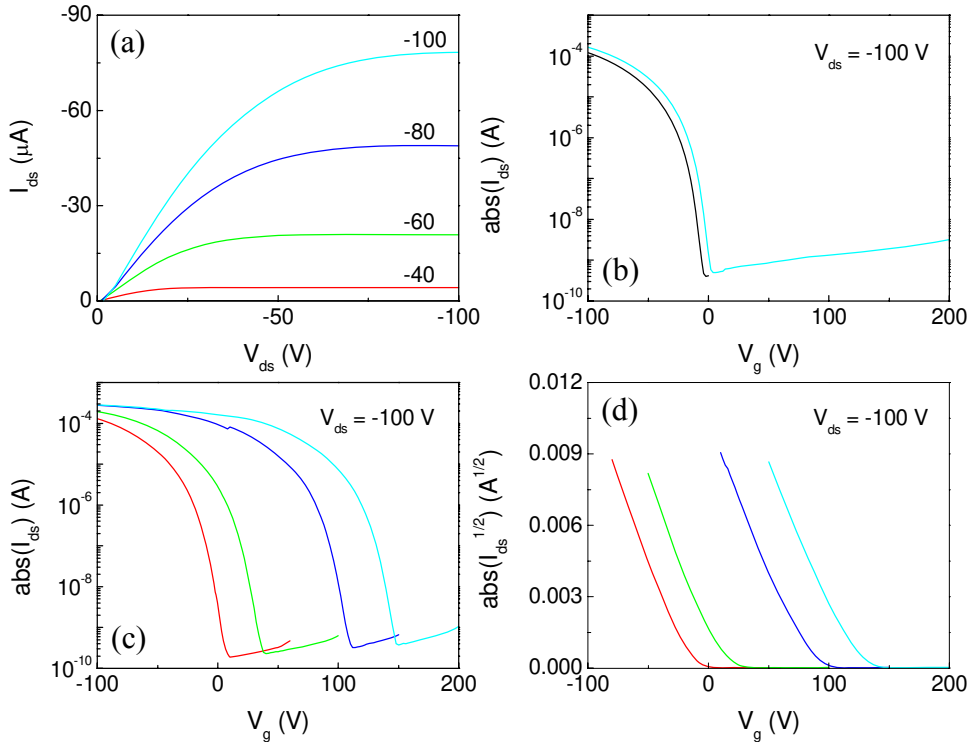


Figure 6-5. (a) Output characteristics of PFO-FETs2 with 500 *nm* SiO_2 *in dark condition. (b) Transfer characteristics in dark condition. (c) Transfer characteristics under illumination with various* V_{g_start}*:* 60 *V (red line),* 100 *V (green line),* 150 *V (blue line) and* 200 *V (cyan line). (d)* $I_{ds}^{1/2}$ *vs* V_g *curves under illumination.*

Interestingly, by varying the starting gate voltage V_{g_start} from 0 to 200 V in the off-to-on transfer curve to study charge transfer across the heterointerface in the dark condition, a shift in V_{th} (i.e. ΔV_{th}) of 6 V was obtained, namely, V_{th} varied from -15 to -9 V. Similarly, a small ΔV_{th} also can be observed in PFO-FETs1, when a large V_{g_start} is applied in dark condition (not shown here, due to large device-to-device variation). It indicated that a small amount of field-induced electrons can be injected from pentacene active layer and trapped in nanostructured PFO and the interface, even though

the thin PMMA planarizing layer provided an additional injection barrier for electrons. It is thus expected that when the device is under illumination, the shift in transfer curves would become much clearer due to the participation of photo-excited high-energy electrons. As expected, the transfer curves systematically shifted toward the positive direction with increasing V_{g_start}, by applying light illumination on the channel region, as shown in Fig. 6-5c. It was observed that V_{th} remarkably shifted from -14.6 to 122.5 V when V_{g_start} changed from 60 to 200 V. It should be noted that the photo-induced threshold voltage shift was so significant that the operation mode can be changed from the enhancement mode to the depletion mode.

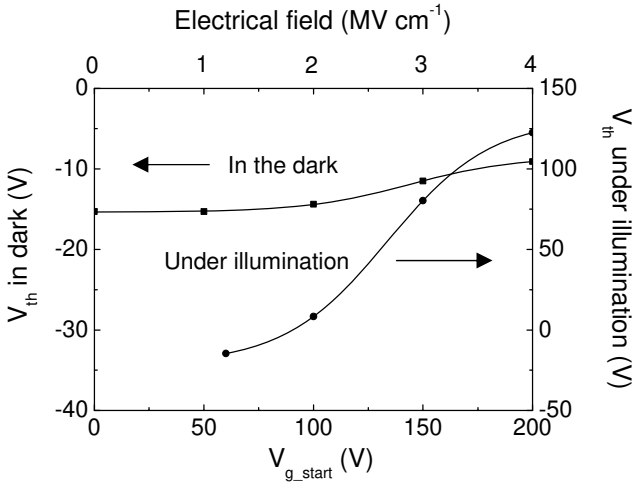


Figure 6-6. V_{th} as a function of V_{g_start} of PFO-FETs2 using $500\ nm$ *SiO_2 as gate dielectric with (circle)/without (square) visible light illumination.*

The photo-induced shift in V_{th} can be explained through the efficiency of the exciton separation in organic semiconductors and the electron trapping in nanostructured PFO and the interface. When light is absorbed, transitions between two molecular orbitals result in excitonic states with weak or strong Coulomb interaction binding electron and hole depending on photon energy.

These paired electrons and holes are separated under proper gate bias. Detailed discussion of charge separation can also be found in studies of organic solar cells.[257-259] As shown in Fig. 6-5c, V_{th} was almost unaffected till $V_{g\_start} = 60$ V under light illumination. However, a conducting channel between the source and the drain began to form even at $V_g = 150$ V by applying $V_{g\_start} = 200$ V, indicating that a large amount of electrons were injected across PFO/pentacen heterointerface and trapped. Based on eq 6.1, the estimated density of transferred charges was ca. 5.14×10^{12} cm^{-2}. These trapped electrons were contributed from the excitonic states dissociated under the transverse electrical field determined by the applied gate bias. The efficiency of exciton dissociation and charge injection from the channel layer depends on the strength of the transverse electrical field and thus the threshold voltage can be set by V_{g_start}, whereas light illumination can be a control parameter for the modulation of the threshold voltage, as seen in response curves in Fig. 6-6.

In order to investigate the stability of a shifted V_{th}, we did the experiment on the lifetime of trapped charges in the dark. The device was programmed with red light ($\lambda = 628$ nm) under a gate bias of 200 V with respect to the short-circuited source and drain electrodes for a duration of 60 s. The considerably enhanced drain current was obtained at zero gate bias at $V_{ds} = -100$ V after programming, showing the "ON" state of the device. On the other hand, by applying an erasing voltage at $V_g = -200$ V at $V_{ds} = 0$ V in the dark to sweep away the trapped electrons, the transistor can be restored to the "OFF" state. The experiment result indicated that the trapped electrons were injected from the pentacene active layer, as the absorption spectrum of PFO mainly occurred in the blue light region (see the inset of Fig. 6-7) due to the

large HOMO-LUMO band-gap while pentacene film was reported to be sensitive to red light.[260] A decay process in I_{ds} exhibited non-exponential characteristics with two distinguishable decay rates: (i) an initial rapid relaxation due to the recombination of closely packed holes and electrons and (ii) a subsequent slower relaxation originated from deeply trapped carriers, depending on the quality of the PFO&PMMA film as well as the PMMA buffer dielectric. A charge storage lifetime of 60 min was obtained in this experiment. Due to the small, but non-zero leakage currents, these device in its current state needs to be refreshed every few hours, which might not reach the requirement for data storage application in organic electronics, but really motivating for the development of OFETs with tunable V_{th} through the photo-induced charge transfer.

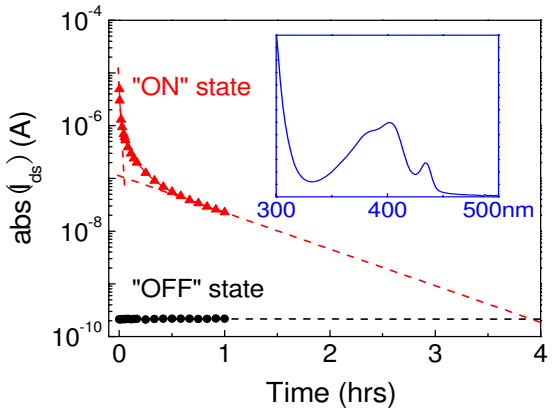


Figure 6-7. Time evolution of I_{ds} of PFO-FETs2 with 500 nm SiO_2 measured at $V_{ds} = -100\,V$ & $V_g = 0\,V$ in the dark. The programming bias ($V_g = 200\,V$ & $V_{ds} = 0\,V$) and erasing bias ($V_g = -200\,V$ & $V_{ds} = 0\,V$) was applied to obtain the "ON"- and "OFF"-current states.

To better understand the photo-induced dynamic charge trapping/ detrapping at the heterostructure devices, here it would be investigated in terms of their hysteresis behavior. Fig. 6-8a shows the output characteristics of PVK-

FETs measured under illumination, exhibiting a typical p-channel operation with slightly wider saturation region. Obviously, the PVK layer does not cause havoc with the FET characteristics of PVK-FETs, this is, the saturation current at $V_g = -40$ V is ca. -20 μA, even slightly higher than that of the control devices without PVK layer.

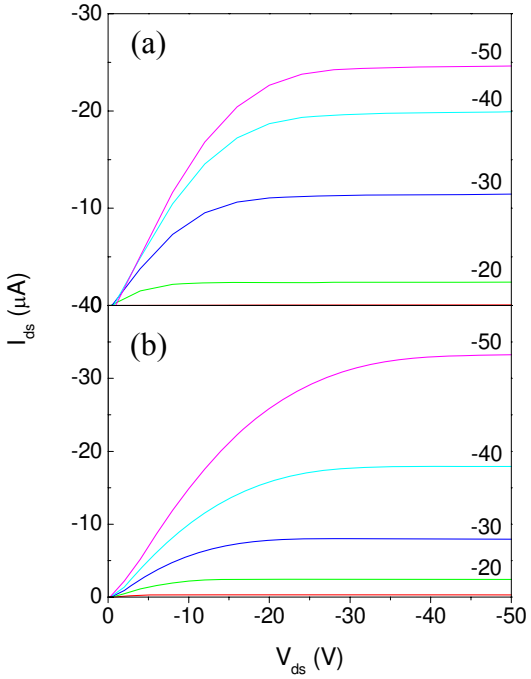


Figure 6-8. Output characteristics of (a) PVK-FETs with 200 nm SiO_2 and (b) control device with bare SiO_2 without PVK (or PFO) layer under illumination.

The effect of PVK layer on the device performance was examined by XRD and AFM of pentacene film grown on top of it, shown in Fig. 6-8, which gives us an insight into why the high mobility of our heterostructure devices remains. A highly ordered pentacene film was deposited on both substrates with/without PVK (Fig. 6-9), showing the "thin film phase",[7,262] which is different from the structure of single crystals of pentacene, i.e. the “single crystal phase”. And the morphology of pentacene polycrystalline film changes

from dendritic grain structure on SiO_2/Si substrate to small granular grain structure on PVK/SiO_2/Si substrate (inset of Fig. 6-9). As pentacene film was deposited on both substrates in an identical way. Thus, the effect of external parameters like difference of vacuum pressure, deposition rate, and substrate temperature on device performance can be excluded.

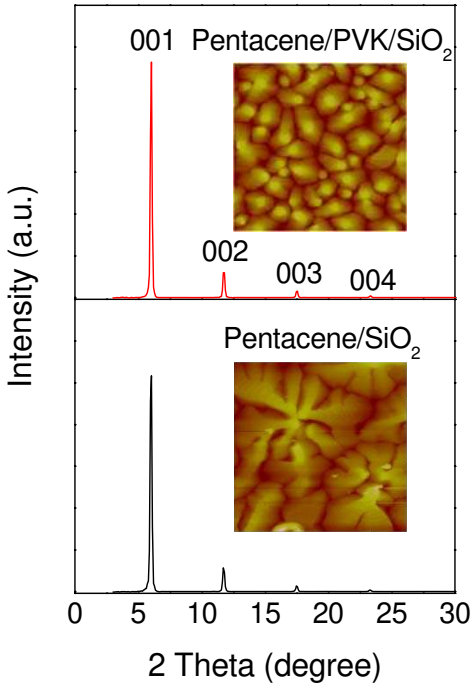


Figure 6-9. X-ray diffraction patterns of $50\ nm$ *pentacene films deposited on (black) bare and (red) PVK-treated SiO_2/Si substrates. Inset: topography of pentacene film (*$2.5 \times 2.5\ \mu m$*).*

The mobility measured from PVK-FETs was ca. $0.6\ cm^2\ V^{-1}\ s^{-1}$, which is slightly higher than that of our control devices with bare SiO_2 and comparable to previous reported results.[43,71] It might be because of the weak interaction potential between PVK and pentacene, resulting in a different growth mode of pentacene film: the (001) orientation of pentacene film on PVK/SiO_2/Si substrate was enhanced, resulting in a more highly ordered film and three dimensional islands of pentacene (i.e. reduced grain size, tighter

packing of pentacene molecules), facilitating the charge transport through the channel layer.[223] Similar results have been reported in the case of pentacene FETs with OTS modified gate oxide.[71,133,222]

However, the set of current curves showed decreased steps of I_{ds} with increasing gate voltage V_g, which was quite different from that of control devices shown in Fig. 6-8b, indicating that the introduction of a PVK layer leads to gate bias dependent threshold voltages V_{th} due to charge trapping mechanisms under illumination. This feature was nearly coincident with the observation in Ref. (247) in dark condition. For low negative V_g, both field induced charges and photo-generated charges could be confined in the channel layer due to the large ΔE_{HOMO}, as shown schematically in Fig. 6-10a. According to the high mobility of our PVK-FETs, we can know that most of the charges are located in the pentacene layer and not the PVK, because of the widely differing field-effect mobilities in PVK ($10^{-6}\,cm^2\,V^{-1}\,s^{-1}$) and pentacene (normally larger than $0.1\,cm^2\,V^{-1}\,s^{-1}$ SiO_2/Si substrates). The heterostructure device possesses a field-effect mobility approximately equal to that of single-layer pentacene FETs, clearly indicating that a majority of the field-induced carriers transfer to the pentacene layer because of the HOMO energy level difference that exists between PVK and pentacene, providing yet another clear illustration of the applicability of heterostructure concepts in organic field-effect transistors. For high negative V_g, i.e. $F \cdot t_{max} > \Delta E_{HOMO}$, where F is the transverse electric field and t_{max} is the film thickness of PVK, holes were expected to be distributed in both layers.[255,261] Recently, the charge transport and distribution in dark condition in a series of semiconducting polymer heterostructure devices (e.g. P3HT/PFO hetero-junction with PMMA

gate dielectric) in a BCTG architecture was simulated using the ATLAS software, which would be influenced by the magnitude of ΔE_{HOMO}, V_g, V_{ds} and the mobility difference between two semiconductors.[261] The simulated results were consistent with our experimental data, this is, the current saturation is determined by the injection rate of charges from the first into the second layer, which is the result of a balance between the energy offset that blocks the charge carrier transfer and the gate field that assists the transfer. These trapped charges in PVK and the interface explains the increase of V_{th}, and thus the decreasing increment of I_{ds} for constant V_g incremental step. Similar trend of $I_{ds} - V_g$ curves was also obtained for PFO-FETs3 (data not shown).

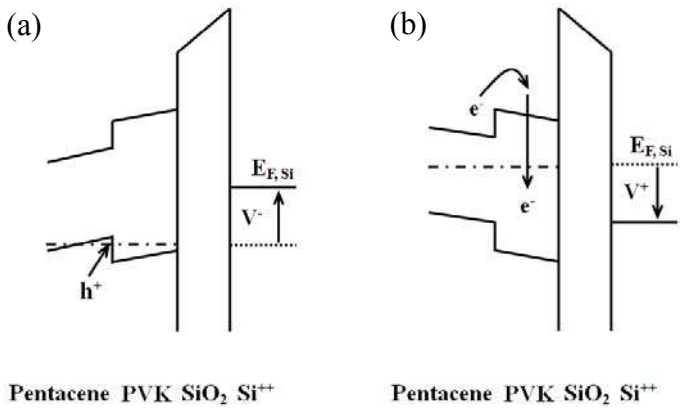


Fig. 6-10. Schematic energy level diagrams of a heterojunction device with pentacene and PVK (or PFO) bilayer when (a) negative gate bias applied: the field-induced holes transfer to pentacene since the HOMO energy level of pentacene is lower than that of PVK (or PFO), (b) positive gate bias applied: electrons injected to PVK (or PFO) at a high transversal electric field.

Clearly, these interfacial layers played an important role in affecting device performance under illuminated condition. To further understand the photo-assisted charge transfer process, the cyclic transfer characteristics of PVK-FETs were tested by sweeping V_g from V_{g_start} to V_{g_stop} and back to

V_{g_start}. As shown in Fig. 6-11a, the devices exhibited a significant dependence of the hysteresis on the sweep range of V_g with fixed V_{g_start} and varied V_{g_stop} (from -10 V to -80 V). The transfer curves coincided with each other during the off-to-on sweep due to the same initial state of the device. On the other hand, the curves during the on-to-off sweep progressively moved toward the negative side, indicating that the magnitude of V_{th} increased negatively and the hysteresis window ΔV_{th} increased with increasing V_{g_stop}.

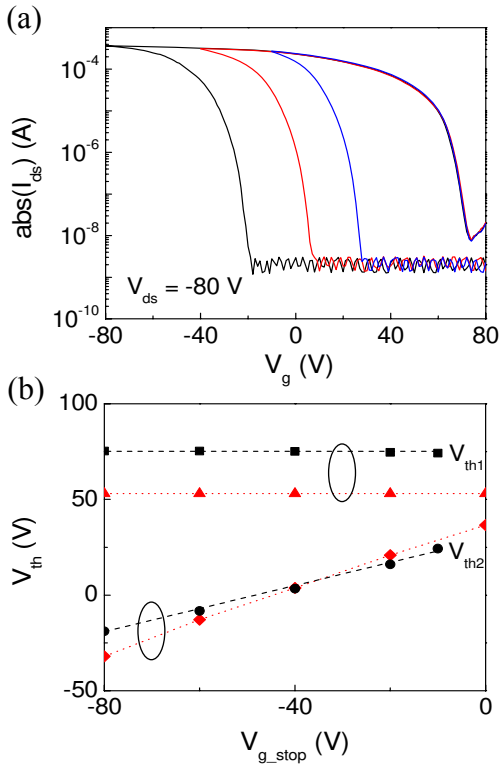


Figure 6-11. (a) Cyclic $I_{ds} - V_g$ characteristics of PVK-FETs with V_g scanned from $80\ V$ to V_{g_stop} and back to $80\ V$, where $V_{g\_stop} = -10\ V$ (blue line), $-40\ V$ (red line), and $-80\ V$ (black line), respectively, at $V_{ds} = -80\ V$. (b) V_{th1} and V_{th2} as a function of V_{g_stop} for PVK-FETs (black) and PFO-FETs3 with $200\ nm$ SiO_2 (red).

It was believed that such a phenomenon was due to (i) the fast release of trapped electrons after a certain positive V_g during the off-to-on sweep, and (ii) direct capture of photo-induced holes in PVK interfacial layer and/or

transferred from the channel layer, especially underneath the drain region, under the high transverse electric field during the on-to-off sweep.[57,247,263] A similar feature was also obtained in the cyclic transfer characteristics of PFO-FETs3 (data not shown). Combining the observations in Fig. 6-8a and Fig. 6-11a, it can be proven that the donor-like traps were presented in both PVK (PFO) layers and the interface, which can cause the hysteresis. The threshold voltages in the off-to-on sweep (V_{th1}) and on-to-off sweep (V_{th2}) were also plotted against V_{g_stop}, shown in Fig. 6-11b. V_{th2} ranged from negative to positive values with nearly linear relation with V_{g_stop}, which meant that once an amount of electrons were pre-trapped in these interfacial layers, either electrons or holes could be retained depending on the extent of hole injection during the on-to-off sweep.

It is known that electron mobility is several orders of magnitude lower than hole mobility in both non-conjugated PVK and conjugated PFO, and the trapping of electrons in these films has been reported.[220,247,254] However, the transfer of electrons from pentacene to PVK (PFO) seemed apparently difficult, especially in dark condition, as (i) the electron carrier density in the p-type semiconductor is low, and (ii) a large LUMO offset ($\Delta E_{LUMO} = 0.7$ eV) between pentacene and these interfacial layers, as well as the large injection barrier between the source-drain contact Au and pentacene, has to be surmounted. It is expected that the trapping of electrons injected from pentacene can be improved through the photo-assisted charge transfer. Fig. 6-12a,b showed the transfer curves of PFO-FETs3 and PVK-FETs measured under illumination by changing the sweep range with various V_{g_start}. For $V_{g\_start} = 0$ V, I_{ds} began to rise at a negative V_g value during the off-to-on

sweep for both devices. The observed hysteresis was proposed to be attributed to the trapping of holes.

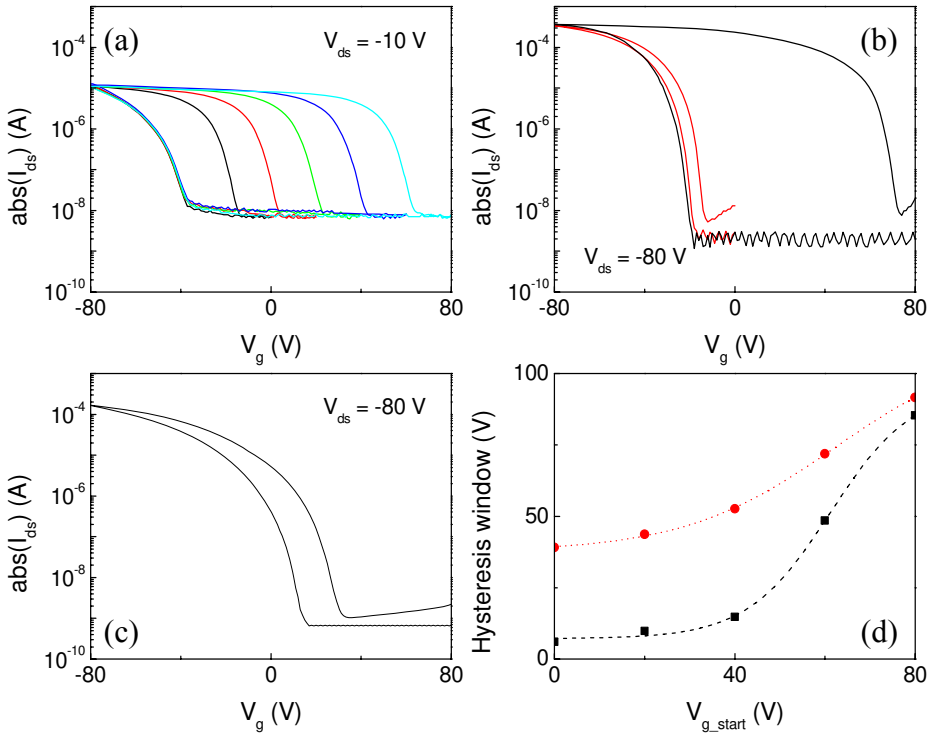


Figure 6-12. (a) Cyclic $I_{ds} - V_g$ characteristics of PFO-FETs3 with $V_{g\_start} = 0\ V$ (black line), $20\ V$ (red line), $40\ V$ (green line), $60\ V$ (blue line), and $80\ V$ (Cayn line), at $V_{ds} = -10\ V$. (b) Cyclic $I_{ds} - V_g$ characteristics of PVK-FETs with $V_{g\_start} = 0\ V$ (red line) and $80\ V$ (black line), at $V_{ds} = -80\ V$. (c) Cyclic $I_{ds} - V_g$ characteristics of control device; (d) Hysteresis window ΔV_{th} as a function of V_{g_start} under illumination for PFO-FETs3 (red circle) and PVK-FETs with $200\ nm$ SiO_2 (black square).

Obviously, the magnitude of hysteresis window in the cyclic transfer curve of PFO-FETs3 was much larger than that of PVK-FETs, indicating the difference in charge injection process. It meant that the injection of holes into PFO and the interface was easier, although the PFO layer was protected by PMMA. This might be because of the nanostructured PFO crystal cannot be fully covered, and then holes would be easily swept into PFO under the high electric field at the head of needle-like PFO crystal (see Fig. 6-4). For the off-

to-on sweeps, we assumed that the amount of trapped electrons, Q_{e_trap}, was initially zero. When V_{g_start} increased positively, the off-to-on curves gradually moved to the positive side, because much more amount of electrons was trapped in PVK (PFO) layer and the interface under higher transverse electric field. Especially at $V_{g\_start} = 80$ V, a conducting channel between the source and the drain began to form even at very high positive V_g between 50 V and 70 V, leading to a wide range of saturation region of the output current I_{ds}. Thus, the amount of trapped negative charges can be estimated according to $Q_{e\_trap} = -\Delta V_{th}^{*} \cdot C_i$, where ΔV_{th}^{*} and C_i are the shift of V_{th} in off-to-on curves between $V_{g\_start} = 0$ V and 80 V, and the unit capacitance of dielectric layer, respectively. At the same time, the on-to-off curves showed little difference for different V_{g_start}, implying that almost all trapped electrons were completely swept out and even some holes might be trapped. Therefore, the hysteresis window, i.e. the total shift in threshold voltage $\Delta V_{th} (= V_{th1} - V_{th2})$, originated from trapped electrons and holes, $Q_{total} [= Q_{e_{trap}} - Q_{h_{trap}} = -C_i(V_{th1} - V_{th2})]$. The hysteresis window ΔV_{th} versus V_{g_start} was shown in Fig. 6-12d, whereas the maximum value of ΔV_{th} exceeded 80 V, i.e. the half sweeping range of V_g. For the control device, not only the shift in V_{th} toward positive direction but also ΔV_{th} was greatly reduced, shown in Fig. 6-12c. It was due to the lack of additional traps introduced by PVK (PFO), only the structural defects (e.g. grain boundaries) and hydroxyl groups at the surface of SiO_2 can contribute to the trapping of electrons. Once electrons were captured by these trapping states, they would be deeply trapped, this is, hard to be released at the time scale of completing the scan of V_g, which explained the positively shifted

V_{th} and small hysteresis window of the control devices. The calculated Q_{total} at $V_{g\_start} = 80\ V$ was between $1 \times 10^{-6}\ C\ cm^{-2}$ for PVK-FET and $1.5 \times 10^{-6}\ C\ cm^{-2}$ for PFO-FETs3, indicating a great charge storage ability of PVK and PFO in the FET structure. This is the very example of how the use of heterostructures in organic devices can enhance their functionality. Additionally, there was a different trend of ΔV_{th} versus V_{g_start} for PFO-FETs3 and PVK-FETs, as seen in Fig. 6-12d. Clearly, a more considerable hysteresis window was obtained at low V_{g_start}, e.g. at 0 V, for PFO-FETs3 than that for PVK-FETs, which was attributed to the easier trapping of holes at negative gate voltage in the former device. For PVK-FETs, ΔV_{th} increased rapidly only when V_{g_start} exceeded $40\ V$ that corresponded to an electric field F of 2 $MV\ cm^{-1}$, leading to an increase in the injection of electrons across PVK/ pentacene heterointerface, as shown schematically in Fig. 6-10b.

Fig. 6-13a showed the cyclic transfer characteristics of PVK-FETs measured by varying V_{ds} while keeping the same sweep range of V_g. Obviously, for a small V_{ds}, e.g. at $-10\ V$, only a small ΔV_{th} was observed. When V_{ds} increased negatively, ΔV_{th} increased accordingly. However, the situation for PFO-FETs3 was slightly different (data not shown). V_{th1} was almost kept constant while V_{th2} was slightly shifted toward positive side with increasing V_{ds}, giving rise to a slightly smaller ΔV_{th} (see Fig. 6-13b). These observations can be qualitatively explained based on our model as follows. Charges arriving at the interface between pentacene and PVK (PFO) can follow one of the two fates: holes are either swept into the drain along the pentacene/PVK (or pentacene/PFO) interface or injected into PVK (PFO) under negative V_g;

electrons are transferred from pentacene active layer and trapped in PVK (PFO) at the depletion region (under positive V_{g_start}).

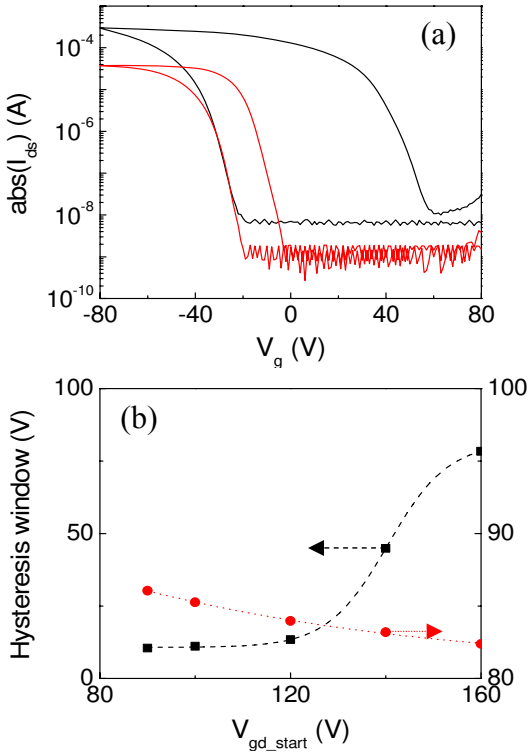


Figure 6-13. (a) Cyclic $I_{ds} - V_g$ characteristics for PVK-FETs with $V_{ds} = -10\,V$ (red line) and $-80\,V$ (black line), respectively. (b) Hysteresis window ΔV_{th} as a function of V_{gd_start} for PVK-FETs (black square) and for PFO-FETs3 with $200\,nm$ SiO_2 (red circle).

The value of V_{ds} influences the drift velocity of holes in pentacene and, therefore, the time the holes spend in the transistor channel. On the other hand the time for charge injection into PVK (PFO) is determined by V_g. For PFO-FETs3, almost the same amount of electrons can be trapped in PFO and the interface at fixed $V_{g\_start} = 80$ V regardless of V_{ds}. At higher negative V_{ds}, the pre-trapped electrons would be fully de-trapped and probably the holes can cross the channel along the pentacene/PFO interface sufficiently fast that they do not have high probability of being injected into PFO during the time they

spend in the channel, which explained the decreased ΔV_{th}. But PVK-FETs underwent an opposite trends, this is, V_{th1} was greatly shifted to the negative side while V_{th2} was little affected by decreasing V_{ds}. We believed that the derecased hysteresis window due to the reduction of V_{ds} was ascribed to the lower transverse electric field near drain region, which was strongly correlated with charge transfer from pentacene into PVK. Fig 6-13b showed hysteresis window ΔV_{th} that were plotted against $V_{gd_{start}} (= V_{g\_start} - V_{ds})$, which was highly in agreement to that in Fig. 6-12d for PVK-FETs. It meant that the electron injection into PVK was mainly determined by both V_{g_start} and V_{ds}.

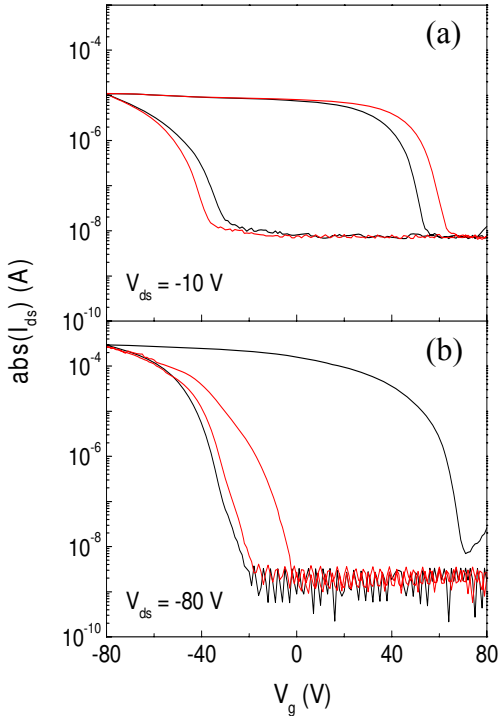


Figure 6-14. Cyclic $I_{ds} - V_g$ characteristics of (a) PFO-FETs3 with $200\,nm$ SiO_2 measured at $V_{ds} = -10\,V$, (b) PVK-FETs measured at $V_{ds} = -80\,V$, with V_g swept in both directions: (i) off-to-on and back to off sweeping (black line), denoted as S_1, (ii) on-to-off and back to on sweeping (red line), denoted as S_2.

Fig. 6-14 showed cyclic transfer characteristics swept in both directions: (i) off-to-on and back to off sweeping, denoted as S_1, (ii) on-to-off and back to on sweeping, denoted as S_2. The off-to-on curves in both S_1 and S_2 exhibited larger drain current $|I_{ds}|$ for all V_g and more positive V_{th1} than V_{th2} in the on-to-off curves due to the charge trapping mechanism. There was little difference between S_{PFO1} and S_{PFO2}, although S_{PFO2} exhibited slightly larger hysteresis window than that in S_{PFO1} (see Fig 6-14a), it might be because of the residual trapped charges during the continuous measurement. However, S_{PVK1} was very different from S_{PVK2}, as shown in Fig. 6-14b. From the off-to-on curve in S_{PVK1} measurement, we knew that a large amount of electrons were transferred across PVK/pentacene heterointerface and trapped in PVK film and the interface, indicated by the large positive V_{th1}. When V_g increased negatively, almost all the trapped electrons would be released and/or recombined with trapped holes, as the on-to-off curves in S_{PVK1} and S_{PVK2} were almost kept constant. When V_g swept back to 0 V in the on-to-off curve of S_{PVK1} and S_{PVK2}, positive charges were trapped and took the place to control V_{th}. During 0-to-80 V in the on-to-off section and 80-to-0 V in the off-to-on section, most captured electrons were used to neutralize these long-life trapped holes, causing a smaller shift in V_{th} in S_{PVK2}. Therefore, it was to say that the lifetime of trapped electrons and holes in PFO-FETs3 was comparable, while holes were more deeply trapped in PVK-FETs, which were related with the structural and electrical properties of PFO and PVK film. The above experiments showed that the trapping of both electrons and holes played a role for the hysteresis behavior in these devices.

6.4 CHAPTER SUMMARY

In conclusion, our interest in heterostructure devices based on two hole conducting materials (e.g. pentacene/PFO) is motivated less by the need for high transistor performance, but more by the desire to better understand the electronic structure of the interface between two semiconductors as well as the charge transport along and charge transfer across such interfaces.

Firstly, the heterojunction FET devices based on pentacene and PFO were demonstrated, exhibiting a typical unipolar p-channel operation. The charge transfer between pentacene and nanostructured PFO in the FET structure was studied and these devices presented a light-programmable electrical feature. Such unique properties were ascribed to the discontinuities in energy levels at the heterointerface between pentacene and PFO, and the charge-trapping ability of nanostructured PFO. The shift of the threshold voltage can be controlled in a wide range so that the operation mode of such devices can be switched from the enhancement mode to the depletion mode by varying V_{g_start} under light illumination, while the field-effect mobility and on/off current ratio were well maintained when the surface condition of nanostructured PFO was optimized. However, to achieve a more useful memory device, the improved performance is expected, in terms of charge retention and the operating voltage by introducing new combinations of various materials, smoother interface, along with optimization of geometrical parameters.

Secondly, the photo-induced hysteresis behavior in devices based on pentacene/PVK (or pentacene/PFO) heterojunction was also investigated, and a hysteresis window larger than 80 V (a half of the total sweep range of gate

voltage) was obtained in both devices. It is also found that the hysteresis window ΔV_{th} was mainly determined by V_g in PFO-FETs3, while it was strongly correlated with the value of both V_g and V_{ds}, and the sweeping direction of V_g in PVK-FETs. In the latter case, ΔV_{th} underwent a clear transition, which began to increase rapidly when the transverse electric field F exceeded 2 MV cm^{-1}. Our experimental results showed that the holes were more deeply trapped into the bulk of PVK and the interface in pentacene FET devices, causing an obvious difference between S_{PVK1} and S_{PVK2}, while the lifetime of trapped electrons and holes in PFO-FETs3 was comparable under the same condition. Such light-programmable feature may motivate the development of this new type of organic memory devices.

CHAPTER 7: SUMMARY AND FUTURE WORK

7.1 SUMMARY OF WORK

In this thesis, we investigated a series of dielectric surface modification related to the electrical performance and the stability of OFETs. It is not a brand new subject, and there is lots of research work that has been carried out to investigate the growth mode of OSCs, subsequently the charge transport along the channel layer. When OSCs approach their "maturity" and OFETs move closer to application, the study on how to enhance the operational as well as realistic atmospheric stability would become the focal point of future research work. I am very honored and pleased to have contributed to the growth of this field through my experiment, which can be categorized into two main groups: (i) stabilize the threshold voltage under dark and/or illuminated condition by dielectric passivation to minimize the charge trapping, and (ii) control the threshold voltage by manipulating the charge transfer across the interface between two OSCs.

In the first area, it is found that the demonstration of hysteresis-free FET devices with dual dielectrics in dark condition is not nearly enough. The buried traps between buffer dielectric and gate dielectric still need to be cared about, which is usually left unexplored. In order to characterize it, PMMA and its derivative (P4VP-*co*-PMMA) are used as buffer dielectric in an OFET structure to clarify the importance of the selection of a buffer layer and the thickness optimization for the enhancement of device stability, especially when

exposure to light illumination. Furthermore, in the fabrication of low-voltage OFET devices using high-κ metal oxide as gate dielectric, oxygen plasma treatment can effectively promote the surface condition through the elimination of certain organic contaminants and the compensation of the vacancies. Using a proper plasma exposure time, not only the field-effect mobilities and the device stability can be improved, but also the control of threshold voltage can be realized. And the study on the age of pentacene film grown at the surface of plasma-treated HfO_2 provides visual evidence upon what degrades the device performance in the atmospheric condition. These findings help to bring about an easy-to-realization fabrication method to produce high-performance and reliable OFET devices.

The second main work focuses on studying the electronic structure of the interface between two OSCs as well as the charge transport along and charge transfer across such interface. PFO/pentacene heterojunction FET devices, for instance, exhibit a typical conventional p-channel operation, benefiting from the discontinuities in energy levels at their heterointerface. When it is under illumination, the threshold voltage of such devices can be tuned by varying the bias condition (V_{ds}, V_g and its sweeping direction), because of the photo-assist charge transfer, which is also important for the enhancement of the reliability of complex ICs. The unique light-programmable feature of such devices might also motivate the development of novel OFET based memory devices.

In relation to the work directed towards the realization of practical application of OFETs, this thesis discusses how to manipulate the threshold voltage of an OFET device, which is essential for the development of OFETs

with reliable and/or controllable characteristics. Further study is still needed to fully understand the contribution of traps, which is briefly summarized as follows.

7.2 RECCOMENDATIONS FOR FURTHER RESEARCH

7.2.1 FET DEVICES WITH DUAL DIELECTRIC

It was reported that the grain boundaries of polycrystalline films can act as charge trapping centers. Therefore, when the devices are biased with a gate voltage under illumination for more than 1 min, the photo-generated charge carriers also can be deeply trapped, inducing the large shift of threshold voltage. To minimize such effect, the use of single crystals with low intrinsic defects (e.g. rubrene in Ref. 181 and pentacene single crystals in Ref. 188) will be of great help to understand the mechanism of photo-assist charge transfer across thin buffer dielectric as well as the detailed study of the PMMA (or other buffer dielectrics) thickness dependence and wavelength dependence.

7.2.2 LOW VOLTAGE PENTACENE FET DEVICES

As discussed before, the degradation of pentacene film on plasma-treated HfO_2 in air is accelerated due to the surface stress enhanced weathering effect, which we think can be weaken by increasing the substrate temperature when OSCs is being deposited or annealing the samples after the deposition of OSCs, and/or characterizing the electrical performance in an inert environment to avoid oxygen and moistures, and/or using amorphous OSCs with high mobility and good stability to minimize the changes of morphologies.

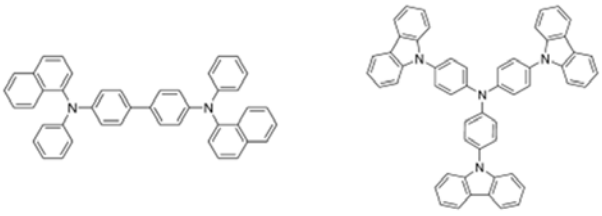
Another issue is the large contact resistance, which might be due to the coevaporation of other metals from the home-made evaporator holders at the high temperature during the metal deposition. Therefore, chilled water needs to be installed to cool down the evaporator holders.

7.2.3 HETEROJUNCTION FET DEVICES

Due to plenty of OSCs developed by chemists, it offers us a great chance to perform a systematical investigation of material combinations, such as difference energy levels, morphologies and glass transition temperatures, with respect to that of pentacene active layer. The exploration of differences in molecular orbital energy levels and transport properties of various materials in this novel design is expected to enhance the functionalities of OFETs.

7.2.3a HOLE TRANSPORT MATERIALS

NPB/pentacene and TCTA/pentacene heterojunction FET devices have been characterized in dark condition. Typical p-channel operation has been observed, but the mobility of these devices is slightly smaller than that of devices with one layer pentacene active layer, because the crystallinity and molecular orientation of pentacene is affected by NPB and/or TCTA layer.



(a) NPB (b) TCTA

Figure 7-1. Chemical structure of (a) NPD ($LUMO = -2.5\ eV$, $= -5.5\ eV$), (b) TCTA ($LUMO = -2.3eV$, $HOMO = -5.7eV$).[264]

The hysteresis behavior was not obtained, when characterized in dark condition, indicating that the charge transfer across the heterointerface was suppressed due to the large offset of energy levels, similar to that of PFO /pentacene heterojunction FET devices. However, such charge transfer is also expected, when the device is under illumination (not investigated yet).[255]

7.2.3b ELECTRON TRANSPORT MATERIALS

Ambipolar transistors, which accumulate and conduct both holes and electrons, have attracted much research interest, due to its low power dissipation, wide noise margins, and higher robustness.[265] Organic bilayer FETs using p-channel and n-channel semiconductor has already been successfully demonstrated.[55,178] The challenge for building high performance of these devices lies in several ways: (i) excellent p- and n-channel semiconductors with proper HOMO and LUMO level, (ii) the optimum deposition order of p- and n- channel materials, (iii) the effective injection of both charges carriers, and (iv) elimination of charge trapping.

However, the trapping of one or both carrier types usually occurs, especially electrons that are likely to be trapped by impurities or certain chemical moieties at the dielectric/semiconductor interface. Aiming at improving the charge trapping, low-mobility light-emitting material, Tris(8-hydroxyquinoline) aluminum (Alq3, also an electron transport material) is chosen to form heterojunction with pentacene in FET structure, this is because Alq3 receives more attention than any other small molecule emitters among LED materials.[236] The LUMO level of Alq3 is -3.1eV, which is closed to that of pentacene and higher than that of PFO; while its HOMO level (-5.8 ev) is

much lower than that of pentacene and similar to that of PFO. As the LUMO offset between Alq3 and pentacene is much smaller than that between PFO and pentacene, therefore, the charge transfer is expected to be easier in Alq3/ pentacene heterojunction FET devices.

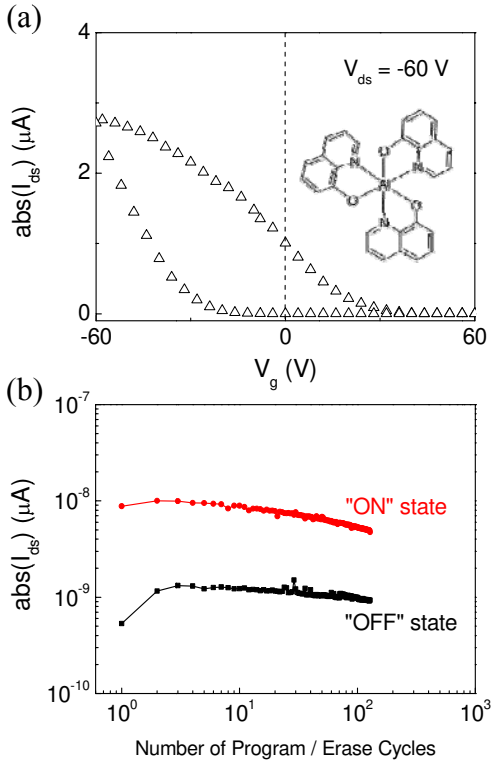


Figure 7-2. (a) Transfer characteristics of pentacene/Alq3 hetero-junction FET devices with $200\,nm$ *SiO_2. (b) Endurance of the "ON" and "OFF" state of devices, measured at* $V_{ds} = -80\,V$ *and* $V_g = 0\,V$ *after programming by a gate bias of* $80\,V$ *at* $V_{ds} = 0\,V$*, and erasing by a gate bias of* $-80\,V$ *at* $V_{ds} = 0\,V$*. Inset: chemical structure of Alq3 molecule.*

As shown in Fig. 7-2a, there is a large, reversible hysteresis in the cyclic transfer curve, due to the trapping of electrons in Alq3 and the interface. Thus, applying an opposite gate bias, V_{ds} can be reversibly altered, giving rise to an observable change in output current I_{ds} at $V_g = 0$ V. By the application of a gate bias of ± 80 V for 1 s, the device can be turned on/off, as shown in Fig. 7-2b. The endurance characteristics show an on/off current ratio of ~ 10, but

both "On" and "Off" state current slightly decrease as a function of number of program/erase cycles, this might be due to the non-optimum programming /erasing condition.

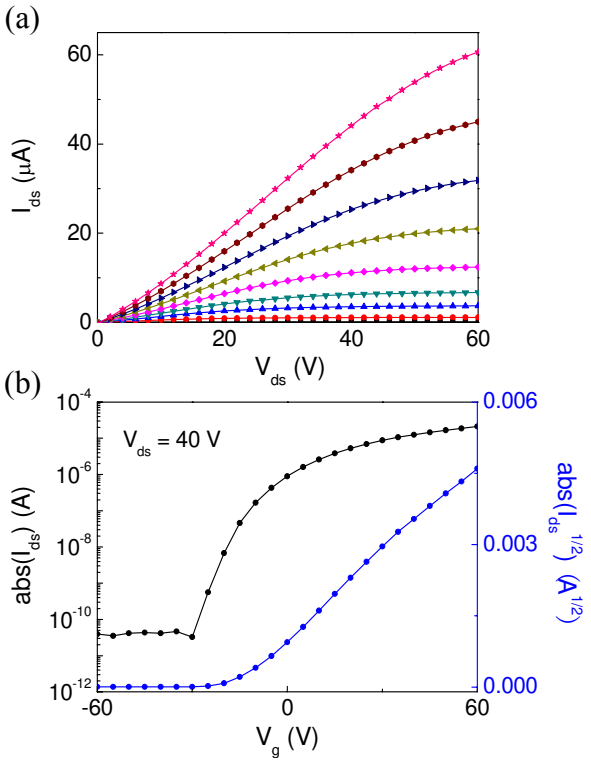


Figure 7-3. (a) Output characteristics and (b) Transfer characteristics of a solution-processed ZnO FET with top-contact structure ($W = 2\ mm, = 100\ um$). ZnO is spin-coated (or inkjet-printed) from the solution comprising of zinc acetate, di-ethane-amine (DEA), and ethane.

On the other hand, solution-processed zinc oxide (ZnO) film is also fabricated in our lab, which can be used to replace the layer of Alq3 in the heterojunction FET device. The output and transfer characteristics of a ZnO based FET device are presented in Fig. 7-3, indicating the excellent electron transport properties. By controlling the thickness and the crystallinity of ZnO layer, ZnO/pentacene heterojunction FET devices are expected to shown p-channel, ambipolar and n-channel operation. When the ZnO layer is very thin, the field-effect electrons are easy to be captured in ZnO and the interface due

to the large offset of LUMO levels of ZnO (LUMO $= -4.4$ eV and HOMO $= -7.7$ eV)[266] and pentacene, subsequently, a unipolar p-channel behavior with considerable hysteresis is expected. Once electrons are trapped, long retention is also expected due to large offset of LUMO levels that serves as a barrier.

7.2.4 CHARGE TRAPPING IN ELECTRETS

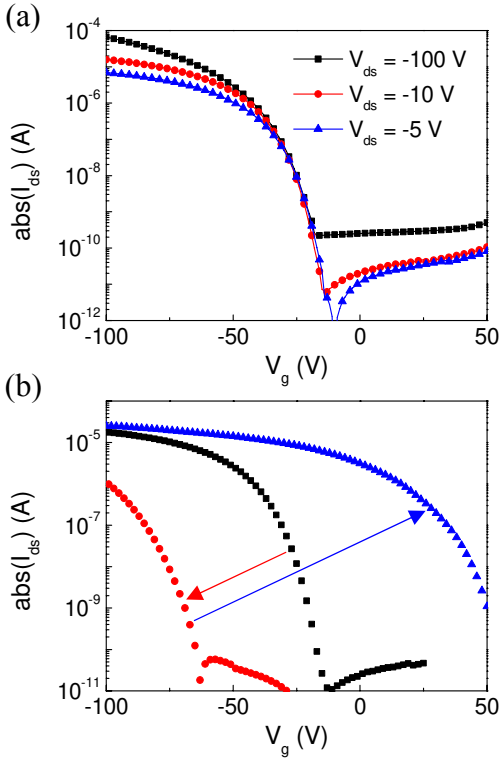


Figure 7-4. (a) Transfer characteristics and (b) Reversible shift in V_{th} of pentacene FET devices with PS/SiO_2 gate stack. The transfer curves are measured at $V_{ds} = -10\,V$ after the application of gate biases ($\mp 200\,V$) at $V_{ds} = 0\,V$ for programming and erasing process.

The study on charge trapping in various styrenic polymeric electrets (e.g. PS, shown in Fig. 7-4b) has been reported by Baeg et al,[161,183] who are first to report programming speeds of around 1 μs—a million times faster than the previous best time of around 1 s. That marks a decisive step towards

making organic memory technology fit for technological purposes, therefore, attracts extensive academic and industrial interest.

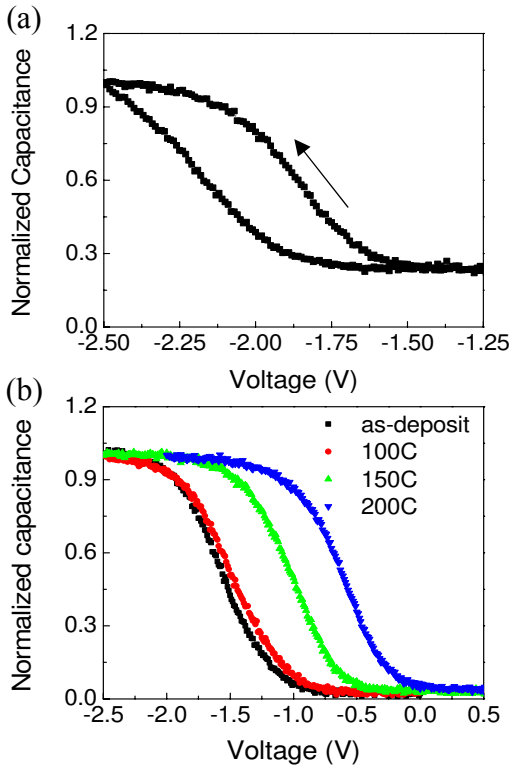


Figure 7-5. Normalized C-V characteristics of (a) as-deposited OTS MIS capacitor, (b) OTS MIS capacitors with various annealing temperatures.

In our work, the trapping of charge in SAMs is investigated. A large hysteresis of 0.7 V was observed together with a large shift towards the negative gate voltage, as shown in Fig. 7-5. This indicates the presence of a large amount of positive charges or interface states in as-deppsoted OTS insulator. When it is used as buffer dielectric in pentacene FET devices, field-effect electrons can be easily transferred from pentacene into OTS and the interface, and trapped deeply (see Fig. 7-6), once the device is programmed by a positive gate bias. Interestingly, these trapped charges are hardly detrapped by the application of a large negative gate voltage. The exact mechanism of charge trapping in such SAMs is still under investigation. However, to the best

of our knowledge, it is the first time to demonstrate the memory effect in FET structure with SAM electrets, although OTS used as gate insulator was reported previously.[267] From the scientific view, it would be very attractive to study the charge trapping in the cluster of SAMs and/or a certain head group of SAMs, rather than the control of surface carrier density in OFETs by using molecules as SAMs with various head groups.[141]

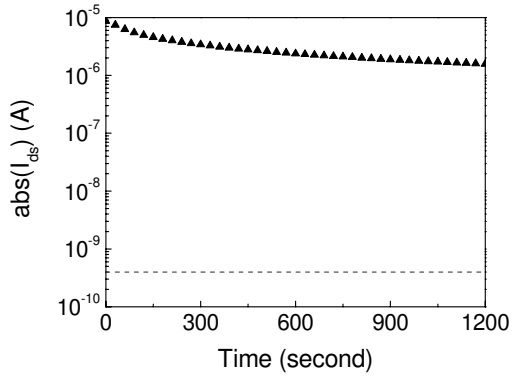


Figure 7-6. Time evolution of I_{ds} measured at $V_{ds} = -50\,V$ and $V_g = 0\,V$ in the dark after pentacene FET device with as-deposited OTS/SiO_2 gate stack is programmed by the application of a $200\,V$ gate bias. The off current (dot line) is shown for reference.

7.3 AREA FOR IMPROVEMENT

Some of the problems during the fabrication and characterization of OFET device are encountered. To get better device performance and further study the reliability of OFET devices etc, more functions of this PVD system will be utilized and thus optimized. The following improvement needs to be made to enhance its functions and efficiency:

- The substrate temperature should be controllable while the thin film is being grown. Subsequently, it also provides a high-vacuum condition for post-deposition annealing without exposure to air.

- Glove box is needed to store the completed devices and the electrical test thus can be performed securely, minimizing the influence of the ambient environment.
- Patterning of organic materials to minimize the leakage current. For a memory device, the characterization of the retention time of trapped charge carriers is less influenced.

PUBLICATIONS FROM THESIS

JOURNAL PUBLICATIONS

1. *Chengang Feng*, Ting Mei, Xiao Hu, "Photo-induced hysteresis behavior in pentacene field-effect transistors using wide bandgap light-emitting material as interfacial layer" submitted.
2. *Chengang Feng*, Ting Mei, Xiao Hu, "The influence of oxygen plasma on the performance of pentacene field-effect transistors using low temperature ALD grown HfO2 as gate dielectric" submitted.
3. *Chengang Feng*, Ting Mei, Xiao Hu, "Influence of trapping states at the dielectric–dielectric interface on the stability of organic field-effect transistors with bilayer gate dielectric" Organic Electronics 12 (2011) 1304 -1313.
4. *Chengang Feng*, Ting Mei, Xiao Hu, Neuzil Pavel, "A pentacene field-effect transistor with light-programmable threshold voltage" Organic Electronics 11 (2010) 1713-1718.

INTERNATIONAL CONFERENCES

1. *Chengang Feng*, Ting Mei, Xiao Hu, "Study on the buried trapping states at the dielectric/dielectric interface in the OFET structure" Organic Microelectronics & Optoelectronics Workshop VII, San Francisco, CA, 18-20 July, 2011.
2. *Chengang Feng*, Ting Mei, Xiao Hu, "Enhanced performance of pentacene OFETs with 12 nm HfO_2 as gate dielectric by oxygen plasma" Nanotechnology and Printed Electronics International Symposium 2011, Singapore, 4-5 July 2011.
3. *Chengang Feng*, Ting Mei, Pavel Neuzil, "Organic Thin Film Transistors with Isotypic Heterojunction" the 7^{th} Internation Conference on Materials for Advanced Technologies, Singapore, 28 June-3 July 2009.

BIBLIOGRAPHY

1. Wisnieff, R. 1998, "Printing screens", *Nature,* vol. 394, no. 6690, pp. 225-227.
2. Comiskey, B., Albert, J.D., Yoshizawa, H. & Jacobson, J. 1998, "An electrophoretic ink for all-printed reflective electronic displays", *Nature,* vol. 394, no. 6690, pp. 253-255.
3. Sheridon, N. K. 1978, US Patent 4, 126, 854.
4. Crone, B., Dodabalapur, A., Gelperin, A., Torsi, L., Katz, H.E., Lovinger, A.J. & Bao, Z. 2001, "Electronic sensing of vapors with organic transistors", *Applied Physics Letters,* vol. 78, no. 15, pp. 2229-2231.
5. Drury, C.J., Mutsaers, C.M.J., Hart, C.M., Matters, M. & De Leeuw, D.M. 1998, "Low-cost all-polymer integrated circuits", *Applied Physics Letters,* vol. 73, no. 1, pp. 108-110.
6. Kymissis, I., Dimitrakopoulos, C.D. & Purushothaman, S. 2001, "High-performance bottom electrode organic thin-film transistors", *IEEE Transactions on Electron Devices,* vol. 48, no. 6, pp. 1060-1064.
7. Dimitrakopoulos, C.D., Brown, A.R. & Pomp, A. 1996, "Molecular beam deposited thin films of pentacene for organic field effect transistor applications", *Journal of Applied Physics,* vol. 80, no. 4, pp. 2501-2508.
8. Choo, M.H., Hong, W.S. & Im, S. 2002, "Characterization of pentacene organic thin film transistors fabricated on SiNx films by non-photolithographic processes", *Thin Solid Films,* vol. 420-421, pp. 492-496.
9. Bolognesi, A., Di Carlo, A. & Lugli, P. 2002, "Influence of carrier mobility and contact barrier height on the electrical characteristics of organic transistors", *Applied Physics Letters,* vol. 81, no. 24, pp. 4646-4648.
10. Wang, Y.W., Cheng, H.L., Wang, Y.K., Hu, T.H., Ho, J.C., Lee, C.C., Lei, T.F. & Yeh, C.F. 2004, "Influence of measuring environment on the electrical characteristics of pentacene-based thin film transistors", *Thin Solid Films,* vol. 467, no. 1-2, pp. 215-219.
11. Lee, J.H., Kim, S.H., Kim, G.H., Lim, S.C., Lee, H., Jang, J. & Zyung, T. 2003, "Pentacene thin film transistors fabricated on plastic substrates", *Synthetic Metals,* vol. 139, no. 2, pp. 445-451.
12. Iino, Y., Inoue, Y., Fujisaki, Y., Fujikake, H., Sato, H., Kawakita, M., Tokito, S. & Kikuchi, H. 2003, "Organic thin-film transistors on a plastic substrate with anodically oxidized high-dielectric-constant insulators", *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* vol. 42, no. 1, pp. 299-304.
13. Deman, A.L. & Tardy, J. 2005, "PMMA-Ta2O5 bilayer gate dielectric for low operating voltage organic FETs", *Organic Electronics: physics, materials, applications,* vol. 6, no. 2, pp. 78-84.
14. Deman, A.L. & Tardy, J. 2006, "Stability of pentacene organic field effect transistors with a low-k polymer/high-k oxide two-layer gate

dielectric", *Materials Science and Engineering C,* vol. 26, no. 2-3, pp. 421-426.

15. Mizukami, M., Hirohata, N., Iseki, T., Ohtawara, K., Tada, T., Yagyu, S., Abe, T., Suzuki, T., Fujisaki, Y., Inoue, Y., Tokito, S. & Kurita, T. 2006, "Flexible AM OLED panel driven by bottom-contact OTFTs", *IEEE Electron Device Letters,* vol. 27, no. 4, pp. 249-251.
16. Chen, F.C., Chu, C.W., He, J., Yang, Y. & Lin, J.L. 2004, "Organic thin-film transistors with nanocomposite dielectric gate insulator", *Applied Physics Letters,* vol. 85, no. 15, pp. 3295-3297.
17. Majewski, L.A., Schroeder, R. & Grell, M. 2005, "Low-voltage, high-performance organic field-effect transistors with an ultra-thin TiO2 layer as gate insulator", *Advanced Functional Materials,* vol. 15, no. 6, pp. 1017-1022.
18. Kim, J.M., Lee, J.W., Kim, J.K., Ju, B.K., Kim, J.S., Lee, Y.H. & Oh, M.H. 2004, "An organic thin-film transistor of high mobility by dielectric surface modification with organic molecule", *Applied Physics Letters,* vol. 85, no. 26, pp. 6368-6370.
19. Koo, J.B., Yun, S.J., Lim, J.W., Kim, S.H., Ku, C.H., Lim, S.C., Lee, J.H. & Zyung, T. 2006, "Low-voltage and high-gain pentacene inverters with plasma-enhanced atomic-layer-deposited gate dielectrics", *Applied Physics Letters,* vol. 89, no. 3, pp. 033511-1.
20. Javey, A., Guo, J., Farmer, D.B., Wang, Q., Wang, D., Gordon, R.G., Lundstrom, M. & Dai, H. 2004, "Carbon nanotube field-effect transistors with integrated ohmic contacts and high-κ gate dielectrics", *Nano Letters,* vol. 4, no. 3, pp. 447-450.
21. Tardy, J., Erouel, M., Deman, A.L., Gagnaire, A., Teodorescu, V., Blanchin, M.G., Canut, B., Barau, A. & Zaharescu, M. 2007, "Organic thin film transistors with HfO2 high-k gate dielectric grown by anodic oxidation or deposited by sol-gel", *Microelectronics Reliability,* vol. 47, no. 2-3, pp. 372-377.
22. Acton, O., Ting, G., Ma, H., Ka, J.W., Yip, H.L., Tucker, N.M. & Jen, A.K.Y. 2008, "π-σ-phosphonic acid organic monolayer/sol-gel hafnium oxide hybrid dielectrics for low-voltage organic transistors", *Advanced Materials,* vol. 20, no. 19, pp. 3697-3701.
23. Yoon, M.H., Yan, H., Facchetti, A. & Marks, T.J. 2005, "Low-voltage organic field-effect transistors and inverters enabled by ultrathin cross-linked polymers as gate dielectrics", *Journal of the American Chemical Society,* vol. 127, no. 29, pp. 10388-10395.
24. Roberts, M.E., Mannsfeld, S.C.B., Queraltó, N., Reese, C., Locklin, J., Knoll, W. & Bao, Z. 2008, "Water-stable organic transistors and their application in chemical and biological sensors", *Proceedings of the National Academy of Sciences of the United States of America,* vol. 105, no. 34, pp. 12134-12139.
25. Noh, Y.Y. & Sirringhaus, H. 2009, "Ultra-thin polymer gate dielectrics for top-gate polymer field-effect transistors", *Organic Electronics: physics, materials, applications,* vol. 10, no. 1, pp. 174-180.
26. Cheng, X., Caironi, M., Noh, Y.-Y., Wang, J., Newman, C., Yan, H., Facchetti, A. & Sirringhaus, H. 2010, "Air stable cross-linked cytop ultrathin gate dielectric for high yield low-voltage top-gate organic

field-effect transistors", *Chemistry of Materials,* vol. 22, no. 4, pp. 1559-1566.
27. Collet, J. & Vuillaume, D. 1998, "Nano-field effect transistor with an organic self-assembled monolayer as gate insulator", *Applied Physics Letters,* vol. 73, no. 18, pp. 2681-2683.
28. Yoon, M.H., Facchetti, A. & Marks, T.J. 2005, "σ-π molecular dielectric multilayers for low-voltage organic thin-film transistors", *Proceedings of the National Academy of Sciences of the United States of America,* vol. 102, no. 13, pp. 4678-4682.
29. Jones, B.A., Facchetti, A., Marks, T.J. & Wasielewski, M.R. 2007, "Cyanonaphthalene diimide semiconductors for air-stable, flexible, and optically transparent n-channel field-effect transistors", *Chemistry of Materials,* vol. 19, no. 11, pp. 2703-2705.
30. Ling, M.M., Erk, P., Gomez, M., Koenemann, M., Locklin, J. & Bao, Z. 2007, "Air-stable n-channel organic semiconductors based on perylene diimide derivatives without strong electron withdrawing groups", *Advanced Materials,* vol. 19, no. 8, pp. 1123-1127.
31. Lu, G., Usta, H., Risko, C., Wang, L., Facchetti, A., Ratner, M.A. & Marks, T.J. 2008, "Synthesis, characterization, and transistor response of semiconducting silole polymers with substantial hole mobility and air stability. Experiment and theory", *Journal of the American Chemical Society,* vol. 130, no. 24, pp. 7670-7685.
32. Osaka, I., Zhang, R., Liu, J., Smilgies, D.M., Kowalewski, T. & McCullough, R.D. 2010, "Highly stable semiconducting polymers based on thiazolothiazole", *Chemistry of Materials,* vol. 22, no. 14, pp. 4191-4196.
33. Koch, N. 2007, "Organic electronic devices and their functional interfaces", *ChemPhysChem,* vol. 8, no. 10, pp. 1438-1455.
34. Ma, H., Yip, H.L., Huang, F. & Jen, A.K.Y. 2010, "Interface engineering for organic electronics", *Advanced Functional Materials,* vol. 20, no. 9, pp. 1371-1388.
35. Kim, W.J., Koo, W.H., Jo, S.J., Kim, C.S., Baik, H.K., Lee, J. & Im, S. 2005, "Enhancement of long-term stability of pentacene thin-film transistors encapsulated with transparent SnO2", *Applied Surface Science,* vol. 252, no. 5, pp. 1332-1338.
36. Lee, J.H., Kim, G.H., Kim, S.H., Lim, S.C., Yang, Y.S., Oh, J., Youk, J.H., Jang, J. & Zyung, T. 2005, "The novel encapsulation method for organic thin-film transistors", *Current Applied Physics,* vol. 5, no. 4, pp. 348-350.
37. Göllner, M., Huth, M. & Nickel, B. 2010, "Pentacene thin-film transistors encapsulated by a thin alkane layer operated in an aqueous ionic environment", *Advanced Materials,* vol. 22, no. 39, pp. 4350-4354.
38. Lilienfeld, J. E. 1930, US Patent 1, 745, 175.
39. Kahng, D. & Atalla, M. M. 1960, "Silicon–silicon dioxide field induced surface devices", in *IRE Solid-State Devices Research Conference*, Pittsburgh, PA.
40. Heilmeier, G.H. & Zanoni, L.A. 1964, "Surface studies of α-copper phthalocya-nine films", *Journal of Physics and Chemistry of Solids,* vol. 25, no. 6, pp. 603-611.

41. Koezuka, H., Tsumura, A. & Ando, T. 1987, "Field-effect transistor with polythiophene thin film", *Synthetic Metals,* vol. 18, no. 1-3, pp. 699-704.
42. Horowitz, G., Fichou, D., Peng, X., Xu, Z. & Garnier, F. 1989, "A field-effect transistor based on conjugated alpha-sexithienyl", *Solid State Communications,* vol. 72, no. 4, pp. 381-384.
43. Gundlach, D.J., Lin, Y.Y., Jackson, T.N., Nelson, S.F. & Schlom, D.G. 1997, "Pentacene organic thin-film transistors - Molecular ordering and mobility", *IEEE Electron Device Letters,* vol. 18, no. 3, pp. 87-89.
44. Bao, Z. & Locklin, J. 2007, "Organic field-effect transistors", *CRC Press*.
45. Pesavento, P.V., Chesterfield, R.J., Newman, C.R. & Frisble, C.D. 2004, "Gated four-probe measurements on pentacene thin-film transistors: Contact resistance as a function of gate voltage and temperature", *Journal of Applied Physics,* vol. 96, no. 12, pp. 7312-7324.
46. Newman, C.R., Frisbie, C.D., Da Silva Filho, D.A., Brédas, J.L., Ewbank, P.C. & Mann, K.R. 2004, "Introduction to organic thin film transistors and design of n-channel organic semiconductors", *Chemistry of Materials,* vol. 16, no. 23, pp. 4436-4451.
47. Frank, D.J., Dennard, R.H., Nowak, E., Solomon, P.M., Taur, Y. & Wong, H.-P. 2001, "Device scaling limits of Si MOSFETs and their application dependencies", *Proceedings of the IEEE,* vol. 89, no. 3, pp. 259-287.
48. Chua, L.L., Ho, P.K.H., Sirringhaus, H. & Friend, R.H. 2004, "High-stability ultrathin spin-on benzocyclobutene gate dielectric for polymer field-effect transistors", *Applied Physics Letters,* vol. 84, no. 17, pp. 3400-3402.
49. Sze, S. M. 2002, "Semiconductor Devices–Physics and Technology", John Wiley and Sons, Inc.: New York.
50. Austin, M.D. & Chou, S.Y. 2002, "Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography", *Applied Physics Letters,* vol. 81, no. 23, pp. 4431-4433.
51. Kagan, C.R., Afzali, A., Martel, R., Gignac, L.M., Solomon, P.M., Schrott, A.G. & Ek, B. 2003, "Evaluations and considerations for self-assembled monolayer field-effect transistors", *Nano Letters,* vol. 3, no. 2, pp. 119-124.
52. Chabinyc, M.L., Lu, J.-P., Street, R.A., Wu, Y., Liu, P. & Ong, B.S. 2004, "Short channel effects in regioregular poly(thiophene) thin film transistors", *Journal of Applied Physics,* vol. 96, no. 4, pp. 2063-2070.
53. Tulevski, G.S., Nuckolls, C., Afzali, A., Graham, T.O. & Kagan, C.R. 2006, "Device scaling in sub-100 nm pentacene field-effect transistors", *Applied Physics Letters,* vol. 89, no. 18, pp. 183101-1.
54. Haddock, J.N., Zhang, X., Zheng, S., Zhang, Q., Marder, S.R. & Kippelen, B. 2006, "A comprehensive study of short channel effects in organic field-effect transistors", *Organic Electronics: physics, materials, applications,* vol. 7, no. 1, pp. 45-54.
55. Zaumseil, J. & Sirringhaus, H. 2007, "Electron and ambipolar transport in organic field-effect transistors", *Chemical reviews,* vol. 107, no. 4, pp. 1296-1323.

56. Veres, J., Ogier, S., Lloyd, G. & De Leeuw, D. 2004, "Gate insulators in organic field-effect transistors", *Chemistry of Materials,* vol. 16, no. 23, pp. 4543-4555.
57. Salleo, A. & Street, R.A. 2003, "Light-induced bias stress reversal in polyfluorene thin-film transistors", *Journal of Applied Physics,* vol. 94, no. 1, pp. 471-479.
58. Rep, D.B.A., Morpurgo, A.F., Sloof, W.G. & Klapwijk, T.M. 2003, "Mobile ionic impurities in organic semiconductors", *Journal of Applied Physics,* vol. 93, no. 4, pp. 2082-2090.
59. Salleo, A. & Street, R.A. 2004, "Kinetics of bias stress and bipolaron formation in polythiophene", *Physical Review B - Condensed Matter and Materials Physics,* vol. 70, no. 23, pp. 235324-1.
60. Street, R.A., Salleo, A., Chabinyc, M. & Paul, K. 2004, "Localized state effects in polymer thin film transistors", *Journal of Non-Crystalline Solids,* vol. 338-340, no. 1 SPEC. ISS., pp. 607-611.
61. Ng, T.N., Marohn, J.A. & Chabinyc, M.L. 2006, "Comparing the kinetics of bias stress in organic field-effect transistors with different dielectric interfaces", *Journal of Applied Physics,* vol. 100, no. 8, pp. 084505-1.
62. Kagan, C.R., Afzali, A. & Graham, T.O. 2005, "Operational and environmental stability of pentacene thin-film transistors", *Applied Physics Letters,* vol. 86, no. 19, pp. 193505-1.
63. Schroeder, R., Majewski, L.A. & Grell, M. 2004, "All-organic permanent memory transistor using an amorphous, spin-cast ferroelectric-like gate insulator", *Advanced Materials,* vol. 16, no. 7, pp. 633-636.
64. Naber, R.C.G., Tanase, C., Blom, P.W.M., Gelinck, G.H., Marsman, A.W., Touwslager, F.J., Setayesh, S. & De Leeuw, D.M. 2005, "High-performance solution-processed polymer ferroelectric field-effect transistors", *Nature Materials,* vol. 4, no. 3, pp. 243-248.
65. Blochwitz, J., Pfeiffer, M., Fritz, T. & Leo, K. 1998, "Low voltage organic light emitting diodes featuring doped phthalocyanine as hole transport material", *Applied Physics Letters,* vol. 73, no. 6, pp. 729-731.
66. Maennig, B., Pfeiffer, M., Nollau, A., Zhou, X., Leo, K. & Simon, P. 2001, "Controlled p-type doping of polycrystalline and amorphous organic layers: Self-consistent description of conductivity and field-effect mobility by a microscopic percolation model", *Physical Review B - Condensed Matter and Materials Physics,* vol. 64, no. 19, pp. 1952081-1952089.
67. Nollau, A., Pfeiffer, M., Fritz, T. & Leo, K. 2000, "Controlled n-type doping of a molecular organic semiconductor: Naphthalenetetracarboxylic dianhydride (NTCDA) doped with bis(ethylenedithio)-tetrathiafulvalene (BEDT-TTF)", *Journal of Applied Physics,* vol. 87, no. 9 I, pp. 4340-4343.
68. Bernius, M.T., Inbasekaran, M., O'Brien, J. & Wu, W. 2000, "Progress with light-emitting polymers", *Advanced Materials,* vol. 12, no. 23, pp. 1737-1750.
69. Becker, H., Spreitzer, H., Kreuder, W., Kluge, E., Schenk, H., Parker, I. & Cao, Y. 2000, "Soluble PPVs with enhanced performance - a mechanistic approach", *Advanced Materials,* vol. 12, no. 1, pp. 42-48.

70. Jurchescu, O.D., Baas, J. & Palstra, T.T.M. 2004, "Effect of impurities on the mobility of single crystal pentacene", *Applied Physics Letters,* vol. 84, no. 16, pp. 3061-3063.
71. Lin, Y.Y., Gundlach, D.J., Nelson, S.F. & Jackson, T.N. 1997, "Stacked pentacene layer organic thin-film transistors with improved characteristics", *IEEE Electron Device Letters,* vol. 18, no. 12, pp. 606-608.
72. Klauk, H., Halik, M., Zschieschang, U., Schmid, G., Radlik, W. & Weber, W. 2002, "High-mobility polymer gate dielectric pentacene thin film transistors", *Journal of Applied Physics,* vol. 92, no. 9, pp. 5259.
73. Lee, S., Koo, B., Shin, J., Lee, E., Park, H. & Kim, H. 2006, "Effects of hydroxyl groups in polymeric dielectrics on organic transistor performance", *Applied Physics Letters,* vol. 88, no. 16, pp. 162109-1.
74. Okamoto, H., Kawasaki, N., Kaji, Y., Kubozono, Y., Fujiwara, A. & Yamaji, M. 2008, "Air-assisted high-performance field-effect transistor with thin films of picene", *Journal of the American Chemical Society,* vol. 130, no. 32, pp. 10470-10471.
75. Ebata, H., Izawa, T., Miyazaki, E., Takimiya, K., Ikeda, M., Kuwabara, H. & Yui, T. 2007, "Highly soluble [1]benzothieno[3,2-b]benzothiophene (BTBT) derivatives for high-performance, solution-processed organic field-effect transistors", *Journal of the American Chemical Society,* vol. 129, no. 51, pp. 15732-15733.
76. Yamamoto, T. & Takimiya, K. 2007, "Facile synthesis of highly π-extended heteroarenes, dinaphtho[2,3-b:2′,3′-f]chalcogenopheno[3,2-b]chalcogenophenes, and their application to field-effect transistors", *Journal of the American Chemical Society,* vol. 129, no. 8, pp. 2224-2225.
77. Sheraw, C.D., Jackson, T.N., Eaton, D.L. & Anthony, J.E. 2003, "Functionalized pentacene active layer organic thin-film transistors", *Advanced Materials,* vol. 15, no. 23, pp. 2009-2011.
78. Payne, M.M., Parkin, S.R., Anthony, J.E., Kuo, C.-C. & Jackson, T.N. 2005, "Organic field-effect transistors from solution-deposited functionalized acenes with mobilities as high as 1 cm2/V·s", *Journal of the American Chemical Society,* vol. 127, no. 14, pp. 4986-4987.
79. Gundlach, D.J., Nichols, J.A., Zhou, L. & Jackson, T.N. 2002, "Thin-film transistors based on well-ordered thermally evaporated naphthacene films", *Applied Physics Letters,* vol. 80, no. 16, pp. 2925-2927.
80. Cicoira, F., Santato, C., Dinelli, F., Murgia, M., Loi, M.A., Biscarini, F., Zamboni, R., Heremans, P. & Muccini, M. 2005, "Correlation between morphology and field-effect-transistor mobility in tetracene thin films", *Advanced Functional Materials,* vol. 15, no. 3, pp. 375-380.
81. De Boer, R.W.I., Klapwijk, T.M. & Morpurgo, A.F. 2003, "Field-effect transistors on tetracene single crystals", *Applied Physics Letters,* vol. 83, no. 21, pp. 4345-4347.
82. Lim, S.H., Bjorklund, T.G., Spano, F.C. & Bardeen, C.J. 2004, "Exciton Delocalization and Superradiance in Tetracene Thin Films and Nanoaggregates", *Physical Review Letters,* vol. 92, no. 10, pp. 107402-1.

83. Takeya, J., Yamagishi, M., Tominari, Y., Hirahara, R., Nakazawa, Y., Nishikawa, T., Kawase, T., Shimoda, T. & Ogawa, S. 2007, "Very high-mobility organic single-crystal transistors with in-crystal conduction channels", *Applied Physics Letters,* vol. 90, no. 10, pp. 102120-1.
84. Eley, D.D., Parfitt, G.D., Perry, M.J. & Taysum, D.H. 1953, "The semiconductivity of organic substances. Part 1", *Transactions of the Faraday Society,* vol. 49, pp. 79-86.
85. Barbe, D.F. & Westgate, C.R. 1970, "Surface state parameters of metal-free phthalocyanine single crystals", *Journal of Physics and Chemistry of Solids,* vol. 31, no. 12, pp. 2679-2687.
86. Madru, R., Guillaud, G., Al Sadoun, M., Maitrot, M., André, J.J., Simon, J. & Even, R. 1988, "A well-behaved field effect transistor based on an intrinsic molecular semiconductor", *Chemical Physics Letters,* vol. 145, no. 4, pp. 343-346.
87. Clarisse, C. & Riou, M.T. 1991, "The operation and characteristics of diphthalocyanine field effect transistors", *Journal of Applied Physics,* vol. 69, no. 5, pp. 3324-3327.
88. Bao, Z., Lovinger, A.J. & Dodabalapur, A. 1996, "Organic field-effect transistors with high mobility based on copper phthalocyanine", *Applied Physics Letters,* vol. 69, no. 20, pp. 3066-3068.
89. Sirringhaus, H., Tessler, N. & Friend, R.H. 1998, "Integrated optoelectronic devices based on conjugated polymers", *Science,* vol. 280, no. 5370, pp. 1741-1744.
90. Wang, G., Swensen, J., Moses, D. & Heeger, A.J. 2003, "Increased mobility from regioregular poly(3-hexylthiophene) field-effect transistors", *Journal of Applied Physics,* vol. 93, no. 10 1, pp. 6137-6141.
91. Dimitrakopoulos, C.D. & Malenfant, P.R.L. 2002, "Organic thin film transistors for large area electronics", *Advanced Materials,* vol. 14, no. 2, pp. 99-117.
92. Haddon, R.C., Perel, A.S., Morris, R.C., Palstra, T.T.M., Hebard, A.F. & Fleming, R.M. 1995, "C60 thin film transistors", *Applied Physics Letters,* vol. 67, pp. 121.
93. Laquindanum, J.G., Katz, H.E., Dodabalapur, A. & Lovinger, A.J. 1996, "n-Channel organic transistor materials based on naphthalene frameworks", *Journal of the American Chemical Society,* vol. 118, no. 45, pp. 11331-11332.
94. Bao, Z., Lovinger, A.J. & Brown, J. 1998, "New air-stable n-channel organs thin film transistors", *Journal of the American Chemical Society,* vol. 120, no. 1, pp. 207-208.
95. Katz, H.E., Lovinger, A.J., Johnson, J., Kloc, C., Siegrist, T., Li, W., Lin, Y.Y. & Dodabalapur, A. 2000, "A soluble and air-stable organic semiconductor with high electron mobility", *Nature,* vol. 404, no. 6777, pp. 478-481.
96. Facchetti, A., Deng, Y., Wang, A., Koide, Y., Sirringhaus, H., Marks, T.J. & Friend, R.H. 2000, "Tuning the semiconducting properties of sexithiophene by α,ω-substitution-α,ω-diperfluorohexylsexithiophene: The first n-type sexi-thiophene for thin-film transistors", *Angewandte Chemie - International Edition,* vol. 39, no. 24, pp. 4547-4551.

97. Malenfant, P.R.L., Dimitrakopoulos, C.D., Gelorme, J.D., Kosbar, L.L., Graham, T.O., Curioni, A. & Andreoni, W. 2002, "N-type organic thin-film transistor with high field-effect mobility based on a N,N′-dialkyl-3,4,9,10-perylene tetracarboxylic diimide derivative", *Applied Physics Letters,* vol. 80, no. 14, pp. 2517.
98. Kobayashi, S., Takenobu, T., Mon, S., Fujiwara, A. & Iwasa, Y. 2003, "Fabrication and characterization of C60 thin-film transistors with high field-effect mobility", *Applied Physics Letters,* vol. 82, no. 25, pp. 4581-4583.
99. Babel, A. & Jenekhe, S.A. 2003, "High Electron Mobility in Ladder Polymer Field-Effect Transistors", *Journal of the American Chemical Society,* vol. 125, no. 45, pp. 13656-13657.
100. Chesterfield, R.J., McKeen, J.C., Newman, C.R., Ewbank, P.C., Da Silva Filho, D.A., Brédas, J.-., Miller, L.L., Mann, K.R. & Frisbie, C.D. 2004, "Organic thin film transistors based on N-alkyl perylene diimides: Charge transport kinetics as a function of gate voltage and temperature", *Journal of Physical Chemistry B,* vol. 108, no. 50, pp. 19281-19292.
101. Jones, B.A., Ahrens, M.J., Yoon, M.H., Facchetti, A., Marks, T.J. & Wasielewski, M.R. 2004, "High-mobility air-stable n-type semiconductors with processing versatility: Dicyanoperylene-3,4:9,10-bis(dicarboximides)", *Angewandte Chemie - International Edition,* vol. 43, no. 46, pp. 6363-6366.
102. Facchetti, A., Mushrush, M., Yoon, M.-., Hutchison, G.R., Ratner, M.A. & Marks, T.J. 2004, "Building blocks for n-type molecular and polymeric electronics. Perfluoroalkyl- versus alkyl-functionalized oligothiophenes (nT; n = 2-6). Systematics of thin film microstructure, semiconductor performance, and modeling of majority charge injection in field-effect transistors", *Journal of the American Chemical Society,* vol. 126, no. 42, pp. 13859-13874.
103. Yoon, M.H., DiBenedetto, S.A., Facchetti, A. & Marks, T.J. 2005, "Organic thin-film transistors based on carbonyl-functionalized quaterthiophenes: High mobility N-channel semiconductors and ambipolar transport", *Journal of the American Chemical Society,* vol. 127, no. 5, pp. 1348-1349.
104. Ando, S., Murakami, R., Nishida, J.I., Tada, H., Inoue, Y., Tokito, S. & Yamashita, Y. 2005, "n-type organic field-effect transistors with very high electron mobility based on thiazole oligomers with trifluoromethylphenyl groups", *Journal of the American Chemical Society,* vol. 127, no. 43, pp. 14996-14997.
105. Yoon, M.H., Facchetti, A., Stern, C.E. & Marks, T.J. 2006, "Fluorocarbon-modified organic semiconductors: Molecular architecture, electronic, and crystal structure tuning of arene- versus fluoroarene-thiophene oligomer thin-film properties", *Journal of the American Chemical Society,* vol. 128, no. 17, pp. 5792-5801.
106. Inoue, Y., Sakamoto, Y., Suzuki, T., Kobayashi, M., Gao, Y. & Tokito, S. 2005, "Organic thin-film transistors with high electron mobility based on perfluoropentacene", *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* vol. 44, no. 6 A, pp. 3663-3668.

107. Itaka, K., Yamashiro, M., Yamaguchi, J., Haemori, M., Yaginuma, S., Matsumoto, Y., Kondo, M. & Koinuma, H. 2006, "High-mobility C60 field-effect transistors fabricated on molecular-wetting controlled substrates", *Advanced Materials,* vol. 18, no. 13, pp. 1713-1716.
108. Anthopoulos, T.D., Singh, B., Marjanovic, N., Sariciftci, N.S., Montaigne Ramil, A., Sitter, H., Cölle, M. & De Leeuw, D.M. 2006, "High performance n -channel organic field-effect transistors and ring oscillators based on C60 fullerene films", *Applied Physics Letters,* vol. 89, no. 21, pp. 213504-1.
109. Kumaki, D., Ando, S., Shimono, S., Yamashita, Y., Umeda, T. & Tokito, S. 2007, "Significant improvement of electron mobility in organic thin-film transistors based on thiazolothiazole derivative by employing self-assembled monolayer", *Applied Physics Letters,* vol. 90, no. 5, pp. 053506-1.
110. Wang, H., Zhu, F., Yang, J., Geng, Y. & Yan, D. 2007, "Weak epitaxy growth affording high-mobility thin films of disk-like organic semiconductors", *Advanced Materials,* vol. 19, no. 16, pp. 2168-2171.
111. Schmidt, R., Ling, M.M., Oh, J.H., Winkler, M., Könemann, M., Bao, Z. & Würthner, F. 2007, "Core-fluorinated perylene bisimide dyes: Air stable n-channel organic semiconductors for thin film transistors with exceptionally high on-to-off current ratios", *Advanced Materials,* vol. 19, no. 21, pp. 3692-3695.
112. Tang, M.L., Reichardt, A.D., Miyaki, N., Stoltenberg, R.M. & Bao, Z. 2008, "Ambipolar, high performance, acene-based organic thin film transistors", *Journal of the American Chemical Society,* vol. 130, no. 19, pp. 6064-6065.
113. Chikamatsu, M., Itakura, A., Yoshida, Y., Azumi, R. & Yase, K. 2008, "High-performance n-type organic thin-film transistors based on soiution-processable perfluoroalkyl-substituted C60 derivatives", *Chemistry of Materials,* vol. 20, no. 24, pp. 7365-7367.
114. See, K.C., Landis, C., Sarjeant, A. & Katz, H.E. 2008, "Easily synthesized naphthalene tetracarboxylic diimide semiconductors with high electron mobility in air", *Chemistry of Materials,* vol. 20, no. 11, pp. 3609-3616.
115. Tan, H.S., Mathews, N., Cahyadi, T., Zhu, F.R. & Mhaisalkar, S.G. 2009, "The effect of dielectric constant on device mobilities of high-performance, flexible organic field effect transistors", *Applied Physics Letters,* vol. 94, no. 26, pp. 263303-1.
116. Yan, H., Chen, Z., Zheng, Y., Newman, C., Quinn, J.R., Dötz, F., Kastler, M. & Facchetti, A. 2009, "A high-mobility electron-transporting polymer for printed transistors", *Nature,* vol. 457, no. 7230, pp. 679-686.
117. Schmidt, R., Oh, J.H., Sun, Y.-S., Deppisch, M., Krause, A.M., Radacki, K., Braunschweig, H., Könemann, M., Erk, P., Bao, Z. & Würthner, F. 2009, "High-performance air-stable n-channel organic thin film transistors based on halogenated perylene bisimide semiconductors", *Journal of the American Chemical Society,* vol. 131, no. 17, pp. 6215-6228.
118. Gsänger, M., Oh, J.H., Könemann, M., Höffken, H.W., Krause, A.M., Bao, Z. & Würthner, F. 2010, "A crystal-engineered hydrogen-bonded

octachloroperylene diimide with a twisted core: An n-channel organic semiconductor", *Angewandte Chemie - International Edition,* vol. 49, no. 4, pp. 740-743.

119. Gao, X., Di, C.A., Hu, Y., Yang, X., Fan, H., Zhang, F., Liu, Y., Li, H. & Zhu, D. 2010, "Core-expanded naphthalene diimides fused with 2-(1,3-Dithiol-2-Ylidene) malonitrile groups for high-performance, ambient-stable, solution-processed n-channel organic thin film transistors", *Journal of the American Chemical Society,* vol. 132, no. 11, pp. 3697-3699.
120. Osaka, I., Abe, T., Shinamura, S., Miyazaki, E. & Takimiya, K. 2010, "High-mobility semiconducting naphthodithiophene copolymers", *Journal of the American Chemical Society,* vol. 132, no. 14, pp. 5000-5001.
121. Salaneck, W. R., Stafström, S., Brédas, J. L. 1996, "Conjugated Polymer Surfaces and Interfaces", *Cambridge University Press*, Cambridge.
122. Horowitz, G. 1998, "Organic field-effect transistors", *Advanced Materials,* vol. 10, no. 5, pp. 365-377.
123. Holstein, T. 1959, "Studies of polaron motion. Part II. The "small" polaron", *Annals of Physics,* vol. 8, no. 3, pp. 343-389.
124. Pai, D.M. 1970, "Transient photoconductivity in poly(W-vinylcarbazole)", *The Journal of chemical physics,* vol. 52, no. 5, pp. 2285-2291.
125. Frenkel, J. 1938, "On pre-breakdown phenomena in insulators and electronic semi-conductors [3]", *Physical Review,* vol. 54, no. 8, pp. 647-648.
126. Coropceanu, V., Cornil, J., da Silva Filho, D.A., Olivier, Y., Silbey, R. & Brédas, J.L. 2007, "Charge transport in organic semiconductors", *Chemical reviews,* vol. 107, no. 4, pp. 926-952.
127. Mushrush, M., Facchetti, A., Lefenfeld, M., Katz, H.E. & Marks, T.J. 2003, "Easily processable phenylene-thiophene-based organic field-effect transistors and solution-fabricated nonvolatile transistor memory elements", *Journal of the American Chemical Society,* vol. 125, no. 31, pp. 9414-9423.
128. Katz, H.E., Bao, Z. & Gilat, S.L. 2001, "Synthetic chemistry for ultrapure, processable, and high-mobility organic transistor semiconductors", *Accounts of Chemical Research,* vol. 34, no. 5, pp. 359-369.
129. Bao, Z., Lovinger, A.J. & Dodabalapur, A. 1997, "Highly ordered vacuum-deposited thin films of metallophthalocyanines and their applications in field-effect transistors", *Advanced Materials,* vol. 9, no. 1, pp. 42-44.
130. Kelley, T.W., Boardman, L.D., Dunbar, T.D., Muyres, D.V., Pellerite, M.J. & Smith, T.P. 2003, "High-performance OTFTs using surface-modified alumina dielectrics", *Journal of Physical Chemistry B,* vol. 107, no. 24, pp. 5877-5881.
131. Chapman, S. & Cowling, T.G. 1990, "The mathematical theory of non-uniform gases", 3rd. edition, *Cambridge University Press*.

132. Choo, M.H., Kim, J.H. & Im, S. 2002, "Hole transport in amorphous-crystalline-mixed and amorphous pentacene thin-film transistors", *Applied Physics Letters,* vol. 81, no. 24, pp. 4640-4642.
133. Shtein, M., Mapel, J., Benziger, J.B. & Forrest, S.R. 2002, "Effects of film morphology and gate dielectric surface preparation on the electrical characteristics of organic-vapor-phase-deposited pentacene thin-film transistors", Applied Physics Letters, vol. 81, no. 2, pp. 268.
134. Pratontep, S., Brinkmann, M., Nüesch, F. & Zuppiroli, L. 2004, "Nucleation and growth of ultrathin pentacene films on silicon dioxide: Effect of deposition rate and substrate temperature", Synthetic Metals, vol. 146, no. 3, pp. 387-391.
135. Kelley, T.W. & Frisbie, C.D. 2001, "Gate voltage dependent resistance of a single organic semiconductor grain boundary", Journal of Physical Chemistry B, vol. 105, no. 20, pp. 4538-4540.
136. Minakata, T., Imai, H. & Ozaki, M. 1992, "Electrical properties of highly ordered and amorphous thin films of pentacene doped with iodine", Journal of Applied Physics, vol. 72, no. 9, pp. 4178-4182.
137. Minakata, T., Ozaki, M. & Imai, H. 1993, "Conducting thin films of pentacene doped with alkaline metals", Journal of Applied Physics, vol. 74, no. 2, pp. 1079-1082.
138. Dodabalapur, A., Torsi, L. & Katz, H.E. 1995, "Organic transistors: Two-dimensional transport and improved electrical characteristics", Science, vol. 268, no. 5208, pp. 270-271.
139. Dinelli, F., Murgia, M., Levy, P., Cavallini, M., Biscarini, F. & De Leeuw, D.M. 2004, "Spatially Correlated Charge Transport in Organic Thin Film Transistors", Physical Review Letters, vol. 92, no. 11, pp. 116802-1.
140. Ruiz, R., Papadimitratos, A., Mayer, A.C. & Malliaras, G.G. 2005, "Thickness dependence of mobility in pentacene thin-film transistors", Advanced Materials, vol. 17, no. 14, pp. 1795-1798.
141. Kobayashi, S., Nishikawa, T., Takenobu, T., Mori, S., Shimoda, T., Mitani, T., Shimotani, H., Yoshimoto, N., Ogawa, S. & Iwasa, Y. 2004, "Control of carrier density by self-assembled monolayers in organic field-effect transistors", Nature Materials, vol. 3, no. 5, pp. 317-322.
142. Sirringhaus, H., Kawase, T., Friend, R.H., Shimoda, T., Inbasekaran, M., Wu, W. & Woo, E.P. 2000, "High-resolution inkjet printing of all-polymer transistor circuits", Science, vol. 290, no. 5499, pp. 2123-2126.
143. Choi, H.Y., Kim, S.H. & Jang, J. 2004, "Self-organized organic thin-film transistors on plastic", Advanced Materials, vol. 16, no. 8, pp. 732-736.
144. Uemura, S., Yoshida, M., Hoshino, S., Kodzasa, T. & Kamata, T. 2003, "Investigation for surface modification of polymer as an insulator layer of organic FET", Thin Solid Films, vol. 438-439, pp. 378-381.
145. Veres, J., Ogier, S.D., Leeming, S.W., Cupertino, D.C. & Khaffaf, S.M. 2003, "Low-k insulators as the choice of dielectrics in organic field-effect transistors", Advanced Functional Materials, vol. 13, no. 3, pp. 199-204.
146. Lim, S.C., Kim, S.H., Lee, J.H., Kim, M.K., Kim, D.J. & Zyung, T. 2005, "Surface-treatment effects on organic thin-film transistors", Synthetic Metals, vol. 148, no. 1, pp. 75-79.

147. Lee, M.W. & Song, C.K. 2003, "Oxygen plasma effects on performance of pentacene thin film transistor", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 42, no. 7 A, pp. 4218-4221.
148. Wang, A., Kymissis, I., Bulović, V. & Akinwande, A.I. 2006, "Engineering density of semiconductor-dielectric interface states to modulate threshold voltage in OFETs", IEEE Transactions on Electron Devices, vol. 53, no. 1, pp. 9-13.
149. Kim, W.K., Hong, K. & Lee, J.L. 2006, "Enhancement of hole injection in pentacene organic thin-film transistor of O2 plasma-treated Au electrodes", Applied Physics Letters, vol. 89, no. 14, PP.142117-1.
150. Kang, S., Park, J., Jung, S., Lee, H.J., Son, P., Kim, J.C., Yoon, T.H. & Yi, M. 2007, "Performance enhancement of organic thin-film transistors by low-energy argon ion beam treatment of gate dielectric surface", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 46, no. 4 B, pp. 2696-2699.
151. Lee, J.W., Chang, J.W., Kim, D.J., Yoon, Y.S. & Kim, J.K. 2007, "Performance improvement of organic thin-film transistors by electrode/pentacene interface treatment using a hydrogen plasma", IEEE Electron Device Letters, vol. 28, no. 5, pp. 379-382.
152. Fan, C.L., Yang, T.H., Lin, C.C. & Huang, C.H. 2008, "N2O-plasma effect on low-temperature deposited gate dielectric for organic thin-film transistors", Electronics Letters, vol. 44, no. 19, pp. 1158-1160.
153. Salleo, A., Chabinyc, M.L., Yang, M.S. & Street, R.A. 2002, "Polymer thin-film transistors with chemically modified dielectric interfaces", *Applied Physics Letters,* vol. 81, no. 23, pp. 4383-4385.
154. Pernstich, K.P., Haas, S., Oberhoff, D., Goldmann, C., Gundlach, D.J., Batlogg, B., Rashid, A.N. & Schitter, G. 2004, "Threshold voltage shift in organic field effect transistors by dipole monolayers on the gate insulator", *Journal of Applied Physics,* vol. 96, no. 11, pp. 6431-6438.
155. Yoshida, M., Uemura, S., Kodzasa, T., Kamata, T., Matsuzawa, M. & Kawai, T. 2003, "Surface potential control of an insulator layer for the high performance organic FET", Synthetic Metals, vol. 137, no. 1-3, pp. 967-968.
156. Yoon, M.H., Kim, C., Facchetti, A. & Marks, T.J. 2006, "Gate dielectric chemical structure-organic field-effect transistor performance correlations for electron, hole, and ambipolar organic semiconductors", Journal of the American Chemical Society, vol. 128, no. 39, pp. 12851-12869.
157. Kim, C., Facchetti, A. & Marks, T.J. 2007, "Gate dielectric microstructural control of pentacene film growth mode and field-effect transistor performance", Advanced Materials, vol. 19, no. 18, pp. 2561-2566.
158. Chua, L.L., Zaumseil, J., Chang, J.F., Ou, E.C.W., Ho, P.K.H., Sirringhaus, H. & Friend, R.H. 2005, "General observation of n-type field-effect behaviour in organic semiconductors", Nature, vol. 434, no. 7030, pp. 194-199.
159. Zhang, X.H., Tiwari, S.P. & Kippelen, B. 2009, "Pentacene organic field-effect transistors with polymeric dielectric interfaces:

Performance and stability", Organic Electronics: physics, materials, applications, vol. 10, no. 6, pp. 1133-1140.
160. Katz, H.E., Hong, X.M., Dodabalapur, A. & Sarpeshkar, R. 2002, "Organic field-effect transistors with polarizable gate insulators", Journal of Applied Physics, vol. 91, no. 3, pp. 1572.
161. Baeg, K.J., Noh, Y.Y., Ghim, J., Kang, S.J., Lee, H. & Kim, D.Y. 2006, "Organic non-volatile memory based on pentacene field-effect transistors using a polymeric gate electret", Advanced Materials, vol. 18, no. 23, pp. 3179-3183.
162. Narayan, K.S. & Kumar, N. 2001, "Light responsive polymer field-effect transistor", Applied Physics Letters, vol. 79, no. 12, pp. 1891-1893.
163. Hoshino, S., Yoshida, M., Uemura, S., Kodzasa, T., Takada, N., Kamata, T. & Yase, K. 2004, "Influence of moisture on device characteristics of polythiophene-based field-effect transistors", Journal of Applied Physics, vol. 95, no. 9, pp. 5088-5093.
164. Jung, T., Dodabalapur, A., Wenz, R. & Mohapatra, S. 2005, "Moisture induced surface polarization in a poly(4-vinyl phenol) dielectric in an organic thin-film transistor", Applied Physics Letters, vol. 87, no. 18, pp. 182109-1.
165. Ucurum, C., Goebel, H., Yildirim, F.A., Bauhofer, W. & Krautschneider, W. 2008, "Hole trap related hysteresis in pentacene field-effect transistors", Journal of Applied Physics, vol. 104, no. 8, pp. 084501-1.
166. Goldmann, C., Gundlach, D.J. & Batlogg, B. 2006, "Evidence of water-related discrete trap state formation in pentacene single-crystal field-effect transistors", Applied Physics Letters, vol. 88, no. 6, pp. 063501.
167. Gu, G. & Kane, M.G. 2008, "Moisture induced electron traps and hysteresis in pentacene-based organic thin-film transistors", Applied Physics Letters, vol. 92, no. 5, pp. 053305-1.
168. Ng, T.N., Daniel, J.H., Sambandan, S., Arias, A.-C., Chabinyc, M.L. & Street, R.A. 2008, "Gate bias stress effects due to polymer gate dielectrics in organic thin-film transistors", Journal of Applied Physics, vol. 103, no. 4, pp. 044506-1.
169. Yun, Y., Pearson, C. & Petty, M.C. 2009, "Pentacene thin film transistors with a poly(methyl methacrylate) gate dielectric: Optimization of device performance", Journal of Applied Physics, vol. 105, no. 3, pp. 034508-1.
170. Kim, S.H., Jang, J., Jeon, H., Yun, W.M., Nam, S. & Park, C.E. 2008, "Hysteresis-free pentacene field-effect transistors and inverters containing poly(4-vinyl phenol-co-methyl methacrylate) gate dielectrics", Applied Physics Letters, vol. 92, no. 18, pp. 183306-1.
171. Liu, P., Wu, Y., Li, Y., Ong, B.S. & Zhu, S. 2006, "Enabling gate dielectric design for all solution-processed, high-performance, flexible organic thin-film transistors", Journal of the American Chemical Society, vol. 128, no. 14, pp. 4554-4555.
172. Brown, A.R., Jarrett, C.P., De Leeuw, D.M. & Matters, M. 1997, "Field-effect transistors made from solution-processed organic semiconductors", Synthetic Metals, vol. 88, no. 1, pp. 37-55.

173. Horowitz, G., Hajlaoui, M.E. & Hajlaoui, R. 2000, "Temperature and gate voltage dependence of hole mobility in polycrystalline oligothiophene thin film transistors", Journal of Applied Physics, vol. 87, no. 9 I, pp. 4456-4463.
174. Orton, J.W. & Powell, M.J. 1980, "The hall effect in polycrystalline and powdered semiconductors", Reports on Progress in Physics, vol. 43, no. 11, pp. 1263-1307.
175. Mathijssen, S.G.J., Cölle, M., Gomes, H., Smits, E.C.P., De Boer, B., McCulloch, I., Bobbert, P.A. & De Leeuw, D.M. 2007, "Dynamics of threshold voltage shifts in organic and amorphous silicon field-effect transistors", Advanced Materials, vol. 19, no. 19, pp. 2785-2789.
176. Goldmann, C., Krellner, C., Pernstich, K.P., Haas, S., Gundlach, D.J. & Batlogg, B. 2006, "Determination of the interface trap density of rubrene single-crystal field-effect transistors and comparison to the bulk trap density", Journal of Applied Physics, vol. 99, no. 3, pp. 034507-1.
177. Yasuda, T., Goto, T., Fujita, K. & Tsutsui, T. 2004, "Ambipolar pentacene field-effect transistors with calcium source-drain electrodes", Applied Physics Letters, vol. 85, no. 11, pp. 2098-2100.
178. Dodabalapur, A., Katz, H.E., Torsi, L. & Haddon, R.C. 1995, "Organic heterostructure field-effect transistors", Science, vol. 269, no. 5230, pp. 1560-1562.
179. Liu, Z., Xue, F., Su, Y., Lvov, Y.M. & Varahramyan, K. 2006, "Memory effect of a polymer thin-film transistor with self-assembled gold nanoparticles in the gate dielectric", IEEE Transactions on Nanotechnology, vol. 5, no. 4, pp. 379-384.
180. Zhang, X.H., Domercq, B. & Kippelen, B. 2007, "High-performance and electrically stable C60 organic field-effect transistors", Applied Physics Letters, vol. 91, no. 9, pp. 092114-1.
181. Podzorov, V. & Gershenson, M.E. 2005, "Photoinduced charge transfer across the interface between organic molecular crystals and polymers", Physical Review Letters, vol. 95, no. 1, pp. 016602-1.
182. Guo, Y., Di, C.A., Ye, S., Sun, X., Zheng, J., Wen, Y., Wu, W., Yu, G. & Liu, Y. 2009, "Multibit storage of organic thin-film field-effect transistors", Advanced Materials, vol. 21, no. 19, pp. 1954-1959.
183. Baeg, K.J., Noh, Y.Y., Ghim, J., Lim, B. & Kim, D.Y. 2008, "Polarity effects of polymer gate electrets on non-volatile organic field-effect transistor memory", Advanced Functional Materials, vol. 18, no. 22, pp. 3678-3685.
184. Chen, H., Gong, H. & Ong, C.K. 1995, "The charging behaviour and internal electric field of PMMA irradiated by a kiloelectronvolt electron beam", Journal of Physics: Condensed Matter, vol. 7, no. 6, pp. 1129-1137.
185. Taylor, R., Parsons, J.P., Avent, A.G., Rannard, S.P., Dennis, T.J., Hare, J.P., Kroto, H.W. & Walton, D.R.M. 1991, "Degradation of C60 by light", Nature, vol. 351, no. 6324, pp. 277.
186. Sullivan, P. & Jones, T.S. 2008, "Pentacene/fullerene (C60) heterojunction solar cells: Device performance and degradation mechanisms", Organic Electronics: physics, materials, applications, vol. 9, no. 5, pp. 656-660.

187. Potscavage, W.J., Yoo, S., Domercq, B. & Kippelen, B. 2007, "Encapsulation of pentacene/C60 organic solar cells with Al 2O3 deposited by atomic layer deposition", Applied Physics Letters, vol. 90, no. 25, pp. 253511-1.
188. Kalb, W.L., Mathis, T., Haas, S., Stassen, A.F. & Batlogg, B. 2007, "Organic small molecule field-effect transistors with Cytop™ gate dielectric: Eliminating gate bias stress effects", Applied Physics Letters, vol. 90, no. 9, pp. 092104-1.
189. Braga, D. & Horowitz, G. 2009, "High-Performance organic field-effect transistors", Advanced Materials, vol. 21, no. 14-15, pp. 1473-1486.
190. Said, E., Crispin, X., Herlogsson, L., Elhag, S., Robinson, N.D. & Berggren, M. 2006, "Polymer field-effect transistor gated via a poly(styrenesulfonic acid) thin film", Applied Physics Letters, vol. 89, no. 14, pp. 143507-1.
191. Herlogsson, L., Crispin, X., Robinson, N.D., Sandberg, M., Hagel, O.-., Gustafsson, G. & Berggren, M. 2007, "Low-voltage polymer field-effect transistors gated via a proton conductor", Advanced Materials, vol. 19, no. 1, pp. 97-101.
192. Zirkl, M., Haase, A., Fian, A., Schön, H., Sommer, C., Jakopic, G., Leising, G., Stadlober, B., Graz, I., Gaar, N., Schwödiauer, R., Bauer-Gogonea, S. & Bauer, S. 2007, "Low-voltage organic thin-film transistors with high-k nanocomposite gate dielectrics for flexible electronics and optothermal sensors", Advanced Materials, vol. 19, no. 17, pp. 2241-2245.
193. Hwang, D.K., Kim, C.S., Choi, J.M., Lee, K., Park, J.H., Kim, E., Baik, H.K., Kim, J.H. & Im, S. 2006, "Polymer/YOx hybrid-sandwich gate dielectrics for semitransparent pentacene thin-film transistors operating under 5 V", Advanced Materials, vol. 18, no. 17, pp. 2299-2303.
194. Dimitrakopoulos, C.D., Kymissis, I., Purushothaman, S., Neumayer, D.A., Duncombe, P.R. & Laibowitz, R.B. 1999, "Low-voltage, high-mobility pentacene transistors with solution-processed high dielectric constant insulators", Advanced Materials, vol. 11, no. 16, pp. 1372-1375.
195. Ezhilvalavan, S. & Tseng, T.-Y. 2000, "Progress in the developments of (Ba,Sr)TiO3 (BST) thin films for Gigabit era DRAMs", Materials Chemistry and Physics, vol. 65, no. 3, pp. 227-248.
196. Scott, J.F. 1999, "Device physics of ferroelectric thin-film memories", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 38, no. 4 B, pp. 2272-2274.
197. Wilk, G.D., Wallace, R.M. & Anthony, J.M. 2001, "High-κ gate dielectrics: Current status and materials properties considerations", Journal of Applied Physics, vol. 89, no. 10, pp. 5243-5275.
198. Ortiz, R.P., Facchetti, A. & Marks, T.J. 2010, "High-k organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors", Chemical reviews, vol. 110, no. 1, pp. 205-239.
199. Kukli, K., Ritala, M., Sundqvist, J., Aarik, J., Lu, J., Sajavaara, T., Leskelä, M. & Hårsta, A. 2002, "Properties of hafnium oxide films grown by atomic layer deposition from hafnium tetraiodide and oxygen", Journal of Applied Physics, vol. 92, no. 10, pp. 5698-5703.

200. Koyama, M., Kaneko, A., Ino, T., Koike, M., Kamata, Y., Iijima, R., Kamimuta, Y., Takashima, A., Suzuki, M., Hongo, C., Inumiya, S., Takayanagi, M. & Nishiyama, A. 2002, "Effects of nitrogen in HfSiON gate dielectric on the electrical and thermal characteristics", Technical Digest - International Electron Devices Meeting, pp. 849.
201. Zhu, W.J., Tamagawa, T., Gibson, M., Furukawa, T. & Ma, T.P. 2002, "Effect of Al inclusion in HfO2 on the physical and electrical properties of the dielectrics", IEEE Electron Device Letters, vol. 23, no. 11, pp. 649-651.
202. Choi, C.H., Rhee, S.J., Jeon, T.S., Lu, N., Sim, J.H., Clark, R., Niwa, M. & Kwong, D.L. 2002, "Thermally stable CVD HfOxNy advanced gate dielectrics with poly-Si gate electrode", Technical Digest - International Electron Devices Meeting, pp. 857.
203. Kang, C.S., Cho, H.-J., Onishi, K., Choi, R., Kim, Y.H., Nieh, R., Han, J., Krishnan, S., Shahriar, A. & Lee, J.C. 2002, "Nitrogen concentration effects and performance improvement of MOSFETs using thermally stable HfOxNy gate dielectrics", Technical Digest - International Electron Devices Meeting, pp. 865.
204. Akbar, M.S., Gopalan, S., Cho, H.-J., Onishi, K., Choi, R., Nieh, R., Kang, C.S., Kim, Y.H., Han, J., Krishnan, S. & Lee, J.C. 2003, "High-performance TaN/HfSiON/Si metal-oxide-semiconductor structures prepared by NH3 post-deposition anneal", Applied Physics Letters, vol. 82, no. 11, pp. 1757-1759.
205. Wang, J.C., Shie, D.C., Lei, T.F. & Lee, C.L. 2003, "Characterization of temperature dependence for HfO2 gate dielectrics treated in NH3 plasma", Electrochemical and Solid-State Letters, vol. 6, no. 10, pp. F34-F36.
206. Lai, C.S., Wu, W.C., Fan, K.M., Wang, J.C. & Lin, S.J. 2005, "Effects of post CF4 plasma treatment on the HfO2 thin film", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 44, no. 4 B, pp. 2307-2310.
207. Acton, O., Dubey, M., Weidner, T., O'Malley, K.M., Kim, T.-W., Ting, G.G., Hutchins, D., Baio, J.E., Lovejoy, T.C., Gage, A.H., Castner, D.G., Ma, H. & Jen, A.K.-Y. 2011, "Simultaneous modification of bottom-contact electrode and dielectric surfaces for organic thin-film transistors through single-component spin-cast monolayers", Advanced Functional Materials, vol. 21, no. 8, pp. 1476-1488.
208. Zhang, X.-H., Tiwari, S.P., Kim, S.-J. & Kippelen, B. 2009, "Low-voltage pentacene organic field-effect transistors with high-κ HfO2 gate dielectrics and high stability under bias stress", Applied Physics Letters, vol. 95, no. 22, pp. 223302-1.
209. Masaki, G., Naka, S. & Okada, H. 2008, "Organic field-effect transistors with high-κ HfO2/resin double gate insulator", Journal of Photopolymer Science and Technology, vol. 21, no. 2, pp. 189-192.
210. Wang, Y., Acton, O., Ting, G., Weidner, T., Ma, H., Castner, D.G. & Jen, A.K.-Y. 2009, "Low-voltage high-performance organic thin film transistors with a thermally annealed polystyrene/hafnium oxide dielectric", Applied Physics Letters, vol. 95, no. 24, pp. 243302-1.
211. Yu, A., Qi, Q., Jiang, P. & Jiang, C. 2009, "The effects of hydroxyl-free polystyrene buffer layer on electrical performance of pentacene-based

thin-film transistors with high-k oxide gate dielectric", Synthetic Metals, vol. 159, no. 14, pp. 1467-1470.

212. Nishizawa, R., Naka, S., Okada, H., Suzuki, K. & Kato, K. 2010, "Organic thin-film transistors with tailored liquid sources of HfO 2 as a high-κ insulator", Japanese Journal of Applied Physics, vol. 49, no. 4 PART 2.
213. Kim, Y.-H., Kwon, J.-H., Shin, S.-I., Oh, B.-Y., Park, H.-G., Paek, K.-K., Ju, B.-K. & Seo, D.-S. 2009, "Organization of pentacene molecules on anisotropic ultrathin HfO2/Al2O3 templates for organic thin-film transistors using an ion-beam treatment", Electrochemical and Solid-State Letters, vol. 12, no. 8, pp. H305-H308.
214. Tang, W.M., Helander, M.G., Greiner, M.T., Dong, G., Ng, W.T. & Lu, Z.H. 2009, "Enhanced performance for OTFT on glass with HfO2 as gate dielectric by UV-ozone treatment", 2009 IEEE International Conference on Electron Devices and Solid-State Circuits, EDSSC 2009, pp. 513.
215. Tang, W.M., Ng, W.T., Helander, M.G., Greiner, M.T. & Lu, Z.H. 2010, "UV ozone passivation of the metal/dielectric interface for HfO2 -based organic thin film transistors", Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures, vol. 28, no. 6, pp. 1100-1103.
216. Han, K.-K., Lee, S.W. & Lee, H.H. 2006, "Oxygen plasma treatment of gate metal in organic thin-film transistors", Applied Physics Letters, vol. 88, no. 23, pp. 233509-1.
217. Deng, L.F., Tang, W.M., Leung, C.H., Lai, P.T., Xu, J.P. & Che, C.M. 2008, "Pentacene thin-film transistors with HfO2 gate dielectric annealed in NH3 or N2O", 2008 IEEE International Conference on Electron Devices and Solid-State Circuits, EDSSC.
218. Singh Meena, J., Chu, M.-C., Kuo, S.-W., Chang, F.-C. & Ko, F.-H. 2010, "Improved reliability from a plasma-assisted metal-insulator-metal capacitor comprising a high-k HfO2 film on a flexible polyimide substrate", Physical Chemistry Chemical Physics, vol. 12, no. 11, pp. 2582-2589.
219. Kukli, K., Ritala, M., Sajavaara, T., Keinonen, J. & Leskelä, M. 2002, "Atomic layer deposition of hafnium dioxide films from hafnium tetrakis(ethylmethylamide) and water", Chemical Vapor Deposition, vol. 8, no. 5, pp. 199-204.
220. Feng, C., Mei, T., Hu, X. & Pavel, N. 2010, "A pentacene field-effect transistor with light-programmable threshold voltage", Organic Electronics: physics, materials, applications, vol. 11, no. 11, pp. 1713-1718.
221. Lee, S., Lee, S.S., Park, J.H., Park, I.-S. & Ann, J. 2009, "Characteristics of pentacene organic field-effect transistors with self-assembled-monolayer-treated hfo2 gate oxide", Japanese Journal of Applied Physics, vol. 48, no. 6 PART 2, pp. 06FD061-06FD065.
222. Knipp, D., Street, R.A., Völkel, A. & Ho, J. 2003, "Pentacene thin film transistors on inorganic dielectrics: Morphology, structural properties, and electronic transport", Journal of Applied Physics, vol. 93, no. 1, pp. 347-355.

223. Yang, S.Y., Shin, K. & Park, C.E. 2005, "The effect of gate-dielectric surface energy on pentacene morphology and organic field-effect transistor characteristics", Advanced Functional Materials, vol. 15, no. 11, pp. 1806-1814.
224. Drummy, L.F. & Martin, D.C. 2005, "Thickness-driven orthorhombic to triclinic phase transformation in pentacene thin films", Advanced Materials, vol. 17, no. 7, pp. 903-907.
225. Wei, C.-Y., Adriyanto, F., Lin, Y.-J., Li, Y.-C., Huang, T.-J., Chou, D.-W. & Wang, Y.-H. 2009, "Pentacene-based thin-film transistors with a solution-process hafnium oxide insulator", IEEE Electron Device Letters, vol. 30, no. 10, pp. 1039-1041.
226. Horowitz, G. & Hajlaoui, M.E. 2000, "Mobility in polycrystalline oligothiophene field-effect transistors dependent on grain size", Advanced Materials, vol. 12, no. 14, pp. 1046-1050.
227. Rogers, J.A., Dodabalapur, A., Bao, Z. & Katz, H.E. 1999, "Low-voltage 0.1 μm organic transistors and complementary inverter circuits fabricated with a low-cost form of near-field photolithography", Applied Physics Letters, vol. 75, no. 7, pp. 1010-1012.
228. Chwang, A.B. & Daniel Frisbie, C. 2000, "Field effect transport measurements on single grains of sexithiophene: Role of the contacts", Journal of Physical Chemistry B, vol. 104, no. 51, pp. 12202-12209.
229. Necliudov, P.V., Shur, M.S., Gundlach, D.J. & Jackson, T.N. 2003, "Contact resistance extraction in pentacene thin film transistors", Solid-State Electronics, vol. 47, no. 2, pp. 259-262.
230. Kerber, A., Cartier, E., Pantisano, L., Degraeve, R., Kauerauf, T., Kim, Y., Hou, A., Groeseneken, G., Maes, H.E. & Schwalke, U. 2003, "Origin of the threshold voltage instability in SiO2/HfO2 dual layer gate dielectrics", IEEE Electron Device Letters, vol. 24, no. 2, pp. 87-89.
231. Shen, C., Li, M.F., Wang, X.P., Yu, H.Y., Feng, Y.P., Lim, A.T.-L., Yeo, Y.C., Chan, D.S.H. & Kwong, D.L. 2004, "Negative U traps in HfO2 gate dielectrics and frequency dependence of dynamic BTI in MOSFETs", Technical Digest - International Electron Devices Meeting, IEDM, pp. 733.
232. Guo, D., Ikeda, S., Saiki, K., Miyazoe, H. & Terashima, K. 2006, "Effect of annealing on the mobility and morphology of thermally activated pentacene thin film transistors", Journal of Applied Physics, vol. 99, no. 9, pp. 094502-1.
233. Ye, R., Baba, M., Suzuki, K., Ohishi, Y. & Mori, K. 2003, "Effect of thermal annealing on morphology of pentacene thin films", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 42, no. 7 A, pp. 4473-4475.
234. Capasso, F. & Margaritondo, G. 1987, "Heterojunction Band Discontinuiti-es: Device Physics and Applications", North Holland, New York.
235. Weisbuch, C. & Vinter, B. 1991, "Quantum Semiconductor Structures", Academic Press, Boston.
236. Tang, C.W., Vanslyke, S.A. & Chen, C.H. 1989, "Electroluminescence of doped organic thin films", Journal of Applied Physics, vol. 65, no. 9, pp. 3610-3616.

237. Tang, C.W. 1986, "Two-layer organic photovoltaic cell", Applied Physics Letters, vol. 48, no. 2, pp. 183-185.
238. Dodabalapur, A., Katz, H.E., Torsi, L. & Haddon, R.C. 1996, "Organic field-effect bipolar transistors", Applied Physics Letters, vol. 68, no. 8, pp. 1108-1110.
239. Dinelli, F., Capelli, R., Loi, M.A., Murgia, M., Muccini, M., Facchetti, A. & Marks, T.J. 2006, "High-mobility ambipolar transport in organic light-emitting transistors", Advanced Materials, vol. 18, no. 11, pp. 1416-1420.
240. Haemori, M., Yamaguchi, J., Yaginuma, S., Itaka, K. & Koinuma, H. 2005, "Fabrication of highly oriented rubrene thin films by the use of atomically finished substrate and pentacene buffer layer", Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers, vol. 44, no. 6 A, pp. 3740-3742.
241. Hu, W.-S., Weng, S.-Z., Tao, Y.-T., Liu, H.-J. & Lee, H.-J. 2008, "Oriented growth of rubrene thin films on aligned pentacene buffer layer and its anisotropic thin-film transistor characteristics", Organic Electronics: physics, materials, applications, vol. 9, no. 3, pp. 385-395.
242. Song, D., Wang, H., Zhu, F., Yang, J., Tian, H., Geng, Y. & Yan, D. 2008, "Phthalocyanato tin(IV) dichloride: An air-stable, high-performance, n-type organic semiconductor with a high field-effect electron mobility", Advanced Materials, vol. 20, no. 11, pp. 2142-2144.
243. Wu, W., Liu, Y., Wang, Y., Xi, H., Gao, X., Di, C., Yu, G., Xu, W. & Zhu, D. 2008, "High-performance, low-operating-voltage organic field-effect transistors with low pinch-off voltages", Advanced Functional Materials, vol. 18, no. 5, pp. 810-815.
244. Abe, Y., Hasegawa, T., Takahashi, Y., Yamada, T. & Tokura, Y. 2005, "Control of threshold voltage in pentacene thin-film transistors using carrier doping at the charge-transfer interface with organic acceptors", Applied Physics Letters, vol. 87, no. 15, pp. 153506-1.
245. Scharnberg, M., Zaporojtchenko, V., Adelung, R., Faupel, F., Pannemann, C., Diekmann, T. & Hilleringmann, U. 2007, "Tuning the threshold voltage of organic field-effect transistors by an electret encapsulating layer", Applied Physics Letters, vol. 90, no. 1, pp. 013501-1.
246. Guo, Y., Liu, Y., Di, C.-A., Yu, G., Wu, W., Ye, S., Wang, Y., Xu, X. & Sun, Y. 2007, "Tuning the threshold voltage by inserting a thin molybdenum oxide layer into organic field-effect transistors", Applied Physics Letters, vol. 91, no. 26, pp. 263502-1.
247. Wang, Y., Liu, Y., Song, Y., Ye, S., Wu, W., Guo, Y., Di, C.-A., Sun, Y., Yu, G. & Hu, W. 2008, "Organic field-effect transistors with a low pinch-off voltage and a Controllable threshold voltage", Advanced Materials, vol. 20, no. 3, pp. 611-615.
248. Dutta, S. & Narayan, K.S. 2004, "Gate-voltage control of optically-induced charges and memory effects in polymer field-effect transistors", Advanced Materials, vol. 16, no. 23-24, pp. 2151-2155.
249. Redecker, M., Bradley, D.D.C., Inbasekaran, M. & Woo, E.P. 1998, "Nondispersive hole transport in an electroluminescent polyfluorene", Applied Physics Letters, vol. 73, no. 11, pp. 1565-1567.

250. Grice, A.W., Bradley, D.D.C., Bernius, M.T., Inbasekaran, M., Wu, W.W. & Woo, E.P. 1998, "High brightness and efficiency blue light-emitting polymer diodes", Applied Physics Letters, vol. 73, no. 5, pp. 629-631.
251. Kido, J., Hongawa, K., Okuyama, K. & Nagai, K. 1993, "Bright blue electroluminescence from poly(N-vinylcarbazole)", Applied Physics Letters, vol. 63, no. 19, pp. 2627-2629.
252. Kido, J., Hongawa, K., Okuyama, K. & Nagai, K. 1994, "White light-emitting organic electroluminescent devices using the poly(N-vinylcarbazole) emitter layer doped with three fluorescent dyes", Applied Physics Letters, vol. 64, no. 7, pp. 815-817.
253. Grell, M., Bradley, D.D.C., Inbasekaran, M. & Woo, E.P. 1997, "A glass-Forming conjugated main-chain liquid crystal polymer for polarized electroluminescence applications", Advanced Materials, vol. 9, no. 10, pp. 798-802.
254. Lai, Y.-S., Tu, C.-H., Kwong, D.-L. & Chen, J.S. 2005, "Bistable resistance switching of poly(N-vinylcarbazole) films for nonvolatile memory applications", Applied Physics Letters, vol. 87, no. 12, pp. 122101-1.
255. Dodabalapur, A., Katz, H.E. & Torsi, L. 1996, "Molecular orbital energy level engineering in organic transistors", Advanced Materials, vol. 8, no. 10, pp. 853-855.
256. Wong, J.I., Chen, T.P., Yang, M., Liu, Y., Ng, C.Y., Ding, L., Chong, C.F. & Tseng, A.A. 2008, "Influence of excess Si distribution in the gate oxide on the memory characteristics of MOSFETs", Applied Physics A: Materials Science and Processing, vol. 91, no. 3, pp. 411-413.
257. Yu, G. & Heeger, A.J. 1995, "Charge separation and photovoltaic conversion in polymer composites with internal donor/acceptor heterojunctions", Journal of Applied Physics, vol. 78, no. 7, pp. 4510-4515.
258. Knupfer, M. 2003, "Exciton binding energies in organic semiconductors", Applied Physics A: Materials Science and Processing, vol. 77, no. 5, pp. 623-626.
259. Hoppe, H. & Sariciftci, N.S. 2004, "Organic solar cells: An overview", Journal of Materials Research, vol. 19, no. 7, pp. 1924-1945.
260. Noh, Y.-Y. & Kim, D.-Y. 2007, "Organic phototransistor based on pentacene as an efficient red light sensor", Solid-State Electronics, vol. 51, no. 7, pp. 1052-1055.
261. Liu, C. & Sirringhaus, H. 2010, "Polymer field-effect transistors based on semiconducting polymer heterojunctions", Journal of Applied Physics, vol. 107, no. 1, pp. 014516-1.
262. Jentzsch, T., Juepner, H.J., Brzezinka, K.-W. & Lau, A. 1998, "Efficiency of optical second harmonic generation from pentacene films of different morphology and structure", Thin Solid Films, vol. 315, no. 1-2, pp. 273-280.
263. Kim, S.H., Nam, S., Jang, J., Hong, K., Yang, C., Chung, D.S., Park, C.E. & Choi, W.-S. 2009, "Effect of the hydrophobicity and thickness of polymer gate dielectrics on the hysteresis behavior of pentacene-

based field-effect transistors", Journal of Applied Physics, vol. 105, no. 10, pp. 104509-1.
264. D'Andrade, B.W. & Forrest, S.R. 2004, "White organic light-emitting devices for solid-state lighting", Advanced Materials, vol. 16, no. 18, pp. 1585-1595.
265. Crone, B., Dodabalapur, A., Lin, Y.-Y., Filas, R.W., Bao, Z., LaDuca, A., Sarpeshkar, R., Katz, H.E. & Li, W. 2000, "Large-scale complementary integrated circuits based on organic transistors", Nature, vol. 403, no. 6769, pp. 521-523.
266. Özgür, Ü, Alivov, Y.I., Liu, C., Teke, A., Reshchikov, M.A., Doğan, S., Avrutin, V., Cho, S.-J. & Morkoç, H. 2005, "A comprehensive review of ZnO materials and devices", Journal of Applied Physics, vol. 98, no. 4, pp. 041301-1.
267. Fontaine, P., Goguenheim, D., Deresmes, D., Vuillaume, D., Garet, M. & Rondelez, F. 1993, "Octadecyltrichlorosilane monolayers as ultrathin gate insulating films in metal-insulator-semiconductor devices", Applied Physics Letters, vol. 62, no. 18, pp. 2256-2258.