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Gate Driver for the Active Thermal Control of a DC/DC GaN-based Converter

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***Abstract*—Wide-Band-Gap power semiconductors based on SiC and GaN offer some significant advantages compared to Si-devices, in particular higher switching speed and higher operating temperature. These features offer potentially increased power density, which makes the temperature management critical especially for the PCB and components to which the GaN is connected. In this paper, an active gate driver with active thermal control is implemented and can be used to alter the losses of a DC/DC buck converter based on GaN transistors, with the aim of reducing the thermal cycling thus improving the converter's lifetime.**

I. Introduction

Recently, GaN power transistors came to the market. For the near future, it is assumed that GaN transistors will replace Si-based IGBTs and MOSFETs in some applications in the voltage range between 600V−1,000V [1]. GaN-based transistors are unipolar devices which have in comparison with IGBTs no tail current and no threshold voltage during conduction. Despite several advantages, there are challenges related with GaN transistors, i.e. the electro magnetic interferences (EMI) related to the fast switching in hard switching applications, the necessary minimization of stray inductance, the design of the packages [2] and the control of the temperature.

One means of failure and associated reliability issues are caused by thermo-mechanical fatigue. Components with different thermal expansion coefficients are subjected to different thermo mechanical stresses. When such components which are in contact are subjected to thermal cycling, it causes mechanical fatigue and as a consequence failure. In case of IGBTs and MOSFETs, these thermo-mechanical stresses and fatigue arises between wire bonds and copper; wire bonds and power chips causing bond wire lift off or perhaps chip solder fatigue etc.. [3] When using GaN transistors, the concept of thermo-mechanical fatigue associated reliability issues shift from within the device to the solder contacts. This happens because of the absence of wire bonds and solder contacts within the packaging. GaNSystems GaN*PX* packaging makes use of copper-filled vias to make contacts to the device. The vias also function as heat exchange from within the device to the case, thereby reducing the thermal resistance values of these devices [4]. In short large magnitude thermal cycling can introduce considerable thermo-mechanical fatigue to mechanical contacts with different thermal expansion coefficients. Thus with the aim of reducing thermal stress in power modules, various active thermal control algorithms have been proposed [5]. Normally, converters are designed to limit the losses, thermal cycling reduction can be achieved, as an example, by increasing the losses when the load is decreasing. This comes at the expense of the overall efficiency, so a tradeoff should be found for a proper system design .

Small device capacitances enable very high switching speeds, which lead to smaller switching losses and smaller gate driver losses. The rise of the current slope di/dt as well as the voltage slope dv/dt are significantly higher for GaN-based semiconductors, which implies that parasitic capacitances and parasitic inductances in the power part as well as in the gate driver unit have a significant influence on the device performance [2]. One of the main challenges is the minimization of the parasitic elements in the circuit which is investigated in [6], [7]. Even with optimized semiconductor packaging and the circuit layout, stray inductance will still be present in an optimized layout. Therefore, a reduction of the switching speed might be mandatory in order to prevent a device failure and this can be realized by selecting a larger gate resistance R_G which is advised in [8] with the disadvantage of higher losses. Another possibility to influence the switching performance is the application of active gate driver units which have been investigated for IGBTs and MOSFETs for the turn-on and turn-off. The application of a two-step gate voltage is one possibility to influence the switching behavior as well as conduction losses of IGBTs and MOSFETs [9]–[11].

In this paper, a gate driver for a GaN Enhancement Mode High Electron Mobility Transistor (E-HEMT) GS66508T, from GaN Systems [12] is analyzed. The suitability of this active gate control method is investigated for the E-HEMT for a single pulse. The effect of the developed active gate driver unit on slew rate control, switching and conduction losses are presented and the impact on the junction temperature is studied in PLECS simulation of a GaN based Buck converter. The active gate driver circuit can be used to reduce the variation of the junction temperature.

This paper is structured as follows: In the first part, the E-HEMT is briefly described and the applied double-pulse test setup is presented. An analysis of the performance of the two-step gate driver unit is conducted in section 3. In section 4, the potential of active thermal control is studied for a DC/DC-converter.

II. Switching performance of the E-HEMT

For safety reasons, power semiconductors in voltage source converters need to be normally-off. The first GaN power semiconductors were normally-on and were called HEMT. Different approaches have been applied to reach normally-off behavior which can be summarized as E-HEMT [13]. In this paper, the performance of a 650V E-HEMT of GaNSystems will be investigated. Besides low capacitance, the E-HEMT has a bidirectional conduction mode without a pn-junction between the Drain (D) and the Source (S) which implies that no free-wheeling diode is necessary.

Although the general control of GaN E-HEMTs is similar to Si-IGBTs and Si-MOSFETs, two main differences exist: the applied gate voltage is smaller (usually $6V-7V$) and the threshold-voltage is lower (usually $1V-2V$). The lower gate voltage means lower power gate driver solutions compared to similar rated Si or SiC devices. But the low threshold voltage create difficulties for safe operation. The gate driver robustness against spurious turn-on can be improved by providing a negative gate voltage instead of zero voltage. But negative gate voltage increases the reverse conduction loss of GaN devices as well as increase losses in the gate driver circuit. The following points should be ensured for proper gate driver and half-bridge operation with GaN [14], [8], [15] [16]:-

- Provide very low inductance device - driver loop in order to avoid unwanted ringing.
- Guarantee immunity against ground bounce.
- Avoid common current return paths among control, gate driver and power side.
- Provide low impedance gate current return path to avoid dv/dt induced turn-on.
- Guarantee very high CMTI (common mode transient immunity) above 100V/ns for the control.
- Ensure enough power to signal isolation.
- Ensure gate drivers are capable of delivering desired peak gate currents.
- Ensure gate drivers have low output pull-down impedance.

The double-pulse test is used for the characterization of the switching performance. The specifications of the double pulse test stand and measurement instruments used in the power electronics laboratory is given in Table I. The turn-on and turn-off performance of the E-HEMT are shown in Fig. 1a and Fig. 1b respectively for different R_G. A ringing with 5 MHz can be observed in the current for turn-on and in the voltage for turn-off which is damped in both cases with an increase of R_G. Especially the voltage overshoot during turn-off is critical for safe operation. The dv/dt and di/dt for turn-on and turn-off are shown in Fig. 2a; the turn-on and turn-off losses E_{on} and E_{off} are given in Fig. 2b. An analysis of the current and voltage slopes for different gate resistances is given in Fig. 2a, the variation of turn-on and turn-off loss energies with gate resistance is given in Fig. 2b. The turn-on and turn-off loss energies increase linearly with R_G. The turn-on and turn-

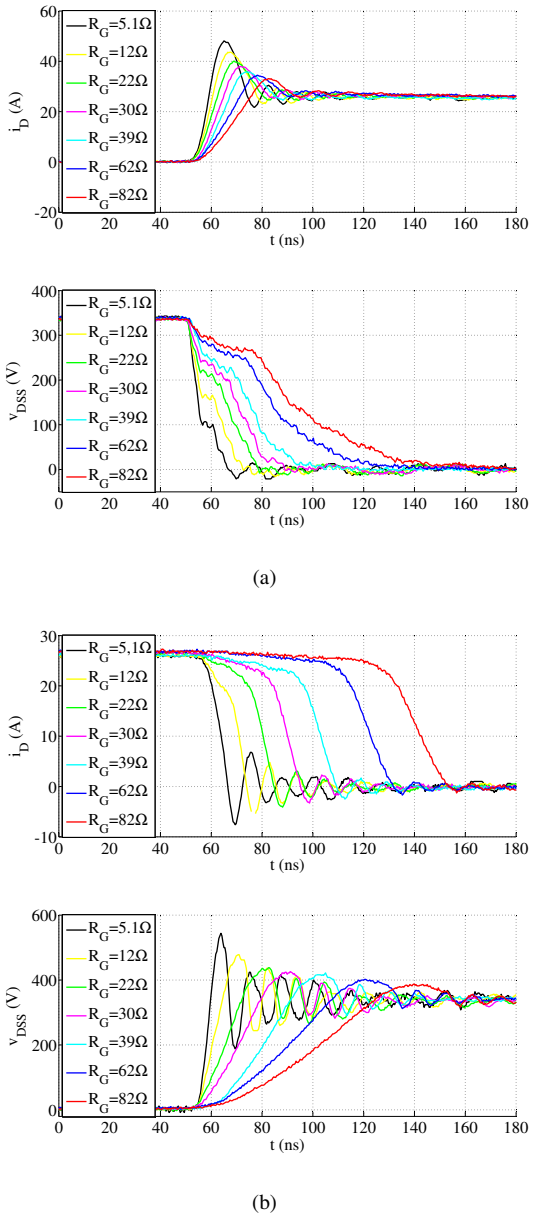
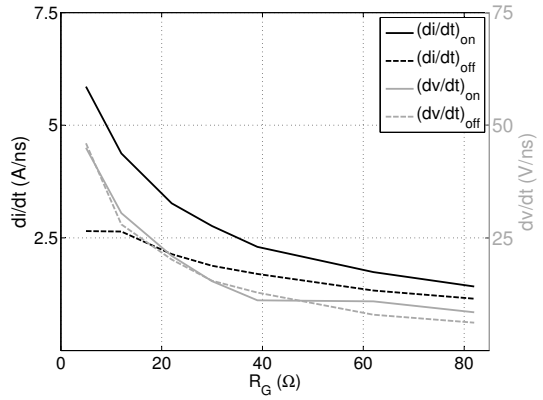


Figure 1: Switching performance of the E-HEMT GaN-Transistor for different R_G ($I_{ds}=25A$, V_{ds}=330V) (a) Turn-on switching performance (b) Turn-off switching performance

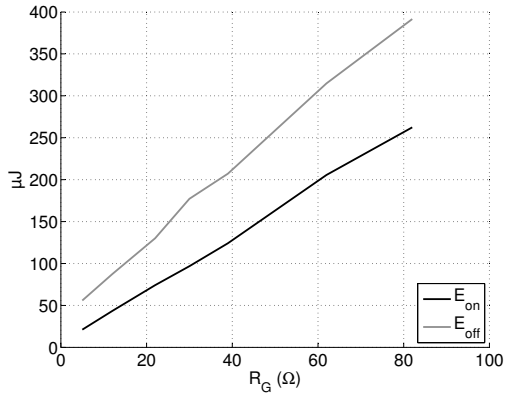
Table I: Double pulse test stand specifications

Input Voltage	24 V - 48 V
DPT Output Voltage range	50 V - 910 V
Voltage Probes	Le Croy PPE 2kV, Hameg HZ51 600V
Current Probes	SDN 414-10 (T&M), Tektronix TCP0030A
Differential Probe	Tektronix P5205
Voltage Probe Bandwidth	400 MHz
Current Probe Bandwidth	2 GHz and 120 MHz (Tektronix)
Differential Probe Bandwidth	100 MHz

off losses with a simple gate resistor will be used as reference.



(a)



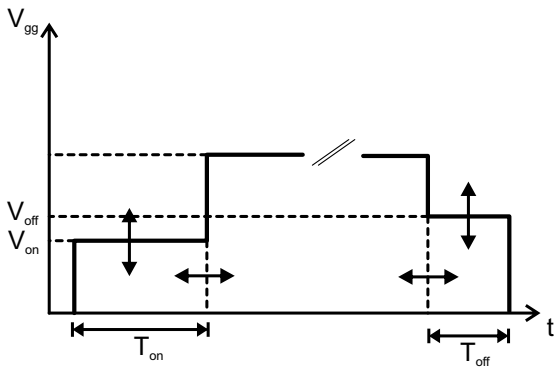
(b)

Figure 2: (a) Current and voltage slopes for turn-on and turn-off for different gate resistances R_{G} ($I_{\mathrm{L}} = 25\,\mathrm{A}$, $V_{\mathrm{dc}} = 330\,\mathrm{V}$) (b) Turn-on and turn-off loss energies for different R_{G} ($I_{\mathrm{L}} = 25\,\mathrm{A}$, $V_{\mathrm{dc}} = 330\,\mathrm{V}$)

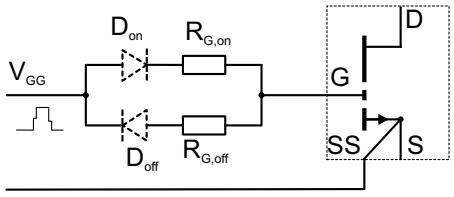
III. Two-Step Gate Drive Unit

The considered two-step gate voltage shape for turn-on and turn-off is shown in Fig. 3a, the applied gate driver circuit is shown in Fig. 3b. By adjusting the gate voltage shape parameters T_{on} , T_{off}, V_{on} and V_{off}, the shape of the gate voltage can be varied. The diodes D_{on} and D_{off} are optional for two reasons. One is to enable different minimum rise times ($\mathrm{t}_{r,min}$) and fall times ($\mathrm{t}_{f,min}$) if desired for the GaN device. Another reason is to ensure a very low impedance return gate current path to ground which also helps avoid dv/dt induced turn-on of the off-device in a half-bridge.

The two-step gate driver designed and developed in this work is for GS66508T (top side cooled GaN device from GaNSystems). The important parameters of the GaN device relevant for the 2 -step gate driver design are given in Table II [12]. The parameter measurement conditions are not listed here



(a)



(b)

Figure 3: (a) Waveform of the two-step gate driver (b) Gate driver for the two-step gate voltage approach

Table II: GaN GS66508T characteristics

Parameters	Values
Blocking Voltage, BV_{DS}	650 V
Gate-Source Voltage, V_{GS}	-10 to +7 V
Gate-Source Threshold Voltage, $V_{GS,th}$	1.1 to 1.3 V
Gate-Source Plateau Voltage, $V_{GS,pl}$	3 V
Drain Source Resistance, R_{DS}	50 mΩ
Reverse recovery charge, Q_{RR}	0 nC
Rise time, t_R	3.7 ns
Fall time, t_F	5.2 ns

as they are available in the Datasheet [12] from GaNSystems.

Using similar terms to define parameters for a MOSFET, it can be seen that the gate plateau voltage (Vg,pl) is at 3.0 V and the gate threshold voltage (Vg,th) is at 1.3 V. This means that during turn-on gating ($Vgs > 0$) , when $Vg,th < Vgs < Vg,pl$, the current (I_{ds}) in the device rises up to the steady state value. Similarly, for the duration when $Vgs = Vg,pl$ (miller plateau region), the device will undergo voltage (V_{ds}) fall or transient. This is shown in Fig. 4.

The turn-on time or voltage fall is determined basically by the amount of charge ($Q_{g,pl}$) supplied by the gate driver during miller-plateau. Thus by limiting $Q_{g,pl}$, the device turn-on voltage transition may be controlled. As can be seen in Fig. 4 the voltage transition phase begins only after $Vgs = Vg,pl$. Referring to Fig. 3a, thus the first step (V_{on}) of the 2-step driver is set to 3.0 V. The second step voltage is always set at typical gate voltage desired which is 6.0V for GS66508T. The time T_{on} (interval between steps) can now be adjusted to

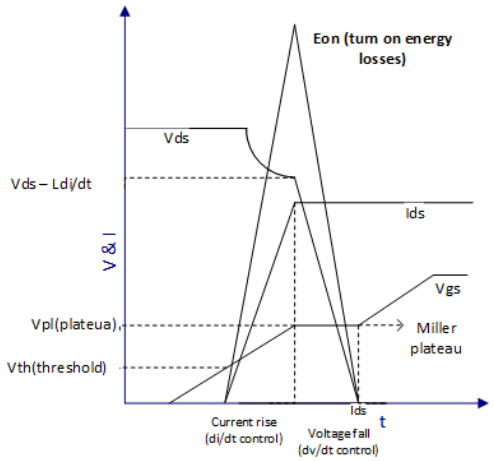


Figure 4: Commutation of Wide band gap devices

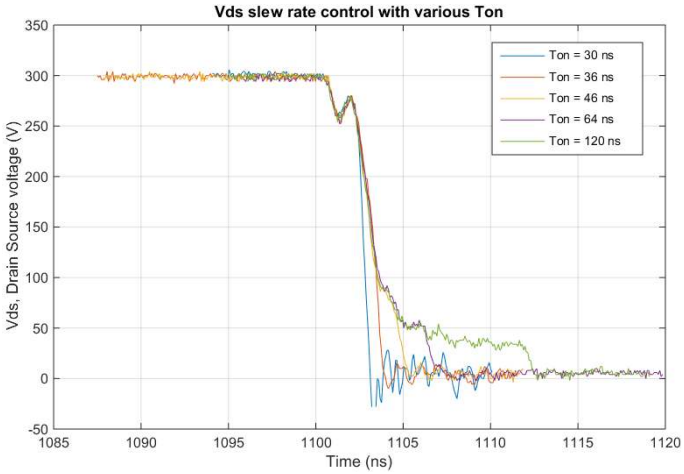


Figure 5: Results showing Slew rate control for various Ton ($I_{\mathrm{DS}} = 6\,\mathrm{A}$, $V_{\mathrm{DS}} = 300\,\mathrm{V}$)

vary the current delivered during device turn-on. This helps to adjust dv/dt during turn-on by adjusting only T_{on}. During turn-off the voltage setting $Voff = Vg,pl$ will not have an effect since the gate discharge for V_{ds} rise begins only after Vgs falls below Vg,pl.

Similarly, by setting Von between Vg,th and Vg,pl during turn-on, the device turn-on current transient time (di/dt) can be regulated. And by setting $Voff$ between Vg,th and Vg,pl during turn-off, the voltage V_{ds} rise time during turn-off can be adjusted by varying T_{off}, where T_{off} is the time interval between $Voff$ and final off-state voltage of the gate driver (here it is set to zero).

Thus by implementing the 2-step gate driver concept, it is possible to vary the device slew rates dv/dt or di/dt and thereby vary the switching losses. To verify this , DPT (Double pulse tests) are conducted at V_{ds} = 300V, I_{ds} = 6A on the GS66508T GaN device in order to vary the device V_{ds} turn-on slew rates and actively adapt switching losses. The experimental results obtained are shown in Fig. 5 and Fig. 6. Here, Von is set to 3.0 V and the T_{on} is adjusted. Fig. 5 and Fig. 7 show the influence of various T_{on} values on the device dv/dt during turn-on. It can be seen from Fig. 5 that for different values of T_{on}, the rise time t_r is different. Fig. 6 shows the variation in switching losses during turn-on for various T_{on} of the 2-step gate driver. It can be seen from Fig. 6, that the area under the Energy curve is larger for higher values of T_{on}. These experimental results show that the device slew rate (Fig. 7) as well as losses can be controlled using the 2-step gate driver developed. The Table III shows the losses for various T_{on} values. The oscilliscope readings of two cases of T_{on} = 46ns and 32ns are shown in Fig. 8 and Fig. 9 which shows turn-on times of 38.8ns and 22.8ns. However if the T_{on} is increased further, then the device turns-on at around 40ns. But with an R_{DS} (device on-state resistance) value at V_{GS} = 3 V. The device will then have higher conduction losses due to increased R_{DS} value compared to R_{DS} at V_{GS} = 6 V (from Table II). This effect of the 2-step gate driver on the GaN GS66508T

Table III: Energy loss vs T_{on}

Energy loss (μ)J	**T_{on}(ns)**
38.77	32
46.2	46
53.79	52
54.9	64
69.18	120

is shown in Fig. 10 where after a certain duration the device is having conduction energy loss. The conduction loss region is the almost flat non-zero part of the sky blue (Energy) curve in Fig. 10. This peculiarity in controllability using 2-step gate driver is shown in Fig. 11. Also the energy loss distribution while making use of a 2-step gate driver is also provided in 12. It can be deduced from Fig. 10 that above T_{on} = 48ns, further slew rate control is not possible and the device is already turned on. But the presence of $V_{GS} < 6$V means presence of higher conduction losses than completely turned-on situation (V_{GS} = 6V). This means it is possible to actively control the device switching losses as well as conduction losses of GaN GS66508T using the developed 2-step gate driver. It is to be noted that the conduction loss region in Fig. 11, does not have slew rate controllability. The device is already conducting in this region, although t_r variation is seen. This is only because the limits of t_r are set at 90% V_{DS} and at 10% V_{DS}.

The lower limits of device turn-on and turn-off time are decided by values of $R_{G,on}$ and $R_{G,off}$ in Fig. 3b.

The experimental results from this section prove that the 2-step gate driver is capable of actively introducing switching and conduction losses if the parameter T_{on} is adapted online.

IV. Active Thermal Control for the DC/DC Converter

The impact of the active thermal control on a bidirectional single-phase DC/DC converter is also briefly presented here. The topology of the converter is shown in Fig. 13a. The

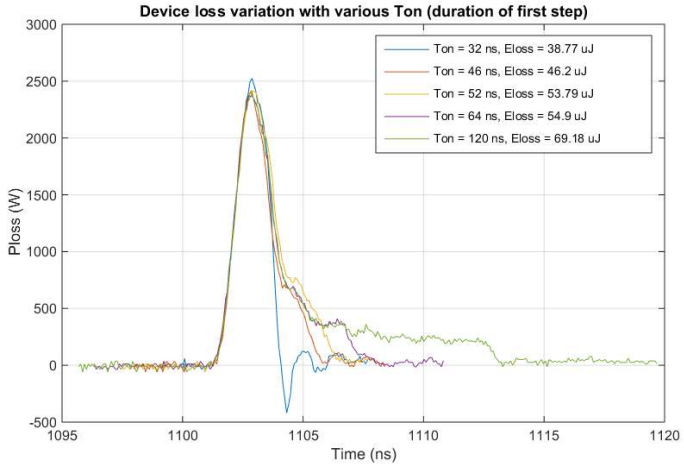


Figure 6: Results showing Energy loss variation with various Ton($I_{DS} = 6\,A$, $V_{DS} = 300\,V$)

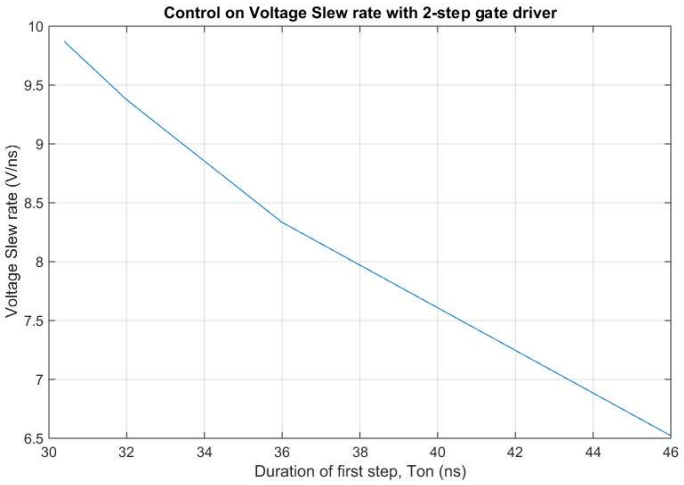


Figure 7: Device slew rate (dv/dt) for various Ton ($I_{DS} = 6\,A$, $V_{DS} = 300\,V$)

idea is to increase the switching losses and/ conduction losses when the output power decreases, in order to prevent excessive cooling down.

The losses of the DC/DC converter and therefore its temperature variation can be controlled by an active gate driver in four different ways which are explained using Fig. 13b. The first possibility is the application of the active gate driver to tune the turn-off and turn-on switching losses of V_1 at point II or IV (Fig. 13b). The conduction losses of V_1 during the time period can be controlled by proper selection of the gate voltage level. The conduction losses of V_2 (being a GaN transistor) during free wheeling operation can be modified by an adjustment of the negative gate voltage level.

Despite the increase of the overall losses which implies an over all reduction of the efficiency, the reduced thermal stress on the power converter could balance this drawback. Applying the two-step gate voltage approach, it is possible to adapt either

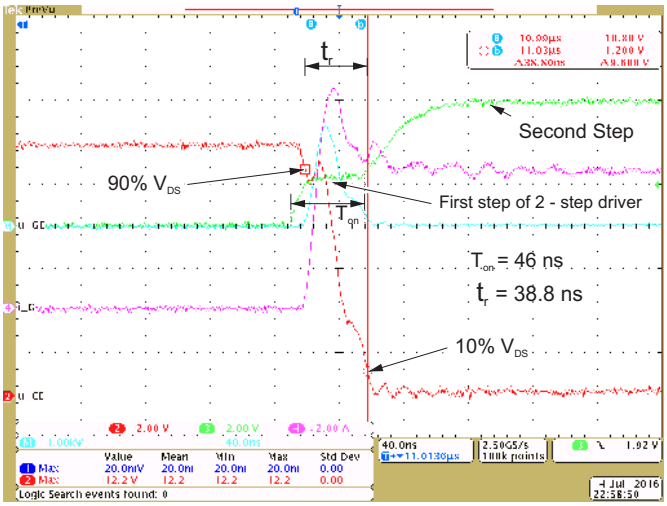


Figure 8: Device Turn-on characteristics for T_{on} = 46ns, (Green - Gate Voltage, Red - V_{DS} (need to scale by multiplying by 25 - 300V to 0V), Maroon - Inductor current (0A to 6A), sky blue - Turn-on switching energy loss)

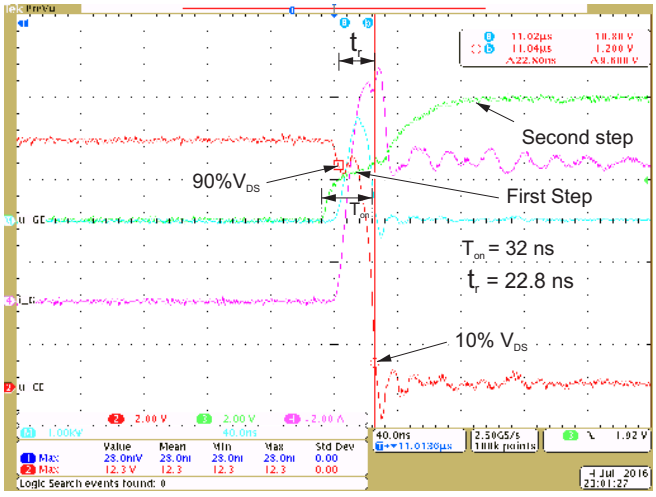


Figure 9: Device Turn-on characteristics for T_{on} = 32ns, (Green - Gate Voltage, Red - V_{DS} (need to scale by multiplying by 25 - 300V to 0V), Maroon - Inductor current (0A to 6A), sky blue - Turn-on switching energy loss)

the turn-on and turn-off switching losses, the conduction losses or both. The experimentally measured energy losses can be used to simulate the junction temperature in PLECS and the possibilities of reducing the thermal cycles can be understood. In Fig. 16b, the junction temperature variation of V_1 with and without active thermal control for a selected mission profile is shown. At lower power levels, the switching losses of V_1 are increased by 1.5 to 2 times so as to limit the magnitude of thermal cycling within a predefined temperature range. The junction temperature feedback is used in the control loop to

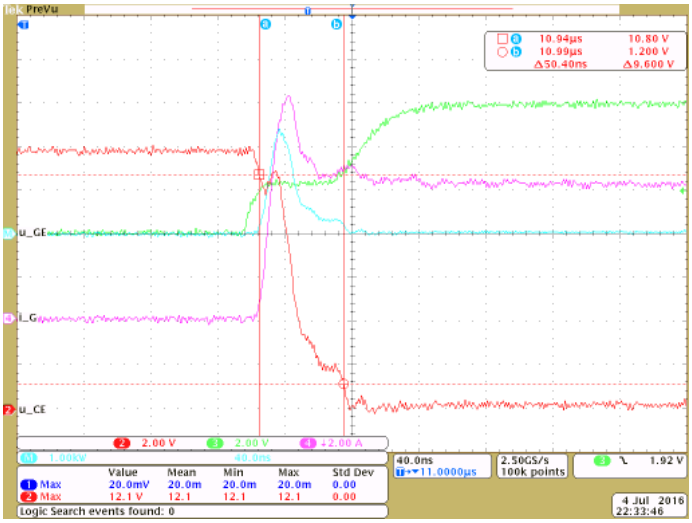


Figure 10: Device Turn-on characteristics for T_{on} = 57ns, (Green - Gate Voltage, Red - V_{DS} (need to scale by multiplying by 25 - 300V to 0V), Maroon - Inductor current (0A to 6A), sky blue - Turn-on switching energy loss)

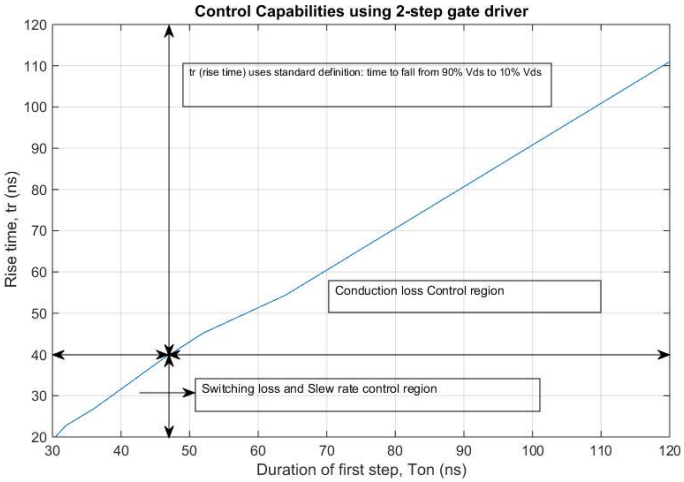


Figure 11: Device rise time for various Ton ($I_{\mathrm{DS}} = 6\,\mathrm{A}$, $V_{\mathrm{DS}} = 300\,\mathrm{V}$)

determine the percentage by which switching loss need to be increased depending on the thermal cycling limits desired.

The device thermal cycling can be controlled with the aim of reducing the thermal stress. In Fig. 16a, the impact of a variation of the conduction losses of V_1 on its junction temperature is shown. Again, a reduction of the thermal cycling is possible by a power loss increase by increasing conduction losses. These results show the possibilities of reducing thermal cycling by varying device losses. The developed two-step gate driver unit and half-bridge in which the proposed active thermal control can be implemented is shown in Fig. 14. The Double pulse test setup which can be used for switching characterization of Si, SiC and GaN devices is shown in Fig. 15

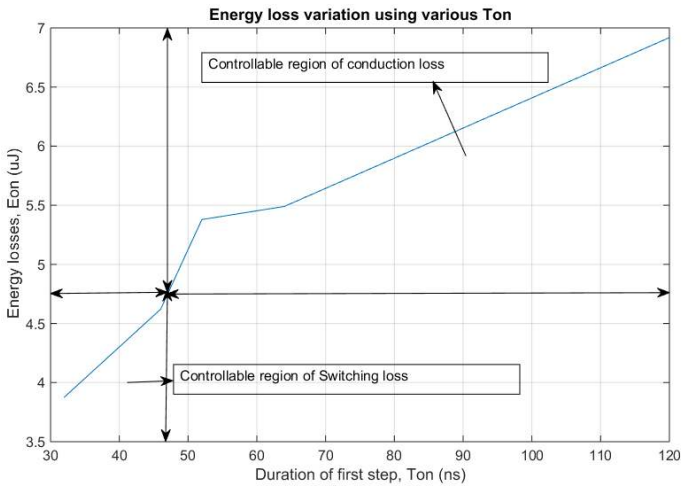


Figure 12: Energy loss controllable regions with various Ton ($I_{\mathrm{DS}} = 6\,\mathrm{A}$, $V_{\mathrm{DS}} = 300\,\mathrm{V}$)

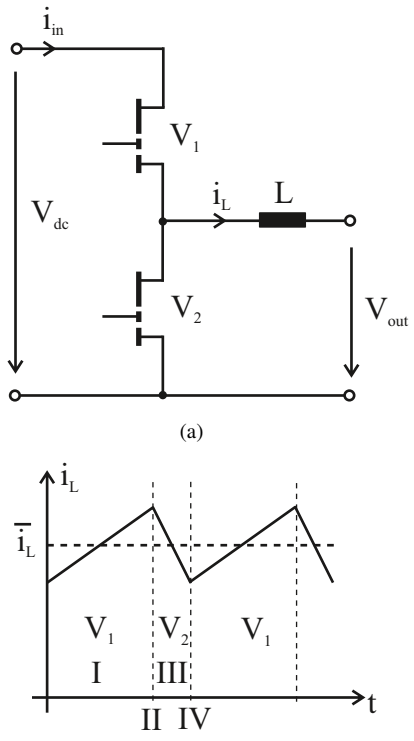


Figure 13: (a) DC/DC buck converter (b) Current waveform of i_L of the DC/DC buck converter

V. Conclusion

In this paper, the turn-on and turn-off switching performance of GaNSystems GS66508T GaN 650 V E-HEMT have been investigated. The concept of a two-step gate driver unit is presented and the effects of the tunable parameter on the switching performance and device losses has been presented. The effect of different gate resistors on the device switching performance has been determined experimentally. This can

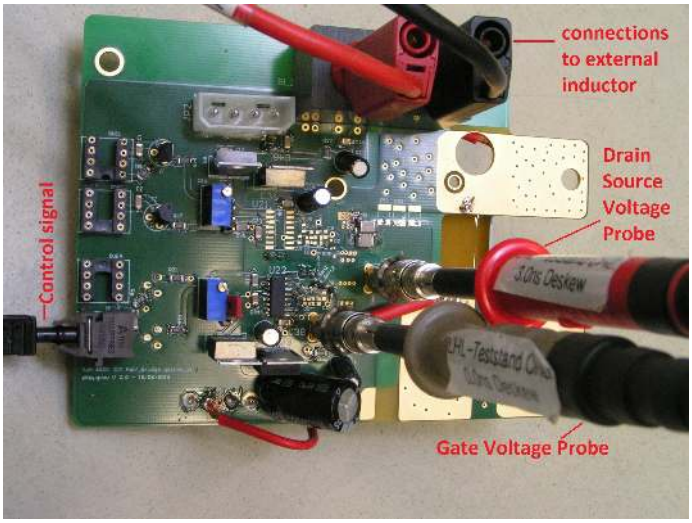


Figure 14: Developed two-step gate driver unit and GaN HEMTs in half-bridge configuration

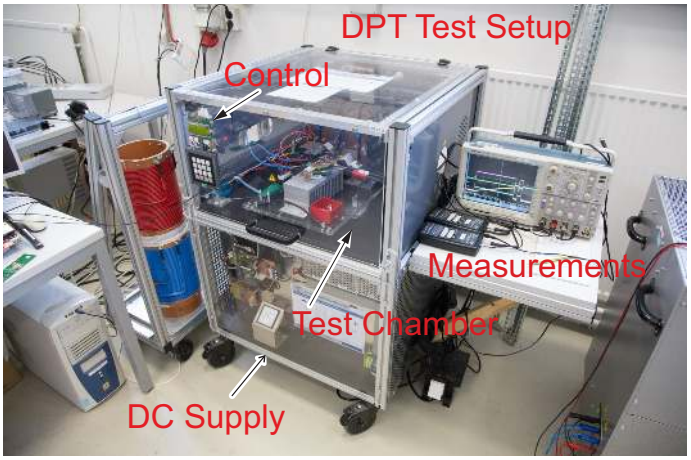


Figure 15: Double Pulse test setup

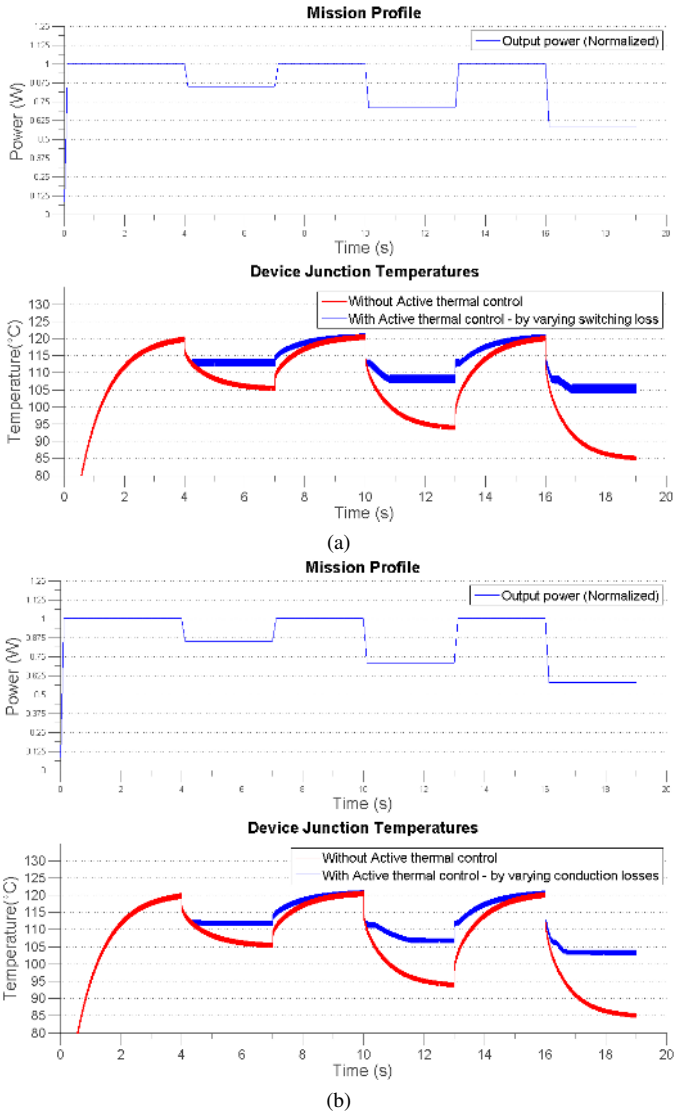


Figure 16: Simulation results of active thermal control strategies on the junction temperature of a GaN E-HEMT (a) Variation of the switching loss energies for $V_{dc} = 400\,V$ and a switching frequency $f_{sw} = 100\,kHz$ (b) Variation of the conduction losses for $V_{dc} = 400\,V$ and $f_{sw} = 100\,kHz$

be used as the factor that limits the least achievable turn-on and turn-off times using the two-step driver . First simulative results showing effect of an increase of the switching or conduction losses at lower output power levels on the device junction temperature have been presented. This work developed a two-step gate driver for active thermal control of a basic DC-DC GaN based converter.

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