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# Gate-emitter Pre-threshold Voltage as a Health Sensitive Parameter for IGBT Chip Failure Monitoring in High Voltage Multichip IGBT Power Modules

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*Authors confirm none of the material in this paper has been published or is under consideration for publication elsewhere.*

**Abstract** - This paper proposes a novel health sensitive parameter, called the gate-emitter pre-threshold voltage  $V_{GE(\text{pre-th})}$ , for detecting IGBT chip failures in multichip IGBT power modules. The proposed method has been applied in an IGBT gate driver and measures the  $V_{GE}$  at a fixed time instant of the  $V_{GE}$  transient before the threshold voltage occurs. To validate the proposed method, theoretical analysis and practical results for a 16-chip IGBT power module are presented in the paper. The results show a 500 mV average shift in the measured  $V_{GE(\text{pre-th})}$  for each IGBT chip failure.

**Keywords** – High voltage multichip Insulated Gate Bipolar Transistor (IGBT) module, IGBT chip failure, health monitoring, threshold voltage.

## I. INTRODUCTION

IGBT power modules are widely used in high power converter applications [1, 2]. They dominate the market due to their superior overall performance which results from the IGBT structure incorporating the gating of Metal Oxide Semiconductor Field-Effect Transistors (MOSFETs) for fast switching speed, and the body region of Bipolar Junction Transistors (BJTs) for low conduction losses [3, 4]. Recently, there has been a growing interest in the application of health monitoring techniques to improve the operational reliability of the IGBT power modules. In general, there are mainly three points which are of interest in IGBT health monitoring: i) virtual junction temperature ( $T_{vj}$ ) [5-28], ii) solder degradation [29-32], and iii) bond wire failure [29, 33-39]. Some of the health monitoring techniques proposed are in-situ, meaning health monitoring is achieved via a test circuit exclusively developed for detecting degradation and implemented onboard power converters. In-situ health monitoring avoids the fallout of a disrupted field service due to power converter teardown prior to inspection.

This paper proposes an online detection technique for IGBT chip failures in High Voltage (HV) multichip IGBT power modules as their applications are mostly critical [41-43]. A typical multichip module is depicted in Fig.1 which shows a 3.3 kV, 800 A single switch IGBT power module (DIM800NSM33-F) from Dynex Semiconductor Limited that was used for experimentation. The DIM800NSM33-F has 16 IGBT chips and 8 anti-parallel diodes. This work focusses only on the health monitoring of the IGBT chips and not the diode chips. This is because IGBTs have a more complex semiconductor structure and due to the gate a more complex chip surface structure which makes IGBT chip less reliable compared to diodes. Also, IGBTs experience higher turn-on and turn-off losses compared to diodes and are therefore more stressed. Finally, in large power modules, it is common to have more IGBT chips than diode chips due to the different current density for each device type.

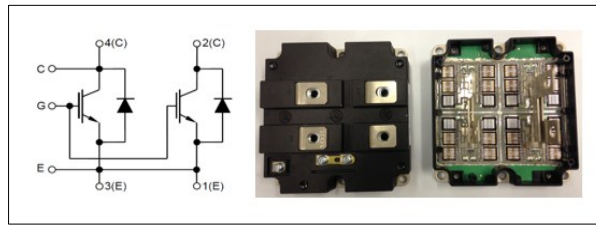


Fig. 1. Dynex 3.3 kV, 800 A IGBT Power Module (DIM800NSM33-F): Electrical Configuration [44], External and Interior View.

Bond wire failure is one of the primary failure mechanisms of the IGBT module. For an IGBT chip, since several bond wires are employed for the chip connection, it remains functional upon the initial occurrence of one bond wire lift-off. However, an IGBT chip eventually ceases to function when all of its bond wires fail. Likewise, upon the initial chip failure, a multichip IGBT module still remains functional due to several IGBT chips being in parallel [33, 45]. Nevertheless, an IGBT power module's robustness is in line with its health conditions which depends on each of the constituent chips. Eventually, the power module fails outright. In this regard, this paper proposes the IGBT chip failure as a health monitoring precursor for multichip IGBT power modules.

A new method for detecting the IGBT chip failures in multichip HV IGBT power modules is presented in this paper by monitoring the pre-threshold voltage ( $V_{GE(\text{pre-th})}$ ) which takes place during the turn-on transient of  $V_{GE}$ . A distinct advantage of  $V_{GE(\text{pre-th})}$  is that it is measured before the conduction of the IGBT collector current ( $I_C$ ), and hence does not suffer from changes in the load current or the noise caused by the switching on of the device after the threshold point. Furthermore,  $V_{GE(\text{pre-th})}$  does not require HV isolation and HV insulation as all of the measurement circuitry is on the gate side rather than the HV collector side. For HV isolation, we refer to the electric circuitry employed for isolation between the HV and gate-emitter circuits. For HV insulation, we mean the insulation of the cables and the components. Unlike current sensor based methods,  $V_{GE(\text{pre-th})}$  uses a simple low cost and lightweight voltage sensor which can be easily embedded into any gate driver.

This paper discusses the theoretical analysis and hardware implementation of  $V_{GE(\text{pre-th})}$  on the gate driver of the 16-chip DIM800NSM33-F, where  $V_{GE(\text{pre-th})}$  is monitored at a fixed time instant from the IGBT turn-on command. It is shown that the sensitivity is 500 mV per IGBT chip failure and the

1 results are consistent under different operational and environmental conditions. As it is measured  
 2 before the IGBT's turn-on threshold,  $V_{GE(\text{pre-th})}$  can be embedded within a standard PWM controller.  
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## 7 II. COMPARISON OF EXISTING HEALTH MONITORING METHODS

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 9 Over the last two decades, many efforts have been dedicated to online bond wire failure detection  
 10 of IGBT power devices. Most of the research focuses on the IGBT health sensitive parameters (HSPs)  
 11 which can be measured externally through the main terminals – collector, gate and emitter (as well  
 12 as Kelvin connectors where appropriate) – of an IGBT module. A selection of these methods is  
 13 presented in Table I.  
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22 Table I. Examples of bond wire and chip failure detection techniques.

HSP	IGBT Type	Relative Sensitivity		Immunity to $T_{vj}$ A/B	Reference
		Bond wire/chip failure (A)	$T_{vj}$ (B)		
$V_{CE(\text{on})}^{[1]}$	1-chip	1% (bond wire)	0.01%	100 (weak)	[29, 33, 34]
$V_{CE(\text{on})}^{[2]}$	1-chip	14.6 % (bond wire)	0.01%	1460 (strong)	[37]
$R_{CE(\text{on})}$	2-chip	1.9% (bond wire)	0.44%	4 (weak)	[36]
$I_{G(\text{peak})}$	2-chip	36% (chip)	0.05%	720 (medium)	[46-48]
$dV_{CE}/dt$	2-chip	25% (bond wire)	0.17%	147 (weak)	[38]

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 36 <sup>[1]</sup>  $V_{CE(\text{on})}$  is the on-state voltage drop under load current.

37 <sup>[2]</sup>  $V_{CE(\text{on})}$  is the on-state voltage drop at the inflexion point.  
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 39

40 Table I shows five HSPs to determine bond wire failure ( $V_{CE(\text{on})}$ ,  $R_{CE(\text{on})}$ ,  $dV_{CE}/dt$ ) and chip failure  
 41 ( $I_{G(\text{peak})}$ ). A chip failure means the loss of all bond wires connected to one chip. It is well known that  
 42 the temperature dependency of a HSP can conceal their failure signature or depreciate their ability to  
 43 detect a bond wire/chip failure. In order to determine the impact that  $T_{vj}$  has on the reading of bond  
 44 wire failure and chip failure the relative sensitivity for bond wire/chip failures and the relative  
 45 sensitivity for  $T_{vj}$  is shown in Table I. The quotient of both indicates how immune each HSP is from  
 46  $T_{vj}$  changes. As HSPs are measured in different units -  $V_{CE(\text{on})}$  is measured in V,  $dV_{CE}/dt$  in V/s,  $I_{G(\text{peak})}$   
 47 in A and  $R_{CE(\text{on})}$  in  $\Omega$  - a direct comparison of their sensitivity to temperature changes or to changes  
 48 in the number of bond wire failure or chip failure is difficult. As such the sensitivity of each HSP  
 49 must be normalised for comparison. Relative sensitivity is a normalised parameter and shown in Eq.  
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(1). In Eq. (1) ‘Variation’ is either the  $T_{vj}$  reading of HSP for a given temperature above room temperature or the reading of HSP for a given number of bond wire or chip failures. ‘Baseline value’ is either the  $T_{vj}$  reading of HSP at room temperature or the reading of HSP where all bond wires or chips are healthy.

$$\text{Relative Sensitivity} = \frac{|\text{Variation}|}{\text{Baseline value}_{\text{room temperature}}} \times 100\% \quad (1)$$

In Table I,  $R_{CE(\text{on})}$  and  $dV_{CE}/dt$  have weak immunity. That is because both have the highest temperature-dependent HSPs with 0.44% and 0.17% respectively which causes challenges in reading bond wire lift-offs. According to the references stated in the table, both techniques are not able to detect the first bond wire lift-off.  $R_{CE(\text{on})}$  is effective in determining the second bond wire lift-off whereas  $dV_{CE}/dt$  is only capable of detecting the fourth bond wire lift-off, and hence they can not be regarded as good HSPs for single bond wire lift-off.  $V_{CE(\text{on})}$  measured at load current also has a weak immunity. However,  $V_{CE(\text{on})}$  measured at the inflexion point shows the strongest resistance to  $T_{vj}$  variation. Measurement of  $V_{CE(\text{on})}$  requires regrettably HV isolation, and the measurement circuit must deal with large  $V_{CE}$  voltage swings ranging from kilovolts during the blocking stage to a few volts during the on-state stage.  $I_{G(\text{peak})}$  has a medium immunity to  $T_{vj}$  changes but detecting a peak gate current value is difficult to implement practically. As gate currents are relatively small and measurements are taken close to the IGBT module the detection circuit must also deal with EMI challenges.

So far the techniques in Table I have only been applied to IGBT switches with only one or two chips. HSP will become more challenging when there are more IGBT chips in parallel, which are typical in multichip IGBT power modules. The main challenge is the increase in the complexity in the physics of failure as well as their characteristic formation, owing to the inhomogeneous power semiconductor chips combined with the heterogeneous construction of power modules. This can lead to an accelerate chip failure subject to operational stresses, which can depreciate the HSPs or conceal their failure signature. Multichip IGBT power modules are designed for large current ratings, and the number of chips connected in parallel depends on the chip current rating and the load current rating.

The proposed method for detecting the IGBT chip failures in multichip HV IGBT power modules is presented next.

### III. PRE-THRESHOLD VOLTAGE AS HSP

The gate-emitter circuitry comprises  $R_{G(\text{ext})}$ ,  $R_{G(\text{int})}$ ,  $C_{GE}$  and  $C_{GC}$  which form an  $RC$  circuit with  $V_{GG}$  as shown in Fig. 2.  $R_{G(\text{int})}$  and  $R_{G(\text{ext})}$  are the internal and the external gate resistors respectively.  $C_{GE}$  and  $C_{GC}$  are the gate-emitter and gate-collector capacitors of the IGBT.  $V_{GG}$  is the gate voltage supply.

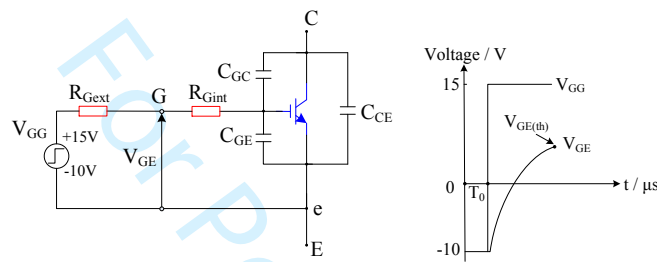


Fig. 2. RC circuit forming the waveform of  $V_{GE}$  from the PWM trigger event  $T_0$  to  $V_{GE(\text{th})}$  during turn-on.

Eq. (2) describes the exponential rising of  $V_{GE}$  at turn-on before threshold point which is reflected in Fig. 2 [36]. In Fig. 2, the off-state gate voltage supply,  $V_{GG(\text{off})}$ , is -10 V whereas the on-state gate voltage supply,  $V_{GG(\text{on})}$ , is +15 V. Thus the exponential rising of  $V_{GE}$  is due to the charging of the capacitive IGBT gate structure which is necessary prior to the IGBT module switching on.

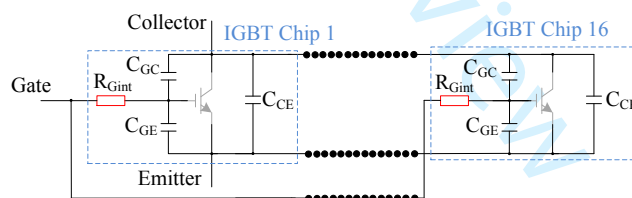
$$V_{GE(\text{pre-th})} = (V_{GE(\text{th})} - V_{GG(\text{off})}) \left( 1 - e^{-\left[ \frac{t}{R_G C_{ies}} \right]} \right) + V_{GG(\text{off})} \quad (2)$$

Where  $V_{GE(\text{th})}$  is the gate-emitter threshold voltage;  $t$  is the time;  $R_G$  is the total gate resistance which includes  $R_{G(\text{int})}$  and  $R_{G(\text{ext})}$ .  $C_{ies}$  is the gate input capacitance:

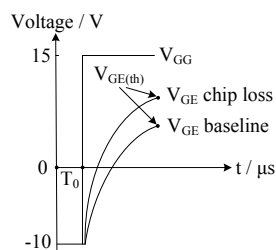
$$C_{ies} = C_{GE} + C_{GC} \quad (3)$$

In multichip IGBT power modules, each of the paralleled IGBT chips exhibits an inherent gate input capacitance and an internal gate resistance as shown in Fig. 3. Thus a healthy IGBT power module has an overall internal gate resistance,  $R_{G(\text{int}),\text{total}}$  ( $R_{G(\text{int}),\text{total}} = R_{G(\text{int})} / n$ ), and gate input capacitance,  $C_{ies,\text{total}}$  ( $C_{ies,\text{total}} = (C_{GE} + C_{GC}) \cdot n$ ), with  $R_{G(\text{int}),\text{total}}$  and  $C_{ies,\text{total}}$  being the lumped resistances and capacitances by taking each parallel connected chip  $n$  into account. DIM800NSM33-

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2 F IGBT modules have a typical  $C_{ies,total}$  of 144 nF and  $R_{G(int),total}$  of 135  $\mu\Omega$  [44]. In the case of the  
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4 total loss of bond wire connections to an IGBT chip, the effective inter-chip connection will be altered  
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6 resulting in a corresponding decline in  $C_{ies,total}$  and a rise in  $R_{G(int),total}$ . This partial open-circuit fault  
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8 within the multichip module may not necessarily lead to an outright module breakdown, but will  
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10 cause changes to its gate dynamic performance due to the  $R_{G(int),total}$  and  $C_{ies,total}$  changes with every  
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12 chip failure and therefore the  $V_{GE}$  trajectory will be altered and the baseline value of  $V_{GE(pre-th)}$  as  
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14 defined in Eq. (2) and Fig. 2 will be shifted as shown in Fig. 4. A limitation of the proposed  $V_{GE(pre-th)}$   
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16 method is that single bond wire lift-offs cannot be detected. This is because singular bond wire  
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18 failures prior to outright chip failure will not cause changes to  $R_{G(int),total}$  and  $C_{ies,total}$  because the chip  
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20 is still connected and functional through the remaining bond wires. For this reason; it is the loss of  
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22 all emitter bond wires connected to a chip which results in an outright chip failure that  $V_{GE(pre-th)}$  can  
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24 detect. Considering multichip power modules such as the DIM800NSM33-F IGBT power module  
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26 which has 16 IGBT chips and each chip has 8 emitter bond wires resulting in 128 emitter bond wires  
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28 in total, the loss of a single or few bond wires will not affect the operation at the rated current of the  
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30 power module.  
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44 Fig. 3. Representation of IGBT chip capacitances and internal resistances in multichip IGBTs.



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54 Fig. 4. Changes on  $V_{GE}$  with IGBT chip failures.

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56 Fig. 4 shows that  $V_{GE}$  always starts from a fixed voltage level and as  $V_{GE(th)}$  changes with chip  
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58 failures, the trajectory of the  $V_{GE}$  will also change. Consequently, when measuring at a fixed point of  
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60 time before  $V_{GE(th)}$ , the voltage level changes with the number of chips and this effect can be used as



a HSP for IGBT chip failures. The HSP is therefore called the pre-threshold voltage  $V_{GE(\text{pre-th})}$ . This knowledge allows the use of a simple counter that determines the point of measurement slightly before  $V_{GE(\text{th})}$  is reached. The counter will be triggered by the PWM signal to synchronise the measurement of  $V_{GE(\text{pre-th})}$ .

Although IGBT power modules would continue to operate after the initial chip failures due to the paralleling of the chips, when more chips continue to fail, a warning status is reached that can be determined as critical. This means that beyond the loss of a certain amount of chips the power module will fail. The number of acceptable loss of chips depends on the application, and this decision lies with the customer. Generally, the loss of 10% of the silicon chips can be regarded as acceptable. Therefore, for the DIM800NSM33-F module, the detection of two chip failures out of sixteen has been set as the safety margin. Consequently, the experimentations discussed next are for the initial two chip failures of the DIM800NSM33-F.

#### IV. EXPERIMENTAL SET-UP

A purpose-built high voltage high current IGBT test rig was set up based on the schematic in Fig. 5 to investigate the proposed  $V_{GE(\text{pre-th})}$  method for detecting the IGBT chip failure.

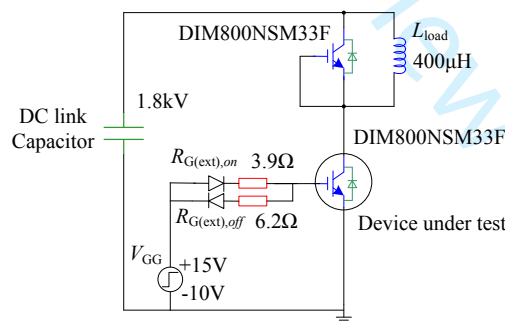


Fig. 5. Schematic for the  $V_{GE(\text{pre-th})}$ -IGBT chip failure tests.

In Fig. 5, a 400  $\mu\text{H}$  inductive load was utilised, and the DC-link supply voltage and current were set to 1800 V DC and 800 A DC respectively. The IGBT at the top is off at all times and is employed as an anti-parallel diode. The 16-chip IGBT module under test was pulsed from a gate driver with a voltage supply ranging from -10 V to +15 V. The gate driver used is the 2SC0535T2A1-33 from CONCEPT [49]. 3.9  $\Omega$  gate resistors for turn-on ( $R_{G(\text{ext}),\text{on}}$ ) and 6.2  $\Omega$  gate resistors for turn-off

( $R_{G(\text{ext}),\text{off}}$ ) were used between the ideal pulsed voltage supply and the IGBT gate terminal. The gate resistors used are thick film surface mount resistors 1206 which are recommended in the gate driver datasheet, application note and manual [49-51]. The film surface mount resistors 1206 are typically used in gate driver circuits for real applications due to their low resistance tolerance of 1% and high-power proofing to minimize the gate-loop inductances (typical with wire wound resistors which could alter the switching performance of the IGBT [52]).

A liquid temperature controlled heatsink was used to alter the IGBT power module's baseplate temperature  $T_C$  which in turn varies  $T_{vj}$  according to Eq. 4.

$$T_{vj} = T_C + P_D \cdot Z_{Th(jc)} \quad (4)$$

Where  $P_D$  and  $Z_{Th(jc)}$  are the IGBT power dissipation and the thermal impedance between the IGBT junction and case, respectively. A settling time is required to fulfil  $T_{vj}=T_C$ . The IGBT baseplate temperature ( $T_C$ ) was measured with thermocouples. The thermocouples used are Type K stainless steel washer probes with a tolerance of +/-1.5 °C [53]. In order to average out the thermocouple errors, six thermocouples were placed around the IGBT module mounting holes on the baseplate. For characterization, the IGBT  $V_{GE}$  waveform was measured by the oscilloscope to determine the best point of  $V_{GE(\text{pre-th})}$  measurement just before  $V_{GE(\text{th})}$ . A photograph of the test rig is shown in Fig. 6.

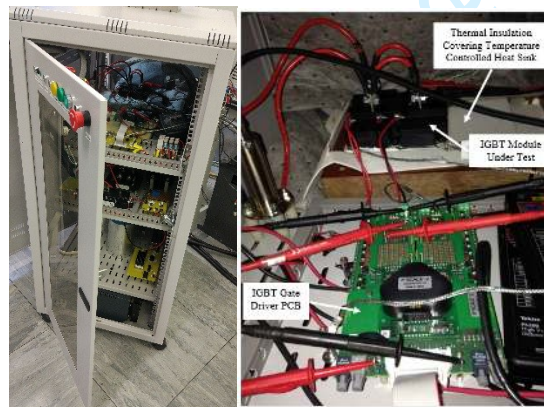


Fig. 6. Photograph of the experimental set-up: complete test rig and IGBT close-up.

IGBT chip failure has been emulated by cutting off all the emitter bond wires of the IGBT chip. Consequently, the loss of 8 emitter bond wires connected to one chip which results in an outright chip failure is referred to as '1 chip loss' in the context. The loss of 16 emitter bond wires connected

to two chips leads to the loss of two IGBT chips, which is referred to as ‘2 chip loss’, and the healthy state before chip failure is referred to as the ‘baseline’ in the experiments. An access hatch shown in Fig. 7a was developed in order to access the IGBT chips and cut off the emitter bond wires of one or two IGBT chips as shown in Fig. 7b.

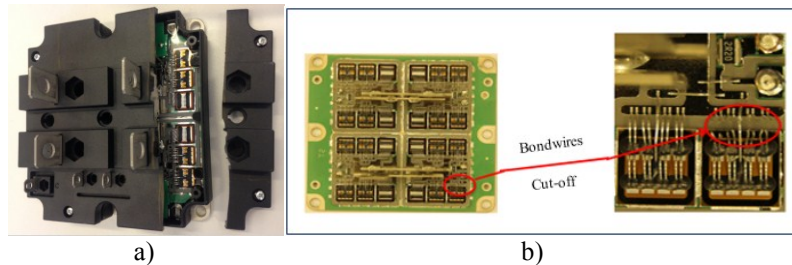


Fig. 7. Cutting off bond wires to impose IGBT chip failures: a) chip access hatch, b) Close-up of bond wires cut off.

## V. CHARACTERISATION OF $V_{GE(\text{PRE-TH})}$

Fig. 8a shows the experimental results of  $V_{GE(\text{pre-th})}$  for initial two chip failures on DIM800NSM33-F power module at  $T_{vj}$  of 20 °C. Fig. 8b illustrates the measurement point of  $V_{GE(\text{pre-th})}$  using a fixed time delay of 1.2  $\mu\text{s}$  after  $V_{GE}$  starts rising from -10 V. The results show that two successive IGBT chip failures of the sixteen-chip DIM800NSM33-F revealed a consistent trend on  $V_{GE(\text{pre-th})}$  that the voltage level  $V_{GE(\text{pre-th})}$  rises with every chip failure.

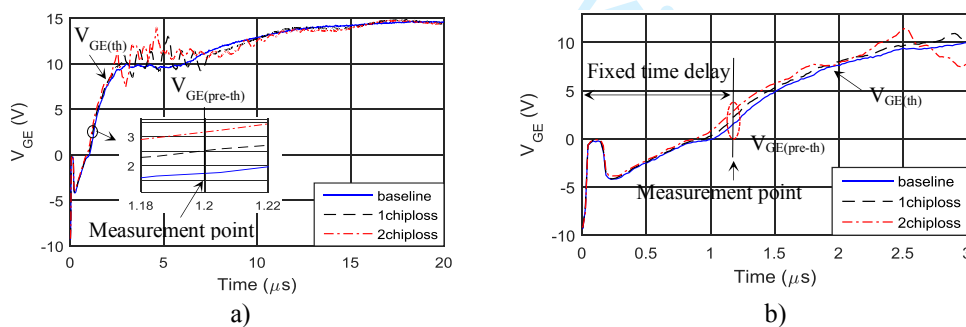


Fig. 8. a) Changes in  $V_{GE(\text{pre-th})}$  with IGBT chip failures at 20 °C, b) Use of fixed time delay for  $V_{GE(\text{pre-th})}$  measurement at 20 °C.

Fig. 9 shows that  $V_{GE(\text{pre-th})}$  is not affected by the switching transients of  $V_{CE}$  and  $I_C$  as the distortion of the uniform trend on  $V_{GE}$  occurs after  $V_{GE(\text{th})}$  when  $V_{CE}$  transient begins to fall and  $I_C$  begins to conduct/rise. Hence  $V_{GE(\text{pre-th})}$  has an advantage that it is not affected by the switching transients of  $V_{CE}$  and  $I_C$  or changes in the load size.

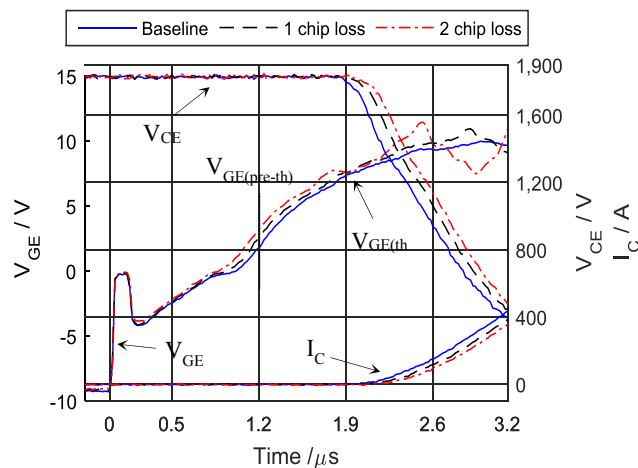


Fig. 9. Clearance of  $V_{GE(pre-th)}$  from  $I_C$  and  $V_{CE}$  switching noise at different IGBT health states.

In practice, the DC-link supply voltage ( $V_{DC-link}$ ) is regulated to a 5% fluctuation [54]. Variations in the DC-link voltage levels impact on  $V_{GE}(t)$  as shown in Eq. (5). However, the term  $dV_{CE}/dt$  in (5) remains zero 0 until  $V_{GE}(t)$  reaches  $V_{GE(th)}$ . At  $V_{GE(th)}$  current starts flowing in the IGBT and  $dV_{CE}/dt$  becomes  $dV_{CE}/dt \neq 0$  impacting on the voltage  $V_{GE}(t)$ . Therefore the proposed measurement is independent of DC-link supply voltage changes.

$$V_{GE}(t) = R_{G(int)} \left[ C_{GE} \frac{dV_{GE}}{dt} + C_{GC} \frac{d[V_{CE} - V_{GE}]}{dt} \right] \quad (5)$$

#### A. Performance with respect to temperature changes

Eq (2) shows that  $V_{GE(pre-th)}$  is directly related to  $V_{GE(th)}$ .  $V_{GE(th)}$  is temperature dependent and can be expressed [55, 56] as,

$$V_{GE(th)} = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F} \quad (6)$$

Where  $V_{FB}$  is the flat band voltage,  $\gamma$  is the body effect parameter and  $\phi_F$  is the Fermi energy which is given by:

$$\phi_F = \phi_T \ln \frac{N_A}{n_i} \quad (7)$$

with  $n_i$  as the intrinsic density,  $N_A$  as the substrate concentration, and  $\phi_T$  as the thermal voltage:

$$\phi_T = \frac{kT}{q} \quad (8)$$

Where  $k$  is the Boltzmann's constant,  $q$  is the charge of an electron and  $T$  is the temperature. The intrinsic density  $n_i$  in (6) can be written as,

$$n_i = N_A e^{-\frac{E_g}{2kT}} \quad (9)$$

Where  $E_g$  is the energy gap.

Eqs. (8) and (9) show that the thermal voltage  $\mathcal{O}_T$  (8) and the intrinsic carrier concentration  $n_i$  (9) are temperature dependent parameters which account for the temperature dependency of  $V_{GE(th)}$ . The flat band voltage in Eq. (6) has also been reported as temperature dependent [28]. Consequently, in Eq. (2),  $V_{GE(th)}$  varies with temperature and it varies the gradient of the  $V_{GE}$  waveform which can influence  $V_{GE(pre-th)}$ . Eq. (2) also shows that  $V_{GE(pre-th)}$  is related to  $R_{G(int)}$  which is also temperature dependent [11, 12]. Hence  $R_{G(int)}$  can also vary the gradient of the  $V_{GE}$  waveform when the IGBT chip temperature changes.

Therefore, it is essential to investigate how  $V_{GE(pre-th)}$  is influenced by the temperature and by the loss of chips. For this investigation, the temperature of the IGBT module has been varied through the heat plate. Tests at different temperatures are carried out before and after the chip failures. Fig. 10 shows the results of  $T_{vj}$  changes and the chip failures.

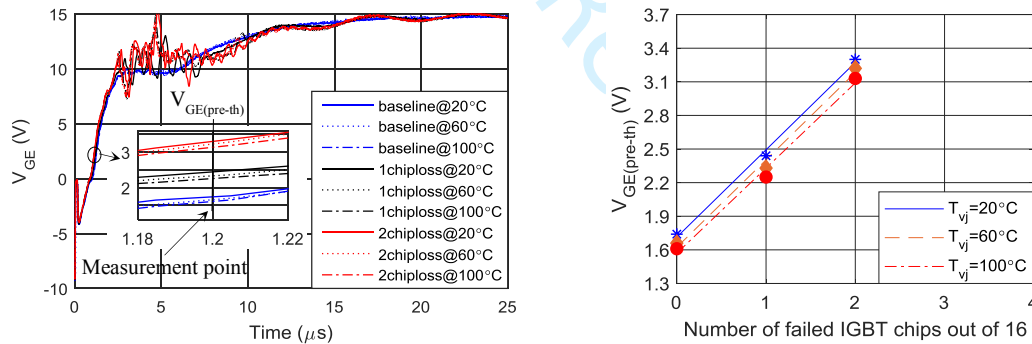


Fig. 10. Variation of  $V_{GE(pre-th)}$  with IGBT chip failures at different temperatures.

The results in Fig. 10 show linear relationships between  $V_{GE(pre-th)}$  and chip failures at each of the three temperatures. The results indicate that temperature variations do not affect the chip failure signature in  $V_{GE(pre-th)}$ . The reason is that gate-emitter voltage waveforms are very close with a small negative sensitivity of  $-2.5 \text{ mV} / ^\circ C$  when  $T_{vj}$  changes from  $20^\circ C$  to  $100^\circ C$  before the chip failure. The same observation is made when the power module lost one or two chips. Fig. 10 shows clearly that once the first chip has failed, there is a jump in the  $V_{GE(pre-th)}$  level compared to the healthy module, with a positive sensitivity of  $500 \text{ mV/chip failure}$  which is a significantly bigger change in

1  
2 voltage compared to the voltage change generated by the temperature as the  $T_{vj}$  sensitivity is only -  
3  
4 2.5 mV / °C. Another +500 mV jump in  $V_{GE(pre-th)}$  is detected when the second chip becomes  
5  
6 disconnected with the bond wires. Consequently, it can be concluded that  $V_{GE(pre-th)}$  is immune to  $T_{vj}$   
7  
8 changes as the change in  $V_{GE(pre-th)}$  due to changes in  $T_{vj}$  is always lower compared to the voltage  
9  
10 change caused by the disconnected chips. Based on Fig 10, a warning system for the power module  
11  
12 tested can be easily implemented with a simple lookup table that holds the following information:  
13  
14  $V_{GE(pre-th)} < 2.0$  V - power module is healthy (baseline);  $2.0$  V  $< V_{GE(pre-th)} < 2.8$  V - one IGBT chip  
15  
16 has failed;  $V_{GE(pre-th)} > 2.8$  V - two IGBT chips have failed.  
17  
18  
19

20  
21 In Table I,  $I_{G(peak)}$  is the only HSP for IGBT chip failure detection which can be compared with  
22  
23  $V_{GE(pre-th)}$ . Using Eq. (1), the relative sensitivity of  $V_{GE(pre-th)}$  is 0.11 % for  $T_{vj}$  and 28.7 % for chip  
24  
25 failures. This compares well with  $I_{G(peak)}$  which has a strong immunity to  $T_{vj}$  with a  $T_{vj}$  relative  
26  
27 sensitivity of 0.05 % and the chip failure sensitivity of 36 %. The main advantage of  $V_{GE(pre-th)}$  over  
28  
29  $I_{G(peak)}$  is that  $V_{GE(pre-th)}$  employs a voltage sensor while  $I_{G(peak)}$  utilises a current sensor. In general,  
30  
31 voltage sensors are cheaper, simpler and lightweight compared to current sensors hence voltage-  
32  
33 based HSPs are preferred from a practical perspective [57].  
34  
35  
36

### 37 B. Changes in $R_{G(ext)}$

38  
39  $R_{G(ext)}$  is one of the most influential components on  $V_{GE(pre-th)}$  according to Eq. (2).  $R_{G(ext)}$  is located  
40  
41 on the IGBT power module's external circuitry and is temperature sensitive. For this reason, the  
42  
43 impact of changes in  $R_{G(ext)}$  has been investigated.  
44  
45

46  
47 The gate resistors employed for  $R_{G(ext)}$  have a temperature coefficient of resistance (TCR) of  
48  
49 100ppm/K and thus the overall turn-on resistance changes from 3.9  $\Omega$  to 3.93  $\Omega$  for an 80 °C rise in  
50  
51 temperature rise of the 3.9  $\Omega$   $R_{G(ext),on}$  utilised [52]. This effect was examined with the next available  
52  
53  $R_{G(ext),on}$  of 3.96  $\Omega$ . The results in Fig. 11a depict a negligible impact on the chip failure signature of  
54  
55  $V_{GE(pre-th)}$ .  
56  
57  
58  
59  
60

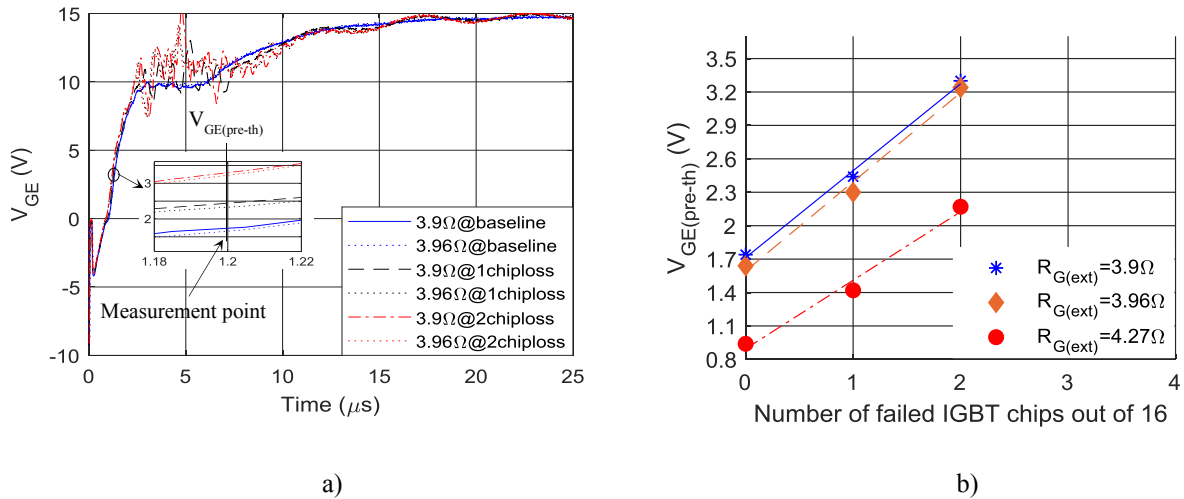


Fig. 11.  $V_{GE}$  behaviour with changes in  $R_{G(\text{ext})}$  and chip failures at 20 °C.

Fig. 11b shows six  $V_{GE(\text{pre-th})}$  measurements with  $R_{G(\text{ext}),on}$  of 3.9  $\Omega$  and  $R_{G(\text{ext}),on}$  of 3.96  $\Omega$  in the baseline, 1 chip failure and 2 chip failure conditions. The maximum error in the 3.9  $\Omega$  and 3.96  $\Omega$  measurements is only 4.5 % and does not have an impact on the chip failure signature of  $V_{GE(\text{pre-th})}$ .

The sizing of  $R_{G(\text{ext})}$  depends on the application. Fig. 11b includes three  $V_{GE(\text{pre-th})}$  measurements for 5 % increase in  $R_{G(\text{ext}),on}$  when it is physically changed to 4.27  $\Omega$ . The results show that only two chip failures can be detected as a  $V_{GE(\text{pre-th})}$  reading of 1.42 V for the first chip failure falls within the baseline threshold and only the 2.2 V reading for two chip failures exceeded the baseline threshold. However, the  $V_{GE(\text{pre-th})}$  reading of 2.2 V for two chip failures with  $R_{G(\text{ext}),on}$  of 4.27  $\Omega$  is within the one chip failure threshold of  $2.0 \text{ V} < V_{GE(\text{pre-th})} < 2.8$  for this power module. Hence the chip failure alarm is true, but the prediction is one chip failure rather than two chip failures which is false.

Consequently, it has been concluded that  $V_{GE(\text{pre-th})}$  is highly dependent on  $R_{G(\text{ext})}$ . When the same  $R_{G(\text{ext})}$  is utilised, the impact of temperature changes on  $R_{G(\text{ext})}$  can be ignored. Whereas when  $R_{G(\text{ext})}$  is physically changed, different  $R_{G(\text{ext})}$  values will lead to different results, but the fundamental  $V_{GE(\text{pre-th})}$  principle remains. Therefore any physical change of  $R_{G(\text{ext}),on}$  by more than 1 % requires a recalibration of  $V_{GE(\text{pre-th})}$ .

### C. Changes in $V_{GG}$

The impact of changes in the gate driver supply voltage,  $V_{GG}$ , has been investigated due to the relation with  $V_{GE(\text{pre-th})}$  in Eq. (2). The gate driver used includes voltage regulation for a reliable  $V_{GG(on)}$



to +15 V for IGBT turn-on, and -10 V ( $V_{GG(\text{off})}$ ) for IGBT turn-off is not regulated as it provides the compensation when  $V_{GG(\text{on})}$  fluctuates [51]. Eq. (2) shows a direct relation of  $V_{GE(\text{pre-th})}$  with  $V_{GG(\text{off})}$ . Consequently if  $V_{GG(\text{off})}$  varies,  $V_{GE(\text{pre-th})}$  varies too. Given  $V_{GG}$  fluctuation, component tolerances and temperature dependence of the gate driver components, the impact of 2 % and 5 % error on -10 V  $V_{GG(\text{off})}$  resulting in -9.8 V and -9.5 V has been investigated.

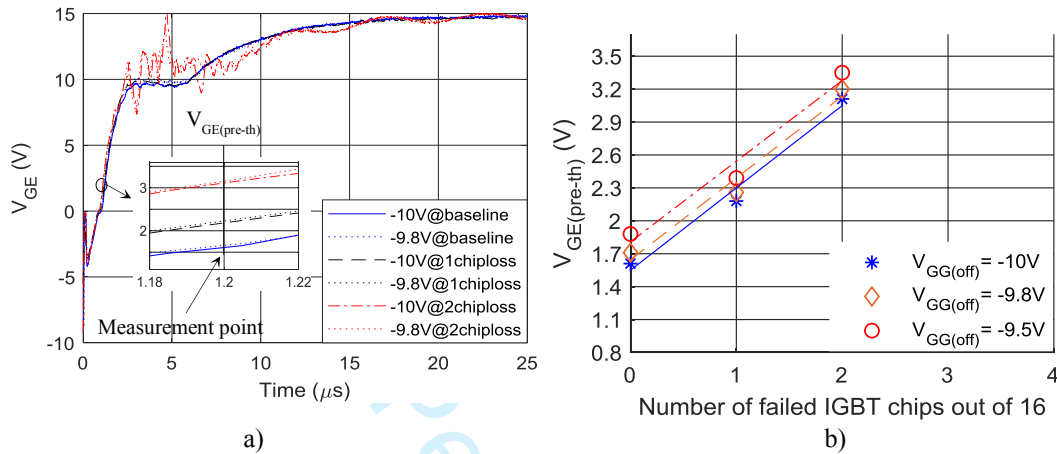


Fig. 12.  $V_{GE}$  behaviour with changes in  $V_{GG}$  and chip failures at 20 °C.

Fig. 12a. shows the voltage waveform for a 2 % change in  $V_{GG(\text{off})}$  and Fig. 12b shows a comparison between 2 % and 5 % error compared to -10V in  $V_{GG(\text{off})}$ . Fig. 12b shows that there is enough margin in  $V_{GE(\text{pre-th})}$  between every chip failure to allow signalling the detection of chip failures. Fig. 12b also shows repeatability in the context of changes in  $V_{GG(\text{off})}$  during two measurements. For example, if voltage fluctuations cause an error of 5 % in  $V_{GG(\text{off})}$  during baseline condition,  $V_{GE(\text{pre-th})}$  is in the order of 1.9 V following Fig. 12b. This is 100 mV under the threshold margin that flags up 1 chip failure as described in section B. If the voltage fluctuation disappears so that  $V_{GG(\text{off})}$  stabilises back to -10 V and a chip has failed during that period then the second  $V_{GE(\text{pre-th})}$  reading results in 2.1 V (from Fig. 12b). This value is within the reference to flag up 1 chip failure in the look-up table (2.0 V to 2.8 V). Consequently, the proposed circuit is immune to  $V_{GG(\text{off})}$  fluctuations up to 5 %. If, however, a higher error is expected then a voltage sensor should be added to measure  $V_{GG(\text{off})}$ . This information can then be processed to correct the value of  $V_{GE(\text{pre-th})}$ .



### D. Repeatability

The previous sections have so far demonstrated the impact of  $V_{DC-link}$ ,  $T_{vj}$ ,  $R_{G(ext)}$ ,  $V_{GG(off)}$  on the  $V_{GE(pre-th)}$  measurement for one power module to determine chip failures. A second DIM800NSM33-F IGBT power module has been used to show if the proposed method produces the same results in terms of chip failure detection. Fig. 13 shows the measurement results conducted on two DIM800NSM33-F IGBT power modules (Modules A and B). Results at  $T_{vj}=20^\circ\text{C}$  are portrayed in Fig. 13 where, for the same fixed time delay ( $1.2\mu\text{s}$ ), the recorded errors are: 4.0 % at baseline, 10.3 % with 1 chip failure and 6.7 % with 2 chip failures. The small differences in errors show that  $V_{GE(pre-th)}$  is repeatable based on the same decision statement used before:  $V_{GE(pre-th)} < 2.0\text{ V}$  - baseline;  $2.0\text{ V} < V_{GE(pre-th)} < 2.8\text{ V}$  - 1 chip failure; and  $V_{GE(pre-th)} > 2.8\text{ V}$  - 2 chip failures.

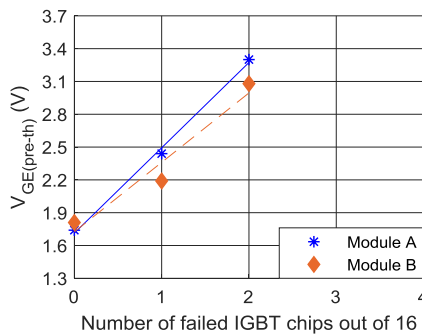


Fig. 13. Experimental Results of  $V_{GE(pre-th)}$  on a Different DIM800NSM33-F Power Modules at  $20^\circ\text{C}$ .

## VI. $V_{GE(PRE-TH)}$ PRACTICAL IMPLEMENTATION

On the premise of a known baseline value, two methods can normally be carried out for signal acquisition of the  $V_{GE(pre-th)}$  profile. Firstly, a snapshot measurement of  $V_{GE(pre-th)}$  can be taken at a fixed time instant corresponding to a pre-defined threshold value during the  $V_{GE}$  ramping-up. Alternatively, a fixed  $V_{GE(pre-th)}$  can be related to the lapse in time taken to reach  $V_{GE(pre-th)}$ . The results obtained in this paper are based on the former method where the time is fixed and  $V_{GE(pre-th)}$  is measured.

IGBT gate turn-on transients are in the order of hundreds of nanoseconds thus precise measurements necessitate a fast-respond triggering function and high bandwidth Sample-and-Hold (S/H) amplifiers to track the signal. Fig. 14 shows a simplified schematic of the hardware

implementation for  $V_{GE(\text{pre-th})}$  measurement, which was embedded in the DIM800NSM33-F gate driver.

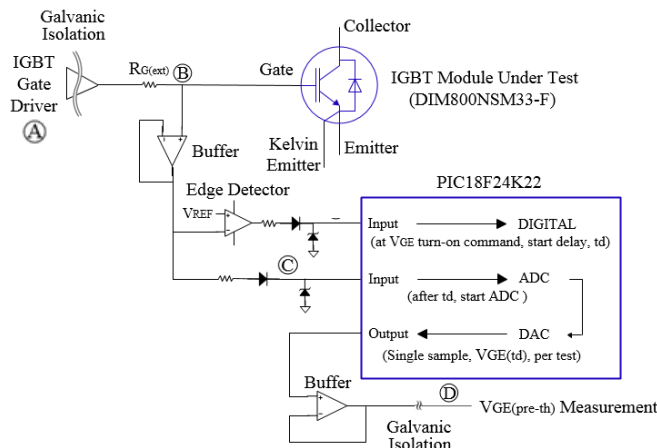


Fig. 14. Schematic of  $V_{GE(\text{pre-th})}$  measurement circuit for IGBT chip failure monitoring.

Fig. 14 shows the measurement points marked A, B, C and D where  $V_{GD(\text{cs})}$  (gate driver control signal),  $V_{GE}$ ,  $V_{GE(\text{pic})}$  ( $V_{GE}$  analogue input to a programmable interrupt controller (PIC) for  $V_{GE(\text{pre-th})}$  measurement) and D  $V_{GE(\text{pre-th})}$  signals are measured from respectively. The input buffer uses an operational amplifier (op-amp) to ameliorate the source impedance as the first stage in collecting  $V_{GE(\text{pre-th})}$ . The buffer also prevents the  $V_{GE(\text{pre-th})}$  measurement circuit from loading the gate driver. In this way, the gate's normal operation is not affected, and thus the proposed  $V_{GE(\text{pre-th})}$  monitoring interface is suitable for online applications.

An edge detector is also shown in Fig. 14. The gate driver applies -10 V to maintain the off-state of the IGBT. Following a turn-on command, the gate input capacitance is charged by a +15 V gate voltage supply and  $V_{GE}$  starts to rise from -10 V. The edge detector is used to monitor the  $V_{GE}$  rising process and when it reaches -8 V, the edge detector sets off a delay counter in the PIC via a general purpose input-output (GPIO) on the PIC. The PIC utilized is the PIC18F24K22 with a clock speed of 64 MHz. A delay of 1.2  $\mu\text{s}$  has been predetermined to trigger the S/H circuit. After a 1.2  $\mu\text{s}$  delay, an Analogue-to-Digital Converter (ADC) in the PIC measures  $V_{GE(\text{pre-th})}$ . To allow the precise acquisition of  $V_{GE(\text{pre-th})}$  the PIC code enables the ADC module at the same time when the time delay counter is started by the edge detector and configures it ready to measure  $V_{GE(\text{pre-th})}$ . When the 1.2  $\mu\text{s}$  time delay is reached, the  $V_{GE(\text{pre-th})}$  sample is acquired immediately by the ADC. The  $V_{GE(\text{pre-th})}$

1  
2 technique only requires a single sample at a time. Hence the fast-rising  $V_{GE}$  does not need to be  
3  
4 tracked. If assurance is required, the proposed single  $V_{GE(\text{pre-th})}$  measurement process can be repeated.  
5  
6 A lookup table is included in the PIC using a simple code with the  $V_{GE(\text{pre-th})}$  threshold values for  
7  
8 different IGBT chip failure count. Thus the measured  $V_{GE(\text{pre-th})}$  value, as well as the on-going chip  
9  
10 failure count of the IGBT, are provided.  
11  
12

13  
14  $V_{GE(\text{pre-th})}$  is more pronounced in the  $V_{GE}$  region between the zero-crossing and 5 V which are  
15  
16 within the voltage rating of the PIC pins. Thus a diode and Zener diode combination has been utilised  
17  
18 as shown in Fig. 14 to allow only the  $V_{GE}$  portion between zero and 5 V to progress through to the  
19  
20 PIC. This protects the PIC from overvoltage and negative voltage. Fig. 14 also shows galvanic  
21  
22 isolation of the gate driver input as well as the  $V_{GE(\text{pre-th})}$  output. These isolation barriers are necessary  
23  
24 to protect users as well as the associated low voltage components and equipment from the high  
25  
26 voltage environment on the IGBT power module's collector-emitter circuit.  
27  
28

#### 30 A. $V_{GE(\text{pre-th})}$ measuring techniques

31  
32 As the proposed  $V_{GE}$  measurement is before the threshold  $V_{GE(\text{th})}$ , at which the IGBT switches on,  
33  
34  $V_{GE(\text{pre-th})}$  measurements can be conducted in two modes: Mode 1 is during the turn-on period that is  
35  
36 signalled by the PWM controller, and Mode 2 during the off-state of the IGBT which is determined  
37  
38 by the PWM signal. In both cases, the same information about the chip failure(s) can be detected.  
39  
40

##### 41 1) *Mode 1*

42  
43 This is when  $V_{GE(\text{pre-th})}$  measurements are collected online during the normal IGBT switching  
44  
45 operation. The IGBT is thus driven normally and  $V_{GE}$  continues to its full gate voltage of 15 V of the  
46  
47 normal duty cycle.  
48  
49

50  
51 In Fig. 15  $V_{GE(\text{pre-th})}$  of 1.8 V is successfully measured online in a typical PWM at 20 °C for a  
52  
53 healthy power module. The frequency of the PWM is 1 kHz which is typically used in high voltage  
54  
55 applications [58]. In each pulse,  $V_{GE(\text{pre-th})}$  is measured at the required time instant of 1.2  $\mu\text{s}$  after  $V_{GE}$   
56  
57 starts rising from -10 V. The measured  $V_{GE(\text{pre-th})}$  is then available approximately 10  $\mu\text{s}$  later after the  
58  
59 measurement event which is caused by the processing time of the ADC employed. A faster ADC  
60

may be utilised, but this is not necessary because in health monitoring, wear out failures are gradual and slow compared to switching frequencies thus time can be afforded for processing and transfer of data to a host computer.

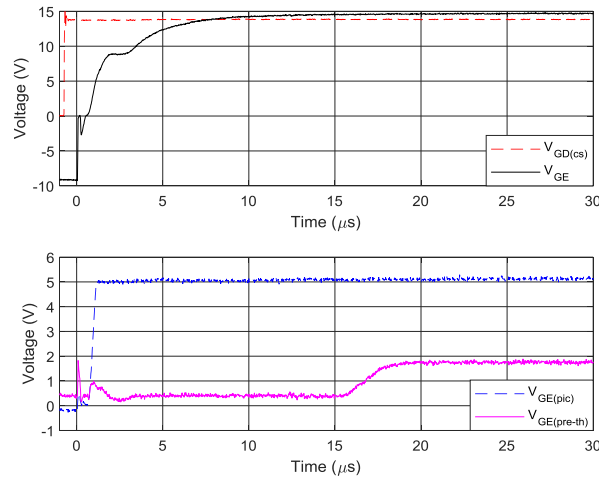


Fig. 15. Mode 1 waveforms of  $V_{GE(\text{pre-th})}$  applied during the on-state of the IGBT (duty cycle: 35%).

## 2) Mode 2

In this mode the PWM signal is low, and the IGBT is in the off-state. An interrupt routine which determines the health measurement override the off-status of the PWM signal and triggers the gate driver with a duty cycle that allows only enough time to produce the required  $V_{GE}$  transient at which  $V_{GE(\text{pre-th})}$  is measured, and then turning off the IGBT. In this way, the status of  $V_{CE}$  and  $I_C$  is not affected:  $V_{CE}$  remains in the blocking state, thus the switch never turns-on. This mode can be extended to test IGBTs during stand-by where for a longer period of time the devices are off. Fig. 16 shows such a pre-mature  $V_{GE}$  pulse for testing  $V_{GE(\text{pre-th})}$  during the off-time of the IGBT. The pulse lasts only  $2\mu\text{s}$ . Activation of this pre-mature pulse must be considered in the controller. Hence the test is only possible when the IGBT is in the off-state at the end of the pre-mature pulse and before the next PWM pulse. Fig. 16 shows the successful  $V_{GE(\text{pre-th})}$  measurement of 1.8 V at 20 °C for a healthy power module similar to Mode 1 above.

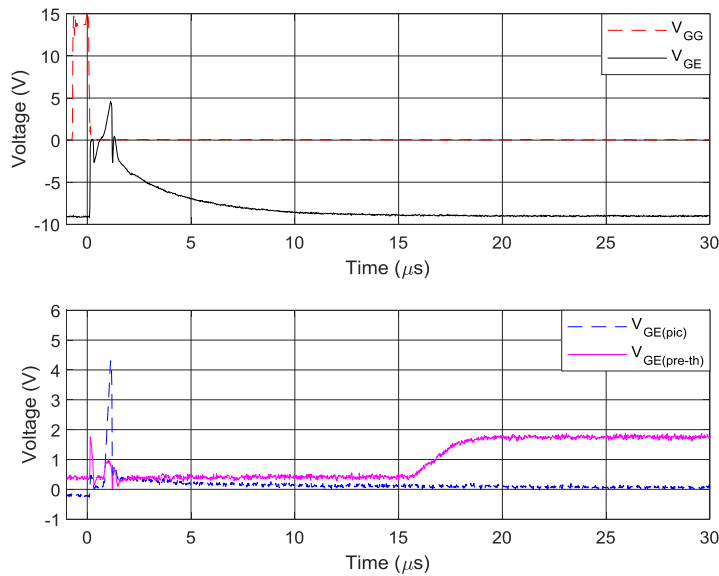


Fig. 16. Mode 2 waveforms of  $V_{GE(pre-th)}$  applied during the off-state of the IGBT (duty cycle: 0.07%).

Table II shows the results using the  $V_{GE(pre-th)}$  measurement circuit in Fig.14. The measurements are conducted on different DIM800NSM33-F IGBT power modules from the same manufacturing batch as the modules tested in section IV. The lookup table is derived from the characterization of the IGBT modules presented in section IV. The results show successful implementation as the correct information about the chip failure count is obtained according to the lookup table.

Table II. IGBT measurements with  $V_{GE(pre-th)}$  circuit.

Lookup table (V)		$V_{GE(pre-th)}$ circuit		
		$V_{GE(pre-th)}$ (V)		Prediction IGBT chip failure count
		20 °C	100 °C	
<b>Baseline</b>	$V_{GE(pre-th)} < 2.0$	1.86	1.71	<b>0</b>
<b>1 Chip failure</b>	$2.0 < V_{GE(pre-th)} < 2.8$	2.25	2.12	<b>1</b>
<b>2 Chip failures</b>	$2.8 < V_{GE(pre-th)}$	3.03	2.88	<b>2</b>

## VII. CONCLUSION

A new health sensitive parameter for IGBT chip failure monitoring in multichip IGBT modules was proposed. The method is  $V_{GE(pre-th)}$  which takes place during the  $V_{GE}$  transient for turning on the IGBT.  $V_{GE(pre-th)}$  is measured at a defined time instant between  $V_{GE}$  zero-crossing and the threshold voltage.  $V_{GE(pre-th)}$  thus requires less hardware with only a voltage sensor and a counter. Practical

1  
2 results reveal a good  $V_{GE(\text{pre-th})}$  performance with IGBT chip failures with an average sensitivity of  
3  
4 500 mV per chip failure.  
5

6 The hardware implementation of  $V_{GE(\text{pre-th})}$  has been described. Two techniques have been  
7  
8 illustrated where an IGBT can be tested during IGBT turn-on as well as during the off-state. In both  
9  
10 cases, the same information about number of chip failure(s) can be detected which makes  $V_{GE(\text{pre-th})}$   
11  
12 more versatile than any other health sensitive parameter. The proposed circuit has been successfully  
13  
14 implemented on the IGBT gate driver and the correct information about the chip failure count has  
15  
16 been obtained. A limitation of the method is that detection of singular bond wires failures are not  
17  
18 possible. However, for multichip power modules, the loss of a single or few bond wires will not affect  
19  
20 the normal operation or the capability of the power module.  
21  
22  
23

24 Since it is based on the low voltage gate side rather than the high voltage collector side of the  
25  
26 IGBT,  $V_{GE(\text{pre-th})}$  does not require high voltage isolation nor high voltage insulation.  $V_{GE(\text{pre-th})}$  shows  
27  
28 a good temperature immunity and high sensitivity to chip failures. However,  $V_{GE(\text{pre-th})}$  is highly  
29  
30 dependent on  $R_{G(\text{ext})}$ . While the impact of temperature changes on  $R_{G(\text{ext})}$  can be ignored, the physical  
31  
32 alteration of  $R_{G(\text{ext})}$  in excess of 1% requires a re-calibration of  $V_{GE(\text{pre-th})}$ . Other influences like gate  
33  
34 driver voltage fluctuations have also been investigated. The method performs well with a 5%  
35  
36 fluctuation in  $V_{GG(\text{off})}$ .  
37  
38  
39

40  $V_{GE(\text{pre-th})}$  is applicable to standard multichip IGBT power modules such as 3.3 kV, 4.5 kV and 6.5  
41  
42 kV IGBT modules as they have similar structures. Future work will aim to demonstrate the  
43  
44 performance of  $V_{GE(\text{pre-th})}$  in an operative converter configuration.  
45  
46  
47

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### Reviewer 1

We like to say thank you to Reviewer 1 in reading our manuscript and in providing us with helpful information to improve the paper. We have in-cooperated all of your comments.

Recommendation: Revision – The paper is not accepted, but authors are given one chance to respond to reviewers' comments with a revision in 6 weeks or less.

Comments:

The paper deals with a very hot topic and presents a new method to estimate the degradation of high power IGBT modules. This method seems to be very attractive because it is very simple to implement. The sensitivity is good allowing for simple measurements. However, I think that lots of improvements must be made prior to publish it in this journal.

Introduction:

- for me it is too long.

We have shortened the introduction section.

- I don't understand why the authors present lots of papers on junction temperature measurements because the paper is not focused on this topic.

We agree that we added too many references for TSEPs. We, therefore, reduced the TSEP references.

- On the contrary, Table I seems to be poor and very few references on health monitoring methods are given.

We have added more references on health monitoring methods and improved the table. The table now compares the techniques proposed for bond wire failure and chip failure detection which are common in IGBT health monitoring.

-p3, line 56: "Collector" instead of "collector"

We thank the Reviewer for picking this up and have changed it accordingly.

Section II:

-I don't see the interest of Fig. 2,

1  
2  
3 Originally, we wanted to illustrate the general operation procedure of the health monitoring technique.  
4 We agree that this is confusing and consequently deleted the figure.  
5  
6

7  
8 -you don' speak about diodes but they are present in the module. Could you explain why?  
9

10  
11 The work focusses only on health monitoring of IGBT chips. We now highlighted this in the title and  
12 added a sentence in the abstract, the introduction and section IV. We have also explained why we  
13 focus on IGBT chips rather diode chips. The main reason is that IGBT chips experience higher  
14 thermal stresses compared to diodes hence IGBT chips are more susceptible to failures compared to  
15 diode chips.  
16  
17  
18

19  
20 -you have a A. paragraph but not a B.  
21

22  
23 Thank you for spotting this. We deleted A. paragraph.  
24

25  
26 -you dont speak about the temperature dependency of all these parameters which is, for me,  
27 a real issue.  
28

29  
30 We agree with the Reviewer that the temperature dependency of all the existing techniques is an  
31 important factor and it should be considered when assessing performance of the methods. Therefore,  
32 additional features are added in Table I to show the temperature dependency of the techniques and the  
33 impact of the temperature dependency on their ability to detect bond wires or chip failures. In addition,  
34 we also compared the immunity to  $T_{vj}$  variation of all these techniques. An additional illustration is also  
35 included.  
36  
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39

40  
41 -a table could be interesting to compare all these parameters with yours.  
42

43  
44 We agree with the Reviewer that a table is necessary to compare the techniques. As the methods are  
45 measured in different units, we have added a technique to normalise their sensitivities to relative  
46 sensitivities and then compared them using Table I. The existing techniques which are  $V_{CE(on)}$ ,  $I_{G(peak)}$ ,  
47  $R_{CE(on)}$  and  $dV_{CE}/dt$  are then analysed according to the following aspects: the number of IGBT chips of  
48 the device under test, relative sensitivity of the HSP for bond wire failure, relative sensitivity the HSP  
49 for  $T_{vj}$  as well as their immunity to  $T_{vj}$  variation in section. We then made a comparison with  $I_{G(peak)}$  which  
50 detect chips and is comparable with the proposed technique in section IV. We concluded that both  
51 methods have has a strong immunity to  $T_{vj}$  and the main advantage of the proposed method,  $V_{GE(pre-th)}$ ,  
52 over  $I_{G(peak)}$  is that  $V_{GE(pre-th)}$  employs a voltage sensor while  $I_{G(peak)}$  utilises a current sensor. And in general,  
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3 voltage sensors are cheaper, simpler and lightweight compared to current sensors hence voltage-based  
4 HSPs are preferred from a practical perspective.  
5  
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8 Section III.

9 -Fig. 6 is unreadable,  
10  
11

12 We agree that the quality of the figure is not good. The result presented is from a Saber simulation. The  
13 simulation work has been taken out in the revised manuscript. Thus the figure has been deleted.  
14  
15

16  
17 - p9 line 23: why do you speak about a new TSEP?  
18  
19

20 Thank you for spotting this. We mean HSP instead of TSEP. Thus TSEP has changed to HSP.  
21  
22

23 -what is the interest of eq. 2 in this paper?  
24  
25

26 The equation is used to illustrate the relationship between the virtual junction temperature,  $T_{vj}$ , and the  
27 baseplate temperature,  $T_c$ . We want to show that the virtual junction temperature can be varied from  
28 the baseplate as they are related in Eq. 2. Assuming power loss of a single switching transient is minimal.  
29 Hence  $P_d$  is small, we assume that  $T_{vj}=T_c$ . Therefore, in the tests, a temperature controlled heat plate  
30 was utilised to alter  $T_{vj}$ .  
31  
32  
33

34  
35 -is the  $R_{gint}$  variation with the temperature implemented in Saber? Why have you not the  
36 same temperature dependency here compared with the experiments?  
37  
38

39 The simulation has been taken out in the revised manuscript. We have added some experimental  
40 results on the impact of temperature changes.  
41  
42  
43

44 - Are simulations necessary? The use of eq. 1 is not sufficient to demonstrate the main  
45 results?  
46  
47

48 We agree that simulations are not essential hence simulations have been taken out. We have added  
49 more theoretical analysis to explain the main results.  
50  
51

52 -finally, I don't understand the interest of the simulation section because you don't compare  
53 the results with the experimental ones.  
54  
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56  
57 We agree that simulations are not essential and consequently are taken out in the revised manuscript.  
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3 Section IV:

4 -generally, the quality of the figures has to be largely improved  
5  
6

7 We have improved the quality of the figures.  
8  
9

10 -p12, line 32, could you be more specific about the "low temperature tolerance"? Are these  
11 resistances classically used to drive power modules?  
12  
13

14 We thank the reviewer for picking this up. It is a terminology error, which should have been resistance  
15 tolerance. This is now corrected and the wording has been improved.  
16  
17  
18

19 Yes, and we have improved the statement by stating that the film surface resistors 1206 are  
20 recommended in gate driver datasheets and are common in gate driver circuits due to attractive features  
21 such as low resistance tolerance.  
22  
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24

25 -p13: you give voltage variations due to IGBT loss. Could you compare these variations with  
26 theoretical ones? Why this voltage variation is not the same for the first and the second  
27 losses?  
28  
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30

31 The equal voltages for one or two chip losses scenarios align with theoretical analysis since we have  
32 improved the discussions of results with more analysis linking results with theory. We have included  
33 more tests results which show that the variation of the first and second chip losses are generally the  
34 same.  
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40 -p14: you write that voltage drop due to temperature variation is negligible. I don't agree:  
41 the variation is 0.2V after the second loss which is not far away from the temperature drop  
42 due to the loss itself (0.5V)! Maybe if you would have used another power module, the result  
43 could be completely different.  
44  
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48

49 Initially, we want to illustrate the immunity of  $V_{GE(pre-th)}$  to temperature. We mean that the change of  
50  $V_{GE(pre-th)}$  over 80°C temperature variation is about 0.2V. The change of  $V_{GE(pre-th)}$  at one chip loss is  
51 more than 0.2V, about 0.5V on average. This means that the temperature variation will not affect the  
52 chip failure detection. Now we have largely improved the temperature analysis to make the temperature  
53 dependence clear as it is crucial. We included more test results and demonstrated that the proposed  
54 method performs well even when there are temperature changes in the IGBT module.  
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3 - About this variation with temperature: why do you have this variation, what is the physical  
4 explanation? Why do you have different simulation results?  
5  
6

7 In general, the HSPs are temperature dependent which means temperature variation will lead to change  
8 in HSP. As we know, bond wire and chip failures also lead to changes in HSP. Therefore, we want to  
9 include the discussion about the temperature dependency of the HSP and to verify that the temperature  
10 dependency of the proposed  $V_{GE(pre-th)}$  approach will not influence the bond wire and chip failure  
11 detection. We have shown more results and explained their link to the theory, to make the temperature  
12 dependence discussion clear.  
13  
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16

17 The simulation results do not coincide with the experimental results which can be accounted to  
18 inaccurate simulation model of the real device tested. We have taken out the simulation and added  
19 more experimental results, and demonstrated that the proposed methods performs well even when  
20 there is temperature changes in the IGBT module.  
21  
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26 -Fig. 11: could you explain the shape of the waveform: they are completely different from the  
27 shapes obtained in simulation?  
28  
29

30 We admit that the simulation results do not coincide with the experimental results. The simulation  
31 results displayed in the original paper are only part of the switching waveform. The overall switching  
32 waveform shows the same tendency as the experimental results. As simulation results have been taken  
33 out, we added more explanation about why the  $V_{GE}$  trajectory changes when there are bond wire failure  
34 and junction temperature change in section IV and section V. We have also added more experimental  
35 results and linked them with the theory.  
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41 -Fig. 15 and 16: are they experimental or simulation results? In the case of experimental  
42 results, give the measurement points.  
43  
44

45 Fig. 15 and 16 are simulation results. We have replaced them since simulation have been taken out. We  
46 added Fig.9 to illustrate the immunity of  $V_{GE(pre-th)}$  to the DC-link voltage. More analysis has been  
47 included in the revised manuscript. Fig.16 is replaced with experimental results shown in Fig.12. The  
48 measurement points have also been highlighted in the results.  
49  
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52

53 - Why do you test the influence of  $V_{DC}$ ? Please explain the physical impact of this voltage.  
54  
55

56 The relationship between  $V_{DC}$  and the waveform of  $V_{GE(pre-th)}$  is explained in section V. The analysis  
57 shows that  $V_{GE(pre-th)}$  has good immunity to the DC-link voltage.  
58  
59  
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1  
2  
3 -why do you not study the influence of  $R_{G(ext)}$ ?  
4  
5

6 We thank the reviewer for noticing this. As we know, the change of the gate resistor will vary the  
7 switching speed of the IGBT module. Hence, the measurement point of the  $V_{GE(pre-th)}$  will change,  
8 which makes the voltage at fixed time instant incomparable when the external resistor is not the same.  
9 However, it is important to investigate the influence of the  $R_{G(ext)}$ . Now, we have highlighted the need  
10 to examine the influence of changes in  $R_{G(ext)}$  as the equation of the method shows a relation with  $R_{G(ext)}$ .  
11 We have included a section with the study and experimental results of the impact of  $R_{G(ext)}$  impact. We  
12 have concluded that  $V_{GE(pre-th)}$  is highly dependent on  $R_{G(ext)}$ . However, when the same  $R_{G(ext)}$  is utilised,  
13 the impact of temperature changes on  $R_{G(ext)}$  can be ignored. Whereas when  $R_{G(ext)}$  is physically  
14 changed, different  $R_{G(ext)}$  values will lead to different results, but the fundamental  $V_{GE(pre-th)}$  principal  
15 remains. Therefore we recommended that any physical change of  $R_{G(ext)}$  of more than 1% require re-  
16 calibration of  $V_{GE(pre-th)}$ .  
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26 -some information about repeatability should be interesting.  
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29 We have included a section about the repeatability of the proposed method and defined the  
30 repeatability in the revised manuscript. Practical results and analysis have also been presented which  
31 show that the proposed method is repeatable.  
32  
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35 Section V.

36 -I don't understand the interest of Fig. 18 and 19,  
37  
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39 We agree and have removed both figures as the information has already been shown in other figures.  
40  
41  
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43 - The scales of Fig. 20 and 22 are not adapted  
44  
45

46 We have improved the figures and shown results for both figures on better scales. Now they are Fig.15  
47 and Fig.16.  
48  
49

50 - Some information about repeatability? What is the difference between two consecutive  
51 measurements? Is an averaging necessary or not?  
52  
53

54 We have included a section on repeatability of the proposed method and defined repeatability in the  
55 revised manuscript. We have included practical results and analysis to exhibit that the proposed method  
56 is repeatable. We have demonstrated the application procedure of the proposed approach in section  
57 VI.  
58  
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3 -p21: I don't understand your comments about the 5% measurement error. I understood that  
4 you worked with a 5V ADC 10 bits --> resolution 5mV very far from 5%.  
5  
6

7 We thank the reviewers for picking this up. It should be 0.1%. In the revised manuscript we have taken  
8 a different approach to discuss the results as the 10-bit ADC had no impact on the results. We have  
9 demonstrated the application and measuring procedure of the proposed approach in section VI. We  
10 have added section on repeatability and shown that the proposed method is repeatable.  
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14  
15 -the implementation is not complete --> you have to explain how you find a chip loss in on-  
16 line conditions.  
17  
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19 The implementation section has been improved to show how the lookup tables, the PIC and the ADC  
20 were utilised. We have shown successful implementation of the online chip loss monitoring circuit in a  
21 commercially available IGBT gate driver.  
22  
23  
24

## 25 Reviewer 2

26  
27  
28 We like to say thank you to Reviewer 2 in reading our manuscript and in providing us with helpful  
29 information to improve the paper. We have in-cooperated all of your comments.  
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33 Major comments  
34 -----  
35

36 Please, include in Table I some more relevant references as below:  
37  
38

39 Y. Avenas et al., "Condition Monitoring: A Decade of Proposed Techniques," in IEEE Industrial  
40 Electronics Magazine, vol. 9, no. 4, pp. 22-36, Dec. 2015.  
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43 M. Dbeiss et al., "In-situ condition monitoring system to study the ageing of power semi-  
44 conductor devices in photovoltaic inverters," CIPS 2018; 10th International Conference on  
45 Integrated Power Electronics Systems, Stuttgart, Germany, 2018, pp. 1-6.  
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49 Moreover, among temperature monitoring techniques (Refs [15-36]) also include:  
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51

52 H. Luo et al., "Enabling Junction Temperature Estimation via Collector-Side Thermo-Sensitive  
53 Electrical Parameters Through Emitter Stray Inductance in High-Power IGBT Modules," in IEEE  
54 Transactions on Industrial Electronics, vol. 65, no. 6, pp. 4724-4738, June 2018.  
55  
56

57 N. Baker et al., "The Temperature Dependence of the Flatband Voltage in High Power IGBTs,"  
58 in IEEE Transactions on Industrial Electronics.  
59 doi: 10.1109/TIE.2018.2854568  
60



1  
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5 Peak gate current measurements:  
6

7 N. Baker et al., "IR Camera Validation of IGBT Junction Temperature Measurement via Peak  
8 Gate Current," in IEEE Transactions on Power Electronics, vol. 32, no. 4, pp. 3099-3111, April  
9 2017.  
10  
11

12  
13 N. Baker et al., "IGBT Junction Temperature Measurement via Peak Gate Current," in IEEE  
14 Transactions on Power Electronics, vol. 31, no. 5, pp. 3784-3793, May 2016.  
15  
16

17 Delay time on the gate side:  
18  
19

20 H. Luo et al., "Enabling Junction Temperature Estimation via Collector-Side Thermo-Sensitive  
21 Electrical Parameters Through Emitter Stray Inductance in High-Power IGBT Modules," in IEEE  
22 Transactions on Industrial Electronics, vol. 65, no. 6, pp. 4724-4738, June 2018.  
23  
24

25 *We thank the Reviewer for providing the useful references. We have added the references accordingly.*  
26  
27

28  
29 Equation (1) is wrong. The asymptotic value of the first phase of a turn on is  $V_{GG(on)}$ , which  
30 means that  $V_{GE(th)}$  must be replaced with  $V_{GG(on)}$  in that equation.  
31  
32

33 *The equation is to illustrate the waveform of the gate-emitter voltage before the threshold voltage.*  
34 *Therefore,  $V_{GE(th)}$  is used. The  $V_{GG(on)}$  is not used due to the fact that there is Miller plateau after the*  
35 *threshold point which makes the equation not applicable for the behaviour after Miller plateau. We*  
36 *have added this discussion in the revised manuscript.*  
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41 The founding assumption of the present work must be better clarified:  
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43 "In the case of the loss of bond wire connections to an IGBT chip or some number of chips,  
44 the effective inter-chip connection will be altered resulting in a corresponding decline in  
45  $C_{ies}$ , total and a rise in  $R_{G(int),total}$ ." Indeed, the authors refer to complete chip lift off, i.e.  
46 isolation of a whole chip emitter, not to single bond wire lift-off, which cannot be detected  
47 with their method. The authors need to state clearly this intrinsic limitation of their approach.  
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51 *We agree with the Reviewer. The proposed method does have the limitation as it cannot detect single*  
52 *bond wire failure. We have included the limitation in the revised manuscript. We have also shown that*  
53 *in multichip power modules the detection of the first few bond wires lift-off is not practical and is not*  
54 *critical as the module could still operate. For that reason, chip failure is an attractive failure precursor*  
55 *compared to a single bond wire lift-off for power modules with a very large number of chips.*  
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3 The impact of changes in VGG is to be investigated deeper, as it is very crucial to the  
4 measurement success. The sentence "has a negligible impact on  $V_{GE(\text{pre-th})}$  which can be  
5 ignored." is not at all satisfactory, and needs quantitative proof of evidence. Moreover, the  
6 claimed 2% temperature compensation has nothing to do with  $V_{GG(\text{off})}$  stability, which is  
7 indeed the most crucial one. According to my experience, gate drivers, and Concept ones  
8 among them, DO NOT provide any regulation of  $V_{GG(\text{off})}$ .  
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13 We have highlighted the need to examine  $V_{GG}$  in the revised manuscript as the equation shows a direct  
14 relation with  $V_{GG(\text{off})}$ . The gate driver used has an on board regulation for +15V but -10V is not  
15 regulated, when +15Vdc drops down the -10V rail will provide the compensation. We have now  
16 included this discussion in the revised manuscript and supported with a reference of the gate driver  
17 application note.  
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22 We have added experimental results and shown that the proposed method performs well with a  
23 stringent 5 % maximum fluctuation of  $V_{GG(\text{off})}$  and we have recommended that for gate drivers operating  
24 with larger error, a voltage sensor should be added to determine if the same  $V_{GG}$  conditions are met  
25 when measuring  $V_{GE(\text{pre-th})}$ .  
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30 The time scale of Fig. 8 is obviously not realistic and anyhow not the same as the  
31 experimental ones of Fig. 11 and 14. Please, comment.  
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33

34 Fig. 8 was results from simulations and Reviewer 1 also echoed to value of adding simulation work. We  
35 have therefore taken out all of the simulation work in the revised manuscript.  
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39 The adopted PIC has obviously too low clock frequency (which has nothing to do with the  
40 bandwidth concept, by the way). 64MHz yields 15 nanosecond time resolution, which is too  
41 coarse to detect properly the variations shown in Fig. 14.  
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46 We agree with the reviewer. This approach was not relevant. We have now explained how the ADC  
47 was utilised to ensure successful implementation knowing that the  $V_{GE}$  transient is fast. Output  
48 waveforms are presented which show successful measuring of  $V_{GE(\text{pre-th})}$ . We have shown that the  
49 proposed method requires a single sample of  $V_{GE}$ , and tracking of  $V_{GE}$  or collection of multiple samples  
50 is not required.  
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55 The claimed immunity to VGG changes must be proven experimentally.  
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3 We have presented practical results to investigate the impact of  $V_{GG}$  and improved discussion of  $V_{GG}$   
4 impact and results.  
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8 Minor comments  
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13 The abstract section should always start with the sentence "In this paper..." Please, move the  
14 sentences "Multichip high voltage...will incur risks of failures." to the introduction section  
15

16 We thank the Reviewer for the useful suggestions. We have refined the abstract accordingly.  
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18

19 Distinction between 'isolation' and 'insulation' is not common. If the authors want to use  
20 those terms with different meanings, they should better clarify on beforehand what they  
21 exactly mean.  
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23

24 We agree with the Reviewer. Now, we have highlighted the definition of isolation and insulation in the  
25 revised manuscript.  
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28 Please, introduce the concept of 'chip loss' before you use it. You mean a complete failure  
29 (i.e. all bond wires lifted off) of a single chip out of many in parallel. If so, please put a  
30 sentence on it.  
31  
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33 Thank you for the suggestion. We meant the loss of all bond wires in one chip. We agree with the  
34 Reviewer that our wording was not clear. Thus we use now the term chip failure in the revised  
35 manuscript and also explained it more clearly.  
36  
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38 Please, avoid acronyms in the conclusion, like "A new HSP for IGBT chip failure..."  
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41 We thank the Reviewer for reminding us. We now use the full description in the conclusion.  
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44 Please, elaborate or clarify the meaning of the following sentences  
45  
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47 "Despite their shortcomings, the IGBT health monitoring methods described above are not  
48 exhaustive and are not applicable in multichip IGBT power modules."  
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51 We have now updated the comparison of the existing techniques in the introduction.  
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3 Fig.6 is very poor quality.  
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6 Fig 6 is part of simulations which we have taken out as per the previous comment.  
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10 Fig. 14 has no legend.  
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13 We have replaced Fig.14 with the chip failure results, and we have improved the quality of the figure  
14 and included a legend.  
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19 Typos  
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23 In the following list, please turn the first sentences in the second ones:  
24

25 "shows a very low temperature sensitivity but high sensitivity to chip failures"  
26

27 "shows a good temperature immunity and high sensitivity to chip failures"  
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29

30 "is in line with its health conditions which depends"  
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32 is in line with its health conditions which depend"  
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36 "and hence"  
37

38 "hence"  
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41 "is not persistently higher or lower compared"  
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43 "is not significantly higher or lower compared"  
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46

47 "Fig. 16 show that"  
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49 "Fig. 16 shows that"  
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52 We thank the Reviewer for his/her kindness by helping us with typos. We corrected all typos.  
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