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Gate Field Plate Structure for Subthreshold Swing Improvement of Si Line-Tunneling FETs

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ABSTRACT Tunnel field-effect transistors (TFETs) are promising for use in ultralow-power applications owing to their distinct band-to-band tunneling operation. However, the ON-state current of these Si-based tunnel devices is considerably lower than that of MOSFETs. Furthermore, a high-κ dielectric is used as a gate insulator or spacer to increase the TFET's tunneling field strength; this usually causes fringe-induced barrier lowering and deterioration of its subthreshold characteristics. Here, in this paper, a gate field plate TFET (GFP-TFET) structure is proposed to enhance the driving current and suppress the current kink induced by fringe-induced barrier lowering. A detailed investigation into the effects of a gate field plate on TFET performance was conducted with the help of extensive device simulations. The gate oxide and gate field plate oxide could be used to tailor the electric field lines to increase the electric field in the tunnel junction. Meanwhile, the fringing field concentration was reduced by using a metal with a relatively high work function as the field plate electrode. Thus, the electric field strength decreased near the gate edge and increased in the channel. The GFP-TFET exhibited high driving current and low subthreshold characteristics at the cost of a reduction in cutoff frequency. A GFP-TFET structure with optimized parameters had a $10^3\times$ higher ON-state current compared with a normal silicon tunnel FET. The minimum subthreshold swing decreased from 146.3 to 21.4 mV/dec and the ON/OFF current ratio increased from 10^7 to 10^{13} compared with a normal TFET.

INDEX TERMS Band-to-band tunneling (BTBT), fringe-induced barrier lowering (FIBL), subthreshold swing (SS), gate field plate, tunnel field-effect transistor (TFET).

I. INTRODUCTION

IN the past decades, device dimensions in complementary metal-oxide-semiconductor (CMOS) technology have been continuously downscaled in accordance with Moore's Law, finally reaching nanometer sizes in recent years. As device dimensions have decreased, advanced CMOS technology has had to face a substantial challenge, namely to stop the increasingly high leakage currents that degrade the devices' ON/OFF current ratios (I_{ON}/I_{OFF}) [1], [2]. Because metal-oxide-semiconductor field-effect transistors (MOSFETs) operate via thermionic carrier injection, their subthreshold swing (SS) is limited to ~60 mV/dec at room temperature. This physical constraint imposes limits on the applicability of MOSFETs with a low power supply voltage [3], [4].

Owing to its distinct operation mechanism, namely band to band tunneling (BTBT), tunnel field-effect transistors (TFETs) can overcome the SS limitation of MOSFETs and have thus attracted substantial attention for their use in low power applications [5]–[7]. However, Si tunnel FETs always suffer from a low ON-state current, I_{ON}, that is well below the conduction current of CMOS devices [1], [8], [9]. Therefore, a variety of approaches have been proposed to boost the BTBT current, such as using lower band-gap materials at the source [9], [10] or fabricating TFETs with a high-κ gate dielectric [11]–[12], with double-gate [13], [14], with a high-κ spacer [15]–[17], and with a thin epitaxial tunnel layer (ETL) [17]–[20]. Although using a low bandgap material in the tunnel region works to increase the tunnel current, such devices subsequently have a high OFF-sate current, I_{OFF}. High-κ gate dielectrics and high-κ spacers are used to enhance the p-i junction electric field. ETL tunnel FETs display an improved performance owing to their thin tunnel barrier enhancing the additional vertical tunneling component, which is approximately proportional to the gate-to-source overlap length. However, a current kink

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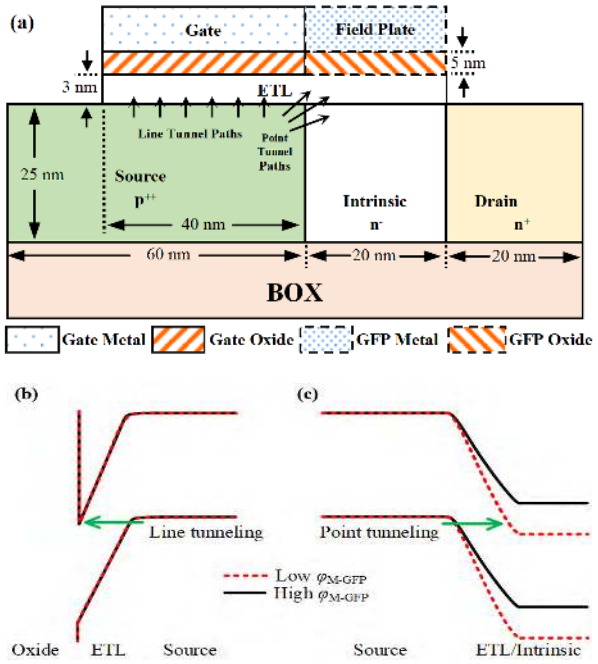

FIGURE 1. (a) A cross-sectional view of the n-channel GFP-TFET, with metal gate, high-k gate dielectric, metal field plate, high-k field plate dielectric, and a thin Si epitaxial channel layer. The energy band diagram of the GFP-TFET for (b) the line tunneling path with the source-to-ETL direction and (c) the point tunneling path with the upper-right corner of source to ETL/intrinsic direction.

phenomenon is observed in their transfer characteristics [17], [18], [21], which deteriorates the average SS of ETL tunnel FETs. Furthermore, the usage of a high-κ gate dielectric or a high-κ spacer causes a fringing field to arise out of the high-κ dielectric; this effect is known as fringe induced barrier lowering (FIBL) [12]. The FIBL effect induced electric field concentration near the gate edge may cause a more warped transfer curve and leads to further unfavorable changes of the average SS and I_{ON} of TFETs.

In this paper, we report an n-channel all-silicon TFET with a gate field plate (GFP) to enhance I_{ON} by using a high-κ dielectric and to improve the average SS by suppressing the FIBL effect induced current kink. A schematic diagram of the GFP-TFET structure is shown in Fig. 1(a). The operation of the GFP-TFET is described below. There are two tunneling paths in the device as depicted in Fig. 1(a). One is the line tunnel path, in which carriers tunnel through from the upper surface of the source to the ETL channel in a direction parallel to the gate field (Fig. 1(b)). The other is the point tunnel path, in which carriers tunnel through from the upper-right corner of the source to the ETL or intrinsic region under the gate field plate (Fig. 1(c)). When the same low work function metal is used for the gate and field plate, the energy band under the GFP shows sharp band bending owing to the high-κ field plate dielectric. As a result, the point tunneling path under the GFP is shorter than the line tunneling path under the gate; this leads to an earlier BTBT turn-on under the GFP. Furthermore, line tunneling starts at a high gate voltage and gradually dominates the device conduction, which leads to a current kink in the transfer curve. Conversely, as the work function φ_M of the GFP metal is increased, the energy band under the GFP bends gently; this at first causes the line tunneling under the gate to dominate device conduction. Therefore, the current kink effect is suppressed and the device performance is improved.

Overall, the GFP-TFET architecture displays a superior drive current and subthreshold swing (SS) compared with a normal TFET with a high-κ spacer. We studied the GFP-TFET's structure parameters, field plate oxide, and field plate electrode as well as their effects on device performance in detail.

II. DEVICE STRUCTURE AND SIMULATION

Fig. 1(a) illustrates the structure of an n-channel all-silicon GFP-TFET. The highly doped p^{++} region, thin ETL region, and highly doped n^+ region act as the source, channel, and drain, respectively. The gate field plate structure (dashed lines) consists of a metal field plate and the field plate oxide. To suppress the ambipolar effect, an asymmetric source/drain structure was employed and an intrinsic region was inserted just under the GFP between the source and drain.

To investigate the effect of the GFP structure on the improvement of the driving current and reduction of the subthreshold swing, a group of TFETs were simulated as control devices with the same parameters as those of the GFP-TFET shown in Fig. 1(a), except that both the metal field plate and its oxide were replaced with a dielectric (TFETs with a spacer).

The device dimensions shown in Fig. 1(a) were used in our simulations unless otherwise stated. A uniform doping profile was used for all the regions (i.e., for the source, channel, and drain) with an abrupt profile at the interfaces between each region as applicable. The doping concentration of the p^{++} (boron) source and n^+ (phosphorus) drain regions were 1×10^{20} and 1×10^{18} cm^{-3}, respectively. The epitaxial layer and the intrinsic region both had a phosphorus doping concentration of 1×10^{15} cm^{-3}, and both of them served as the channel of the devices. The thickness of ETL is tuned to 3 nm, as in [20]. To retain the abrupt doping profile of the source-channel and drain-channel, the thin ETL may be grown on silicon without producing serious defects using low-temperature plasma-deposition [22] or reduced pressure chemical vapor deposition [23]. Hafnium oxide with a physical thickness of 5 nm was used as the gate insulator, and La_2O_3 ($\kappa = 30$) served as the field plate oxide. In addition, the thin gate oxide and GFP oxide can be grown using atomic layer epitaxy [24]. The work function φ_M of the gate metal and GFP metal were 3.5 and 4.2 eV, respectively. The threshold voltage, V_T, and the off voltage, V_{OFF}, were extracted using the constant current definition, and were found to be 10^{-7} and 10^{-13} A/μm, respectively. The ON-state current, I_{ON}, and OFF-state current, I_{OFF}, were extracted at $V_{GS} = V_{OFF} + 1$ V, $V_{DS} = 1$ V and $V_{GS} = 0$ V, $V_{DS} = 1$ V, respectively. The average SS is the slope of the transfer curve within the voltage region of 10^{-13}–10^{-7} A/μm.

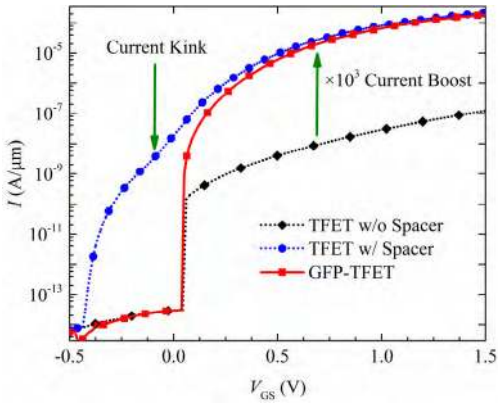

FIGURE 2. Comparison of the transfer characteristics of the GFP-TFET, the TFET with a high-κ spacer, and the normal TFET (without spacer).

The Sentaurus-TCAD tool was used [25] to simulate the performance of the GFP-TFETs. The dynamic nonlocal BTBT model was activated throughout the semiconductor region, including the source, intrinsic, drain, and ETL regions, to precisely compute the tunneling current, which depends on the complicated band edge profile shape along the entire path between the points connected by tunneling. Nonlocal meshes were defined at the interface between the source and ETL/intrinsic region to ensure the accuracy of the calculation. Furthermore, the Slotboom model was used to predict the effect of heavy doping on bandgap narrowing in the source region. The thin-layer mobility model and high field mobility saturation model were employed in the ETL region to precisely estimate the carrier transport properties in an ultra-thin layer. In addition, the Shockley-Read-Hall recombination model and Fermi statistics were taken into consideration to simulate the device characteristics, which is important for high value of carrier densities and bandgap narrowing estimate. Non-ideal effects such as defect-assisted tunneling and the gate leakage current were ignored. It should also be noted that the focus of this work was not to determine exact current values, but to understand more about general trends in this system and to study the relative results caused by varying the devices' parameters.

III. RESULTS AND DISCUSSION

A. TRANSFER CHARACTERISTICS AND CURRENT KINK

We first studied the device performance to determine the various effects of the GFP and the high-κ spacer on the performance of n-type all-silicon tunnel transistors with an epitaxial tunnel layer. Fig. 2 shows the simulated transfer characteristics for the proposed GFP-TFET, the TFET with a high-κ spacer, and the normal TFET (without a spacer). HfO_2 ($\kappa = 22$) was used as the gate insulator for all three device types, and a dielectric with $\kappa = 50$ (representative of the properties of Ta_2O_5) served as the GFP dielectric and the spacer for the GFP-TFET and the TFET with a spacer. A κ value of 50 was used for the convenience of demonstrating the point tunneling and current kink. The work function φ_M of the gate metal was set to 3.5 eV for all devices, and the φ_M of the

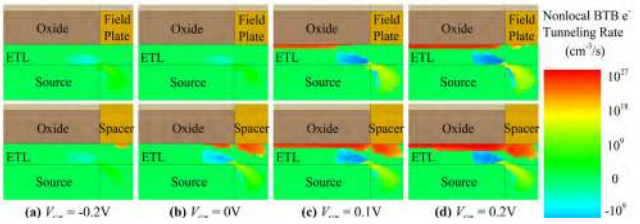

FIGURE 3. Distribution of the BTBT rate of the GFP-TFET (top pictures) and TFET with spacer (bottom pictures) biased at $V_{DS} = 1$ V and for $V_{GS} = -0.2$, 0, 0.1, and 0.2 V.

GFP metal was 4.2 eV. In Fig. 2, the leakage currents of the GFP-TFET and normal TFET were independent of the gate control, as expected; this is a result of the asymmetric structure with its different doping concentrations for the source and drain. In the on-state, the current I_{ON} of the GFP-TFET and the TFET with a spacer were 10^3 times larger than that of the normal TFET without a spacer, which is a result of the high-κ dielectric induced electric field enhancement. Unfortunately, the onset of tunneling in the TFET with a spacer started at a much lower gate voltage than for the other two devices, and the BTBT current of the TFET with a spacer increased slowly as V_{GS} increased. Furthermore, a current kink occurred at $V_{GS} \approx 0$ V for the TFET with a spacer, which further deteriorated the average SS of the device. It is evident from Fig. 2 that the average SS of the GFP-TFET was improved tremendously compared with the other two devices.

To gain detailed insight into the above observations, the simulated BTBT rates of two different devices, namely the GFP-TFET and TFET with a high-κ spacer, are shown in Fig. 3 at $V_{DS} = 1$ V for $V_{GS} = -0.2$, 0, 0.1, and 0.2 V. It can be seen in Fig. 3 that the onset point of BTBT tunneling in the GFP-TFET is located at the source–channel junction beneath the gate stack, while the BTBT tunneling in the TFET with a spacer takes place under the spacer. In other words, the GFP-TFET turns on with line tunneling and the TFET with a spacer turns on with point tunneling, as shown in Fig. 1 (b) and (c). Although the onset of BTBT tunneling in the TFET with a spacer begins with point tunneling at a low gate voltage, line tunneling occurs in the ETL as the gate voltage increases and quickly dominates the current of the device; this is the reason for the kink in the current curve. To uncover the reason behind the different BTBT tunneling onset points for the GFP-TFET and the TFET with a high-κ spacer (shown in Fig. 3), we investigated the electronic fields in the two different tunneling paths of these two device types and compared them with those of a normal TFET without a spacer.

Short-channel effects, especially the FIBL effect, which causes a lowering of V_T and a deterioration of SS, together with high-κ gate dielectrics have already been studied [8], [12], [17]. In line tunneling-based TFETs with a thin ETL channel, a high-κ gate insulator or spacer usually causes the electric field to concentrate near the gate edge owing to the discontinuity equations for the electric field [8], [17]. The contour plot of the electric field in the GFP-TFET and

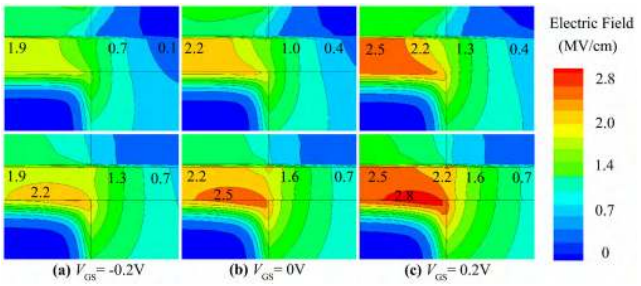

FIGURE 4. Contour lines of the electric field for the GFP-TFET (top pictures) and TFET with spacer (bottom pictures) biased at $V_{DS} = 1$ V and for $V_{GS} = -0.2$, 0, and 0.2 V.

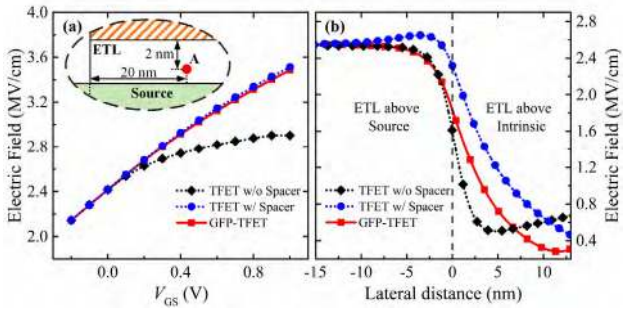

FIGURE 5. Distribution of electric field for GFP-TFET, TFET with spacer, and normal TFET without spacer (a) at the horizontal and vertical center point of the ETL under the gate (shown as "A" in the inset diagram) and (b) along the horizontal direction 1.0 nm above the source–channel interface.

TFET with a spacer shown in Fig. 4 demonstrates that the electric field near the right gate edge is larger for the TFET with a spacer compared with for the GFP-TFET. As a result, the device SS performance is deteriorated.

To suppress the FIBL effect, we propose a GFP on top of the intrinsic region, as shown in Fig. 1, with the aim of suppressing the electric field near the gate edge. To validate the effectiveness of the GFP, we plotted the electric fields of the line tunneling point at the ETL center for the three device types—GFP-TFET, TFET with a high-κ spacer, and TFET without a spacer; the plots are shown in Fig. 5(a) for gate bias voltages form −0.2–1 V. The electric fields along the horizontal direction were extracted 1.0 nm above the source–channel interface (shown in Fig. 5(b)). The three devices in Fig. 5(b) were biased at $V_{GS} = 0.2$ V to ensure they were all in the ON-state. It is clear from Fig. 5(a) that the electric field strengths in the ETL are the same for all three device types at gate voltages below 0.1 V; this is a result of using the same gate insulator and a low gate voltage. As the gate voltage increased, the electric fields in the ETL channel of the GFP-TFET and the TFET with a spacer increased more quickly than for the normal TFET owing to the high-κ field plate insulator and spacer near the gate edge. The difference in the electric field in the ETL at a high gate voltage between a normal TFET and the other two devices corresponds to the current gap shown in Fig. 2. It can be seen in Fig. 5 (b) that the GFP-TFET with a high field plate work function has

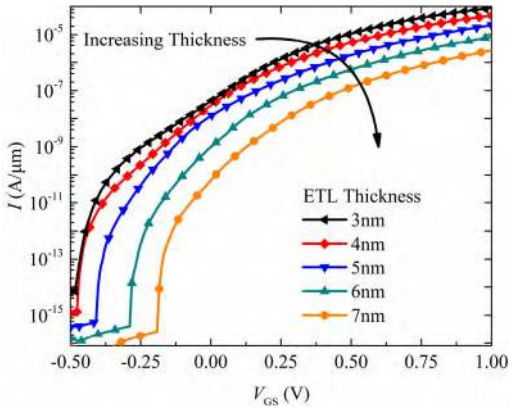

FIGURE 6. Transfer characteristics of the GFP-TFET for different ETL thicknesses. HfO_2 ($\kappa = 22$) and Ta_2O_5 ($\kappa = 50$) are used as the gate oxide and field plate oxide, respectively. The φ_M of the gate and field plate were both 3.5 eV.

an electric field as low as the normal TFET and that it is insufficient for point tunneling at the upper right-hand corner of the source. Therefore, the FIBL effect in the TFET with a spacer that is induced by the high-κ dielectric near the gate edge is suppressed in the GFP-TFET.

B. EFFECT OF THE ETL THICKNESS

Fig. 6 shows the transfer characteristics of the GFP-TFET biased at $V_{DS} = 1$ V for an increase in the ETL thickness from 3 to 7 nm in steps of 1 nm. The κ-values of the gate insulator and field plate dielectric were 22 and 50, respectively. The results in Fig. 6 indicate that the thickness of the ETL has a significant influence on current behavior and device performance. A thicker ETL degrades the driving current at high gate voltages and delays the onset of BTBT tunneling owing to the reduced electric field strength. The thicker the ETL is, the weaker the electric field in the tunneling path becomes. Consequently, the tunneling efficiency is reduced. In addition, it is worth noting that a kink in the current curve is still observed when the ETL thickness is below 4 nm, which indicates that the ETL thickness plays an important role in the current kink effect. This can be explained by the above mentioned existence of the two onset points of BTBT, namely the onset point caused by the point tunneling determined by the FIBL effect near the gate edge and the onset point caused by the line tunneling, where the tunnel distance is limited by the thickness of the ultrathin ETL. Fig. 7 shows the simulated energy band diagram in the ETL channel and near the gate edge of the GFP-TFET biased at a fixed gate voltage and drain voltage for different ETL thicknesses. It can be observed in Fig. 7 (a) that although a thinner ETL results in steeper energy band bending within the ETL, it is harder to align the conduction band with the valence band than when a thicker ETL is used. With a very thin ETL channel a higher gate voltage is therefore required to pull the conduction band down enough to align the valence band. As shown in Fig. 7 (b), the point tunneling at the upper right-hand corner of the source does not suffer from this limitation of the tunneling

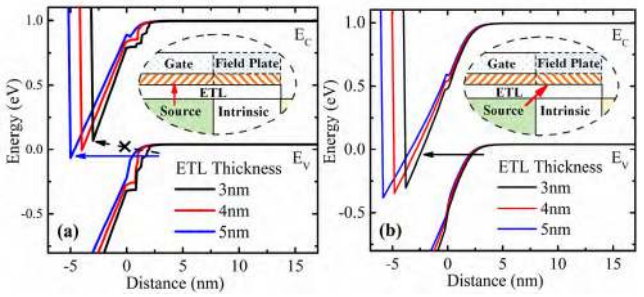

FIGURE 7. Simulated energy band diagram of the GFP-TFET along (a) the line tunneling path and (b) the point tunneling path for different ETL thickness. The device was biased at $V_{GS} = 0$ V, $V_{DS} = 1$ V. The κ of the gate oxide and field plate oxide and the φ_M of the gate and field plate are same as for Fig. 6. The red arrows in the insets schematically show the different tunneling paths.

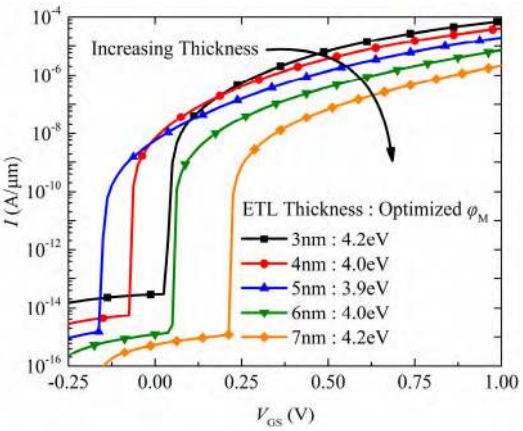

FIGURE 8. Transfer characteristics of the GFP-TFET for different ETL thicknesses. HfO_2 ($\kappa = 22$) and Ta_2O_5 ($\kappa = 50$) were used as the gate oxide and field plate oxide, respectively. The φ_M of the gate metal was 3.5 eV, while the φ_M of the field plate metal was optimized for each ETL thickness.

path distance, even in the case of a thin ETL. However, the electric field in this area is strengthened and higher than that in the ETL channel owing to the high-κ dielectric adjacent to the gate stack, as previously discussed. Therefore, the device begins its turn-on with point tunneling and shows a current kink in its transfer curve when an ultra-thin ETL is used.

To validate the effectiveness of suppressing this current kink caused by the FIBL induced field concentration near the right gate edge, the transfer characteristics of the GFP-TFET with an optimized field plate work function for each ETL thickness were simulated and are shown in Fig. 8. It is evident from Fig. 8 that the current kink effect is suppressed for all ETL thicknesses and that the current curves become steeper than in the case shown in Fig. 6, where the field plate work function was fixed to be the same as the gate work function. As mentioned above, the onset of BTBT in the ETL is postponed for TFETs with a thinner ETL thickness. However, a device with a much thicker ETL would result in a weaker electric field and degrade the ON-state current. Therefore, the ETL thickness must be optimized to achieve the best device performance. Based on the definition of the average SS, the optimized ETL thickness in this work was about 3 nm.

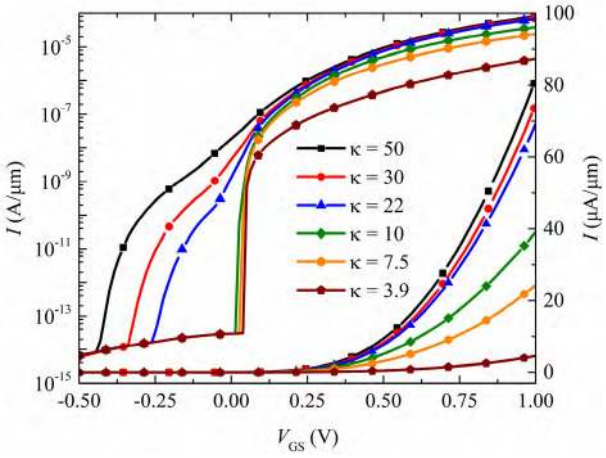

FIGURE 9. Impact of the variation of the spacer dielectric constant on the transfer characteristics of the TFET with a spacer.

C. EFFECT OF THE DIELECTRIC CONSTANT

As discussed previously, a high-κ dielectric used as a GFP oxide or spacer is beneficial to enhance the electric field in the channel but is also likely to induce the FIBL effect, which deteriorates the sub-threshold characteristics of TFETs. To resolve this conflict, we propose a scheme based on a GFP-TFET that uses a high-κ dielectric as its field plate oxide and a metal field plate with an optimized work function to reduce the fringing field. For the purpose of investigating the effects of variations in the κ-value of the dielectric near the gate stack on the device performances, we set the κ-values of the field plate oxide of the GFP-TFET and of the TFET spacer to 3.9, 7.5, 10, 22, 30, and 50; these values correspond to the κ-values of SiO_2, Si_3N_4, Al_2O_3, HfO_2, La_2O_3, and Ta_2O_5, respectively. All other parameters were kept the same as those in the previous case. Fig. 9 shows the transfer characteristics of the TFET with a spacer for different spacer dielectrics. It is clear from Fig. 8 that the sub-threshold characteristics strongly depend upon the spacer's dielectric constant, κ, for the TFET with a spacer; an increase in the κ-value resulted in a corresponding lowering of V_T and V_{OFF} and a degradation of SS, especially for high κ-values. Although the ON-state current I_{ON} of the TFET with a spacer was enhanced substantially with a high-κ spacer, its average subthreshold swing SS was severely deteriorated owing to the onset of the BTBT switching from point tunneling to line tunneling.

As a contrast, the transfer characteristics of GFP-TFETs with different field plate dielectrics are shown in Fig. 10. The change in the κ-value was similar to the previous case of the TFET with a spacer, and the work function of the field plate metal was 4.2 eV. From Fig. 10 it can be seen that the driving current of the GFP-TFET at high gate voltages was increased several tens of times as the dielectric constant of field plate oxide was varied from 3.9 to 50. At the same time, the onset of the BTBT at low gate voltages remained unchanged. The advantage of using a high-κ dielectric (namely, to increase I_{ON}) is retained, while its disadvantage (namely,

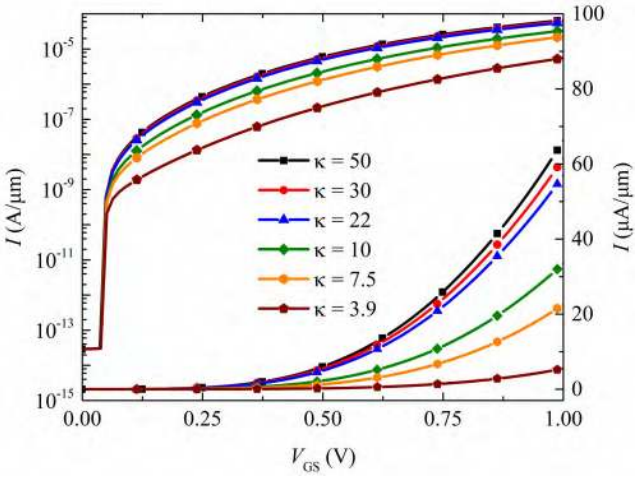

FIGURE 10. Impact of the variation of the dielectric constant on the transfer characteristics of the GFP-TFET.

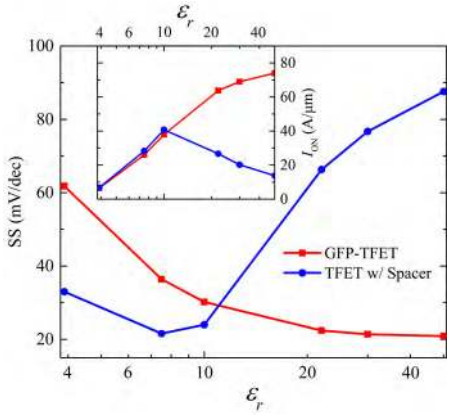

FIGURE 11. Impact of the variation of the dielectric constant on the average SS and I_{ON} for the GFP-TFET and the TFET with a spacer extracted from the curves in Figs. 8 and 9.

inducing FIBL) is suppressed. To gain detailed insight into the above observations, the I_{ON} and average SS extracted from the curves in Figs. 9 and 10 according to the definitions in section II are shown in Fig. 11 for the GFP-TFET and the TFET with a spacer. As the κ-value increases, the average SS of the GFP-TFTE quickly decreases from 60 to 20 mV/dec and the I_{ON} of the GFP-TFTE increases continuously. Conversely, the average SS and the I_{ON} based on the previous definition of the TFET with a spacer increases and reduces, respectively, as the κ-value is increased owing to the FIBL-induced current kink. The results indicate that the average SS characteristics of the GFP-TFET can be tremendously improved by optimizing the field plate work function.

D. EFFECT OF THE WORK FUNCTION

Gate work function engineering is usually used to shift the curves to achieve a small threshold voltage, which is required for low V_{DD} applications [8], [9], [26]. In these cases, the use of a low work function material as the gate electrode of an n-type TFET results in a low V_{OFF}. For GFP-TFETs,

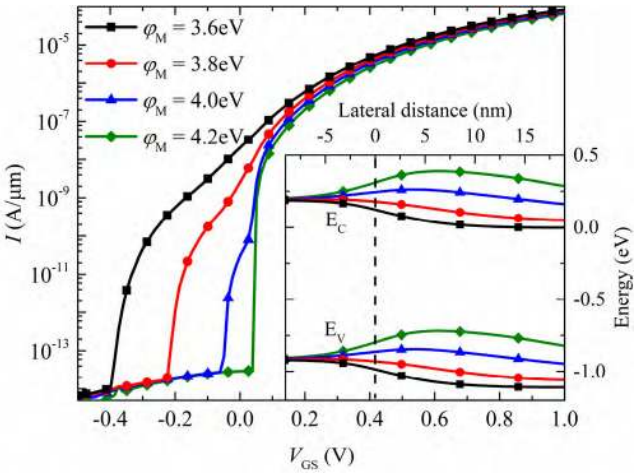

FIGURE 12. Transfer characteristics of the GFP-TFET for different field plate work functions. HfO_2 ($\kappa = 22$) and Ta_2O_5 ($\kappa = 50$) are used as the gate oxide and field plate oxide, respectively. The φ_M of the gate metal was 3.5 eV. The inset shows the energy band diagram in the ETL.

meanwhile, work function engineering is not only used to achieve a reasonable line tunneling onset voltage, but also to suppress point tunneling related to the ETL thickness and high-κ dielectric. To demonstrate the effect of the work function on TFET performance, we conducted a device simulation for a GFP-TFET with different GFP metal work functions. The work function φ_M of the gate metal was 3.5 eV, and the φ_M of the GFP metal was increased from 3.6 to 4.2 eV in steps of 0.2 eV. Fig. 12 shows the transfer characteristics of the GFP-TFET for the various GFP metal work functions. It can be clearly observed in Fig. 12 that when the field plate φ_M was increased, the device's V_{OFF} changed significantly from a large negative value to just above zero and that the current kink gradually weakened. The GFP-TFET with a field plate with a φ_M of 4.2 eV showed the best performance; its V_{OFF} was 0.1 V, and its driving current reached 69 μA/μm.

In addition, the changes in the transfer curves in Fig. 12 demonstrate the effectiveness of using a high field plate work function for suppressing the point tunneling related current kink and improving the SS performance of a TFET with a thin ETL channel and high-κ dielectric. To explain how changing the GFP work function effects the point tunneling suppression, the inset in Fig. 12 shows the energy band diagram in the ETL of the GFP-TFET along the horizontal direction 0.5 nm below the oxide interface for different field plate work functions. As the GFP's φ_M increases, the energy band near the gate edge and under the field plate bends down less, eventually even bending upward a little. As a result, point tunneling within this region is restricted as it requires the energy bands to bend steeply downward.

Whereas the point tunneling was suppressed with a large GFP metal work function, the energy band near the drain–intrinsic interface was raised, which leads to easier ambipolar transport. Hence, the width of GFP was limited to overcome the problem of ambipolar behavior. Fig. 13 shows a comparison of the ambipolarity of the GFP-TFET and the

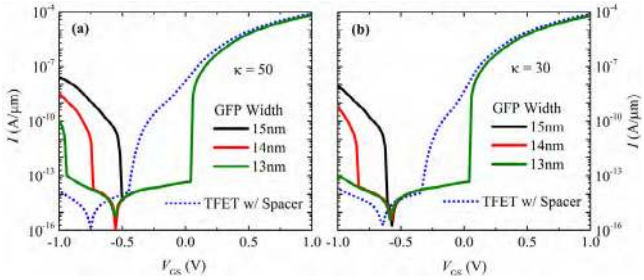

FIGURE 13. Transfer characteristics of the GFP-TFET and TFET with a spacer for different κ-values of the field plate oxide of the GFP-TFET and of the TFET spacer. (a) $\kappa = 50$ (Ta_2O_5); (b) $\kappa = 30$ (La_2O_3). The κ of the gate oxide was 22, the φ_M of gate metal was 3.5 eV, and the φ_M of the GFP metal was 4.2 eV.

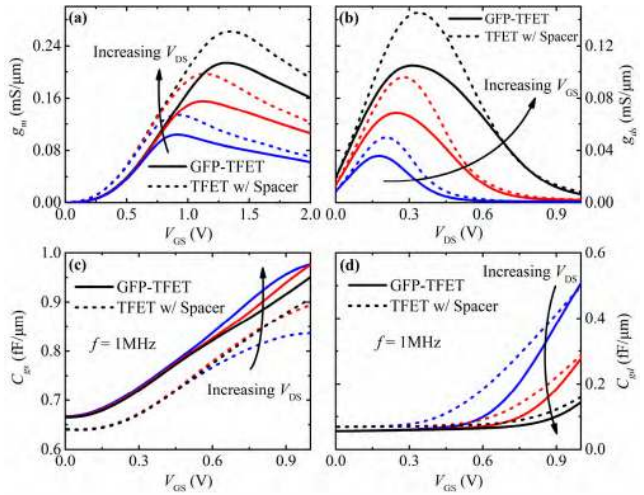

FIGURE 14. Variation of g_m, g_{ds}, C_{gs}, and C_{gd} of the GFP-TFET and the TFET with a spacer with respect to V_{GS} for different V_{DS}. HfO_2 ($\kappa = 22$) was used as the gate oxide, while La_2O_3 ($\kappa = 30$) was used as both the field plate oxide and spacer. The φ_M of the gate and field plate were 3.5 eV and 4.2 eV, respectively.

TFET with a spacer. The width of the GFP decreased from 15 to 13 nm in steps of 1 nm for the GFP-TFET, while the width of the spacer was 20 nm for the TFET with a spacer. It can be clearly seen that the GFP-TFET has stronger ambipolar behavior than the TFET with a spacer owing to the effect of the large φ_M of the GFP metal on the energy band near the drain–intrinsic interface. As the width of the GFP decreases, the ambipolar current of the GFP-TFET declines. For a GFP width of 13 nm, the ambipolar transport was suppressed for the GFP-TFET in which La_2O_3 ($\kappa = 30$) was used as the GFP oxide. Meanwhile, the driving current of the GFP-TFET in forward-bias remained the same as that of the TFET with a spacer.

E. ANALOG/RADIO FREQUENCY (RF) PERFORMANCE

In this section, the analogue/RF performance of the GFP TFET was analyzed in terms of its transconductance (g_m), output conductance (g_{ds}), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and cut-off frequency (f_T). Fig. 14(a) and (b) shows the variation of g_m and g_{ds} for the two device types with respect to V_{GS} and V_{DS}. In Fig. 14(a)

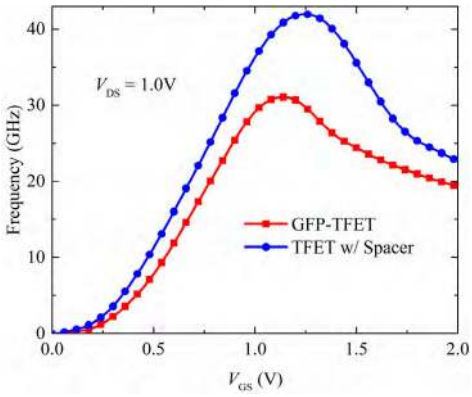

FIGURE 15. Cut-off frequency (f_T) of the GFP-TFET and the TFET with a spacer. HfO_2 ($\kappa = 22$) was used as the gate oxide, while La_2O_3 ($\kappa = 30$) was used as the field plate oxide of the GFP-TFET and of the TFET spacer. The φ_M of the gate and field plate were 3.5 eV and 4.2 eV, respectively.

it can be seen that g_m initially increases with V_{GS} owing to the increment of the BTBT rate; however, a degradation in g_m starts occurring for higher values of V_{GS} owing to a reduction in mobility. Further, the g_m of the TFET with a spacer is larger than that of the GFP-TFET because of its higher driving current, as shown in Fig. 2. The g_{ds} results in Fig. 14(b) indicate that the drain currents of the two device types show a strong dependence on V_{DS}, which is a result of the ETL-based vertical tunneling shown in Fig. 1(a). The g_{ds} of the TFET with a spacer is larger than that of the GFP-TFET because of the contribution of point tunneling to the drain current of the TFET with a spacer. Fig. 14(c) and (d) show C_{gs} and C_{gd} for the two device types with respect to V_{GS}. The values for C_{gs} and C_{gd} were extracted from a small signal ac analysis at a frequency of 1 MHz. From Fig. 14(c) and (d), it can be concluded that the C_{gs} of the two device types have values comparable to their C_{gd} owing to gate-source overlap. C_{gs} increases with V_{GS} because of the variation in the charge in the ETL channel as the device turns on, while C_{gd} increases with V_{GS} when the devices enters saturation region, which is caused by the pinch-off effect increasing the coupling between the gate-to-drain terminal [27].

Fig. 15 shows a comparison of cut-off frequency (f_T) as a function of V_{GS} for the GFP-TFET and the TFET with a spacer. It is evident that f_T starts increasing with V_{GS} until it reaches its maximum value, then falls as the gate bias is increased further. The initial enhancement of f_T is caused by the increase of g_m, and the later decline of f_T is the result of the decrease of g_m combined with increases of C_{gs} and C_{gd}. Because of the low g_m value, the f_T of the GFP-TFET is smaller than that of the TFET with a spacer, which limits the applicability of GFP-TFETs for high-frequency applications.

F. SUMMARY

In summary, suggestions for the device parameters are provided based on the simulations' results. To achieve a high I_{ON}, 3 nm is the most appropriate ETL thickness. The field plate dielectric constant κ should be 30 to increase the electric field

TABLE 1. Performance comparison of different TFETs.

Reference	Materials and structures	I_{OFF} (μA)	SS (mV/dec)	I_{ON} (μA)	I_{ON}/I_{OFF}	Year
Woo Young Choi [4]	SOI based Si TFET	10^{-4}	52.8	12.1	10^{5}	2007
Zhaonian Yang [28]	L-shaped gate, N^+ source pocket	10^{-11}	120.83	1.1	10^{11}	2016
Mallikarjunam Rao [29]	Symmetric High-k Spacer, Trigate	10^{-15}	147.4	0.025	10^{13}	2016
Navjeet Bagga [30]	Two source region, SOI	10^{-10}	44.9	10.1	10^{11}	2017
N. Sharma [31]	Double gate, Ge source	10^{-10}	46.6	108.6	10^{12}	2017
Peng Xu [32]	PNPN tunnel, L-shaped gate, N^+Pocket	10^{-7}	57.2	192.7	10^{9}	2017
This work	Gate field plate	10^{-11}	21.4	69	10^{13}	2018

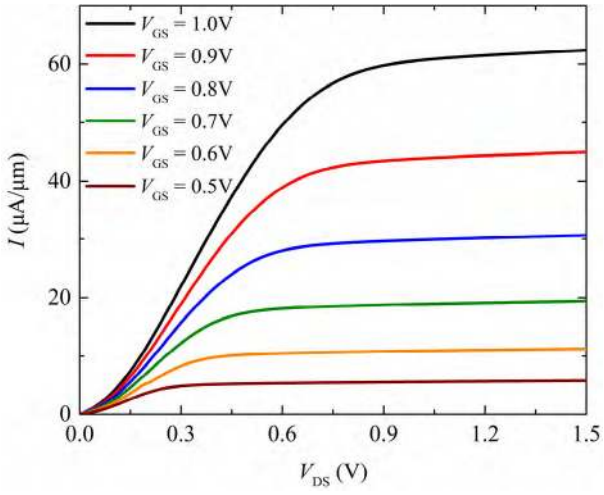

FIGURE 16. Output characteristics of the GFP-TFET. HfO_2 ($\kappa = 22$) and La_2O_3 ($\kappa = 30$) were used as the gate oxide and field plate oxide, respectively. The φ_M of the gate and field plate were 3.5 eV and 4.2 eV, respectively.

in the channel, while the work function of the GFP electrode metal should be 4.2 eV to suppress the FIBL effect and avoid the current kink effect. The field plate width should be 7 nm less than that of the intrinsic region to suppress any ambipolar effects. Although the ability of the gate to control the current is enhanced with a higher κ dielectric, the subthreshold characteristics would degenerate owing to the FIBL effect. In addition, considering the maturity of the process, 5-nm-thick HfO_2 was used as the gate oxide. Fig. 16 shows the output characteristics of the GFP-TFET with the gate voltage increased from 0.5 to 1 V in steps of 0.1 V. It is evident from Fig. 16 that the drain current of the GFP-FET reaches good saturation at high drain voltages as the energy of the channel conduction band becomes independent of the drain bias.

Table I shows the performance enhancement of the GFP-TFET along with the data of TFETs with different structures published in recent years. For convenient comparison, the SS and I_{ON} values listed in the table were recalculated from the corresponding transfer curves using the method previously mentioned in this work. The subthreshold swing of the GFP-TFET in this paper was much smaller than that of other Si TFET devices owing to the suppression of point tunneling. In addition, as a result of the electric field enhancement in the ultra-thin ETL channel, the GFP-TFET shows a strong driving capability comparable to that of a MOSFET and an ON/OFF current ratio as high as 10^{13}.

IV. CONCLUSION

We proposed and discussed in detail a way to improve ON-state current and SS behavior via suppression of the FIBL effect related point tunneling using a gate field plate structure. We demonstrated that using a high-κ dielectric as the drain-side gate field plate oxide and a large work function metal as the field plate electrode results in a suppression of FIBL and an increase in the ON-state BTBT in the channel. As a result, the best performance—in terms of having a steep SS and large driving current—for a device of this kind was obtained. The simulation results demonstrate that the drain current of the GFP-TFET was increased by more than three orders of magnitude compared with a normal line tunneling TFET without a gate field plate. Therefore, a GFP-TFET with a well-chosen dielectric for the field plate oxide and an electrode with an appropriate work function is a promising and practical device to facilitate the development of ultralow-power applications.

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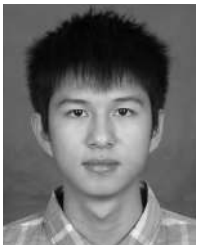

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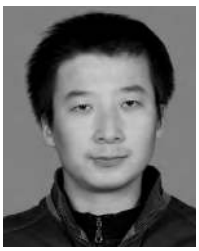

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