



MIT Open Access Articles

Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications

The MIT Faculty has made this article openly available. **Please share** how this access benefits you. Your story matters.

Citation	Saadat, O.I. et al. "Gate-First AlGaN/GaN HEMT Technology for High-Frequency Applications." <i>Electron Device Letters, IEEE</i> 30.12 (2009): 1254-1256. ©2009 Institute of Electrical and Electronics Engineers.
As Published	http://dx.doi.org/10.1109/led.2009.2032938
Publisher	Institute of Electrical and Electronics Engineers
Version	Final published version
Citable link	http://hdl.handle.net/1721.1/55367
Terms of Use	Article is made available in accordance with the publisher's policy and may be subject to US copyright law. Please refer to the publisher's site for terms of use.

Gate-First AlGaIn/GaN HEMT Technology for High-Frequency Applications

Omar I. Saadat, *Student Member, IEEE*, Jinwook W. Chung, Edwin L. Piner, *Member, IEEE*, and Tomás Palacios, *Member, IEEE*

Abstract—This letter describes a gate-first AlGaIn/GaN high-electron mobility transistor (HEMT) with a W/high- k dielectric gate stack. In this new fabrication technology, the gate stack is deposited before the ohmic contacts, and it is optimized to stand the 870 °C ohmic contact annealing. The deposition of the W/high- k dielectric protects the intrinsic transistor early in the fabrication process. Three different gate stacks were studied: W/HfO₂, W/Al₂O₃, and W/HfO₂/Ga₂O₃. DC characterization showed transconductances of up to 215 mS/mm, maximum drain current densities of up to 960 mA/mm, and more than five orders of magnitude lower gate leakage current than in the conventional gate-last Ni/Au/Ni gate HEMTs. Capacitance–voltage measurements and pulsed- I - V characterization show no hysteresis for the W/HfO₂/Ga₂O₃ capacitors and low interface traps. These W/high- k dielectric gates are an enabling technology for self-aligned AlGaIn/GaN HEMTs, where the gate contact acts as a hard mask to the ohmic deposition.

Index Terms—GaN, high- k dielectric, high-electron mobility transistor (HEMT), self-aligned.

I. INTRODUCTION

ATTRACTING great interest for high-frequency and high-power amplifiers are AlGaIn/GaN high-electron mobility transistors (HEMTs). During the last few years, the frequency performance of GaN HEMTs has increased steadily. Recently, Higashiwaki *et al.* reported an f_T of 181 GHz in unpassivated devices with $L_g = 30$ nm and thin AlGaIn barrier [1]. Palacios *et al.* demonstrated an f_T of 153 GHz and an f_{max} of 230 GHz in HEMTs with $L_g = 100$ nm and an InGaIn back barrier [2].

To further improve the frequency performance of AlGaIn/GaN HEMTs, it is necessary to reduce the source and drain access resistances in addition to reducing the gate length [3], [4]. In 2007, Endoh *et al.* demonstrated a maximum f_T of 194 GHz in an $L_g = 45$ nm HEMT by cooling down the devices to 16 K [5], which significantly increased the electron mobility and reduced the access resistances [4].

Conventional fabrication techniques involve patterning and annealing the source and drain contacts before lithographically

aligning the Schottky gate contact. This approach limits the minimum source-to-gate distance to around 500 nm, which makes very difficult to get source access resistances below $0.4 \Omega \cdot \text{mm}$. To reduce the source and drain access resistance further, it is necessary to self-align the ohmic source and drain to the gate electrode. There are different approaches for fabricating self-aligned devices, like using n^+ cap layers [6], regrowing the ohmic contacts [7], and using the T-shaped gate as a hard mask for the ohmic evaporation [8]. In the latter approach, a gate stack that can stand the ohmic anneal temperatures (> 800 °C) is necessary for fabricating self-aligned HEMTs with minimum contact resistance. However, the traditional gate metallization formed by Ni/Au or Ti/Pt/Au does not survive these ohmic anneal temperatures.

In this letter, we report AlGaIn/GaN HEMTs fabricated by using a gate-first process, where a tungsten/high- k dielectric gate is deposited before the ohmic contacts and then survives the 870 °C anneal necessary to form ohmic contacts. Devices were fabricated with Al₂O₃ and HfO₂ gate dielectrics of different thicknesses, along with a combination of a Ga₂O₃/HfO₂ dielectric stack. These gate-first HEMTs are not only very useful for future self-aligned transistor structures but they also exhibit superior drain current density and transconductance compared to a reference HEMT with a standard Ni/Au/Ni gate stack.

II. DEVICE FABRICATION

The AlGaIn/GaN transistor structure used in this letter was grown in Si (111) substrates by metal–organic chemical vapor deposition by Nitronex Corporation. The Al_{0.26}Ga_{0.74}N barrier had a thickness of 17 nm, and it is capped by a 2-nm unintentionally doped GaN layer. Further details about the growth technology can be found in [9].

AlGaIn/GaN transistors and metal–insulator–semiconductor (MIS) capacitors were fabricated on these wafers. First, mesa isolation was performed by electron cyclotron resonance etching with a 100-W BCl₃/Cl₂ plasma. Then, the high- k dielectrics were deposited on the entire sample. Al₂O₃ and HfO₂ films were deposited by a Cambridge Nanotech Savannah atomic layer deposition reactor, and Ga₂O₃ was grown by oxidizing the GaN cap layer with an O₂ plasma, as described in [10]. A summary of the different dielectrics used in this letter is shown in Table I.

After depositing the gate dielectric, a 60-nm-thick tungsten gate with $L_g = 3 \mu\text{m}$ was deposited by e-beam evaporation and patterned by a liftoff process. After the ohmic contact lithography, the dielectric was removed from the contact regions

Manuscript received September 11, 2009. First published November 3, 2009; current version published November 20, 2009. This work was supported in part by the Office of Naval Research MINE MURI Program (monitored by H. Dietrich and P. Maki) and in part by M/A-COM Corporation. The review of this letter was arranged by Editor G. Meneghesso.

O. I. Saadat, J. W. Chung, and T. Palacios are with the Microsystems Technology Laboratory, Massachusetts Institute of Technology, Cambridge, MA 02139 USA (e-mail: tpalacios@mit.edu).

E. L. Piner is with Nitronex Corporation, Durham, NC 27703 USA.

Color versions of one or more of the figures in this letter are available online at <http://ieeexplore.ieee.org>.

Digital Object Identifier 10.1109/LED.2009.2032938

TABLE I
SUMMARY OF GATE DIELECTRICS AND FABRICATED DEVICES

Al ₂ O ₃	HfO ₂	Ga ₂ O ₃ + HfO ₂
15 nm	15 nm	3 nm + 12 nm
20 nm	20 nm	
25 nm	25 nm	

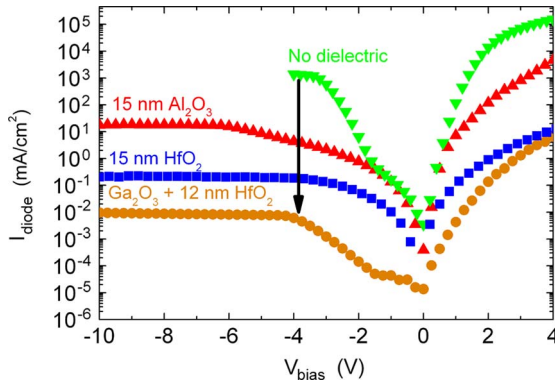


Fig. 1. Current–voltage characteristics for diode structures. The use of high-*k* dielectrics reduces the leakage current by a factor of up to 100 000.

by a buffered oxide etch (HF). Then, Ti–Al–Ni–Au source and drain contacts, with a source–drain separation of 6 μm , were deposited by e-beam evaporation. After the ohmic metal deposition and liftoff, the contacts (including the gate metal) were annealed at 870 °C for 30 s in a N₂ environment.

III. RESULTS AND DISCUSSION

The as-grown AlGaN/GaN wafers show a sheet charge density of $1.5 \times 10^{13} \text{ cm}^{-2}$ and a sheet resistance of 380 Ω/\square . The deposition of the high-*k* dielectrics on the wafer surface increased the charge density by 20% and decreased the sheet resistance by 15%, as measured by the Hall and transmission line measurements. It has been proposed that dielectric layers increase the mobile charge density by reducing the fixed polarization charge [11].

Circular MIS capacitors with a diameter of 180 μm were fabricated on these samples. Fig. 1 shows the leakage current–voltage (*I*–*V*) characteristics of devices with different gate dielectric materials. All the MIS devices studied in this letter showed an important reduction of the reverse and forward leakage currents by up to 100 000 times with respect to the standard Schottky contacts, even though the MIS devices underwent the 870 °C ohmic annealing. Capacitance measurements showed that the dielectric constants for Al₂O₃ and HfO₂ were 10.8 and 18.1, respectively.

Capacitance–voltage hysteresis was measured in these capacitors by sweeping from –10 to 0 V and back to –10 V. The amount of hysteresis is an indicator of slow traps in the oxide and in the interface between the oxide and the semiconductor [12]. The use of a thin Ga₂O₃ layer between the HfO₂ and the GaN epilayer significantly improves the quality of the interface and reduces hysteresis, as shown in Fig. 2. In addition, the conductance method was used to measure the density of interface traps in the different dielectrics between the oxide and semiconductor by sweeping the small signal frequency from

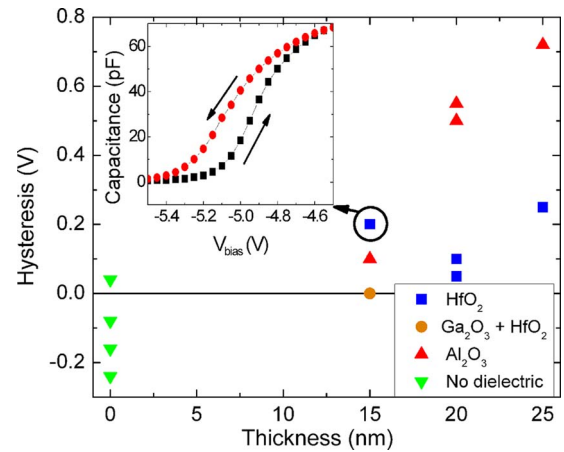


Fig. 2. Hysteresis for different capacitors versus dielectric thickness. The inset shows an example of hysteresis measurement.

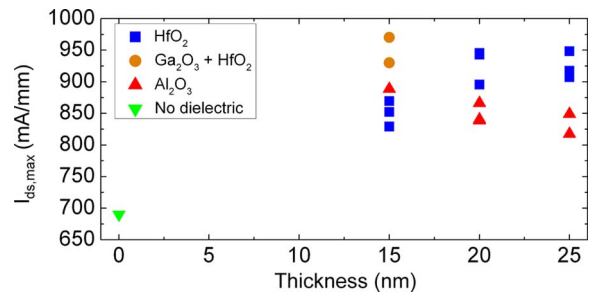


Fig. 3. Maximum drain current densities versus dielectric thickness. Currents measured at the highest V_{gs} , where $I_g < 0.1 \text{ mA/mm}$.

500 Hz to 1 MHz while biasing the capacitors around the depletion point [13]. The capacitors with the HfO₂ dielectric (with and without the Ga₂O₃) and Al₂O₃ had maximum interface trap densities of around 1×10^{12} and $3 \times 10^{13} \text{ cm}^{-2} \cdot \text{eV}^{-1}$, respectively, and the characteristic frequencies of the HfO₂ and Al₂O₃ interface traps were between 500 kHz and 1 MHz and less than 500 Hz, respectively. The predominance of slow traps in Al₂O₃ interface accounts for the greater hysteresis in the *C*–*V* measurements of the W/Al₂O₃ capacitors than in the W/HfO₂ capacitors.

The *I*_{ds}–*V*_{ds} output characteristics were measured for the HEMTs with different dielectrics. The gate voltage of each transistor was swept to the highest possible gate voltage ($V_{gs,max}$) without the gate leakage exceeding 0.1 mA/mm. The use of gate dielectric allows for 30%–40% higher *I*_{ds,max} than in standard devices. As shown in Fig. 3, the *I*_{ds,max} for the HfO₂ HEMTs increases with the dielectric thickness, and in the Al₂O₃ devices, *I*_{ds,max} decreases with the dielectric thickness. These trends are currently under investigation and will be the subject of a future publication.

As shown in Fig. 4, the transconductance of the MIS devices is higher than what would be expected considering the lower gate capacitance, even after taking the decrease in sheet resistance into account. There needs to be a relative increase in the saturation velocity or the mobility in order to account for this increase in transconductance. We believe that the presence of an insulator, particularly Al₂O₃, prevents mobility degradation due to the Schottky gate metal, which can explain the increase

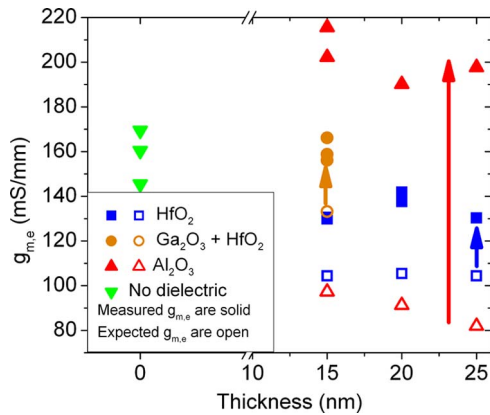


Fig. 4. Maximum extrinsic transconductances versus thickness with $V_{ds} = 5$ V. The measured $g_{m,e}$ for the MIS HEMTs is much higher than what can be expected when taking the reduction in gate capacitance into account.

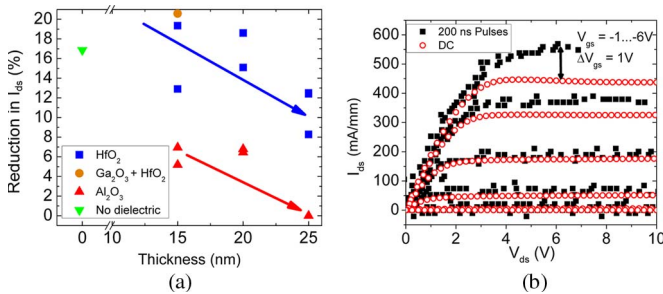


Fig. 5. (a) Reduction in drain current densities, resulting from the change in gate voltage pulse times from 1 ms to 200 ns. (b) Output characteristics of 15-nm Al_2O_3 HEMT for both 200-ns pulsed gate bias and dc gate bias.

in transconductance and electron velocity, as also reported by other groups [14]–[16].

Current collapse in the fabricated devices was characterized by pulsed- IV measurements with pulsewidths of 1 ms, 80 μs , and 200 ns and a load resistance of 100 Ω . Fig. 5(a) shows the reduction in I_{ds} when the gate pulsewidth was changed from 1 ms to 200 ns. For all dielectrics, dispersion reduces with an increase in dielectric thickness, as also demonstrated for Si_3N_4 [17]. The output characteristics shown in Fig. 5(b) show that the Al_2O_3 dielectric passivates the AlGaIn surface [16]. The predominance of slow traps in Al_2O_3 may explain why Al_2O_3 passivates the semiconductor better than the HfO_2 despite having a higher interface density than HfO_2 , but this is still under investigation.

IV. CONCLUSION

A new W/high- k dielectric gate stack has been developed, where Al_2O_3 , HfO_2 , and $\text{Ga}_2\text{O}_3 + \text{HfO}_2$ dielectrics have been evaluated. Devices with the W/dielectric gate stack were annealed at 870 $^\circ\text{C}$ and showed no reduction in performance compared to the reference HEMT. While the W/ Al_2O_3 HEMTs show the best transconductance and dispersion performance, the $\text{Ga}_2\text{O}_3 + \text{HfO}_2$ combination has the best maximum drain current density, low interface traps, and negligible hysteresis along with transconductance that is comparable to that of standard Ni/Au/Ni gate HEMTs. Regardless of the dielectric

used, these W/ high- k dielectric gates show great promise for self-aligned HEMTs in very high frequency applications.

ACKNOWLEDGMENT

Devices were fabricated at the MIT Microsystems Technology Laboratory and the Harvard CNS facilities.

REFERENCES

- [1] M. Higashiwaki, T. Mimura, and T. Matsui, "30-nm-gate AlGaIn heterostructure field-effect transistors with a current-gain cutoff frequency of 181 GHz," *Jpn. J. Appl. Phys.*, vol. 45, no. 42–45, pp. L1111–L1113, Oct. 2006.
- [2] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaIn/GaN high electron mobility transistors with InGaIn back-barriers," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 13–15, Jan. 2006.
- [3] P. J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum f_T of millimeter-wave MODFETs," *IEEE Electron Device Lett.*, vol. 10, no. 7, pp. 291–293, Jul. 1989.
- [4] Nidhi, T. A. Palacios, S. Chakraborty, U. K. Keller, and U. K. Mishra, "Study of impact on access resistance on high-frequency performance of AlGaIn/GaN HEMTs by measurements at low temperatures," *IEEE Electron Device Lett.*, vol. 2, no. 11, pp. 887–880, Nov. 2006.
- [5] A. Endoh, I. Watanabe, Y. Yamashita, T. Mimura, and T. Matsui, "AlGaIn/GaN MIS-HEMTs with f_T of 194 GHz at 16 K," *Electron. Lett.*, vol. 44, no. 4, pp. 319–320, Feb. 2008.
- [6] J. S. Moon, P. Hashimoto, D. Wong, M. Hu, M. Antcliffe, C. McGuire, M. Micovic, P. Willadsen, and D. Chow, "10 W/mm and high PAE field-plated AlGaIn/GaN HEMTs at Ka-band with n + GaIn source contact source contact ledge," in *Proc. 65th Annu. Device Res. Conf.*, Jun. 2007, pp. 33–34.
- [7] C.-H. Chen, S. Keller, G. Parish, R. Ventury, P. Kozodoy, E. L. Hu, S. P. DenBaars, U. K. Mishra, and Y. Wu, "High-transconductance self-aligned AlGaIn/GaN modulation doped field-effect transistors with regrown ohmic contacts," *Appl. Phys. Lett.*, vol. 73, no. 21, pp. 3147–3141, Nov. 1998.
- [8] V. Kumar, D. H. Kim, A. Basu, and I. Adesida, "0.25 μm self-aligned AlGaIn/GaN high electron mobility transistors," *IEEE Electron Device Lett.*, vol. 29, no. 1, pp. 1227–1228, Jan. 2008.
- [9] J. W. Johnson, E. L. Piner, A. Vescan, R. Therrien, P. Rajagopal, J. C. Roberts, J. D. Brown, S. Singhal, and K. J. Linthicum, "12 W/mm AlGaIn-GaN HFETs on silicon substrates," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 459–461, Jul. 2004.
- [10] J. W. Chung, J. C. Roberts, L. Piner, and T. Palacios, "Effect of gate leakage in the subthreshold characteristics of AlGaIn/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 29, no. 11, pp. 1196–1198, Nov. 2008.
- [11] M. Marso, G. Heidelberger, K. M. Indlekofer, J. Bernat, A. Fox, P. Kordos, and H. Luth, "Origin of improved RF performance of AlGaIn/GaN MOSHFETs compared to HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 7, pp. 1517–1523, Jul. 2006.
- [12] M. Fleetwood, R. Shaneyfelt, L. Warren, R. Schwank, L. Meisenheimer, and S. Winokur, "Border traps: Issues for MOS radiation response and long-term reliability," *Microelectron. Reliab.*, vol. 35, no. 3, pp. 403–428, Mar. 1995.
- [13] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. Toronto, ON, Canada: Wiley, 1998.
- [14] D. Gregusova, R. Stoklas, K. Cico, T. Lalinsky, and P. Kordos, "AlGaIn/GaN metal-oxide-semiconductor heterostructure field effect transistors with 4 nm thick Al_2O_3 gate oxide," *Semicond. Sci. Technol.*, vol. 22, no. 5, pp. 947–951, Aug. 2007.
- [15] J. Kuzmik, G. Pozzovivo, S. Abermann, J.-C. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, E. Bertagnolli, G. Strasser, and D. Pogany, "Technology and performance of InAlN/AlN/GaN HEMTs with gate insulation and current collapse suppression using ZrO_2 or HfO_2 ," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 937–941, Mar. 2008.
- [16] R. Stoklas, S. Gazi, D. Gregusova, J. Novak, and P. Kordos, "Enhancement of effective carrier velocity in AlGaIn/GaN MOSHFETs with Al_2O_3 gate oxide," *Phys. Stat. Sol. (C)*, vol. 5, no. 6, pp. 1935–1937, 2008.
- [17] Y. Pei, S. Rajan, M. Higashiwaki, Z. Chen, S. P. DenBaars, and U. K. Mishra, "Effect of dielectric thickness on power performance of AlGaIn/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 313–315, Apr. 2009.