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Gate-Tunable and Multidirection-Switchable Memristive Phenomena in a Van Der Waals Ferroelectric

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Memristive devices have been extensively demonstrated for applications in nonvolatile memory, computer logic, and biological synapses. Precise control of the conducting paths associated with the resistance switching in memristive devices is critical for optimizing their performances including ON/OFF ratios. Here, gate tunability and multidirectional switching can be implemented in memristors for modulating the conducting paths using hexagonal α-In_2Se_3, a semiconducting van der Waals ferroelectric material. The planar memristor based on in-plane (IP) polarization of α-In_2Se_3 exhibits a pronounced switchable photocurrent, as well as gate tunability of the channel conductance, ferroelectric polarization, and resistance-switching ratio. The integration of vertical α-In_2Se_3 memristors based on out-of-plane (OOP) polarization is demonstrated with a device density of 7.1×10^9 in.$^{-2}$ and a resistance-switching ratio of well over 10^3. A multidirectionally operated α-In_2Se_3 memristor is also proposed, enabling the control of the OOP (or IP) resistance state directly by an IP (or OOP) programming pulse, which has not been achieved in other reported memristors. The remarkable behavior and diverse functionalities of these ferroelectric α-In_2Se_3 memristors suggest opportunities for future logic circuits and complex neuromorphic computing.

The memristor has been conceptualized as the fourth fundamental circuit element and has sparked keen interest.[1–5] Ferroelectric memristors, which typically feature a thin ferroelectric layer sandwiched between two electrodes, can retain ON/OFF resistance states through ferroelectric switching generated by the history of the poling bias.[1,6,7] The outstanding performance of these devices, including large ON/OFF switching ratios, long retention times, and simple device architectures, make ferroelectric memristors attractive for binary information storage and biological synaptic emulation.[1,6,8–10] The demand for high-density memories for future artificial intelligence applications has driven memristor research toward miniaturization of both lateral and vertical dimensions. Hence, 2D layered ferroelectric semiconductors[11–16] are strong candidates for future memristor scaling.

Limited by the building block of insulating ferroelectric ceramics, typically reported ferroelectric memristors[1,6,7] are solely restricted to out-of-plane (OOP) polarization switching along the vertical device architectures, which achieve junction conductance through the tunneling effect. Planar ferroelectric memristors or "memtransistors" (i.e., gate-tunable memristors) utilizing the in-plane (IP) polarization switching have not yet been realized. On the other hand, the capability to program a memristor at both planar and vertical orientations (i.e., multidirectional programming) enables the tuning of device conducting paths through a third terminal, which is intriguing and favorable for integrating device array with optimized performances and small device-to-device variations.[17,18] However, multidirectional electrical control of a ferroelectric memristor still remains unexplored.

Here the planar- and vertically structured ferroelectric memristors are successfully implemented using a van der Waals α-In_2Se_3 semiconductor. Benefitting from the superior optical properties[19,20] and interlocked IP and OOP dipoles of α-In_2Se_3,[21] the memristive phenomena in ferroelectric α-In_2Se_3 flakes show remarkable photon modulation, wide gate tunability and unique multidirection programming, which have not otherwise been achieved in previously reported memristive devices.

The α-In_2Se_3 crystal possesses two stacking polymorphs, including hexagonal (2H) and rhombohedral (3R)

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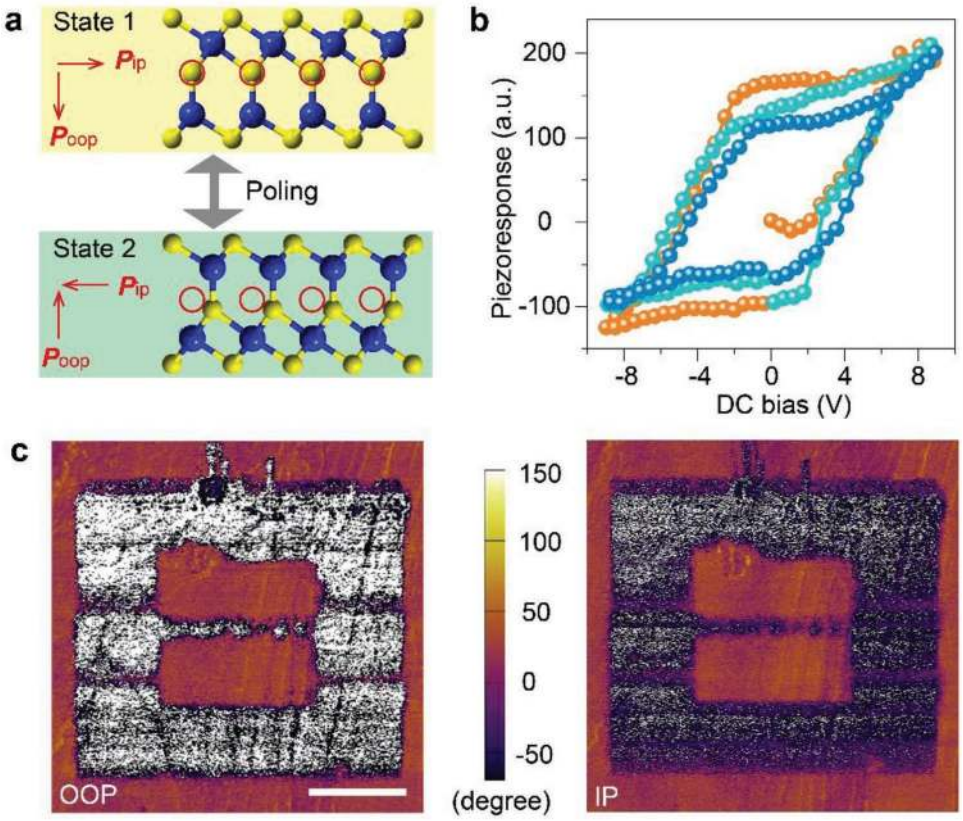

Figure 1. The interlocked out-of-plane and in-plane ferroelectricity in multilayer 2H α-In_2Se_3. a) The α-In_2Se_3 crystal structures depicting the interlocked polarization mechanism in the OOP and IP orientations. The yellow and blue balls represent Se and In atoms, respectively. After large bias poling that exceeds the coercive voltage, the central Se atoms, which are the origin of the interlocked spontaneous polarization, move toward the bottom-right direction, simultaneously reversing the OOP and IP dipoles (State 1 → State 2). b) Piezoresponse hysteresis loops (three cycles) for a multilayer α-In_2Se_3 crystal. c) The OOP and IP phase images after forward (+8 V) and reverse (−8 V) DC bias written in the outer square and two inner rectangles. Scale bar: 500 nm.

structures,[22–24] both of which have been demonstrated as intrinsic ferroelectrics.[25–27] In this work, we studied 2H α-In_2Se_3 flakes (Section S1, Supporting Information) exfoliated from a bulk crystal. As schematically shown in **Figure 1**a, each isolated α-In_2Se_3 monolayer is comprised of five atomic layers connected by covalent bonds in the sequence of Se–In–Se–In–Se. This covalent bond configuration of the central Se atoms with the adjacent In atoms results in interlocked OOP and IP dipoles,[21,28] which stabilizes the ferroelectricity even down to the monolayer limit at room temperature.[26] Due to the unique structural asymmetry, polarization reversal in α-In_2Se_3 can be realized by bias poling along either the OOP or IP orientation.

To demonstrate the interlocked ferroelectricity, we transferred an exfoliated 2H α-In_2Se_3 flake (≈95 nm thick) to a conductive gold substrate. Figure 1b shows the typical off-field piezoresponse hysteresis loops of the α-In_2Se_3 as a function of the DC bias applied on a piezoresponse force microscopy (PFM) tip. Once the OOP tip bias exceeds the coercive voltage of 2–4 V, the piezoresponse begins to flip to the opposite polarization state, a clear signature of ferroelectricity.[21,26] Next, we applied large OOP DC biases to pole the 2H α-In_2Se_3 specimen and recorded its OOP and IP phases (Figure 1c), as well as the amplitude (Section S2, Supporting Information). Because of the dipole interlocking effect, the related IP ferroelectric dipoles switch simultaneously with the OOP dipole reversal.

To explore memristor applications of α-In_2Se_3, we first studied the electrical transport of a planar two-terminal device that was based on IP polarization switching. **Figure 2**a displays an atomic force microscopy (AFM) image and the cross-sectional schematic of a representative two-terminal α-In_2Se_3 memristor (Figure S8a, Supporting Information), which was fabricated on a silicon substrate with a 300 nm oxide layer. As expected, we obtained reproducible pinched hysteresis loops (Figure 2b; Figure S8c, Supporting Information) under various maximum-sweep voltages ($V_{max\text{-}sweep}$). The observed hysteretic window, a typical characteristic of memristors,[6] gradually enlarges with the increasing of $V_{max\text{-}sweep}$. Together with TEM images, Raman spectra and temperature-dependent electric curves in Section S3 (Supporting Information), we can conclude that the ferroelectricity is the origin of the memristive effect in α-In_2Se_3. This operating mechanism is fundamentally distinct from previously reported In_2Se_3 phase change memories,[29,30] which operate by the phase transition between the initial amorphous state and the annealing-induced polycrystalline state of the material.

As indicated by the black arrows in Figure 2b, the α-In_2Se_3 memristor is first at a low-resistance state (LRS) for the V_{drain}

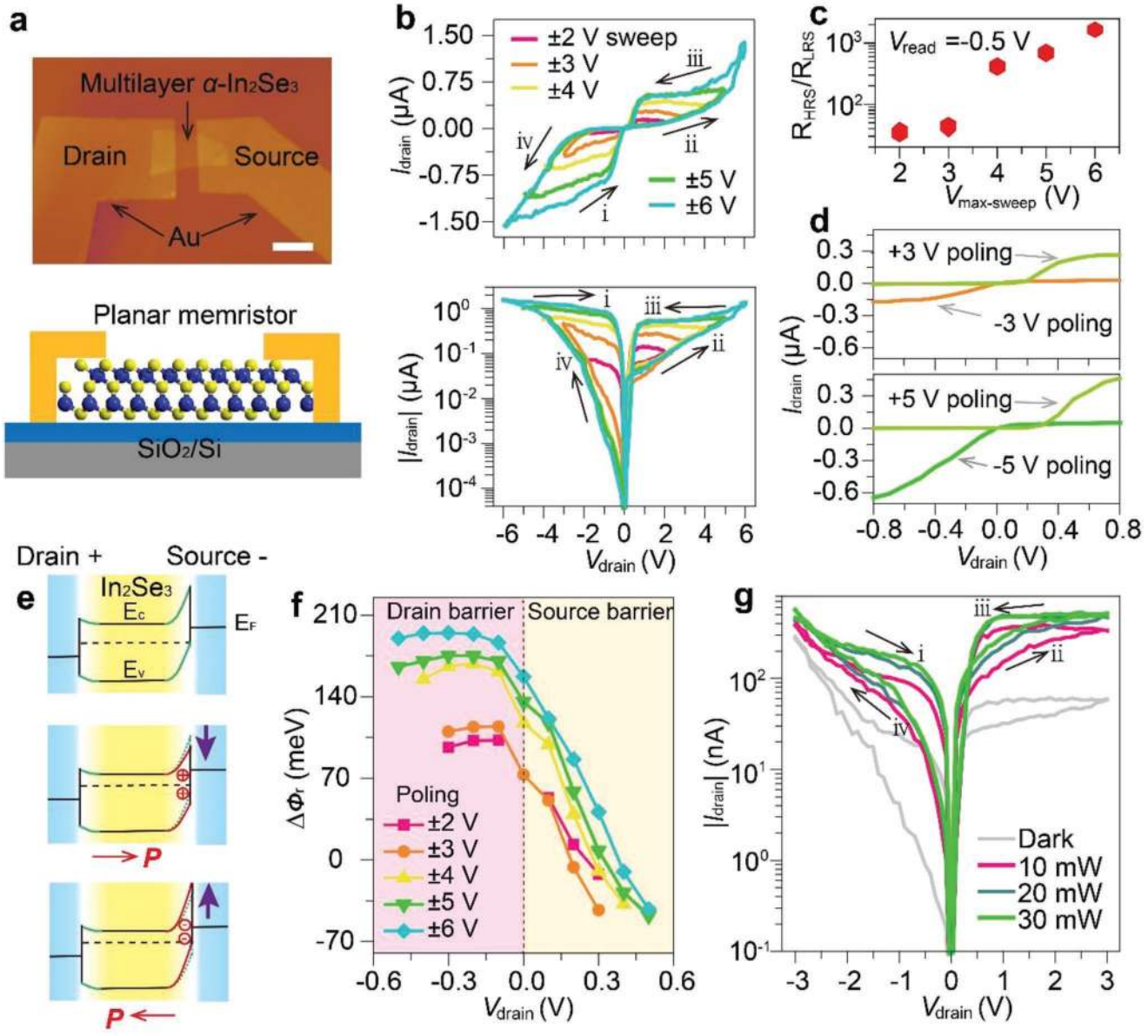

Figure 2. The memristive effect and switchable photocurrent of an IP polarization–based α-In_2Se_3 memristor. a) AFM image and cross-sectional schematic of a typical planar memristor, in which the thickness of the α-In_2Se_3 was ≈46 nm. Scale bar: 2 μm. b) Pinched hysteresis loops with the maximum sweep V_{drain} increased from 2 to 6 V. The sweeping directions are indicated by the arrows. c) The resistance switching ratio with respect to the maximum sweep voltage ($V_{max\text{-}sweep}$). d) The switchable ferroelectric diode effect at different poling biases. The data in (c) and (d) are derived from (b). e) Band diagrams at a positive drain bias to depict the ferroelectric switching mechanism. As the memristor is poled by a forward pulse, the ferroelectric dipole will point right, like the red arrow in the middle diagram. When the memristor is poled by a reverse pulse, it will point left, as the bottom diagram shows. The purple arrows indicate the direction of the Schottky barrier change after applying a poling pulse. f) The quantitative change in the reverse-biased Schottky barrier ($\Delta\varnothing_r$) after successive forward and reverse bias poling. g) Observation of the switchable photocurrent effect in the α-In_2Se_3 memristor under different powers of simulated sunlight illumination.

sweep from a negative $V_{max\text{-}sweep}$ to 0 V (sweep i) and turns to a high-resistance state (HRS, sweep ii). The device retains the HRS until the V_{drain} increases to a positive $V_{max\text{-}sweep}$ (sweep ii), and then is set to an LRS when the V_{drain} sweeps back to 0 V (sweep iii). As the V_{drain} decreases below 0 V, the resistance state changes to the HRS (sweep iv). Thereby, referring to the resistance transition from sweeps i to ii, this device acts as an LRS–HRS memristor. Strikingly, the switching ratio between the HRS and the LRS approaches 10^3 (Figure 2c; Figure S8d, Supporting Information) as the $V_{max\text{-}sweep}$ exceeds 4–5 V, which is even larger than conventional ferroelectric ceramic based memristors.[6] Figure 2d and Figure S8b (Supporting Information) show that the distinct switchable diode effect can be obtained after bias poling. The notable transition between the forward diode curve and the reverse diode curve, poled by a positive and negative bias respectively, could be attributed to

the asymmetric modulation of the Schottky barriers through ferroelectric polarization charges.[9,31] The modulation effect of ferroelectric polarization on two barriers is analogous to the barrier change induced by the drift of oxygen vacancies in TiO_2 memristive devices.[32]

Figure 2e shows the band diagrams depicting the memristive effect, as well as the switchable diode effect in the LRS–HRS α-In_2Se_3 memristor. For a standard metal–semiconductor-metal device with a fixed bias, it is reasonable to simplify its two-Schottky-barrier model to a single barrier model at the reverse-biased terminal.[33] Here, we take the reverse-biased terminal at the source terminal as an example. The positive-bias poling produces positively polarized charges at the source terminal (the middle panel of Figure 2e). Consequently, this dominated barrier height decreases and the observed current in sweep iii and Figure 2d actually increases. In contrast, the negative-bias poling accumulates negatively polarized charges at the source terminal (the bottom panel of Figure 2e), further giving rise to the increased source barrier and decreased current (sweep ii and Figure 2d). The carrier transport across the reverse-biased barrier in the α-In_2Se_3 memristor can be described by the thermionic emission and diffusion theory (see Figure S9 in the Supporting Information and the Experimental Section).[33] Figure 2f shows the reverse-biased Schottky-barrier change after successive forward and reverse bias poling, which are derived from the thermionic emission and diffusion theory (see the Experimental Section). Overall, the negative value of the source-barrier change appears at a forward V_{drain} while the positive value of the drain-barrier change occurs at a reverse V_{drain}. Such change in the Schottky barrier is responsible for the LRS-to-HRS switching of the device. In addition, a large barrier change can result in the large resistance switching.

Significantly, we observed a switchable photocurrent for this two-terminal α-In_2Se_3 memristor (Figure 2g), which provides another degree of freedom for using light to control the conducting path of the device and further construct nonvolatile photomemories. The photocurrent in ferroelectric α-In_2Se_3 memristor arises from the separation of photogenerated electron–hole pairs, rather than noncentrosymmetry induced bulk photovoltaic effect in conventional oxide ferroelectrics.[34] It is reported that the incident-light-induced thermal effect in α-In_2Se_3 can be ignored due to the tiny temperature gradient (0.1 K) under a large power density of 100 W cm^{-2}.[19] Our results demonstrate a saturation in the photocurrent switching with increasing light power to 20–30 mW. As previously reported,[35,36] the photocurrent across a device is closely dependent on its current injection: a large current injection gives rise to a large photocurrent. Thus, we ascribe the photocurrent switchability to the current (resistance) switching shown in Figure 2b, whose origin is the ferroelectricity of α-In_2Se_3.

We further investigated the write and read performances of the IP polarization–based α-In_2Se_3 memristor. **Figure 3**a depicts a plot of the resistance switching as we regularly varied the magnitude of the applied write pulse (with a fixed width of 2 s). We observed a parallelogram-like hysteresis with remarkable memristive behavior between the HRS ($\approx 8 \times 10^9$ Ω) and LRS ($\approx 1.58 \times 10^7$ Ω), which corresponds to an R_{HRS}/R_{LRS} ratio of ≈500. Within the horizonal plane of the α-In_2Se_3 memristor (Figure 2a; the drain and the grounded source are indicated as the left and right electrodes, respectively), the ferroelectric polarization for the LRS mainly points left (P_{left}) and that for the HRS points right (P_{right}), as the inset in Figure 3a shows. The asymmetry switching (turning points for $P_{left} \rightarrow P_{right}$ and $P_{right} \rightarrow P_{left}$) and the existing intermediate states at the slope are also consistent with the piezoresponse loop in Figure 1b.

The resistance switching is not only determined by the magnitude of the write pulse but also by its width.[6] We analyzed the write-pulse width dependent switching dynamic between the HRS and the LRS (Figure 3b). To intuitively present the intermediate states under various pulse widths, we first hypothesized that the conduction could be attributed from the coexisting P_{left} and P_{right}, and then defined the relative ratio of P_{right} as $S = (1/R - 1/R_{LRS})/(1/R_{HRS} - 1/R_{LRS})$; thereby, S actually changes from 1 in the HRS (P_{right}) to 0 in the LRS (P_{left}). The nonzero initial S in the left panel of Figure 3b indicates the preexistence of interfacial dipoles that acts as a nucleation center and favor P_{right} polarization switching.[6] Generally, a 1.5 s wide (or 2 s wide) write pulse with 4 V amplitude can fully enable the right (or left) reversal of the ferroelectric polarization in the LRS–HRS α-In_2Se_3 memristor. This pulse-width-dependent phenomenon is appealing for artificial synapses, which operate at a frequency of 1–10 Hz and in which the synaptic transmission is associated with the accumulative timing of spikes emitted by the pre and post neurons.[37,38]

We also measured the reversible resistance switching of the planar α-In_2Se_3 memristor by repeatedly poling the device and then reading it at −0.5 V. As shown in Figure 3c and Figure S10a (Supporting Information), the bipolar resistance switching presents excellent reproducibility and nearly maintains the large HRS/LRS ratio of $>10^2$ over 100 cycles. Figure 3d and Figure S10b (Supporting Information) show a retention test of the planar α-In_2Se_3 memristor. Influenced by the interface charges related depolarization field, the switching ratio gradually decreases but still maintains well over one order of magnitude for up to 2000 s.

Introducing a gate to electrically control a two-terminal ferroelectric memristor, i.e., a so-called ferroelectric memtransistor, is important for fundamental studies and device applications. We demonstrate that our IP polarization–based planar α-In_2Se_3 memristor is also gate tunable, which has not been previously observed in other ferroelectric-memristive devices.[6,7] The remarkable hysteric transfer curves in **Figure 4**a and Figure S11a (Supporting Information) indicate that the back-gate voltage not only modulates the channel conductance in the α-In_2Se_3 memtransistor, but also its ferroelectric polarization reversal. When the magnitude of the vertical (or OOP) gate field exceeds +35 or −35 V, the OOP polarization in the ferroelectric α-In_2Se_3 can be reversed upward or downward. As shown in Figure 4b, after applying gate pulses, the resistance states in the channel of this memtransistor are subsequently set to the LRS or HRS, which can be considered as the IP polarization pointing left or right (the definition of polarization orientation is the same as that in Figure 3a). The large hysteric window (Figure 4a) and gate-write/channel-read performance (Figure 4b) strongly suggests that the interlocked upward-leftward ferroelectric dipoles in α-In_2Se_3 (like State 2 in Figure 1a) can be flipped over by using a gate field that is

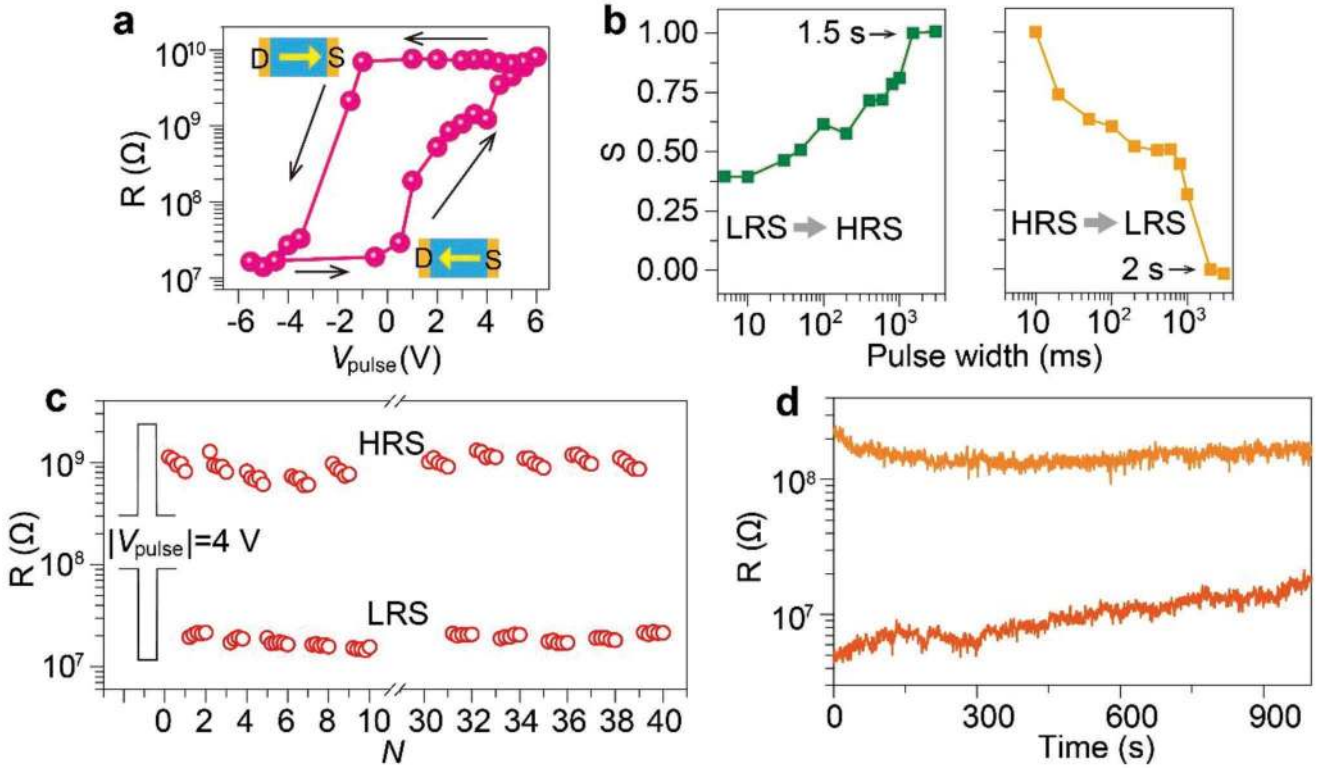

Figure 3. Write/read performance of the IP polarization–based α-In_2Se_3 memristor. a) The write pulse (V_{pulse}) dependence of the memristor resistance for the device shown in Figure 2. The read voltage (V_{read}) was fixed at –0.5 V for (a)–(d). b) Polarization switching dynamics: the switched fraction (S) of left-to-right (left panel) and right-to-left (right panel) switching as a function of the applied pulse width for the LRS-to-HRS (left) and HRS-to-LRS (right) transitions. Regarding each single-point measurement of S, the memristor was set to the initial LRS for the LRS-to-HRS test and to the initial HRS for HRS-to-LRS test. V_{pulse}: ±4 V. c) Reversible resistance switching between the HRS and LRS over 40 cycles. The amplitude and width of the write voltage were set at 4 V and 2 s, respectively. d) Retention test, in which the ratio of the HRS and LRS states remained over one order of magnitude for up to 1000 s.

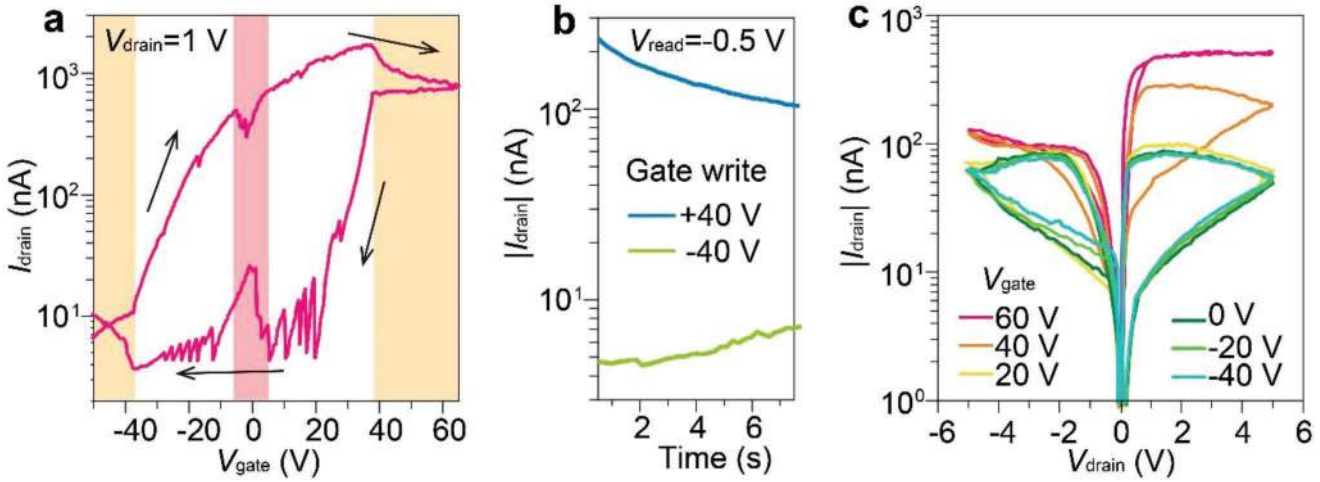

Figure 4. Gate-tunable memristive effect of the planar α-In_2Se_3 memristor. a) Representative V_{gate}–I_{drain} transfer curves. When exceeding the coercive field in α-In_2Se_3, a vertical electric field applied by the back gate can reverse not only OOP dipoles but also IP dipoles, resulting in the IP resistance switching. The voltage sweeping direction is shown by the arrows. b) Source–drain current (resistance) switching collected after gate-pulse writing (i.e., programming). These results suggest the domain reversal in the channel by the gate voltage. The read voltage is applied on the drain–source terminal. c) Output curves (I_D–V_D) at different gate biases. The positive gate bias largely quenches the resistance switching while the negative gate bias recovers it.

nearly perpendicular to the planar device. These results demonstrate that for the first time we observe evidence that a gate bias can enable the flipping of the ferroelectric polarization of the channel material, as well as the optimization of ferroelectric resistance switching (Figure 4c). Note that possibly due to the screening effect on the polarization charges, the transfer curves in Figure 4a for the two fully toggled states (beyond ±40 V) exhibit some variation; the back-and-forth sweep near 0 V approach one other. As depicted in Figure 4c and Figure S11b (Supporting Information), as we decrease the gate voltage, the source–drain current (resistance) switching ratio for this planar α-In_2Se_3 memtransistor can be gradually tuned from zero to over one order of magnitude. When the gate voltage is less than 0 V, we can infer from the clockwisely scanned transfer curve in Figure 4a that the ferroelectric polarization states in channel α-In_2Se_3 are roughly identical, resulting in the unobvious ferroelectric resistance switching in Figure 4c. To summarize, due to the semiconducting ferroelectric nature of α-In_2Se_3, this planar memtransistor demonstrates gate tunability of the channel conductance, ferroelectric domain reversal and the resistance-switching ratio.

Next, we fabricated vertical memristor arrays using 25 nm thick α-In_2Se_3 nanoflakes sandwiched between two electrodes. As shown in **Figure 5**a, the devices can be integrated in a density of 7.1×10^9 per square inch. A set of typical pinched hysteresis loops for a vertical α-In_2Se_3 memristor cell are shown in Figure 5b. We also observe expanded switching windows, with the largest R_{HRS}/R_{LRS} ratio of over 10^3 (Figure S12, Supporting Information), comparable to that of the planar α-In_2Se_3 memristor. Most strikingly, the loops in Figure 5b show a resistance change from LRS (sweep ii) to LRS again (sweep iii) as guided by the arrows, that are distinguishable from the LRS–HRS planar memristor. Thus, we define this vertical device as an LRS–LRS memristor. The LRS–LRS nanodevice is associated with another transport mechanism: Fowler–Nordheim (FN) tunneling through a triangular potential barrier,[39] which we confirmed by its ideal linear plots of $\ln(I/V^2)$ and V^{-1} in Figure S13 (Supporting Information). Therefore, modulation of the polarization charges in the band profile[1] for the LRS–LRS memristor is quite different from that in the LRS–HRS memristor (see the Experimental Section). In addition, the R_{HRS}/R_{LRS} ratio can be tuned over 20-fold by decreasing the frequency of the applied sweep bias (Figure 5c), in agreement with previous works.[6] Figure 5d shows a histogram of the largest R_{HRS}/R_{LRS} ratios measured from 50 LRS–LRS memristors on a 25 nm thick α-In_2Se_3. The variability among the individual memristor cells may be ascribed to the top-electrode inhomogeneity introduced by electron-beam lithography (EBL) patterning and the actual contact-area difference between the α-In_2Se_3 and the bottom Au electrode.

Finally, we designed a multidirectionally operated ferroelectric α-In_2Se_3 memristor, as shown in **Figure 6**a,b, enabling the control of OOP (or IP) electrical transport by IP (or OOP) programming. The device nanofabrication process and pinched hysteresis loops measured from the bottom two electrodes for this multidirectional memristor are presented in Figures S14 and S15 (Supporting Information). Instead of domain poling via an OOP bias, an IP pulse (Figure 6c,d) is also able to efficiently program the vertical memristor cells and modulate their

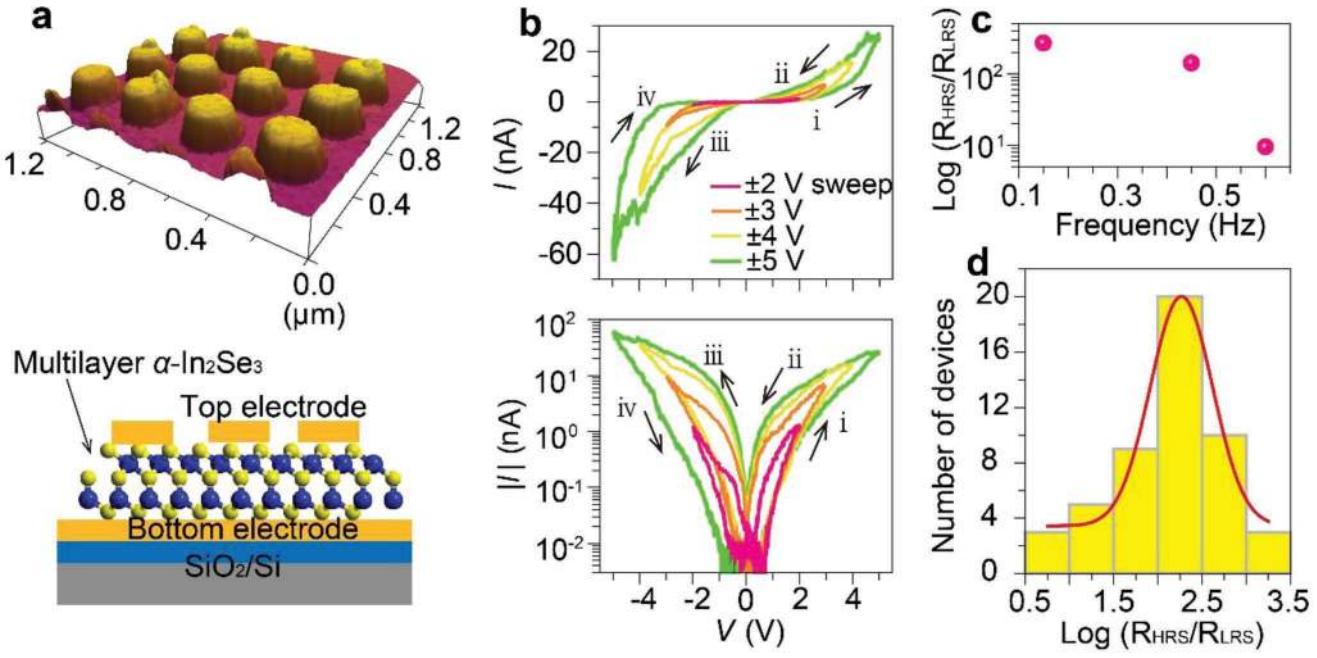

Figure 5. A scalable and high-density memristor array based on the OOP polarization in α-In_2Se_3 nanoflakes. a) AFM image and cross-sectional schematic of a vertical memristor array. The diameter for each memristor cell is ≈200 nm and the distance between each cell is 100 nm, which corresponds to an integrated density of 7.1×10^9 in.$^{-2}$. The thickness for α-In_2Se_3 is about ≈25 nm. b) Pinched hysteresis loops with different magnitudes of the maximum-sweep voltage for a typical memristor cell, as shown in (a). The switching directions are shown by the arrows. c) Frequency dependence of the R_{HRS}/R_{LRS} ratio at $V_{max\text{-}sweep} = 5$ V. d) Histogram showing the largest R_{HRS}/R_{LRS} ratios for 50 distinct memristors. The fitted curve as indicated by the red line corresponds to a Gaussian distribution.

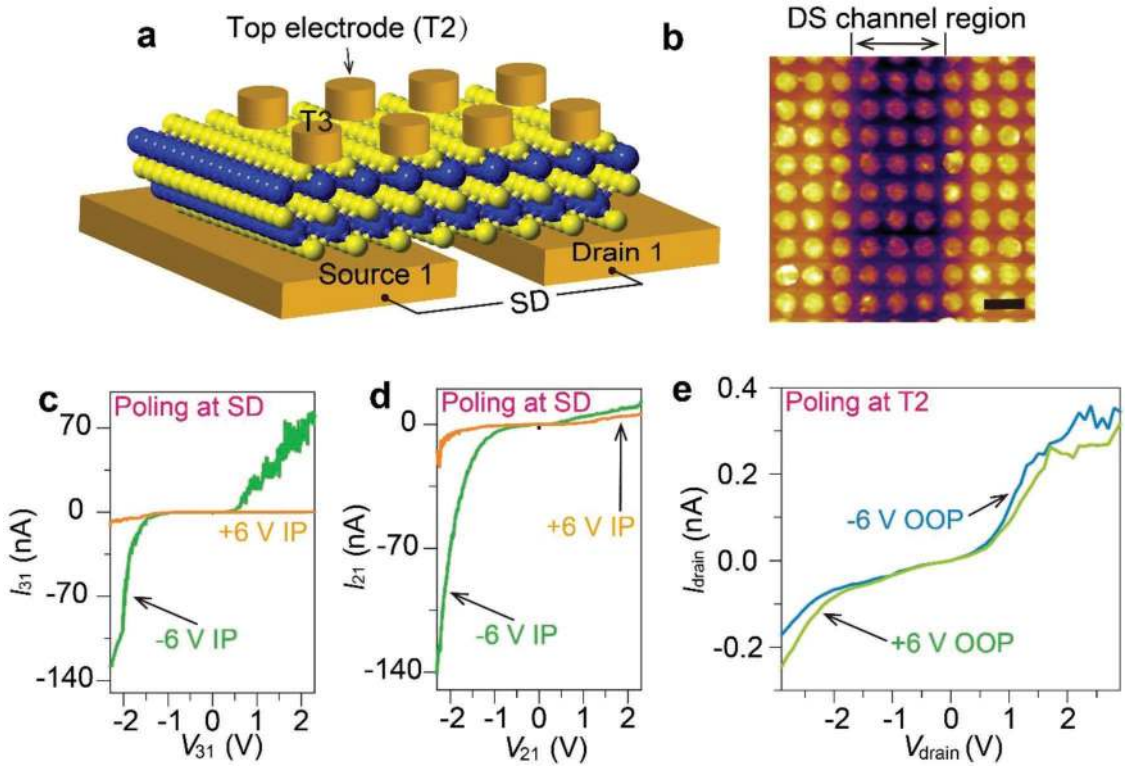

Figure 6. Demonstration of a multidirectionally programmed α-In_2Se_3 memristor. a) Schematic illustration of a novel memristor that can be programmed in both vertical and lateral directions. The two parallel metal strips (drain 1 and source 1; distance: 2 µm) provide bottom IP poling for the data in (c) and (d) or serve as grounded electrodes for the T2 poling in (e). The top nanodisk-shaped electrodes have the same integration density as in Figure 5a. b) AFM image of a typical α-In_2Se_3 memristor as depicted in (a). Scale bar: 500 nm. c,d) OOP current (resistance) switching for the typical T3 (located in the nonchannel region) and T2 (in the channel region) memristor cells, respectively, after ±6 V IP programming. e) IP current (resistance) switching for the bottom source–drain memristor after ±6 V OOP programming at the single T2 cell.

conducting paths in both nonchannel and channel regions. This extra programming terminal could be used to act as the set/reset source for all OOP memristor cells, which is realized by the simultaneous reversal of the interlocked IP and OOP dipoles in 2H α-In_2Se_3. Furthermore, through an OOP programming pulse upon the single memristor cell, that is T2, a discernable change in the IP electrical curves can be seen (Figure 6e).

In summary, we have demonstrated planar and vertical ferroelectric memristors using a layered semiconducting α-In_2Se_3 crystal. The IP polarization based planar memristor presents switchable photocurrent and gate tunability in the channel conductance, ferroelectric domain reversal and resistance-switching ratio. The OOP polarization based vertical α-In_2Se_3 memristor features a maximum resistance-switching ratio of 10^3 and can be integrated at a density of 7.1×10^9 per square inch. Additionally, we developed a multidirectionally operated memristor to demonstrate the OOP (or IP) resistance switching that can be achieved through IP (or OOP) pulse programming. The demonstrations in this work are applicable for future advanced functional nonvolatile memories and complex synaptic emulation.

Experimental Section

Device Fabrication and Measurements: Multilayer α-In_2Se_3 nanoflakes were cleaved from bulk crystal (2DSemiconductor) onto silica or gold substrates for ferroelectric characterization and device fabrication. All the nanodevices were fabricated using EBL and their conducting electrodes were deposited by electrobeam evaporation. If not specified, all measurements were conducted at room temperature. PFM measurements were performed on conductive gold substrates using a Cypher ES-Asylum Research Oxford Instrument with a dual-AC resonance mode. A conductive tip with Pt/Ti coating and an average spring constant of 2 N m^{-1} was chosen. The resonance frequencies for the OOP and IP PFM characterization studies were ≈240 and ≈680 kHz, respectively. The piezoresponse loops were collected by a combination of a changing DC bias and a 0.5 V AC bias.

All electrical measurements for the planar α-In_2Se_3 memristor were carried out using a Keithley 4200 in a quiet sweep mode with an average rate of 0.2 V s^{-1}. The pulse was generated from either an Agilent 33522A or Keithley 4200. The simulated sunlight source was used to excite the planar α-In_2Se_3 memristor. All electrical measurements for the vertical α-In_2Se_3 memristors were performed using conductive AFM or a home-built IV system (Stanford 570 and 345) that connects with a conductive AFM tip.

Switching Mechanism: For a planar α-In_2Se_3 memristor, electrical transport across the reverse-biased barrier ($\varnothing_r$) under a small V_{drain} ($V_{drain} > 3kT/q \approx 77$ meV) can be described by the thermionic emission and diffusion theory[33]

$$I = BA^{**}T^2 \exp\left(-\frac{\varnothing_r}{kT}\right)\exp\left(\frac{q\sqrt{q\xi\,/\,4\pi k_s}}{kT}\right) \quad (1)$$

$$\xi = \sqrt{\frac{2qN_D}{k_s}\left(V + V_{bi} - \frac{kT}{q}\right)} \quad (2)$$

in w hich B is the area of the Schottky barrier, A^{**} is the effective Richardson constant, q is the electron charge, k is the Boltzmann constant, N_D is the donor impurity density, V_{bi} indicates the built-in potential at the barrier, and k_s is the permittivity of α-In_2Se_3. From Equations (1) and (2), it can be seen that $V^{1/4}$ should be linear with the ln I. To confirm that the thermionic emission–diffusion theory can be precisely applied to our observed electrical curves, the extracted curves ($V^{1/4}$–ln$I$) from Figure 2b are plotted in Figure S9 (Supporting Information), demonstrating a close to linear relationship.

Assuming that S, A^{**}, k, N_D, k_s, T, and V_{bi} are all constants, $\varnothing_r$ in principle can be extracted from the ln$I$–V plot. Hence, the change in the Schottky barrier when positive (P) and negative (N) bias subsequently poles the memristors can be estimated from the following simplified equation

$$\ln\left[I(P)/I(N)\right] \sim -\Delta\varnothing_r / kT \tag{3}$$

in which I(P) and I(N), respectively, dictate the currents in the planar α-In_2Se_3 memristor after positive and negative poling biases.

For the vertical α-In_2Se_3 memristor, the sandwiched α-In_2Se_3 nanoflake was about ≈25 nm thick, whose electrical transport, especially for sweeps i and iv, can be explained by the FN tunneling theory.[39] It can be seen from Equation (4) that the $\ln(I/V^2)$ should be linear with V^{-1}, which we confirmed by the plots of $\ln(I/V^2)$ and V^{-1} taken at high electric field in Figure S12 (Supporting Information)

$$I = A_{eff}\frac{e^3 m_{Au}}{8\pi h m_s \phi_B} \times V^2 \exp\left(-\frac{8\pi\sqrt{2m_s}}{3he} \times \frac{\varnothing_B^{3/2}}{V}\right) \tag{4}$$

where A_{eff} is the effective tunneling area, ϕ_B is the barrier height, V is the applied bias, and m_{Au} and m_s dictate the effective electron mass in the gold electrode and α-In_2Se_3 channel, respectively. Modulation of the ferroelectric polarization charges on the electrical transport in the vertical α-In_2Se_3 memristor is the same as that in conventional ferroelectric tunnel junctions.[1] Although partial ferroelectric polarization charges could be imperfectly screened at the two-terminal interfaces, they still play a vital role in tuning the average height of the thin band profile in the metal–semiconductor-metal model. The negative poling bias makes the band profile higher while the positive poling bias lowers the band profile. Because the tunnel probability exponentially depends on the square root of the barrier height, there are more electrons tunneling across the band profile at positive poling bias. Therefore, both sweeps ii and iii in Figure 5b show LRS, which are fundamentally different from the case in Figure 2b.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

ferroelectrics, gate tunability, memristors, multidirectional programming

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