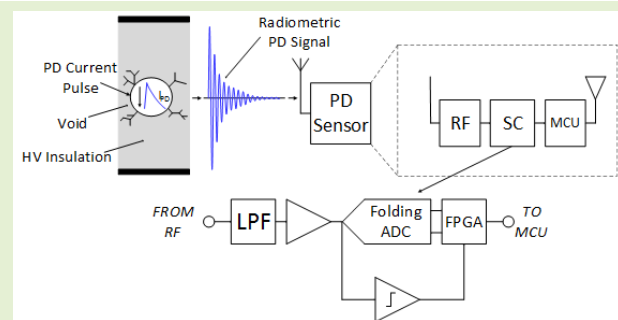


Gated Pipelined Folding ADC-Based Low Power Sensor for Large-Scale Radiometric Partial Discharge Monitoring

David W. Upton¹, Richard P. Haigh, Peter J. Mather², Pavlos I. Lazaridis³, *Senior Member, IEEE*,
Keyur K. Mistry, Zaharias D. Zaharis⁴, *Senior Member, IEEE*,
Christos Tachtatzis⁵, *Senior Member, IEEE*, and
Robert C. Atkinson, *Senior Member, IEEE*

Abstract—Partial discharge is a well-established metric for condition assessment of high-voltage plant equipment. Traditional techniques for partial discharge detection involve physical connection of sensors to the device under observation, limiting sensors to monitoring of individual apparatus, and therefore, limiting coverage. Wireless measurement provides an attractive low-cost alternative. The measurement of the radiometric signal propagated from a partial discharge source allows for multiple plant items to be observed by a single sensor, without any physical connection to the plant. Moreover, the implementation of a large-scale wireless sensor network for radiometric monitoring facilitates a simple approach to high voltage fault diagnostics. However, accurate measurement typically requires fast data conversion rates to ensure accurate measurement of faults. The use of high-speed conversion requires continuous high-power dissipation, degrading sensor efficiency and increasing cost and complexity. Thus, we propose a radiometric sensor which utilizes a gated, pipelined, sample-and-hold based folding analogue-to-digital converter structure that only samples when a signal is received, reducing the power consumption and increasing the efficiency of the sensor. A proof of concept circuit has been developed using discrete components to evaluate the performance and power consumption of the system.

Index Terms—Analog-digital conversion, partial discharge measurement, radiometers, UHF measurements, wireless sensor networks.



Manuscript received January 31, 2020; revised March 3, 2020; accepted March 9, 2020. Date of publication March 23, 2020; date of current version June 18, 2020. This work was supported by the Engineering and Physical Sciences Research Council under Grant EP/J015873/1. The associate editor coordinating the review of this article and approving it for publication was Prof. Bobby George. (Corresponding author: David W. Upton.)

David W. Upton was with the Department of Engineering and Technology, University of Huddersfield, Huddersfield HD1 3DH, U.K. He is now with the Swedish Institute of Space Physics, 981 92 Kiruna, Sweden (e-mail: david.upton@irf.se).

Richard P. Haigh is with Kromek Ltd., Huddersfield HD1 3BN, U.K. (e-mail: richard.haigh@kromek.com).

Peter J. Mather, Pavlos I. Lazaridis, and Keyur K. Mistry are with the Department of Engineering and Technology, University of Huddersfield, Huddersfield HD1 3DH, U.K. (e-mail: p.j.mather@hud.ac.uk; p.lazaridis@hud.ac.uk; keyur.mistry@hud.ac.uk).

Zaharias D. Zaharis is with the Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, 541 24 Thessaloniki, Greece (e-mail: zaharis@auth.gr).

Christos Tachtatzis and Robert C. Atkinson are with the Department of Electronic and Electrical Engineering, University of Strathclyde, Glasgow G1 1XW, U.K. (e-mail: christos.tachtatzis@strath.ac.uk; robert.atkinson@strath.ac.uk).

Digital Object Identifier 10.1109/JSEN.2020.2982576

I. INTRODUCTION

PARTIAL discharge (PD) is an electrical fault that occurs in high-voltage (HV) equipment that does not entirely breach the conductors. It is defined by the IEC60270 as “a localized electrical discharge that only partially bridges the insulation between conductors and which can or cannot occur adjacent to a conductor. Partial discharges are in general a contribution of local electrical stress concentrations in the insulation or on the surface of the insulation. Generally, such discharges appear as pulses having a duration much less than 1 microsecond” [1]. PD is caused by an increase in electric-field strength due to the presence of a void or defect, resulting in a localized discharge within the void [2], [3], which can worsen over time leading to the complete catastrophic failure of the affected plant [4]. PD is the primary metric used in diagnostics of HV plant equipment condition such as gas insulated switchgear (GIS), transmission lines and transformers [5], [6]. Traditional techniques for PD detection and measurement, such as high frequency current

transformers (HFCTs) and transient earth voltage (TEV) sensors [7], [8], require physical connection to the piece of plant under observation. Whilst these techniques provide detailed information about the local fault, including apparent charge and frequency spectra, the range they are capable of monitoring is limited to the item of plant they are physically connected to, due to the close coupling required, and sensitivity to near signal only, of the sensors. These techniques, therefore, would be costly and complex to implement in a comprehensive large-scale PD monitoring system.

Radiometric PD detection techniques avoid the requirement of hardwired sensors to HV equipment. The fundamental technique involves using radio receivers to detect and measure the electromagnetic signal propagated from the 1 – 1000 ns current pulse displaced during the PD event. This electromagnetic pulse signal resembles a classical decaying oscillation [9] within a bandwidth of 50 – 1000 MHz, depending on the type and structure of the fault [10]–[19]. However, the frequency range is generally limited to approximately 50 – 800 MHz due to the band-limiting response of the propagation environment containing various high-frequency attenuating metallic structures [20]. Furthermore, the bandwidth of the radiometric signal is filtered by the resonant structure of the void which produces a band-pass response [21]. The radiated PD signal is received and located by several radiometric sensors spatially separated [22]. Radiometric PD monitoring has the benefit of simple and fast installation, ease of reconfiguration, and the ability to monitor multiple plant items with a single sensor. These benefits come at the cost of reduced diagnostic information, since determining the absolute charge displaced during the PD event and the spectra of the original signal pose a greater challenge as compared to traditional techniques. However, a large-scale PD wireless sensor network (WSN) would be potentially capable of monitoring an entire substation at a far lower cost and complexity than that required by direct plant condition monitoring techniques.

Typically, radiometric PD detection techniques utilize high-speed sampling to acquire the received electromagnetic PD signals [23]–[27], which is a specific necessity for time of arrival (TOA) and time difference of arrival (TDOA) techniques where sub-nanosecond time resolutions need to be measured to provide reasonable location accuracy [28]–[30]. The requirement for high-speed sampling places demands on complexity, cost and power consumption. The latter being the main factor for sensor operational time, utilizing a battery source, which is a stringent requirement for a non-invasive large-scale WSN to be realized. Therefore, the use of high-speed sampling poses limitations on the potential scale of radiometric techniques. Sleep and shutdown modes can be incorporated, where certain sections of the sensor are deactivated to reduce the power consumption, between measurements. Whilst this does prolong battery life, the power consumption will likely still be excessive, and the cost of each sensor will still be high. A further limitation of TOA and TDOA technology is the requirement for coherent detection, and therefore, synchronization between sensor nodes.

Techniques have been described previously that alleviate the requirement of synchronization between sensor nodes

by using incoherent detection that relies on received signal strength (RSS) only [31]–[34], thereby alleviating the restrictions on scalability and allowing for inclusion of any number of nodes. Some RSS-based approaches also employ an envelope detector within the sensor to greatly reduce the required sample-rate [35], [36] whilst reducing the measurement accuracy. A technique involving the use of an op-amp based transistor-reset integrator (TRI) has been previously reported [37]–[41], which completely removes the requirement for high-speed sampling by integrating the radiometrically received envelope detected PD signal. Whilst this drastically reduces the power consumption of the sensor nodes, a potential drawback is that the output of the required envelope detector must respond linearly to the power in the received input signal in order to ensure that the integrator output can be related to the power, or energy, of the received signal for a suitable RSS-based location algorithm to be effective. This reduces the sensitivity of the sensor nodes since linear diode-based detectors are typically sensitive from –20 to –40 dBm [42], [43], whereas logarithmic responding detectors have dynamic ranges that extend below –55 dBm [44]. Therefore, it is advantageous to acquire the received signal via a high-speed ADC if a logarithmic power detector is used for extended dynamic range.

A fundamental issue with the use of high-speed sampling for the acquisition of PD sources is that the signal is a pulse with a duration of 100 ns to several microseconds, and an irregular time delay between events that is in the order of at least tens of microseconds. Therefore, continuously sampling is inefficient in terms of both power consumption and data processing. To increase the efficiency of an ADC-based radiometric PD sensor, the ADC should sample only when there is a signal present whilst still maintaining a sampling-rate capable of acquiring the received signal with reasonable accuracy.

Although modern, commercially available, high-speed pipelined ADCs are capable of sampling at rates of above 10 MSa/s, they cannot be triggered to sample instantaneously due to the propagation delay they require on startup, which is typically hundreds of nanoseconds to several milliseconds. Thus, attempting to initiate sampling from stand-by with such a device would result in the failure to capture a significant section, if not all, of the received signal during the acquisition process. Examples of commercial ADCs which feature high-speed turn on times are the AD9628 at 250 ns, the AD9644 at 5 μ s, and the AD9868 at 7.8 μ s. However, whilst the AD9628 turn on time seems particularly fast, it should be noted that the power consumption is 108 mW in stand-by mode. Most other commercially available ADCs have turn on times in the tens to hundreds of microseconds range, such as the MAX19507 at 15 μ s, the ADC3241 and ADC3441 at 35 μ s, and the ADS4249 at 50 μ s, and the AD9627 at 350 μ s. Furthermore, suitably fast architectures, such as pipelined ADCs which typically sample within a range of 10 – 200 MSa/s, require high complexity and power consumption that renders them incapable of operating for extensive periods of time from a single battery source. Successive approximation register (SAR) architectures are capable of triggering almost instantaneously upon command

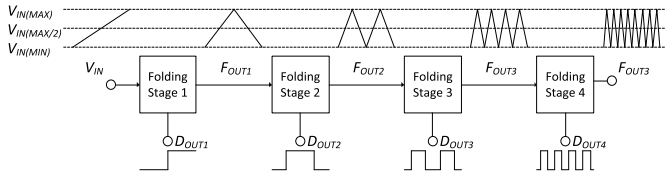


Fig. 1. Principle of folding ADC conversion to Gray-code.

Devices have been reported with sample-rates from 100 MSa/s to several GSa/s, which include both single channel [45]–[47] and multiple-channel, time-interleaved (TI), architectures [48]–[51]. However, commercially available SAR ADCs, such as the AD7626 (10 MSa/s), AD7720 (12.5 MSa/s) and LTC2387 (15 MSa/s), are limited to sample-rates at or below 15 MSa/s, with the exception of the ADS52J90 which is capable of 10-bit conversion at 100 MSa/s using a pair of time-interleaved ADCs. However, the analogue input range is limited to 800 mV, placing limitations on the dynamic range of the sensor. Furthermore, the ADS52J90 is a 16 channel device and requires an onboard phase-locked loop (PLL) in order to generate and distribute the required clock frequency for the TI-SAR architecture, requiring additional power consumption and circuit complexity [52]. The stand-by power dissipation alone is 291 mW. A further disadvantage of the SAR architecture is the requirement for a clock that is at least N times higher than the sample-rate [52], where N is resolution of the converter. This is usually implemented using an on-chip PLL, which requires additional power consumption and die area. Various energy efficient ADCs have been described utilizing a hybrid structure, such as the noise-shaping SAR [53], which combines conversion techniques from both the SAR and sigma-delta ADCs and the VCO-SAR [54], which employs a SAR for conversion of the most significant bits (MSBs) and a VCO-based Nyquist ADC for conversion of the least significant bits (LSBs). The combination of two different architectures provides a means of achieving both high resolution and low power consumption at high sample-rates. However, high resolution is not a critical parameter in this application.

An architecture, first developed in the early 50's [55], which provides bit-per-stage conversion is the serial ripple or folding ADC. Folding ADC architectures have been developed [56]–[58], which incorporate stages to provide a non-linear response to the linear input voltage range and a 1-bit Gray-code output per stage. Fig. 1 shows the principle of the Gray-code conversion using folding stages for 4-bit data conversion.

The basic conceptual architecture of a folding ADC has the input signal applied to a comparator, with a threshold level set to half the input range to provide the MSB (D_{OUT1}) and a folding stage with a gain of two. The output of the folding stage (F_{OUT1}) is then applied to a following comparator and folding stage to gain the next significant bit (D_{OUT2}). Each additionally connected comparator and folding stage provide one additional bit. A disadvantage of previously developed folding ADCs is that the sample rate is limited by the overall transition time of the number of stages connected in series. Hence, high conversion times require higher bias currents for

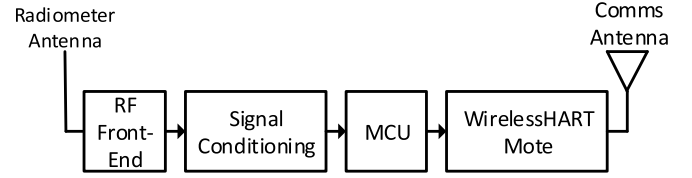


Fig. 2. Proposed wireless PD sensor node.

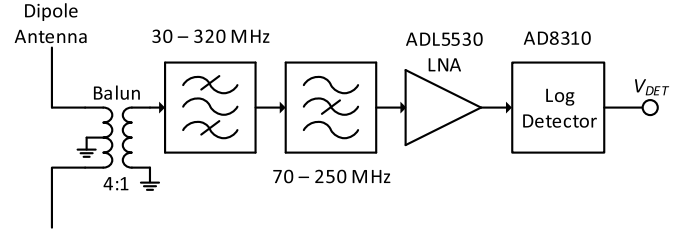


Fig. 3. RF front-end electronics.

each stage to achieve the required bandwidth, which places a limit on the number of stages and thus the resolution. This high conversion rate issue is addressed in [59] by including a separate sample-and-hold (S/H) section after each folding stage, but at the cost of additional circuitry and higher power consumption.

In this paper we present a radiometric PD sensor featuring a prototype low power discrete folding amplifier-based ADC which encompasses the S/H function within each folding amplifier stage, thus reducing the bandwidth constraint to a single stage. Each conversion stage dissipates minimal static current for the majority of the ADC operational time, only increasing for the intermittent signal pulses. Whilst traditional high speed ADC structures are not designed to sample instantaneously from an un-clocked mode, the proposed ADC is only clocked, and therefore only acquires data, when a signal is present at the input. The proposed prototype is, therefore, optimized for acquisition of radiometric PD signals which typically only occur in the 1st and 3rd quadrants of a 50 or 60 Hz power cycle, and provides higher efficiency and lower power consumption as compared to traditional ADC structures, which would require to continuous sampling in order to acquire radiometric PD.

II. WIRELESS HIGH-SPEED SAMPLING PD SENSOR

A. Radiometric Sensor Node Overview

The proposed wireless PD sensor node structure is shown in Fig. 2.

The radiometric PD signal is received via a wideband dipole antenna and applied to an RF front-end shown in Fig. 3. A 4:1 balun provides an increased antenna bandwidth by matching the ‘off resonant’ frequency response to 50 Ω , and the band-pass and band-stop filters create two effective measurement bands from 30–70 MHz and 250–320 MHz to remove possible interfering transmitted signals within the radiometric PD measurement band, such as FM, DAB and digital TV broadcasts. The filtered signal is then applied to an ADL5530 low-noise amplifier (LNA), which provides 10 dB of power gain to compensate for the gain of the antenna. Fig. 4 shows the overall response of the band-pass filters together with the LNA.

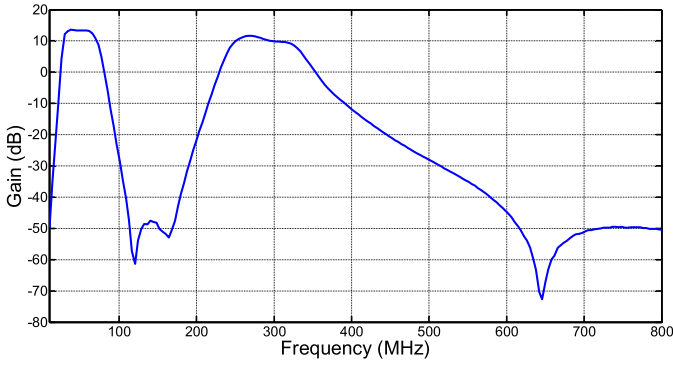


Fig. 4. RF filters and ADL5530 LNA overall response.

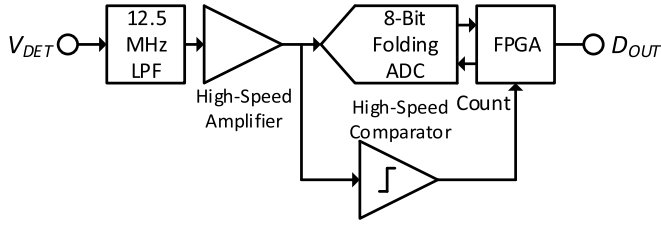


Fig. 5. Signal conditioning electronics.

The signal is then applied to an AD8310 logarithmic power detector, which has a bandwidth of DC – 440 MHz, with 95 dB dynamic range and a sensitivity of approximately –75 dBm. The AD8310 logarithmic power detector envelope detects the PD signal and produces an output voltage that is proportional to the logarithmic power in dBm. The detector output is then applied to the signal conditioning section, shown in Fig. 5.

The output of the detector is filtered by the 12.5 MHz low-pass filter (LPF) to ensure no aliasing occurs. The output of the LPF filter is scaled by a high-speed non-inverting amplifier to match the –10 dBm output voltage of the AD8310 (approximately 2 V) to the 3 V input range of the 8-bit folding ADC. The amplified signal is then simultaneously applied to both the input of the ADC and the high-speed comparator. The comparator is set to a voltage threshold level corresponding to a signal strength of –60 dBm at the input to the detector. When no signal is present the comparator outputs a logic low level, and the folding ADC is kept in a stand-by mode by holding the ADC clock inputs at a logic high level and the ADC input is set to 0 V, ensuring that the only power consumption is due to the active device quiescent currents. When the comparator receives a signal above the –60 dBm threshold it outputs a logic high level, and the ADC is clocked via the FPGA, sampling the received signal at a rate of 25 MSa/s. An FPGA is utilized for clocking and digital output acquisition of the ADC since it is capable of producing accurate bi-phase high speed clock signals with a minimum of components. Furthermore, the reprogrammable nature of the FPGA allowed for quick modifications to the digital logic during development. An internal mono-stable circuit within the FPGA is also triggered which sets the sampling duration to 1 μ s (25 samples) to ensure the sampling window is consistent, and is not affected by the oscillation to the comparator output when the signal is near the threshold level. The ADC parallel outputs are clocked into the FPGA

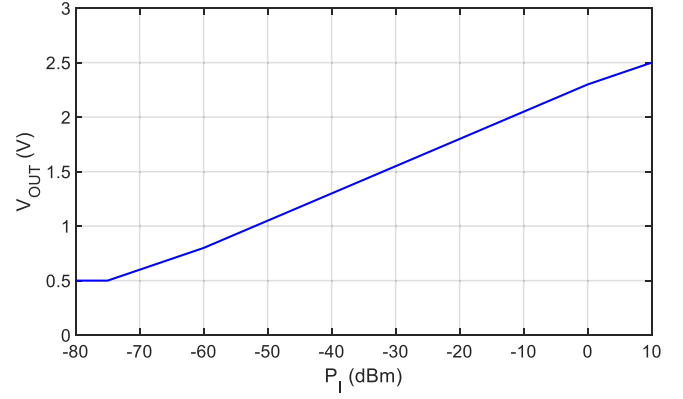


Fig. 6. AD8310 logarithmic power detector response.

where they are processed. At the end of the 1 μ s sampling window the internal mono-stable outputs a low-level signal and the ADC clock outputs are held at a constant high-level, placing the ADC back into standby. The FPGA then transmits the binary samples serially to a micro-controller (MCU) at a rate of 1 MHz. The MCU calculates the logarithmic power levels of each binary sample and then converts these values to linear powers and integrates them to determine the energy of the received PD signal. The signal energy is determined by summing the linear input powers calculated from the discrete samples as shown below. The logarithmic power value at the input of the AD8310 detector is determined as follows:

$$P_{I(\text{dBm})} = \frac{V_{DET}}{V_{SLOPE}} + P_{INTERCEPT} \quad (1)$$

where

$$P_{INTERCEPT} = P_{I(MID)} - \frac{V_{DET(MID)}}{V_{SLOPE}} \quad (2)$$

In the above two expressions, $P_{I(\text{dBm})}$, $P_{I(MID)}$ and $P_{INTERCEPT}$ are the input, detector mid-range input and detector intercept power values in dBm, respectively, and V_{DET} , $V_{DET(MID)}$ and V_{SLOPE} are the detector, mid-range and slope voltage outputs, respectively. $P_{INTERCEPT}$ is the theoretical input power for a detector output voltage of 0 V. Fig. 6 shows the response of the AD8310 output to a 100 MHz sinusoidal input signal from –80 dBm to +10 dBm.

The measured value for V_{SLOPE} and $P_{INTERCEPT}$ were 21.73 mV/dB and –92.72 dBm. Using these values, the linear power of the received signal for a given sample and the total energy can be respectively determined by the following expressions:

$$P_S(i) = \frac{\frac{V_{DET}}{A_V} + V_{DET(DC)}}{V_{SLOPE}} + P_{INTERCEPT} \quad (3)$$

$$E_S(i) = E_S(i-1) + \Delta T \sum_{i=1}^n 10^{\left(\frac{P_S(i)}{10}\right)} \quad (4)$$

where $P_S(i)$, $V_{DET(DC)}$ and A_V are, respectively, the power in dBm at sample i , the detector output voltage when no input signal is present (i.e., 0.5 V) and the total voltage gain before the detector, while $E_S(i)$, $E_S(i-1)$ and T are, respectively, the total energy at sample i , the total energy at the previous sample and the time between samples (i.e., 40 ns). By using (3), the input power of the received signal at the antenna can be

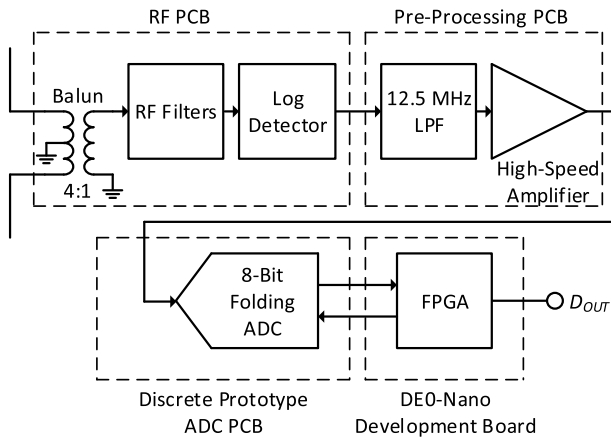


Fig. 7. Prototype PD sensor.

determined directly in dBm, and (4) is then used to integrate the discrete power values to determine the received energy of a single event.

The energy of each received signal is averaged by the MCU over a time duration of several seconds. This time duration is adequate to obtain accurate measurement since in a one second period several hundreds of events will have been received. This average is then transmitted to a central HUB, along with a count of the received PD pulses over the measurement duration, where a suitable RSS-based location algorithm is used to determine the location of the PD source [60], [61].

The prototype sensor, Fig. 7, contained 4 separate PCBs, all of which were constructed using discrete ‘off the shelf’ components, with the exception of the FPGA, implemented using a DE0-Nano development board. The ADL5530 LNA was not included since the strength of received PD source was high enough that a 10 dB power gain was not required for adequate testing.

The MCU and WirelessHART sections were also not included. Instead a TTL to USB converter was used to extract data from the FPGA output.

B. High-Speed Folding ADC Design

The prototype ADC structure, shown in Fig. 8, comprises a front-end sample-hold amplifier (SHA), seven series connected sample-hold folding amplifier (SHFA) stages, one comparator, a precision voltage reference unit, and a low power FPGA to provide the digital processing of the parallel data.

The SHFA stages provide a time offset parallel 8-bit digital Gray code output. Complementary non-overlapping clock signals, generated within the FPGA, are used to cycle each sample through the SHFAs. The precision reference provides the threshold levels for the SHFA, which is set at half the maximum input voltage. The first sample is acquired by the front-end SHA, which applies the signal to SHFA 1 during hold mode before acquiring the next sample. This process is repeated through each SHFA during the S/H transitions. The digital outputs of each SHFA are loaded into the FPGA on each clock cycle, where they are aligned into an 8-bit Gray-code word, since the LSB is sampled 8 clock cycles after the MSB due to the pipelined operation. The sample

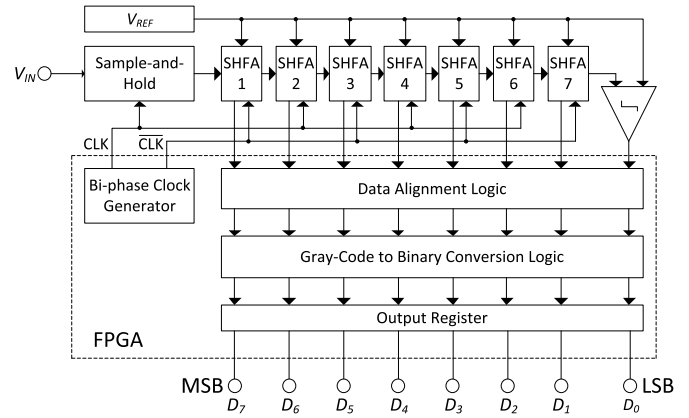


Fig. 8. High-speed folding ADC system structure.

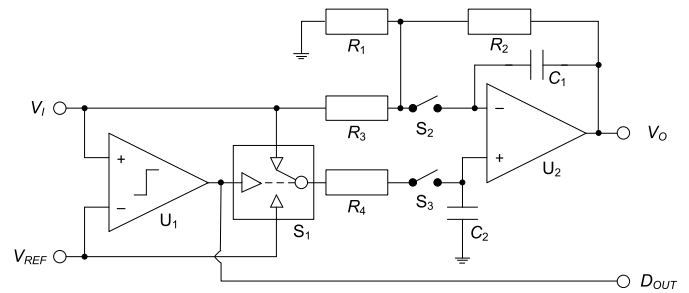


Fig. 9. Proposed sample-hold folding amplifier.

is then converted into a binary word and loaded into the output register. The operation of the proposed system does, as with traditional pipelined ADCs, results in latency due to the clock-per-bit conversion method, which is 4 clock cycles since the data alignment is performed both on rising and falling clock edges. However, this latency has no effect on the acquisition of received signals since the first 4 output codes can be ignored, and the actual pulse sample points are not affected. The latency, therefore, just results in a delay between input and output.

The proposed SHFA shown in Fig. 9 features low static quiescent current and circuit complexity. The architecture would be suitable for implementation on a monolithic IC with minimal space, higher precision and lower power consumption. In the implemented discrete version, each SHFA stage requires 2 mA of static current, which increases only when a pulse is received and processed; the resultant static power dissipation is only 49 mW for an 8-bit resolution even at a sample rate of 25 MSa/s. A dual single-pole single-throw (SPST) switch, S_2 and S_3 , provides the S/H function for the circuit, in an arrangement that also provides charge injection cancellation by utilizing the common-mode rejection of the op-amp to cancel the charge accumulated on C_1 and C_2 from the hold S/H switches [50]. The output voltage droop-rate is minimized also due to this arrangement, as it is only affected by the input offset current of the op-amp, rather than the input bias current which is cancelled at the output due to equal integration onto the hold capacitors, C_1 and C_2 .

For a V_{REF} below 1.5 V the circuit behaves as a non-inverting amplifier with a linear gain of two and a transfer

function given by

$$\frac{V_O}{V_I} = \left(1 + \frac{R_2}{(1 + j\omega R_2 C_1) R_1} \right) \varepsilon_{ANI} \quad (5)$$

where

$$\varepsilon_{ANI} = \frac{1}{(1 + j\omega R_4 C_2) \left(1 + \frac{1 + \frac{\omega}{\omega_C}}{A_{OL}} \left(1 + \frac{R_2}{(1 + j\omega R_2 C_1) R_1} \right) \right)} \quad (6)$$

In the above expressions, ω , ω_C , A_{OL} and ε_{ANI} are the input angular frequency, the compensation angular frequency, the open-loop gain and the non-inverting mode gain error, respectively. The above expressions are derived using standard nodal analysis and feedback theory.

For V_I above the comparator threshold, a logic high level is applied to the SPDT switch S_1 (see Fig. 9), thus configuring the circuit as an inverting amplifier with an offset gain of two and an output voltage given by

$$V_O = \left(\frac{R_2}{(1 + j\omega R_2 C_1) R_3} (V_I - V_{REF}) - \frac{R_2}{(1 + j\omega R_2 C_1) R_3} (V_I - V_{REF}) \right) \varepsilon_{AI} \quad (7)$$

where

$$\varepsilon_{AI} = \frac{1}{(1 + j\omega R_2 C_1) \left(1 + \frac{1 + \frac{\omega}{\omega_C}}{A_{OL}} \left(1 + \frac{R_1 R_2 + R_2 R_3}{R_1 R_3 (1 + j\omega R_2 C_1)} \right) \right)} \quad (8)$$

is the inverting mode gain error. The gain errors, given by (6) and (8), are due to the finite op-amp gain bandwidth, which reduces the gain of the SHFA below the ideal value of two as the input frequency increases, and is minimized by employing an op-amp with a suitably large gain-bandwidth. The S/H capacitors (C_1 and C_2) form poles in the transfer functions along with the gain setting resistors; the values are minimized to ensure a sufficient pass-band response for the sampling frequency, while minimizing hold mode droop. In order for a large-scale PD monitoring WSN to be feasible each sensor must be capable of running from a single battery source for a long period of time without requiring replacement, ideally for 12 months or longer. Techniques such as energy harvesting and solar power can be used to recharge the power source, however, the power consumption must still be minimized to ensure the power source is not completely depleted during operation, particularly during times when energy recovery is slower, for example; during winter where recharge times for solar power would be limited by the lack of sunlight. The cost of each sensor must also be minimized since a large number of sensors would be required to monitor a substation of moderate size. Therefore, the ADC must be as low cost as possible. Table-I shows the turn on times and stand-by currents for the proposed ADC and the most suitable commercially available equivalents.

The values for analogue power consumption are listed separately since the digital interfacing circuitry can consume a significant portion of the operational power, although this digital power also includes circuitry fundamental to the operation of the ADC, such as clock generation and distribution.

TABLE I
TURN-ON TIME AND POWER COMPARISON BETWEEN
PROPOSED ADC AND COMMERCIAL EQUIVALENTS

Part No.	Turn-on Time (μ s)	Analogue Power (mW)	Operational Power (mW)	Stand-by Power (mW)
ADS52J90	> 0.015	998	<1385	291
AD9628	0.35	142.2	172.8	105
AD9644	5	315	423	85
Proposed ADC	>0.02	95	116	56

Usually, however, the analogue power consumption is dominant. Furthermore, the stand-by power, which is the main parameter of interest here, is mainly dissipated due to the higher bias currents required for the analogue circuitry as compared to the static currents consumed by the digital circuitry, which is minor in stand-by mode, since most of the digital power dissipation is a consequence of switching currents during normal operation. The power consumption of the proposed ADC is approximately 56 mW whilst no signal is applied and no clock signals are present, compared to standby powers of 291 mW for the ADS52J90, 105 mW for the AD9628 and 85 mW for the AD9644. It should also be noted that supply voltage of the commercial ADCs listed is 1.8 V compared to 3.3 V for the proposed ADC. Since the proposed ADC is constructed using rail-to-rail devices the supply rail could be reduced to further decrease the power consumption at the cost of a reduction in dynamic range. As stated in I, for sensors that employ high-speed sampling, the overall power consumption is generally dominated by the ADC. Therefore, in reference to Table-I, the power consumption of a sensor employing the commercial types listed would be significantly higher than that of a sensor using the proposed ADC. Furthermore, the turn-on time of the two pipelined ADCs listed would pose significant problems to the accuracy of the sensor due to the short duration of the received pulse. Sensors which alleviate the requirement for high-speed sampling through analogue signal processing, such as that described in [41], are limited by the dynamic range of the linear detectors used.

III. RESULTS

A. High-Speed Folding ADC Evaluation

A discrete 8-bit prototype ADC was constructed using standard high-speed PCB construction and components selected for low power operation. Commercial bipolar op-amps and comparators were selected for the SFHA stages as they generally feature lower power consumption than commercial CMOS equivalents. Whilst the op-amps adopted within the prototype are not optimized for use in a high-speed ADC, such as those typically employed in commercially available ADCs, they are still capable of operating at a high enough sample-rate in order to validate the principle of the proposed design. The dimensions of the board were minimized so that it could be interfaced directly to a Terasic DE0-Nano FPGA development board. The measured power consumption of the prototype ADC was 56 mW with no signal applied to the input. To validate the linearity of the ADC the differential non-linearity (DNL) and integral non-linearity (INL) were

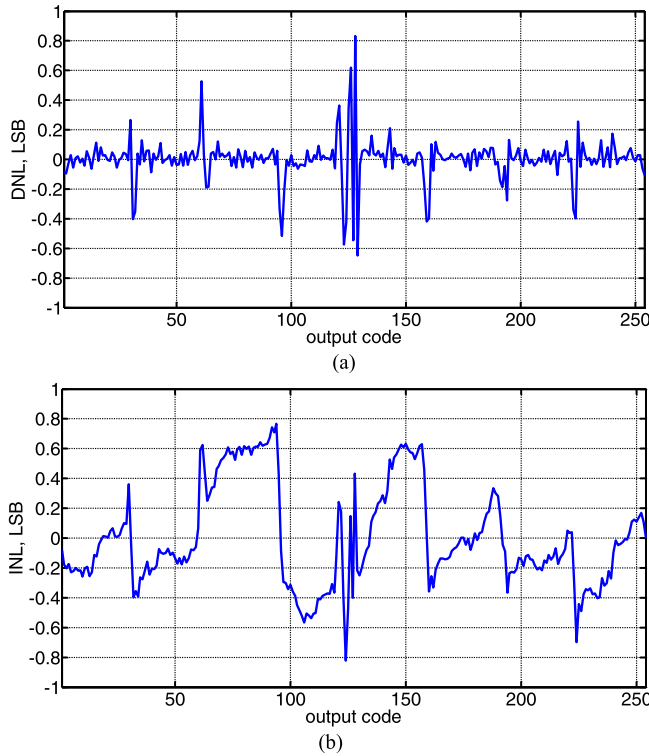


Fig. 10. ADC measurement results for (a) DNL and (b) INL.

measured, shown in Fig. 10, using a 0.01 % linear 1 kHz triangular signal. DNL is used to ascertain the voltage width, or window, of each resolution step across the ADC input range. INL is the integral of the DNL, which shows the deviation from the ideal linear response of the converter. A DNL of minus one LSB translates to a missing code at that particular output code, and conversely, a DNL of plus one LSB translates to a code which has twice the voltage resolution of an ideal code. Therefore, a DNL and INL within 1 LSB is preferred.

The measured DNL ranges between +0.8 and −0.7 LSB, showing no missing codes, and the INL between +0.8 and −0.8 LSB. The regular intervals of positive and negative peaks in Fig. 10a show where errors are introduced as the input voltage of each folding stage crosses the threshold. This is primarily due to the offset-voltage and switching accuracy of the high-speed comparator used in each SHFA structure, with the largest error occurring at the midpoint due to the switching accuracy of the MSB stage dominating the error. This results in the largest error being at the input range midpoint. However, the linearity is comparable with commercial ICs, such as the AD9057-40 and TLC5510, while no calibration or correction was performed to the prototype to improve the linearity. The use of an FPGA allows for possible correction in the digital domain to improve the DNL and INL. However, the linearity is still high enough to attain accurate PD signal measurement, and the use of the AD8310 alleviates the requirement for absolute accuracy since the received signal range is logarithmically compressed before the ADC.

To measure the frequency and noise performance of the ADC, a 3 Vpp sinusoidal signal with a 1.5 V offset was applied to the input of the ADC at a frequency of approximately 850 kHz via a 6th order band-pass filter with an identical

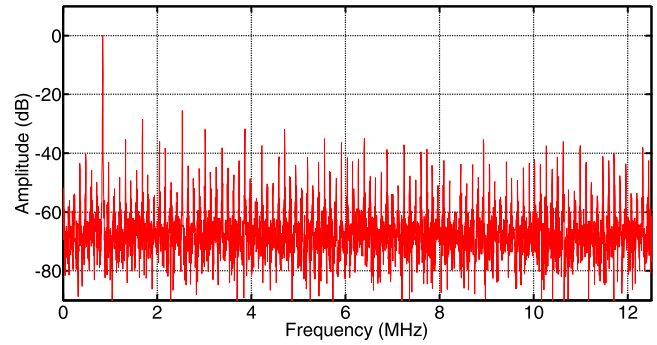


Fig. 11. ADC FFT results for an 850 kHz sinusoidal input signal.

center frequency. A total of 8192 output codes were then recorded from the ADC, and an FFT was performed on the measured data, shown in Fig. 11. The calculated FFT values were used to determine the signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR) and total harmonic distortion (THD) for the ADC. The regular spurs shown in the FFT plot are the combined result of comparator offset, single-ended operation, and the SHFAs which produce spurs at regular harmonics due to the doubling effect of the folding operation. The SNR, SFDR and THD were measured respectively equal to 22.2 dB, 29 dB and −24 dBc. Whilst these specifications are below those commercially available ADCs are capable of, they are not critical in this application, since the logarithmic compression of the signal at the input of the ADC means that low level signals, including the noise floor of the RF front-end, are effectively amplified to a level much greater than the noise floor of the ADC. Therefore, the requirements on the SNR of the ADC are heavily alleviated. Furthermore, since no frequency information is extracted from the samples acquired by the ADC, the SFDR and THD do not have a significant effect on the measurement accuracy of the sensor, as shown below. The dynamic performance of the proposed ADC could be drastically improved with the inclusion of correction circuitry, which, by increasing the accuracy of the SHFAs outputs would reduce the harmonic spurs they produce.

B. Partial Discharge Measurement Accuracy

The employment of a logarithmic responding power detector provides the additional benefit of effectively linearizing the envelope of the received signal, since the received radiometric PD signal can be modelled by the following expression [9]:

$$V_{PD}(t) = V_{pk} e^{-\frac{t}{\tau}} \cos \omega t \quad (9)$$

where $V_{PD}(t)$, V_{pk} , and τ are, respectively, the amplitude of the received PD signal at time t , the peak value of this signal, and the time constant of the signal. The logarithmic envelope detection of (9) yields the following expression:

$$V_{DET}(t) = \log(V_{pk}) - \frac{t}{\tau} \propto P_{Ipk(dBm)} - \frac{t}{\tau} \quad (10)$$

where $P_{Ipk(dBm)}$ is the received peak power in dBm. Therefore, a logarithmic responding detector produces an approximately linear decaying signal, proportional to the logarithmic power of the received PD signal, thus, reducing the complexity of the received signal, and minimizing the demand on the ADC performance. Fig. 12 illustrates this point by

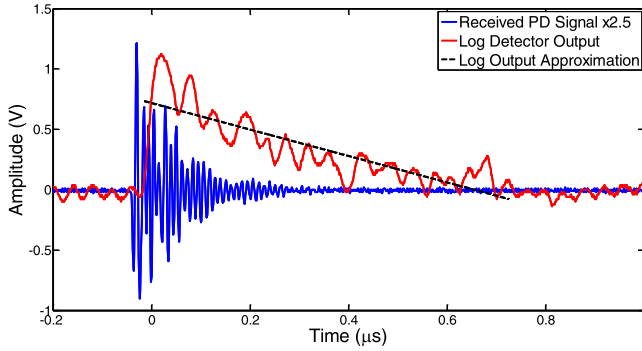


Fig. 12. Emulated PD signal and AD8310 detector output [62].

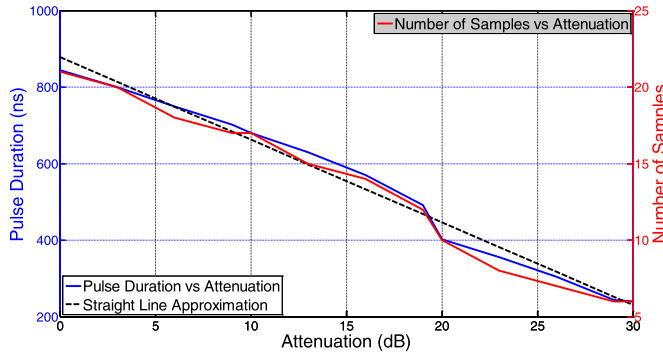


Fig. 13. Received PD pulse width vs attenuation.

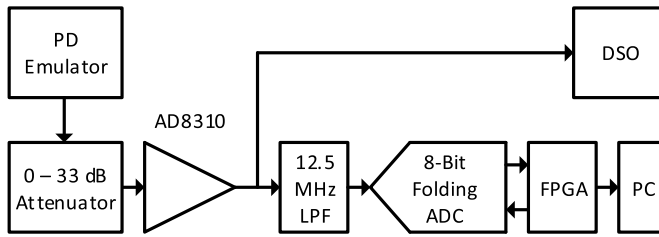
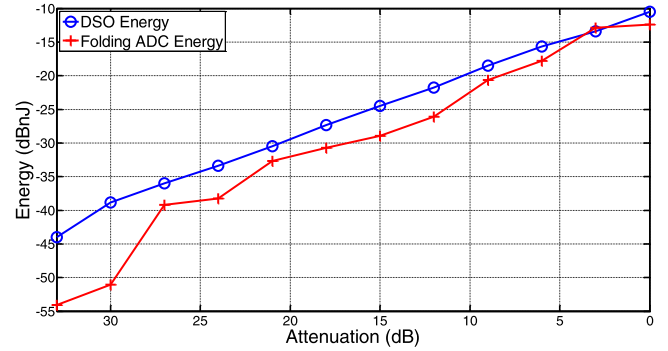


Fig. 14. Proposed PD sensor node test setup.

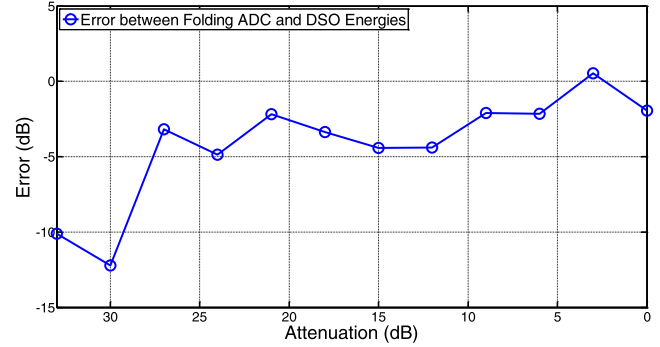
showing the plot of an emulated radiometric PD signal along with the logarithmic detected output from the AD8310. It is clear that the AD8310 output is of the form of a linearly decaying ramp as shown from the straight-line approximation.

A potential issue with this approach is the reduced time duration of the detected pulse envelope due to the attenuation of the received pulse in respect to the noise floor of the AD8310. As the transmitted electromagnetic signal is attenuated, the duration of the detected pulse begins to decrease since the sensitivity of the AD8310 is limited to -75 dBm. Therefore, any portion of the received signal below this level is lost, resulting in a narrower detected signal, and loss of dynamic range. This issue is illustrated in Fig. 13, which shows the pulse duration of the emulated PD signal for given attenuations along with number of samples assuming a sample rate of 25 MSa/s.

To ascertain the viability of the proposed folding ADC-based system for radiometric PD measurement, the RF front-end and folding ADC sections of the sensor were configured in the test setup shown in Fig. 14. An artificial PD source was provided by an emulator which produces a $1 \mu\text{s}$



(a)



(b)

Fig. 15. Prototype sensor node measurement results. Prototype sensor node vs. DSO (a) measured energy and (b) error.

decaying oscillation at a frequency of 70 MHz. The output of the emulator was connected to the AD8310 via an attenuator to simulate increasing distance, from 3 – 33 dB in increments of 3 dB. The RF filters and LNA were omitted since the source was narrowband. The output of the AD8310 was applied to the ADC via a 12.5 MHz anti-aliasing filter, and to the input of a digital storage oscilloscope (DSO). Data from the ADC was acquired by the FPGA before transmission to a PC via a TTL-to-USB interface, which avoided the requirement for the MCU or wirelessHART mote. The energy of the signals measured via the DSO and ADC were determined using (3) and (4) for each step increase in attenuation. The energy determined from the DSO was assumed as the actual energy of the received PD signal, since the DSO has a sample rate of 1 GSa/s, thus ensuring high accuracy. Fig. 15a displays the energies derived from the DSO and prototype sensor node, while Fig. 15b shows the error values between measurements.

The energy calculated from the DSO measurements shows a constant linear decay on a logarithmic scale, with very little deviation, which is expected as the test signal is directly coupled to the sensor, avoiding any errors due to reflections or scattering. The absolute error between the energy calculated from the prototype ADC and that calculated from the DSO is within 2.2 dB for an attenuation of 0 to 9 dB, after which the error increases to a maximum of 5 dB up to an attenuation of 28 dB. Beyond this, the error is above 10 dB, with errors of 12.22 and 10.11 dB at attenuations of 30 and 33 dB respectively. The main source of this error is due to the reducing pulse width of the AD8310 detector output, since the pulse width is 820 ns at an attenuation of 0 dB, referring to Fig. 13, compared to 220 ns at 33 dB.

The turn-on time of the proposed ADC has very little to no contribution to the error of the measured received signal, since it is primarily dependent on the combined propagation delay of the high-speed comparator, and the digital clock and activation circuitry within the FPGA. The total time between a received signal being present at the input of the comparator to the initiation of sampling is below 20 ns. Therefore, since the turn on time is a factor of two below the time between samples, the error is dominated by the sample time.

IV. CONCLUSION

A sensor based on a pipelined folding ADC structure is proposed and is optimized for efficient low power sampling of radiometric PD signals. The discrete prototype is capable of sampling at 25 MSa/s whilst the power consumption is substantially lower than that of similar commercially available ICs. The power consumption could be further decreased by reducing the supply voltage of the ADC. Since the output range of the AD8310 logarithmic detector is limited to approximately 2 V the voltage supply of the ADC could be reduced to at least 2.2 V, decreasing the total power consumption to 37 mW. The preliminary tests performed show that the proposed system has an accuracy within 5 dB up to an attenuation of 28 dB. Whilst this error is significant, it is still possible to perform relatively accurate location estimation if the error is identical for all sensors or appropriate compensation is introduced into the PD location algorithm. Furthermore, the errors could be significantly lowered by integrating the ADC onto monolithic silicon, which would greatly reduce the parasitic elements that are present in the prototype circuit, and would allow for the addition of calibration and correction circuitry to increase the accuracy of the ADC. The sensor error could also be significantly reduced by increasing the sample-rate, and therefore, the number of samples per received pulse. In any case, the work presented here show that the proposed system is a viable technique for low-power radiometric PD detection and measurement, and is suitable for use in a large-scale PD monitoring WSN.

REFERENCES

- [1] *High Voltage Test Techniques—Partial Discharge Measurements*, IEC Standard 60270, 2000.
- [2] R. Bartnikas and E. J. McMahon, *Engineering Dielectrics*, 1st ed. Baltimore, MD, USA: American Society for Testing and Materials, 1979, pp. 134–135.
- [3] Y. Z. Adzis W. A. Izzati, and Z. Adzis, “Modeling of partial discharge mechanisms in solid dielectric material,” *Int. J. Eng. Innov. Tech.*, vol. 1, no. 4, pp. 315–320, 2012.
- [4] A. T. Short, *Electric Power Distribution Handbook*, 2nd ed. Boca Raton, FL, USA: CRC Press, 2014, pp. 118–119.
- [5] M. H. Ryan, *High Voltage Engineering and Testing*, 2nd ed. Xi’an, China: IEE, 2001, pp. 328–329.
- [6] *Guide for Electrical Partial Discharge Measurements in Compliance, Standard IEC 60270*, Technical Brochure 366, CIGRE WG D1.33, Electra, 2008, vol. 60, no. 241.
- [7] G. C. Stone, “Partial discharge diagnostics and electrical equipment insulation condition assessment,” *IEEE Trans. Dielectr. Electr. Insul.*, vol. 12, no. 5, pp. 891–903, Oct. 2005.
- [8] E. Jennings and A. Collinson, “A partial discharge monitor for the measurement of partial discharges in a high voltage plant by the transient Earth voltage technique,” in *Proc. Int. Conf. Partial Discharge*, 1993, pp. 90–91.
- [9] Y. Liu, W. Zhou, P. Li, S. Yang, and Y. Tian, “An ultrahigh frequency partial discharge signal de-noising method based on a generalized S-transform and module time-frequency matrix,” *Sensors*, vol. 16, no. 6, p. 941, 2016.
- [10] Q. Chen, X. Gong, W. Gao, F. Li, and K. Tan, “The UHF method for measurement of partial discharge in oil-impregnated insulation,” in *Proc. 7th Int. Conf. Properties Appl. Dielectr. Mater.*, 2003, pp. 451–454.
- [11] S. Tenbohlen, D. Denissov, S. Hoek, and S. M. Markalous, “Partial discharge measurement in the ultra high frequency (UHF) range,” *IEEE Trans. Dielectr. Electr. Insul.*, vol. 15, no. 6, pp. 1544–1552, Dec. 2008.
- [12] T. Hoshino, K. Kato, N. Hayakawa, and H. Okubo, “A novel technique for detecting electromagnetic wave caused by partial discharge in GIS,” *IEEE Trans. Power Del.*, vol. 16, no. 4, pp. 545–551, 2001.
- [13] I. E. Portugues and P. J. Moore, “Study of propagation effects of wideband radiated RF signals from PD activity,” in *Proc. IEEE Power Eng. Soc. Gen. Meeting (IMTC)*, 2006, pp. 1–6.
- [14] G. Robles, J. M. Martínez-Tarifa, M. V. Rojas-Moreno, R. Albarracín, and J. Ardila-Rey, “Antenna selection and frequency response study for UHF detection of partial discharges,” in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (IMTC)*, May 2012, pp. 1–4.
- [15] G. Robles, M. Sánchez-Fernández, R. A. Sánchez, M. V. Rojas-Moreno, E. Rajo-Iglesias, and J. M. Martínez-Tarifa, “Antenna parametrization for the detection of partial discharges,” *IEEE Trans. Instrum. Meas.*, vol. 62, no. 5, pp. 932–941, May 2013.
- [16] R. Albarracín, J. Ardila-Rey, and A. Mas’ud, “On the use of monopole antennas for determining the effect of the enclosure of a power transformer tank in partial discharges electromagnetic propagation,” *Sensors*, vol. 16, no. 2, p. 148, 2016.
- [17] A. Jabar *et al.*, “Frequency spectrum analysis of radiated partial discharge signals,” in *Proc. IET Eur. Electromag. Symp. (EUROOEM)*, 2016, pp. 1–2.
- [18] R. Yao, Y. Zhang, G. Si, Y. Yuan, and Q. Xie, “Measurement and analysis of partial discharge on floating electrode defect in GIS,” in *Proc. IEEE Int. Conf. High Voltage Eng. Appl. (ICHVE)*, Sep. 2016, pp. 1–4.
- [19] A. Jaber *et al.*, “Diagnostic potential of free-space radiometric partial discharge measurements,” in *Proc. 32nd Gen. Assem. Sci. Symp. Int. Union Radio Sci. (URSI GASS)*, Aug. 2017, pp. 1–4.
- [20] A. A. Jaber *et al.*, “Calibration of free-space radiometric partial discharge measurements,” *IEEE Trans. Dielectr. Electr. Insul.*, vol. 24, no. 5, pp. 3004–3014, Oct. 2017.
- [21] M. Siegel and S. Tenbohlen, “Comparison between electrical and UHF PD measurement concerning calibration and sensitivity for power transformers,” in *Proc. Int. Conf. Condition Monit. Diagnosis (CMD)*, 2006, pp. 5–8.
- [22] P. Kakeeto, M. Judd, J. Pearson, and D. Templeton, “Experimental investigation of positional accuracy for UHF partial discharge location,” in *Proc. Int. Conf. Condition Monit. Diagnosis*, 2008, pp. 1070–1073.
- [23] R. Candela, A. Di Stefano, G. Fiscelli, S. F. Bononi, and L. De Rai, “A novel partial discharge detection system based on wireless technology,” in *Proc. AEIT Annu. Conf.*, Oct. 2013, pp. 1–6.
- [24] P. J. Moore, I. Portugues, and I. A. Glover, “A nonintrusive partial discharge measurement system based on RF technology,” in *Proc. IEEE Power Eng. Soc. Gen. Meeting*, Jul. 2003, pp. 628–633.
- [25] A. J. Reid, M. D. Judd, R. A. Fouracre, B. G. Stewart, and D. M. Hepburn, “Simultaneous measurement of partial discharges using IEC60270 and radio-frequency techniques,” *IEEE Trans. Dielectr. Electr. Insul.*, vol. 18, no. 2, pp. 444–455, Apr. 2011.
- [26] Y. Tian, B. Qi, R. Zhuo, M. Fu, and C. Li, “Locating partial discharge source occurring on transformer bushing by using the improved TDOA method,” in *Proc. Int. Conf. Condition Monit. Diagnosis (CMD)*, Sep. 2016, pp. 144–147.
- [27] H. H. Sinaga, B. T. Phung, and T. R. Blackburn, “Partial discharge localization in transformers using UHF detection method,” *IEEE Trans. Dielectr. Electr. Insul.*, vol. 19, no. 6, pp. 1891–1900, Dec. 2012.
- [28] G. Robles, J. Fresno, M. Sánchez-Fernández, and J. Martínez-Tarifa, “Antenna deployment for the localization of partial discharges in open-air substations,” *Sensors*, vol. 16, no. 4, pp. 1–11, 2016.
- [29] P. J. Moore, I. E. Portugues, and I. A. Glover, “Radiometric location of partial discharge sources on energized high-voltage plant,” *IEEE Trans. Power Del.*, vol. 20, no. 3, pp. 2264–2272, Jul. 2005.
- [30] G. Robles, J. Fresno, and J. Martínez-Tarifa, “Separation of radio-frequency sources and localization of partial discharges in noisy environments,” *Sensors*, vol. 15, no. 5, pp. 9882–9898, 2015.
- [31] J. M. R. de Souza Neto *et al.*, “Plausibility of incoherent detection for radiometric monitoring of insulation integrity in HV substations,” in *Proc. Loughborough Antennas Propag. Conf.*, 2013, pp. 494–499.

- [32] W. Huang, C. Zhang, M. Dong, and J. Zhou, "Research on partial discharge monitoring system of switchgear based on wireless distributed TEV sensors," in *Proc. 1st Int. Conf. Electr. Mater. Power Equip. (ICEMPE)*, May 2017, pp. 647–650.
- [33] E. T. Iorkyase, C. Tachtatzis, R. C. Atkinson, and I. A. Glover, "Localisation of partial discharge sources using radio fingerprinting technique," in *Proc. Loughborough Antennas Propag. Conf. (LAPC)*, Nov. 2015, pp. 1–5.
- [34] W. Zhang, K. Bi, Z. Li, L. Luo, G. Sheng, and X. Jiang, "RSSI fingerprinting-based UHF partial discharge localization technology," in *Proc. IEEE PES Asia-Pacific Power Energy Eng. Conf. (APPEEC)*, Oct. 2016, pp. 1364–1367.
- [35] P. Baker, M. Judd, and S. J. McArthur, "A frequency-based RF partial discharge detector for low-power wireless sensing," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 17, no. 1, pp. 133–140, Feb. 2010.
- [36] J. M. R. de Souza Neto, J. S. D. Rocha Neto, E. C. T. Macedo, I. A. Glover, and M. D. Judd, "An envelope detector as a trading cost technique for radiometric partial discharge detection," in *Proc. IEEE Int. Instrum. Meas. Technol. Conf. (IMTC)*, May 2014, pp. 1584–1589.
- [37] Y. Zhang *et al.*, "Radiometer monitoring system for partial discharge detection in substation," in *Proc. 1st URSI Atlantic Radio Sci. Conf.*, May 2015, p. 1.
- [38] Y. Zhang *et al.*, "Radiometric wireless sensor network monitoring of partial discharge sources in electrical substations," *Int. J. Distrib. Sensor Netw.*, vol. 11, no. 9, Sep. 2015, Art. no. 438302.
- [39] D. W. Upton *et al.*, "Wireless sensor network for radiometric detection and assessment of partial discharge in HV equipment," in *Proc. 32nd Gen. Assem. Sci. Symp. Int. Union Radio Sci. (URSI GASS)*, Aug. 2017, pp. 1–4.
- [40] D. W. Upton *et al.*, "Wireless sensor network for radiometric detection and assessment of partial discharge in high-voltage equipment," *Radio Sci.*, vol. 53, no. 3, pp. 357–364, Mar. 2018.
- [41] D. W. Upton *et al.*, "Low power radiometric partial discharge sensor using composite transistor-reset integrator," *IEEE Trans. Dielectr. Electr. Insul.*, vol. 25, no. 3, pp. 984–992, Jun. 2018.
- [42] *Square Law and Linear Detection*, Agilent Technol., Santa Clara, CA, USA, Appl. Note 986, pp. 1–4.
- [43] *All Schottky Diodes Are Zero Bias Detectors*, Agilent Technol., Santa Clara, CA, USA, Appl. Note 988, pp. 1–4.
- [44] Y. Toh, "Detecting fast RF bursts using log amps," *Analog Dialogue*, vol. 36, no. 5, pp. 1–3, 2002.
- [45] Y. Liang, R. Ding, and Z. Zhu, "A 9.1ENOB 200 MS/s asynchronous SAR ADC with hybrid single-ended/differential DAC in 55-nm CMOS for image sensing signals," *IEEE Sensors J.*, vol. 18, no. 17, pp. 7130–7140, Sep. 2018.
- [46] Q. Fan and J. Chen, "A 1-GS/s 8-bit 12.01-fJ/conv.-step two-step SAR ADC in 28-nm FDSOI technology," *IEEE Solid-State Circuits Lett.*, vol. 2, no. 9, pp. 99–102, Sep. 2019.
- [47] S. Lee, A. P. Chandrakasan, and H.-S. Lee, "A 1 GS/s 10b 18.9 mW time-interleaved SAR ADC with background timing skew calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2846–2856, Dec. 2014.
- [48] L. Qiu, K. Tang, Y. Zheng, L. Siek, Y. Zhu, and U. Seng-Pan, "A 16-mW 1-GS/s with 49.6-dB SNDR TI-SAR ADC for software-defined radio in 65-nm CMOS," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 3, pp. 572–583, Mar. 2018.
- [49] C.-Y. Lin, Y.-H. Wei, and T.-C. Lee, "A 10-bit 2.6-GS/s time-interleaved SAR ADC with a digital-mixing timing-skew calibration technique," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1508–1517, May 2018.
- [50] Z. Ni, Y. Chen, F. Ye, and J. Ren, "A 7.8 fJ/conversion-step 9-bit 400-MS/s single-channel SAR ADC with fast control logic," *Microelectron. J.*, vol. 84, pp. 59–66, Feb. 2019.
- [51] B. T. Reyes, L. Biolato, A. C. Galetto, L. Passetti, F. Solis, and M. R. Hueda, "An energy-efficient hierarchical architecture for time-interleaved SAR ADC," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 6, pp. 2064–2076, Jun. 2019.
- [52] S. A. Zahrai and M. Onabajo, "Review of analog-to-digital conversion characteristics and design considerations for the creation of power-efficient hybrid data converters," *J. Low Power Electron.*, vol. 8, no. 12, pp. 1–29, 2018.
- [53] S. Li, B. Qiao, M. Gandara, D. Z. Pan, and N. Sun, "A 13-ENOB second-order noise-shaping SAR ADC realizing optimized NTF zeros using the error-feedback structure," *IEEE J. Solid-State Circuits*, vol. 53, no. 12, pp. 3484–3496, Dec. 2018.
- [54] Y. Xie, Y. Liang, M. Liu, S. Liu, and Z. Zhu, "A 10-bit 5 MS/s VCO-SAR ADC in 0.18- μ m CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 66, no. 1, pp. 26–30, Jan. 2019.
- [55] B. D. Smith, "An unusual electronic analog-digital conversion method," *IRE Trans. Instrum.*, vol. 5, pp. 155–160, Jun. 1956.
- [56] C. M. Moreland, "An 8b 150 MSample/s serial ADC," in *Proc. IEEE Solid-State Circ. Conf.*, vol. 1995, pp. 272–273.
- [57] C. Moreland, F. Murden, M. Elliott, J. Young, M. Hensley, and R. Stop, "A 14-bit 100-Msample/s subranging ADC," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1791–1798, Dec. 2000.
- [58] H. Dine and F. Maloberti, "An 8-bit current mode ripple folding A/D converter," in *Proc. Int. Symp. Circuits Syst. (ISCAS)*, 2003, pp. 981–984.
- [59] W. Kester, *The Data Conversion Handbook*, 1st ed. Amsterdam, The Netherlands: Elsevier, 2005, pp. 513–533.
- [60] Y. Liu, Z. Yang, X. Wang, and L. Jian, "Location, localization, and localizability," *J. Comput. Sci. Technol.*, vol. 25, no. 2, pp. 274–297, Mar. 2010.
- [61] Y. Xu, J. Zhou, and P. Zhang, "RSS-based source localization when path-loss model parameters are unknown," *IEEE Commun. Lett.*, vol. 18, no. 6, pp. 1055–1058, Jun. 2014.
- [62] D. W. Upton *et al.*, "Low power high-speed folding ADC based partial discharge sensor for wireless fault detection in substations," in *Proc. 2nd URSI Atlantic Radio Sci. Meeting (AT-RASC)*, May 2018, pp. 1–4.



David W. Upton was born in Oldham, U.K., in 1983. He received the B.Eng. (Hons.) and Ph.D. degrees in electronic engineering from the University of Huddersfield, U.K., in 2013 and 2018, respectively. From 2016 to 2018, he was a Research Assistant with the School of Computing and Engineering, University of Huddersfield. He is currently a Research Engineer with the Swedish Institute of Space Physics, Kiruna, Sweden. His research interests include high performance high-voltage switch-mode power supplies, wireless partial discharge sensors, analog signal processing for pulsed signals, precision and high speed analog electronics, and integrated analog design. Dr. Upton is a member of the IET. He was a recipient of the IET Gerald David Memorial Prize for an outstanding mature student, in 2013. He was awarded the Vice-Chancellor scholarship by the University of Huddersfield for his Ph.D. degree.



Richard P. Haigh received the B.Eng. (Hons.) degree in electronic engineering from the University of Huddersfield, U.K., in 2014, and the M.Sc. degree by research in electronic engineering from the University of Huddersfield, in 2018. From 2014 to 2016, he was a Research Associate on a Knowledge Transfer Partnership between the University of Huddersfield and Kromek, U.K., working on developing technology enhancements for portable radiation detectors. He is currently working for Kromek Ltd., U.K., with the focus on developing low power signal processing methods for state-of-the-art scintillators used for gamma and neutron radiation detection.



Peter J. Mather received the B.Eng. (Hons.) degree in electrical and electronic engineering and the Ph.D. degree from the University of Huddersfield, U.K., in 1990 and 1995, respectively. After completing postdoctoral research in mixed signal test techniques, he was a Senior Mixed Signal IC Design Engineer. He is currently a Senior Lecturer with the University of Huddersfield, U.K. His research interests include coding scheme implementation and non-linear-based measurement. Dr. Mather is also a member of the IET and a Fellow of the HEA.



Pavlos I. Lazaridis (Senior Member, IEEE) received the Electrical Engineering degree from the Aristotle University of Thessaloniki, Greece, in 1990, the M.Sc. degree in electronics from the Université Pierre et Marie Curie, Paris, France, in 1992, and the Ph.D. degree in electronics and telecommunications from the Ecole Nationale Supérieure des Télécommunications (ENST) and Paris 6, Paris, in 1996. From 1991 to 1996, he was involved with research on semiconductor lasers, wave propagation, and nonlinear phenomena in optical fibers for the Centre National d'Etudes des Télécommunications (CNET) and teaching at the ENST. In 1997, he became the Head of the Antennas and Propagation Laboratory, Télédiffusion de France/France Télécom Research Center (TDF-C2R Metz), where he was involved with research on antennas and radio coverage for cellular mobile systems (GSM), Digital Audio Broadcasting (DAB), and Digital Video Broadcasting-Terrestrial (DVB-T). From 1998 to 2002, he was with the European Patent Office, Rijswijk, The Netherlands, as a Senior Examiner in the field of Electronics and Telecommunications. From 2002 to 2014, he was involved with teaching and research at the Alexander Technological Educational Institute of Thessaloniki, Greece, and Brunel University, West London. He is currently a Professor of electronic and electrical engineering, University of Huddersfield, U.K. He is leading the EU Horizon 2020 projects ITN-MOTOR5G and RISE-RECOMBINE for the University of Huddersfield. He is a member of the IET.



Keyur K. Mistry received the B.Tech. degree in electronics and telecommunication engineering from NMIMS University, Mumbai, India, in 2015, and the master's degree in electronics and communications engineering from the University of Huddersfield, U.K., in 2016. He is currently pursuing the Ph.D. degree in electronics and communications engineering. His research interests include antenna design and measurements, wireless partial discharge sensors, UHD TV broadcasting, and developing optimization

algorithms. He was awarded the Vice-Chancellor Scholarship by the University of Huddersfield for his Ph.D. degree. He received the First Prize for best design for proof of concept design competition organized by ICE/Honeybot in 2016.



Zaharias D. Zaharis (Senior Member, IEEE) received the B.Sc. degree in physics, the M.Sc. degree in electronics, the Ph.D. degree in antennas and propagation modeling for mobile communications, and the Diploma degree in electrical and computer engineering from the Aristotle University of Thessaloniki, Thessaloniki, Greece, in 1987, 1994, 2000, and 2011, respectively. From 2002 to 2013, he was with the administration of the telecommunications network, Aristotle University of Thessaloniki, where he has been with the Department of Electrical and Computer Engineering since 2013. His current research interests include design and optimization of antennas and microwave circuits, signal processing on smart antennas, development of evolutionary optimization algorithms, and neural networks. Dr. Zaharis is a member of the Technical Chamber of Greece. He is currently serving as an Associate Editor for IEEE Access.



Christos Tachtatzis (Senior Member, IEEE) received the B.Eng. (Hons.) degree in communication systems engineering from the University of Portsmouth, U.K., in 2001, and the M.Sc. and Ph.D. degrees in communications, control and digital signal processing and electronic and electrical engineering from the University of Strathclyde, Glasgow, U.K., in 2002 and 2008 respectively. From 2008 to 2016, he held a Postdoctoral Researcher positions at the University of Strathclyde, and the Letterkenny Institute of Technology, Republic of Ireland. He is currently a Senior Lecturer with the Department of Electronic and Electrical Engineering, University of Strathclyde. His research interests cover communication systems, the Internet of Things, artificial intelligence, and machine learning with over 80 technical publications. Dr. Tachtatzis was appointed as a Chancellor's Fellow at the University of Strathclyde, in 2016. He is a member of the Institute of Engineering and Technology of the United Kingdom



Robert C. Atkinson (Senior Member, IEEE) is currently a Senior Lecturer with the Department of Electronic and Electrical Engineering, University of Strathclyde. He has applied a range of signal processing and machine learning algorithms to a range of fields as diverse as: radiolocation of partial discharge, intrusion detection systems, 4G handover optimization, game theory applied to radio access network selection, prognostics for gearboxes, condition-based maintenance of water pumps, the Internet of Things, smart cities, smart buildings, and image analysis for pharmaceutical crystals. He is the author of over 80 scientific articles, published in internationally recognized conferences and journals. He is a member of the IET.