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Generating Closed 2-Cell Embeddings in the Torus and the Projective Plane

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Abstract. If a graph G is embedded in a manifold M such that all faces are cells bounded by simple closed curves we say that this is a closed 2-cell embedding of G in M. We show how to generate the 2-cell embeddings in the projective plane from two minimal graphs and the 2-cell embeddings in the torus from six minimal graphs by vertex splitting and face splitting.

1. Introduction

There are numerous theorems that provide methods for the recursive generation of various 2-cell complexes and their associated graphs. (See, for example, [1], [2], [3].) Perhaps the best known and most useful is the theorem of Steinitz [4], that the planar 3-connected graphs (which are the graphs of 3-dimensional convex polytopes) can be generated from the graph of the tetrahedron by face splitting.

In this paper we consider graphs that are embedded in the projective plane and the torus. In our work we will be dealing with the embedding as well as the graphs. Since many graphs have more than one embedding in these manifolds it is an entirely different matter to generate all embeddings than to generate all graphs of a given family.

We shall say that a graph embedded in a 2-manifold is a closed 2-*cell embedding* provided each face of the embedding is a 2-cell whose boundary is a simple closed curve. (In what follows we shall omit the word "closed.") In this paper we show how to construct recursively the 2-cell embeddings of graphs in the projective plane and in the torus. This recursive construction will generate the embeddings from a finite set of graphs using two operations: face splitting and vertex splitting. These two operations are illustrated in Fig. 1.

We shall prove that using our two operations all 2-cell embeddings in the projective plane can be generated from the graphs in Fig. 2 and that all 2-cell embeddings in the torus can be generated from the graphs in Fig. 7.

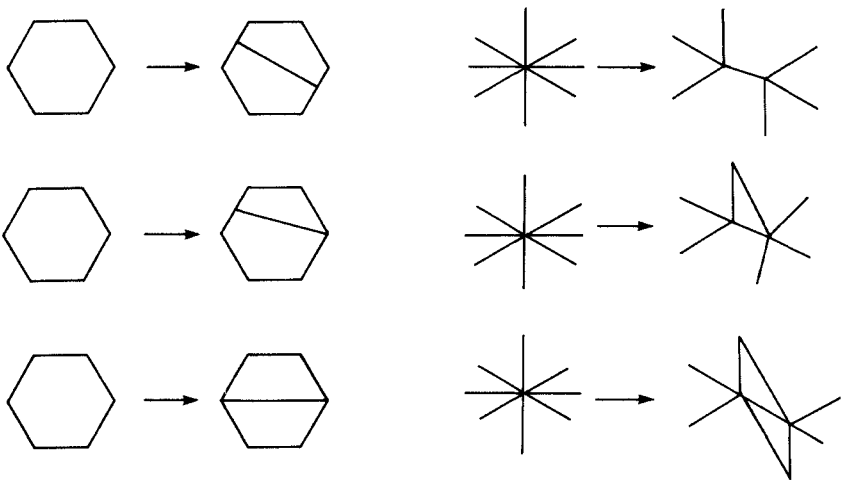


Fig. 1.

From now on, whenever we say *manifold* we shall mean a compact 2-manifold. If a circuit in a graph embedded in a manifold bounds a cell that is a subset of the manifold we say that the circuit *bounds*. A circuit that does not bound will be called *nonplanar*. A circuit that bounds will be called *planar*.

A circuit with n edges is said to have *length* n and is called an *n-circuit*. Circuits and paths will sometimes be denoted by listing their vertices, thus the path abc is the path with an edge from a to b and an edge from b to c. Similarly, edges will be denoted using the symbols for their endpoints, thus the edge from a to b is denoted ab. Polygons will be denoted using this notation. In the case of quadrilaterals the notation $abcd$ denotes a quadrilateral where the upper left vertex is a, the upper right vertex is b, the lower right vertex is c, and the lower left vertex is d.

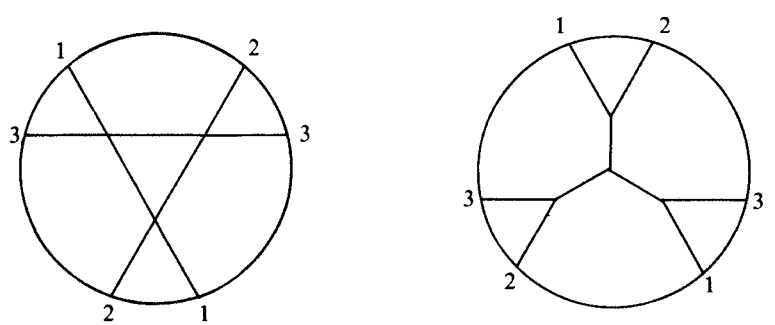


Fig. 2.

The graphs we consider are what are usually called multigraphs, this is, they can have multiple edges but not loops.

If G is a graph 2-cell embedded in a manifold M let p_i be the number of i-sided faces of G and let v_i be the number of i-valent vertices. A well-known consequence of Euler's formula is that

$$\sum (4-i)(p_i+v_i) = \begin{cases} 0 & \text{if } M \text{ is a torus,} \\ 4 & \text{if } M \text{ is the projective plane.} \end{cases}$$

From this we conclude

Lemma 1. *A 2-cell embedding in the projective plane without digons (that is, 2-sided faces) or 2-valent vertices has either a 3-valent vertex or a 3-sided face. A 2-cell embedding in the torus without digons or 2-valent vertices has a 3-valent vertex, a 3-sided face or else all vertices are 4-valent and all faces are 4-sided.*

2. Generating Operations

We shall use two operations to construct our graphs: face splitting and vertex splitting. *Face splitting* consists of adding a new edge across a face of the graph. There are three ways of doing this depending on how many new vertices are created by the splitting. *Vertex splitting* is the dual of face splitting. It consists of choosing two sets A_1 and A_2 of neighbors of the vertex v such $A_1 \cup A_2$ contains all neighbors of v and $A_1 \cap A_2$ contains at most the first and last vertices of A_1 and A_2. Then replacing v by two vertices each joined to the vertices in one of the sets and also joined to each other. There are three types of vertex splittings depending on how many new (3-sided) faces are created by the splitting. Figure 1 shows the three types of each operation. The inverses of these operations will be called *removing edges* and *shrinking edges*, respectively. Notice that if an edge meeting a 3-valent vertex is removed, the vertex disappears, that is, the other two edges meeting the vertex are coalesced into one edge. Also if an edge lying on a 3-sided face is shrunk then the other two edges of the face are coalesced into a single edge.

If G is a graph that is 2-celled embedded in a manifold we shall say that an edge is *removable* provided removing the edge produces a graph that is 2-cell embedded. One impediment to removability is the creation of faces that are not cells. This would occur only when the union of the two faces containing the edge is not a cell, that is, they have a multiply connected union.

Another impediment to removing an edge is that it might create a loop. This would happen when one vertex of the edge is 3-valent such that the other two edges meeting that vertex constitute a multiple edge. If the loop produced does not bound a face then the faces on both sides of the loop are not cells. Thus, one of these faces is not a cell when we return the edge to the graph. We conclude that one face meeting the loop was a cell and thus the original graph has a digon. It follows that if we have a graph without digons then the first impediment is the only impediment to removing an edge.

We say that an edge e is *shrinkable* provided shrinking the edge produces a graph that is 2-cell embedded. Shrinking an edge could produce a loop if the edge is one of a multiple edge, so this is one impediment to shrinking. Shrinking an edge could produce a face that is not a cell only if the edge has both endpoints on a face but the edge does not lie on the face. This is thus another impediment to shrinking. Actually, our first impediment is a special case of the second if our graph has no digons. In this case e is one of a multiple edge. Let another edge of the multiple edge by e'. Any face containing e' cannot contain e because that face would be a digon, thus the endpoints of e lie on a face that does not contain e.

If G is a graph that is 2-cell embedded in a manifold and if no edge is shrinkable or removable we say that the graph is *minimal* (with respect to these two operations). Since edge shrinking is the dual operation to edge removal, the dual of a minimal 2-cell embedding is minimal.

In order to find out how to generate a family of embeddings with the two operations face splitting and vertex splitting it suffices to find all embeddings in that family which are minimal. It follows that from these graphs all of the others can be generated.

There are two easy observations that we can make about minimal 2-cell embedded graphs in a manifold. If our graph has a digon we can remove one of its two edges unless this produces a loop. Let the two vertices of the digon be x and y and let its two edges be a and b. To produce a loop one vertex, say x, must be 3-valent. Let the other edge meeting x be c. Note that the edge e has vertices x and y. The edges b and c lie on a face. Since this is a 2-cell embedding, the face is a digon. Similarly, a and c bound a digon. The union of these three digons is a sphere, thus if we are not on a sphere we can remove an edge of any digon. We conclude that minimal 2-cell embeddings in the torus and projective plane do not have digons.

By duality, minimal 2-cell embeddings in the torus and projective plane do not have 2-valent vertices.

If graphs G and H are embedded in manifolds we say that the embeddings are *isomorphic* provided there is a one-to-one function taking the vertices, edges and faces of G onto the vertices, edges, and faces, respectively, of H such that incidences are preserved. Clearly, if the embeddings are isomorphic then the graphs are isomorphic. It is also easily seen that a graph can have isomorphic embeddings in two different manifolds. A graph consisting of a single edge, for example, is embeddable in all manifolds and all of these embeddings are isomorphic.

If G and H are graphs embedded in a manifold we say that G is a *refinement* of H provided an embedding isomorphic to G can be obtained from H by adding vertices to relative interior points of edges.

We say that an embedding of G in a manifold is a *planar* embedding provided it is isomorphic to an embedding of G in the plane.

Lemma 2. *If G is embedded in a manifold such that every circuit bounds then the embedding is planar.*

Proof. Suppose G is a counterexample with a minimum number of edges. If G has no circuits then it is a forrest and the embeddings clearly must be planar. If G has circuits, let C be a circuit bounding a maximal cell A. If there is an edge of G inside A then we remove all vertices and edges inside A. This produces a graph G' whose embedding is planar. In an isomorphic embedding of G' in the plane, the circuit C bounds a face. In this embedding we can return the removed vertices and edges giving a planar embedding isomorphic to G.

If there are no edges of G inside A we shrink the circuit to a single vertex V. The maximality of C guarantees that no loops will be created, thus this new graph G'' has a planar embedding. In an isomorphic embedding of G'' in the plane we may replace v by a small circuit and obtain an embedding in the plane isomorphic to the embedding of G. □

3. Representations of Graphs

A graph in the projective plane can be represented as a graph drawn on a disc with diametrically opposite points identified. A graph on the torus can be represented as a graph drawn on a rectangle with the top and bottom sides identified and the left and right sides identified. Many of our constructions will make use of these representations so it is necessary to establish some facts about them.

In the representation of a graph on the torus some edges may have points on them which are not vertices and which lie on a side of the rectangle. In this case we say that the edge *crosses* a side of the rectangle. We say that a representation of the graph is *simple* if no edge of the graph crosses a side of the rectangle more than once, and no vertex of the graph lies on a side of the rectangle. We say that the representation of the graph is *regular* provided the sides of the rectangle consist of edges of the graph. (In this case the corners necessarily will be a vertex of the graph.) A *semiregular representation* is a representation of the graph drawn on a parallelogram such that the left and right sides are identified in the usual way, the top and bottom are identified so that the upper left corner is identified with a relative interior point of the bottom side, top and bottom of the parallelogram consist of edges of the graph, and no edges of the graph cross sides of the parallelogram.

The following series of lemmas leads to the theorem that every graph in the torus has a simple representation. The proof of the following lemma is rather tedious but routine. We shall sketch its proof.

Lemma 3. *Every graph G embedded in the torus has a semiregular representation provided it is not a planar embedding.*

Sketch of Proof. We cut along a nonplanar circuit to get an annulus. In the resulting graph on the annulus we start at a vertex on one bounding circuit and make a cut to the other bounding circuit, cutting across faces and ending at a vertex on the other bounding circuit. The two cuts produce the parallelogram and the embedding is semiregular. □

We define a representation of a graph in the torus to be a *straight representation* provided all edges that do not cross sides are segments, and each edge that crosses n edges is the union of $n+1$ segments.

Lemma 4. *Every nonplanar embedding of a graph G in the torus in which no double edge bounds a cell has a straight semiregular representation.*

Proof. We begin with a semiregular representation of G in a parallelogram *abcd*. If we ignore the identifications made on the boundary of the parallelogram, then we have a graph G' without multiple edges embedded in the parallelogram. We prove by induction that this embedding can be realized with straight edges. If there are no vertices of G' inside *abcd* then all edges are chords of *abcd* and can be represented by segments (note that if two segments were to intersect then the original edges also would have intersected). Proceeding by induction, suppose there are vertices inside *abcd*. In this case we shall look for an edge that we can shrink to produce a graph without multiple edges and fewer interior vertices.

We can shrink an edge e lying inside *abcd* unless doing so produces a multiple edge, which happens when e belongs to a 3-circuit that bounds but does not bound a face. If such a 3-circuit exists we choose one bounding a minimal cell A. There must be at least one edge inside this circuit and that edge cannot belong to a 3-circuit that does not bound a face, by the minimality of A. It follows that if there are interior vertices then there are edges meeting interior vertices that we may shrink.

We shrink such an edge and by induction, this embedding in the parallelogram may be realized with straight edges. We now perform the vertex splitting to a vertex v that is the inverse to the edge shrinking. In splitting v, we replace v by two vertices that are close enough to v such that we may use segments for the new edges, thus producing our straight representation. □

Lemma 5. *Every graph G embedded in the torus such that multiple edges do not bound cells has a straight simple representation.*

Proof. If the embedding is planar then the theorem is obvious. If the embedding is nonplanar we take a straight semiregular representation of G in a parallelogram *abcd*. Assume that the vertex a is directly above a relative interior point a' of the bottom side.

We cut with a line parallel to aa' and one perpendicular to aa' so that no vertex lies on these lines. Rearranging the four resulting pieces in the obvious way yields a straight simple representation. □

Theorem 1. *Every graph G in the torus has a simple representation.*

Proof. The previous lemma takes care of the case where multiple edges do not bound cells. If multiple edges bound cells we prove the theorem by induction on the number of edges. The previous lemma serves to start the induction. If there exist multiple edges bounding cells we choose a double edge bounding a

minimal cell A. If the cell is a face we remove one edge of the multiple edge (leaving endpoints). We take a simple representation of the resulting graph and return the removed edge, placing it close enough to the other edge of the multiple edge so that it crosses each side at most once.

Suppose A is not a face. Let e be an edge in the interior of A. By the minimality of A, e cannot belong to a multiple edge, thus shrinking e to a vertex v produces a graph G'. By induction we may take a simple representation of G' and then split the vertex v to produce G. By splitting v so that the two vertices that replace v are very close to v, we obtain a simple representation. □

The next lemma allows us to make certain assumptions about the way some subgraphs of minimal graphs are embedded in a simple representation.

Let G be the complete graph on five vertices v, a, b, c, d, such that a, b, c, d are in cyclic order around v, the circuits vac and vbd do not bound and the circuits vab, vbc, vcd, and vda bound.

Lemma 6. *If a graph H in the torus contains a refinement of G (with the above-mentioned embedding) then there is a simple representation of H such that the path corresponding to ac cuts the top and bottom sides but not the left and right sides, while the path corresponding to bd cuts the left and right sides but not the top and bottom sides.*

Proof. If in the proof of Theorem 1 we make our first cut (as in Lemma 3) along circuit adc and the second cut along path abc we can obtain the required embedding. This is illustrated in Fig. 3. □

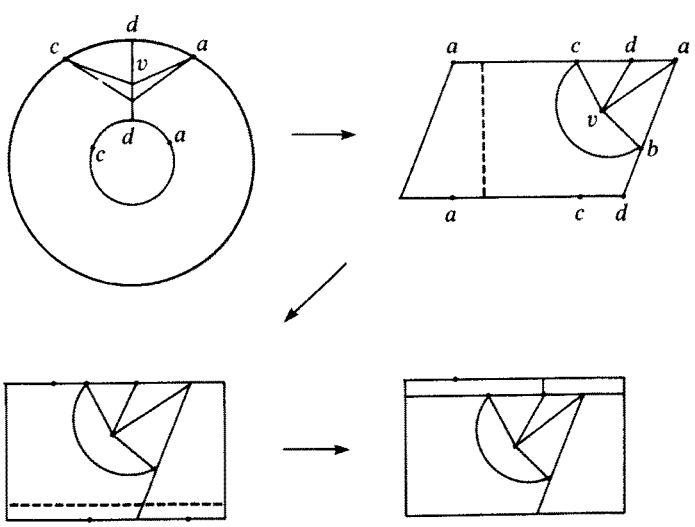


Fig. 3.

Throughout this paper, when we have a nonplanar circuit, or several of them, it will be useful to assume that they cross the edges of the rectangle of a representation in a certain way. Lemma 6 can be used to justify these assumptions.

We shall define a *simple representation* of a graph in the projective plane to be a representation in the disk with diametrically opposite points identified such that no vertex is on the bounding circle and no edge cuts the circle more than once. With arguments similar to the arguments for the torus one can prove.

Theorem 2. *Every graph in the projective plane has a simple representation.*

Implicit in the rest of this paper will be the assumption that we are dealing with simple representations.

4. Minimal Graphs in the Projective Plane

If G is a graph embedded in a manifold then by the *incidence graph* of G we mean a graph $I(G)$ whose vertex set consists of the vertices of G together with vertices corresponding to the faces of G, one vertex for each face, with two vertices joined if and only if one is a vertex v of G and the other is a vertex corresponding to a face containing v. There is a natural embedding of $I(G)$ in the manifold with the vertices corresponding to faces lying in their corresponding faces. When the embedding of G is a 2-cell embedding each edge will belong to exactly two faces and thus the incidence graph will have only 4-sided faces.

Any 4-circuit in $I(G)$ that does not bound a face of $I(G)$ will be called a *nonfacial* 4-circuit.

Lemma 7. *If G is a minimal graph in a manifold other than the sphere and if $e_1 = xv$ is an edge of $I(G)$ where x is a vertex of G and if $e = xy$ is an edge of G lying on the face of G corresponding to v then e_1 lies in a nonfacial 4-circuit that contains the vertices x and y.*

Proof. Let e_1 be an edge of $I(G)$ joining a vertex x of G to a vertex v of $I(G)$ corresponding to a face F_1 of G. Let e be an edge of F_1 meeting x. Let F_2 be the other face of G containing e and let F_3 be a face of G distinct from F_1 and F_2 meeting e at vertices x and y. The face F_3 exists because e is not shrinkable. Let u and w be the vertices of $I(G)$ corresponding to F_2 and F_3 respectively. If each of the 4-circuits *vxuy*, *vxwy*, and *xuyw* bound then the union of the cells they bound is a sphere or else the cell spanned by one of them lies in the cell bounded by another. In this case *vxwy* must bound the cell containing one of the other cells and is thus our desired circuit.

In the case that not all circuits bound, we have at least two of them do not, for any two bounding implies the third bounds. Since *vxuy* bounds, *vxwy* does not and is the desired circuit. □

Lemma 8. *If G is a minimal graph with respect to edge shrinking and edge removal then no nonfacial 4-circuit in $I(G)$ bounds.*

Proof. Suppose there were such a 4-circuit. Let C be one that is minimal with respect to the number of vertices of $I(G)$ in the cell A that it bounds. Since $I(G)$ is bipartite, and clearly has no multiple edges, no two vertices of C are joined by edges not lying on C. Thus, there must be a vertex v of $I(G)$ in A. Any edge of $I(G)$ meeting v will lie in a nonfacial 4-circuit C'. By the minimality if C, there must be a vertex of C' that is not in A. It follows that the portion of C' that lies in A consists of two edges that meet v and also meet two nonconsecutive vertices of C. This breaks A up into two regions bounded by two 4-circuits each consisting of the two edges meeting v and two edges of C. By the minimality of C, these two 4-circuits bound faces of $I(G)$. This however gives us a 2-valent vertex in $I(G)$, namely v, which implies that G has either a 2-valent vertex or a digon, which is a contradiction. □

Corollary 1. *In a minimal graph, double edges do not bound cells.*

Theorem 3. *If G is a minimal 2-cell embedded graph in the projective plane then it is one of the two graphs in Fig. 2.*

Proof. By Lemma 1 there is either a 3-valent vertex or a 3-sided face of G. Suppose there is a 3-valent vertex v. Corresponding to this 3-valent vertex will be three faces of $I(G)$ (see Fig. 4).

By Lemma 7, each edge $e = vw$ of $I(G)$ lies on a 4-circuit that consists of two edges of one of the faces F of $I(G)$ that meets v, another edge of $I(G)$ meeting v and one more edge. (Here the vertex w plays the role of the vertex v in Lemma 7. The edge of G across F plays the role of e_1 in Lemma 7.) Furthermore, these 4-circuits must be nonplanar by Lemma 8. It follows that we have an edge e in $I(G)$ as indicated in Fig. 5. Since there is such a circuit for each edge of $I(G)$ meeting v, it follows that $I(G)$ contains the graph in Fig. 6. Since all planar 4-circuits of $I(G)$ must bound faces of $I(G)$ the graph in Fig. 6 is $I(G)$. Since the vertex v in Fig. 6 corresponds to a vertex of G, the graph in Fig. 6 is the incidence graph of graph 1 in Fig. 2.

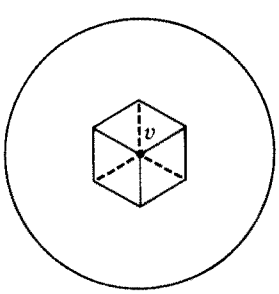
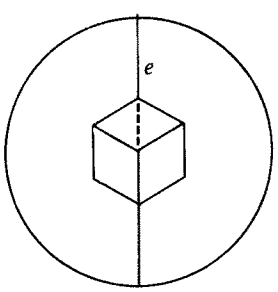


Fig. 4.



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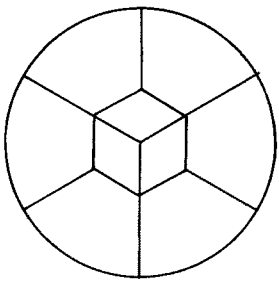


Fig. 6.

In the case that G contains a 3-sided face, the dual G^* has a 3-valent vertex and is minimal. Thus in this case G is the dual of graph 1 in Fig. 2 and is graph 2 in Fig. 2. □

5. Minimal Graphs in the Torus

From here on all graphs will be embedded in the torus.

Lemma 9. *A minimal graph cannot have a 3-sided face with a 3-valent vertex.*

Proof. Let the 3-sided face F have vertices x, y, and z with z 3-valent. The only way a face F' meeting F on xy can have a multiply connected union with F is if $F' \cap F = xy \cup \{z\}$. But if z is in this intersection then so is the edge xz because z is 3-valent. Since F' cannot have a multiply connected union with F, the edge xy is removable and the graph is not minimal. □

Corollary 2. *If G is a minimal graph then $I(G)$ does not have two 3-valent vertices joined by an edge.*

Lemma 10. *Let G be a minimal 2-cell embedding in the torus and let C be a 6-circuit in $I(G)$ bounding a cell A. Then in $I(G)$ either C has a diagonal lying in A or there is exactly one vertex of $I(G)$ but no diagonal of C in A.*

Proof. Suppose that the circuit C is a counterexample bounding a minimal cell A. Suppose e is an edge of $I(G)$ in A with neither of its vertices on C. (We shall show that this is impossible.) The edge e lies on a nonplanar 4-circuit C'. The other two vertices of C' will lie on C, and since $I(G)$ is bipartite they are either consecutive on C or are separated by two vertices on C. If they are consecutive then the circuit C' lies in A (remember $I(G)$ has no multiple edges) which is a contradiction.

If they are separated by two vertices on C, let these vertices be x and y, and let the vertices of e be z and w, so that C' is $xzwy$. The path $xzwy$ together with the two paths on C joining x and y form two planar 6-circuits which by the minimality of C have either exactly one edge or exactly one vertex of $I(G)$ inside

of them. Let the cells bounded by these two circuits be A' and A''. Now the vertices z and w can be at most 4-valent, yet they cannot both be 3-valent. If one of z and w has two edges lying in one region, say A', then A' does not have exactly one edge or exactly one vertex inside it. This means that on one side of the path $xzwy$ say, in A', there must emanate an edge from each of the vertices z and w. It follows that exactly one vertex of $I(G)$ lies inside A' and is thus joined to z and w. This contradicts the fact that $I(G)$ is bipartite.

We now have that any edge of $I(G)$ lying in A has at least one vertex on C. If such an edge had both vertices on C then it would be a diagonal of C breaking A up into two 4-sided faces of $I(G)$ and we are done. If exactly one vertex lies on C let v be the other vertex. Two other edges must emanate from v and must meet vertices of C. Since $I(G)$ is bipartite, this can be done in only one way breaking A up into three 4-sided faces of $I(G)$, and again we are done. □

Theorem 4. *The minimal graphs in the torus are the graphs in Fig. 7.*

Proof. Let G be a minimal graph. We treat several cases.

Case I. G has a 3-valent vertex v. In this case $I(G)$ has three faces surrounding v as in Fig. 8. The edges e' and e'' belong to nonplanar 4-circuits. Each such 4-circuit must use two edges of a face meeting v, another edge meeting v and a fourth edge (Lemma 7). By Lemma 6 we may assume that these edges are as in Fig. 9.

By the same argument there is an edge in $I(G)$ from vertex d to vertex c (see Fig. 10). The face of the graph in Fig. 10 that this edge crosses is a 10-gon with two pairs of edges identified. Since this edge fc misses all vertices that are identified, all ways of drawing it are combinatorially the same (see Fig. 10). Thus $I(G)$ contains the graph in Fig. 11. In this graph the faces labeled F and F' are bounded by 6-circuits, thus each face either has a diagonal in $I(G)$ or has a 3-valent vertex of $I(G)$ inside of it.

Once these diagonals and 3-valent vertices are added all faces will be 4-sided thus we will have drawn the entire graph $I(G)$.

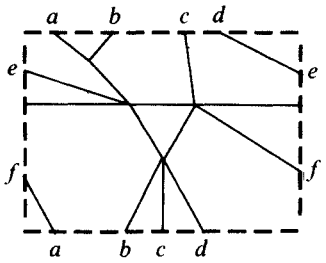
Each face has three ways of having diagonals drawn and two ways of adding 3-valent vertices. It turns out that whenever a diagonal is added to one of these faces we will arrive at a graph $I(G)$ for which the graph G is not a 2-cell embedding. The reader can quickly check this.

The four ways of adding 3-valent vertices to F and F' yield two nonisomorphic incidence graphs shown in Fig. 12. These are the incidence graphs for graphs 1 and 2 in Fig. 7.

Case II. G has a 3-sided face. This is the dual of Case I. It is easily seen that an incidence graph for a graph G is also an incidence graph for its dual. G therefore has as its incidence graph one of the two graphs in Fig. 12. In this case the graph G is either graph 3 or 4 in Fig. 7.

Case III. Every vertex of G is 4-valent and every face is 4-sided.

Let F be a face with vertices a, b, c, and d. Since ab is not removable there



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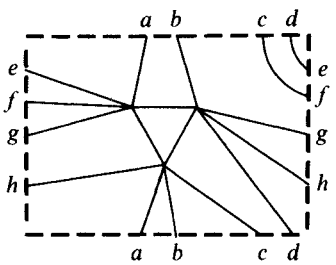

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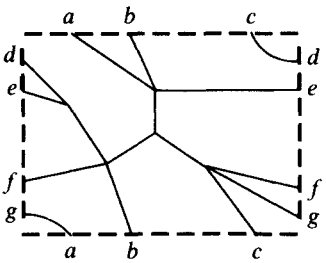

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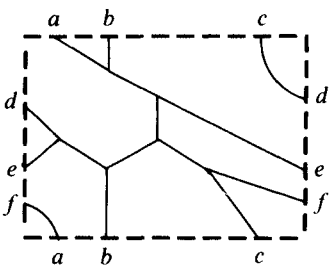

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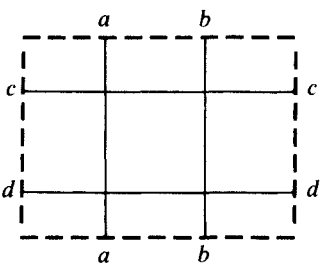

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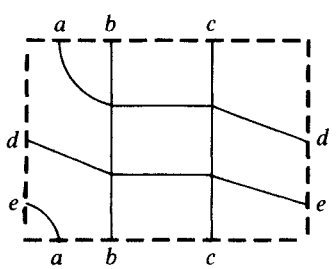

6

Fig. 7.

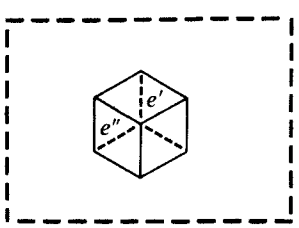

Fig. 8.

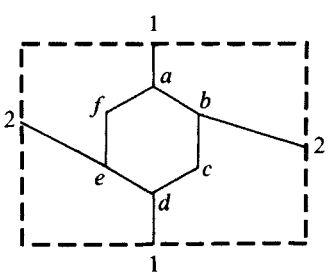

Fig. 9.

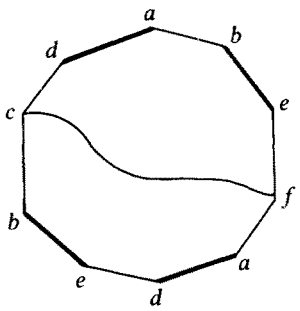

Fig. 10.

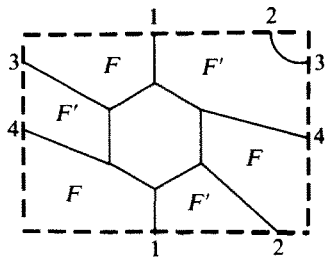

Fig. 11.

is a face F' sharing edge ab with F and meeting F at d, c or on edge dc. We treat several subcases.

(i) There is a face $abxd$ (or $abxc$) for some $x \neq b, c, d$. If the circuit adx is planar then ad is removable. If not we have the configuration in Fig. 13. Now the face $abxd$ meets itself at a. Now since F' is 4-sided it follows that an edge e of G joins a to d or c. Using the same argument for the edge ad there is an edge e' joining a to b or c. Since a is 4-valent e and e' will lie two nonadjacent 4-sided faces meeting a, thus $e' \neq e$.

(ii) Two edges not on F join a to one of b, c, or d. This case is ruled out because the double edge would have to bound the face that meets F at the vertex a and does not contain the edges ab and ad of F. This means that G is not minimal.

We may now assume that no double edges will join two vertices of F unless one of them is an edge of F. We can also conclude that two edges not on F, join a to two of the vertices b, c, and d. By symmetry we may assume that a is joined to d as shown in Fig. 14.

(iii) No edge joins diagonally opposite vertices of F. By the above argument we can conclude that two edges join b to a, d and c, thus b is joined to c as in Fig. 15. Now a must be joined to b, and c to d, which can be done in only one way giving graph 5 in Fig. 7.

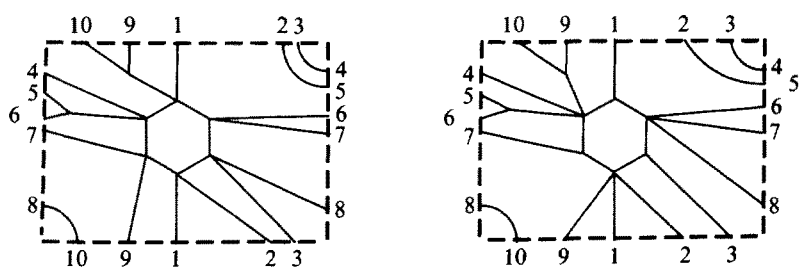

Fig. 12.

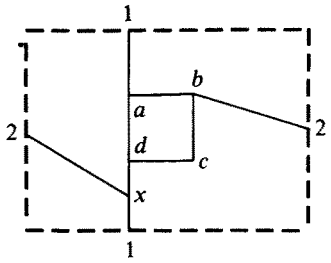

Fig. 13.

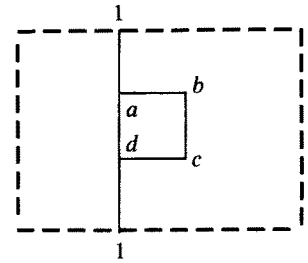

Fig. 14.

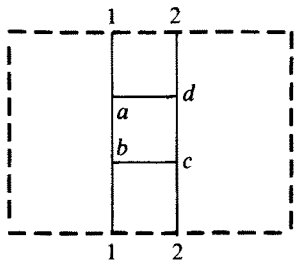

Fig. 15.

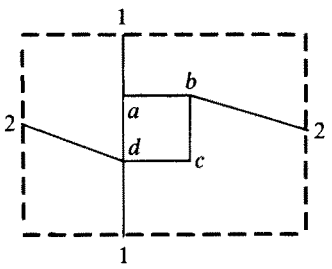

Fig. 16.

(iv) Two diagonally opposite vertices of F are joined. We observe here that all planar circuits must have even length because a planar circuit together with the vertices and edges in the cell it bounds is a planar graph with all bounded faces of even length. Since a planar graph cannot have exactly one face of odd length the circuit is even.

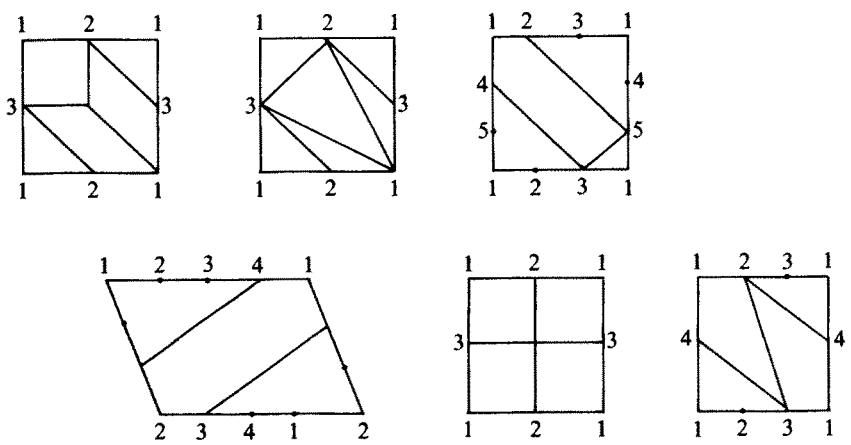

Fig. 17.

Suppose without loss of generality that b is joined to d. Since G cannot have planar 3-circuits, the only way of joining b and d that is not ruled out is shown in Fig. 16. Since d is 4-valent in G we see that c must be joined to a and b. This gives us graph 6 in Fig. 7.

Although simple representations were useful in illustrating the proofs, regular representations are the simplest to view. Figure 17 shows representations of the minimal maps for the torus which are easier to view, most of them regular. □

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