Geometric Programming for Circuit Optimization

[Extended Abstract]

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ABSTRACT

This tutorial concerns a method for solving a variety of circuit sizing and optimization problems, which is based on formulating the problem as a geometric program (GP), or a generalized geometric program (GGP). These nonlinear, constrained optimization problems can be transformed to convex optimization problems, and then solved (globally) very efficiently.

Categories and Subject Descriptors

B.7.2 [**Design Aids**]: Algorithms

General Terms

Algorithms, Design

Keywords

Circuit sizing, geometric programming, generalized geometric programming, convex optimization

1. CIRCUIT SIZING AND OPTIMIZATION

We assume that a circuit topology has been selected, and what remains is to choose appropriate sizes for the gates, transistors, wires, and other components. It is also possible to include other design variables such as threshold voltage, supply voltage, and oxide thickness. In many practical cases, some of these design variables are restricted to lie in discrete sets of values; in other cases, they can be well modeled as continuous variables.

The choice of these design variables determines various top level circuit objectives, such as the total area of the circuit, the total power it consumes, speed at which it can operate (for a digital circuit), its bandwidth (for an analog circuit), and other objectives such as noise tolerance, robustness to process and environment parameter variations, and so on. These objectives can be very complex functions of the design variables. In addition, there are many constraints that must be satisfied. There are many approaches to circuit sizing, including heuristics, and methods based on circuit simulation coupled to a generic numerical optimization method.

In this tutorial we focus on a particular approach, in which the sizing problem is modeled (at least approximately) as a *geometric program* (GP), a special type of mathematical optimization problem. We refer the reader to the paper *A Tutorial on Geometric Programming* [5] for an introduction to geometric programming, some of the basic tricks used to formulate problems in GP form, a number of examples, and an extensive list of references.

Over the last ten years, efficient *interior-point methods* for GP have been developed. Current implementations approach the efficiency of linear program (LP) solvers. Sparse GPs with tens of thousands of variables, and hundreds of thousands of constraints, can be reliably solved in minutes, on a personal computer. For more on algorithms for solving GPs, as well as the broader context of *convex optimization*, we refer the reader to [6].

2. GP-BASED SIZING

GP-based circuit sizing is not new; it has been used for digital circuits since the 1980s. In 1985 Fishburn and Dunlop [16] proposed a method for transistor and wire sizing, based on Elmore delay, that was later found to be a GP. Since then many digital circuit design problems have been formulated as GPs or closely related optimization problems. Work on gate and device sizing can be found in, *e.g.*, [10, 22, 31, 31, 36, 37]. These are all based on gate delay models that are compatible with geometric programming; see [22, 38, 33, 1] for more on such models. The *logical effort method*, described in the influential book [38] by Sproull, Sutherland, and Harris, does not explicitly rely on GP, but is very closely connected. See [4, 35] for more on GP-based digital circuit sizing.

Work on interconnect sizing related to GP includes [12, 13, 14, 17, 23, 25, 26, 34]; simultaneous gate and wire sizing is considered in [21]. In some of these papers, the authors develop custom methods for solving the resulting GPs, instead of using general purpose interior-point methods (see, *e.g.*, [10, 41]). For some simple problems, analytic solutions are available (see, *e.g.*, [8, 17]). Other problems in digital circuit design where GP plays a role include buffering and wire sizing [8, 9], sizing and placement [7], yield maximization [24, 30], parasitic reduction [32], and routing [2].

Geometric programming has also been used for the design

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of analog circuits [15, 19, 27, 39], mixed-signal circuits [11, 18] and RF (radio frequency) circuits [20, 29, 28, 40]. We refer the reader to the tutorial material [3] for GP-based sizing of analog and RF circuits.

3. GP MODELING

The tutorial focuses on the *modeling* of a variety of problems in GP form. There are several advantages to modeling a problem, at least approximately, as a GP. The first is computational: new methods can (globally) solve even large GP problems efficiently. Even if these new methods are not exploited to solve the problem, the knowledge that a problem is (approximately) a GP is useful. For example, it tells us that a particular logarithmic transformation of the variables and constraints yields a convex optimization problem, and this can be exploited to develop a more efficient solution method. In addition, we have the very useful conclusion that any local solution of the problem is in fact global. If an ad hoc solution method can be shown to find a local solution, we can conclude that it finds a global solution. (For more discussion of these issues, see [5, 6].)

Another advantage of expressing a sizing problem in GP form is conceptual: we claim that GP serves as a unifying standard form for circuit sizing problems, the same way that linear programming (LP) serves as a unifying standard form for a wide variety of simple resource allocation problems.

Like all methods, the GP modeling approach has advantages and disadvantages. One advantage is that complex interactions between the optimization variables are easily accounted for, and additional constraints are easily added. The method handles complex problems, such as joint optimization of devices sizes, threshold, and supply voltage; robust design over corners or taking statistical variations into account; and the design of circuits that operate in multiple modes (such as a low power and a high performance mode). When compared with other methods based on numerical optimization, methods based on GP (and interior-point solution methods) have the advantage of not needing an initial design, or any algorithm parameter tuning, and always finding the global solution.

We can also list some shortcomings of the approach. The method does not give much insight into *why* some set of specifications cannot be achieved, nor does it suggest how the designer might change the circuit topology to do better. While solving GPs is fast, it is not as fast as methods that choose sizes using simple rules, with a few passes over the circuit.

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