## GeSn-on-insulator substrate formed by direct wafer bonding

Lee, Kwang Hong; Bao, Shuyu; Wang, Wei; Lei, Dian; Wang, Bing; Gong, Xiao; Tan, Chuan Seng; Yeo, Yee-Chia

2016

Lei, D., Lee, K. H., Bao, S., Wang, W., Wang, B., Gong, X., et al. (2016). GeSn-on-insulator substrate formed by direct wafer bonding. Applied Physics Letters, 109(2), 022106-.

https://hdl.handle.net/10356/81989

## https://doi.org/10.1063/1.4958844

© 2016 American Institute of Physics. This paper was published in Applied Physics Letters and is made available as an electronic reprint (preprint) with permission of American Institute of Physics. The published version is available at:

[http://dx.doi.org/10.1063/1.4958844]. One print or electronic copy may be made for personal use only. Systematic or multiple reproduction, distribution to multiple locations via electronic or other means, duplication of any material in this paper for a fee or for commercial purposes, or modification of the content of the paper is prohibited and is subject to penalties under law.

Downloaded on 26 Aug 2022 04:43:19 SGT



## GeSn-on-insulator substrate formed by direct wafer bonding

Dian Lei,<sup>1</sup> Kwang Hong Lee,<sup>2</sup> Shuyu Bao,<sup>2,3</sup> Wei Wang,<sup>1</sup> Bing Wang,<sup>2</sup> Xiao Gong,<sup>1,a)</sup> Chuan Seng Tan,<sup>3</sup> and Yee-Chia Yeo<sup>1,a)</sup>

<sup>1</sup>Department of Electrical and Computer Engineering, National University of Singapore, Singapore 117576 <sup>2</sup>Low Energy Electronic Systems (LEES), Singapore MIT Alliance for Research and Technology (SMART), 1 CREATE Way, #10-01 CREATE Tower, Singapore 138602

<sup>3</sup>School of Electrical and Electronic Engineering, Nanyang Technological University, 50 Nanyang Avenue, Singapore 639798

(Received 13 June 2016; accepted 3 July 2016; published online 13 July 2016)

GeSn-on-insulator (GeSnOI) on Silicon (Si) substrate was realized using direct wafer bonding technique. This process involves the growth of  $Ge_{1-x}Sn_x$  layer on a first Si (001) substrate (donor wafer) followed by the deposition of SiO<sub>2</sub> on  $Ge_{1-x}Sn_x$ , the bonding of the donor wafer to a second Si (001) substrate (handle wafer), and removal of the Si donor wafer. The GeSnOI material quality is investigated using high-resolution transmission electron microscopy, high-resolution X-ray diffraction (HRXRD), atomic-force microscopy, Raman spectroscopy, and spectroscopic ellipsometry. The  $Ge_{1-x}Sn_x$  layer on GeSnOI substrate has a surface roughness of 1.90 nm, which is higher than that of the original  $Ge_{1-x}Sn_x$  film in the GeSnOI is as low as 0.10% as confirmed using HRXRD and Raman spectroscopy. *Published by AIP Publishing*. [http://dx.doi.org/10.1063/1.4958844]

Germanium-tin (Ge<sub>1-x</sub>Sn<sub>x</sub>) alloy is an attractive Group IV semiconductor for potential application in both nanoelectronic and photonic devices.  $Ge_{1-x}Sn_x$  alloy can be used as the channel layer in metal-oxide-semiconductor field-effect transistors (MOSFETs) to achieve carrier mobilities higher than that of Ge MOSFETs.<sup>1-5</sup> By adjusting the Sn mole fraction x and through strain engineering, the band gap of  $\text{Ge}_{1-x}\text{Sn}_x$  can be tuned,<sup>6-8</sup> enabling the realization of  $\text{Ge}_{1-x}\text{Sn}_x$ photo-detectors (PDs)<sup>9,10</sup> and  $Ge_{1-r}Sn_r$  light emitting diodes (LEDs)<sup>11</sup> that work in the mid-infrared wavelength range. In addition, strain-free  $Ge_{1-x}Sn_x$  was reported to be a direct band gap material with a Sn composition of 6.5%.<sup>12</sup> This makes  $Ge_{1-x}Sn_x$  as a promising material to realize a laser based on Group IV semiconductors.<sup>13</sup> Combination of Group IV-based optical components with high speed complementary metaloxide-semiconductor (CMOS) circuits could be desirable in future integrated chips, and the formation of a high-quality  $Ge_{1-r}Sn_r$  layer on insulator substrate may be a suitable platform for monolithic integration.

Germanium-on-insulator (GeOI) substrates have been realized using Ge condensation technique,<sup>14</sup> liquid phase epitaxy method,<sup>15</sup> and Smart Cut<sup>TM</sup> technology.<sup>16</sup> The formation of GeSn-on-insulator (GeSnOI) substrate is less well explored. Methods like low temperature Sn-induced Ge crystallization<sup>17,18</sup> and segregation controlled rapid-melting growth<sup>19–22</sup> were investigated. These methods either require a seed for crystallization or have difficulties in achieving large-area GeSnOI substrate. Lin *et al.* fabricated a Ge<sub>1-x</sub>Sn<sub>x</sub>/Ge/GeO<sub>2</sub>/SiO<sub>2</sub>/Si structure using wafer bonding technique,<sup>23</sup> where a thick Ge layer exists below the Ge<sub>1-x</sub>Sn<sub>x</sub> layer, i.e., the Ge<sub>1-x</sub>Sn<sub>x</sub> layer was not directly formed on an insulator.

In this letter, we demonstrate the formation of GeSnOI on Si substrate through direct wafer bonding (DWB) technique. The material quality of fabricated GeSnOI substrate was analyzed. The change in strain in the  $Ge_{1-x}Sn_x$  film before and after DWB was also investigated using high-resolution X-ray diffraction (HRXRD) and Raman spectroscopy. The magnitude of the compressive strain in the  $Ge_{1-x}Sn_x$  film in the GeSnOI formed is as low as 0.10%.

An ~100 nm thick  $\text{Ge}_{1-x}\text{Sn}_x$  layer was grown on lightly p-type doped Si (001) substrate using a molecular beam epitaxy (MBE) system at 180 °C. The temperatures of Ge and Sn effusion cells are 1300 °C and 1000 °C, respectively. The Ge<sub>1-x</sub>Sn<sub>x</sub> growth rate is 1.33 nm/min. The surface morphology of the as-grown Ge<sub>1-x</sub>Sn<sub>x</sub> on Si substrate was characterized using atomic force microscopy (AFM), as shown in Fig. 1(a). A root-mean-square (RMS) surface roughness of 0.528 nm was obtained with a scan area of 20  $\mu$ m × 20  $\mu$ m, which reveals that the surface of Ge<sub>1-x</sub>Sn<sub>x</sub> on Si is smooth. HRXRD reciprocal space mapping (HRXRD-RSM) was used to analyze the Ge<sub>1-x</sub>Sn<sub>x</sub> film quality and to obtain the strain. Fig. 1(b) shows the (115) RSM of the Ge<sub>1-x</sub>Sn<sub>x</sub> on Si



FIG. 1. (a) AFM surface scan of the  $Ge_{1-x}Sn_x/Si$  substrate before DWB. The RMS roughness of the  $Ge_{1-x}Sn_x$  surface is 0.528 nm. (b) (115) RSM of the  $Ge_{1-x}Sn_x/Si$  (001) substrate. The substitutional Sn composition of 4.1% and the compressive strain of 0.19% are extracted.

<sup>&</sup>lt;sup>a)</sup>Authors to whom correspondence should be addressed. Electronic addresses: elegong@nus.edu.sg, Telephone: +65 6516-1589, FAX: +65 6516-1589 and yeo@ieee.org, Telephone: +65 6516-2298, FAX: +65 6779-1103. Present address: Department of Electrical and Computer Engineering, National University of Singapore, 10 Kent Ridge Crescent, 119260 Singapore.

substrate. The diagonal and vertical dashed lines indicate reciprocal lattice peak positions for fully strain-relaxed and pseudomorphic epitaxial layer on Si, respectively. The reciprocal lattice vectors  $Q_X$  and  $Q_Z$  are along the [110] and [001] directions, respectively, and are given in terms of *reciprocal lattice units* (*rlu*) that are calculated from the angular positions (incident angle  $\omega$  and diffracted angle  $2\theta$ ) using the following equations:<sup>24</sup>

$$Q_X(rlu) = \sin\theta \times \sin(\theta - \omega), \tag{1}$$

$$Q_Z(rlu) = \sin\theta \times \cos(\theta - \omega). \tag{2}$$

The in-plane  $(a_X)$  and out-of-plane  $(a_Z)$  lattice constants of  $\text{Ge}_{1-x}\text{Sn}_x$  film can be calculated from the (115) RSM using

$$a_X = \frac{\sqrt{2\lambda}}{Q_X(rlu)},\tag{3}$$

$$a_Z = \frac{2\lambda}{Q_Z(rlu)}.\tag{4}$$

The XRD wavelength ( $\lambda$ ) is 0.154 nm. For Ge<sub>1-x</sub>Sn<sub>x</sub> directly grown on Si substrate,  $a_X$  and  $a_Z$  were calculated to be 0.56812 nm and 0.56999 nm, respectively, from the (115) RSM shown in Fig. 1(b). The substitutional Sn composition is calculated to be 4.1% and the compressive strain is 0.19% using Vegard's law.<sup>24</sup>

After the growth of the  $\text{Ge}_{1-x}\text{Sn}_x$  layer, a 500 nm-thick SiO<sub>2</sub> layer was deposited on the Ge<sub>1-x</sub>Sn<sub>x</sub> surface using plasma enhanced chemical vapour deposition (PECVD). Densification was then carried out at 350 °C for 7 h in N<sub>2</sub> environment. This also removed residual by-products or gas molecules that may be incorporated on the deposited film. Chemical mechanical polishing (CMP) was used to planarize the SiO<sub>2</sub> surface to achieve a RMS roughness smaller than 0.2 nm. Such a smooth surface is required for DWB. The SiO<sub>2</sub> layer thickness was reduced to 150 nm after CMP. Both Ge<sub>1-x</sub>Sn<sub>x</sub>/Si and Si handle wafers were subjected to O2 plasma exposure for 15 s, followed by a deionized water rinse and then a spin drying process in a spin rinse dryer (SRD). The O2 plasma exposure increases the surface hydrophilicity (water droplet surface contact angle  $<5^{\circ}$ ) of the dielectric. The rinsing step was necessary to clean the wafers' surfaces and to populate the surface with hydroxyl (OH) groups at a sufficiently high density to initiate wafer bonding. After that, the samples were brought into contact at room temperature. Post bonding annealing of the bonded wafer pair was then carried out at 300 °C in N2 ambient to further enhance the bond strength. Si was then etched away using tetramethylammonium hydroxide (TMAH) solution (25% by weight) at a temperature of 80 °C. A protective layer was spincoated on the backside of handle wafer so that only the Si donor wafer was etched in TMAH solution. The  $Ge_{1-x}Sn_x$  layer can act as an etch-stop layer since the etching selectivity of Si over  $\text{Ge}_{1-x}\text{Sn}_x$  is very high (>1000) in TMAH solution, as obtained in a separate experiment. After the full removal of the donor Si substrate, the protective layer was removed in O<sub>2</sub> plasma to complete the GeSnOI substrate formation process.

Fig. 2(a) shows a low resolution cross-sectional transmission electron microscopy (XTEM) image of the fabricated GeSnOI substrate. The Ge<sub>1-x</sub>Sn<sub>x</sub> surface, Ge<sub>1-x</sub>Sn<sub>x</sub>/SiO<sub>2</sub> interface, and SiO<sub>2</sub>/Si interface are flat and free from micro-voids.



FIG. 2. (a) XTEM image of the fabricated GeSnOI substrate showing the  $Ge_{1-x}Sn_x$  on SiO<sub>2</sub> on Si structure. The  $Ge_{1-x}Sn_x$  surface,  $Ge_{1-x}Sn_x/SiO_2$  interface, and SiO<sub>2</sub>/Si interface are flat. No void can be observed at the SiO<sub>2</sub>/Si bonding interface. HRTEM images in (b) and (c) show the GeSnOI surface and  $Ge_{1-x}Sn_x/SiO_2$  interface. The crystalline lattice fringes of  $Ge_{1-x}Sn_x$  layer can be clearly seen.

The Ge<sub>1-x</sub>Sn<sub>x</sub> layer thickness is ~95 nm which is the same as the original Ge<sub>1-x</sub>Sn<sub>x</sub> layer thickness grown on the Si substrate. This reveals that Ge<sub>1-x</sub>Sn<sub>x</sub> layer was not etched by TMAH solution during the etching of the thick Si layer. The buried oxide layer thickness is ~150 nm. No void was observed at the SiO<sub>2</sub>/Si bonding interface, indicating that a seamless bond was achieved. In addition, the GeSnOI surface and Ge<sub>1-x</sub>Sn<sub>x</sub>/SiO<sub>2</sub> interface are very flat, as shown in the high resolution TEM (HRTEM) images in Figs. 2(b) and 2(c), respectively. The crystalline lattice fringes of Ge<sub>1-x</sub>Sn<sub>x</sub> layer can also be clearly seen.

Fig. 3(a) shows the AFM surface scan of the fabricated GeSnOI substrate with the scan area of  $20 \,\mu\text{m} \times 20 \,\mu\text{m}$ . The RMS surface roughness is 1.90 nm. This is high and should be due to the fact that the defective Ge<sub>1-x</sub>Sn<sub>x</sub>/Si interface is now exposed on the top surface after DWB and the long exposure of Ge<sub>1-x</sub>Sn<sub>x</sub> surface in TMAH solution during the Si substrate removal process. The inset shows an optical microscope (OM) image of the formed GeSnOI surface with a capture area of ~1850 × 2500  $\mu\text{m}^2$ . The GeSnOI surface roughness can be reduced by using a CMP step.

In order to examine the crystalline quality of the GeSnOI substrate and to analyze the change in strain in the



FIG. 3. (a) AFM surface scan of the fabricated GeSnOI substrate. The RMS roughness is 1.9 nm. Inset shows the OM image of the formed GeSnOI sample surface with a capture area of  $\sim 1850 \times 2500 \,\mu\text{m}^2$ . (b) (115) RSM of GeSnOI substrate. Sn composition of 4% and compressive strain of 0.10% are calculated. The reduction of compressive strain is probably due to the different thermal expansion coefficients in Ge<sub>1-x</sub>Sn<sub>x</sub> and SiO<sub>2</sub> layers.



 $Ge_{1-x}Sn_x$  layer after DWB, HRXRD-RSM was performed on the fabricated GeSnOI substrate. (115) RSM of the GeSnOI substrate is shown in Fig. 3(b). Using Equations (1)-(4),  $a_X$  and  $a_Z$  values for  $\text{Ge}_{1-x}\text{Sn}_x$  film are calculated to be 0.56842 nm and 0.56964 nm, respectively. The Sn composition remains at 4.0% after the GeSnOI formation. The compressive strain of the  $Ge_{1-x}Sn_x$  film was 0.10% as calculated from the HRXRD results. This is smaller in magnitude as compared to that in the original  $Ge_{1-x}Sn_x/Si$  substrate (original compressive strain is 0.19% from HRXRD). The slight reduction of compressive strain is probably due to the different thermal expansion coefficients in  $Ge_{1-x}Sn_x$  and SiO<sub>2</sub> layers. The thermal expansion coefficients of SiO2, Ge, and Sn are reported to be  $5.6 \times 10^{-7} \text{ K}^{-1}$ ,  $6 \times 10^{-6} \text{ K}^{-1}$ , and  $2.34 \times 10^{-5} \text{ K}^{-1}$ , respectively.<sup>25,26</sup> Thus, the thermal expansion coefficient of  $\text{Ge}_{1-x}\text{Sn}_x$  film should be larger than that of the SiO<sub>2</sub> buried layer in GeSnOI substrate. After thermal annealing in DWB and during the cooling process, the SiO<sub>2</sub> layer contracts less than the  $\text{Ge}_{1-x}\text{Sn}_x$  layer.<sup>27</sup> As a result, the compressive strain in the  $Ge_{1-x}Sn_x$  layer is reduced.

Raman spectroscopy was also carried out using a Witec alpha 300 R confocal Raman system equipped with a 532 nm green laser source. The laser intensity was fixed at 1.1 mW. Fig. 4(a) shows the Raman spectra of the GeSnOI substrate. Only one peak located near 300 cm<sup>-1</sup> was observed and can be assigned to the Ge-Ge vibration mode. The non-existence of the Si-Si vibration mode near  $520 \,\mathrm{cm}^{-1}$  indicates that the Si layer from the donor wafer has been completely removed in TMAH solution. Fig. 4(b) shows the normalized Raman spectra of the  $Ge_{1-x}Sn_x/Si$  substrate before DWB, the completed GeSnOI substrate, and, for reference, a Ge (001) bulk substrate. One strong Ge-Ge Raman peak at  $\omega_{Ge} = 301.52 \text{ cm}^{-1}$ appears on the spectrum of Ge bulk substrate. The Raman spectra of  $Ge_{1-x}Sn_x$  also consist of only one strong peak near  $300 \text{ cm}^{-1}$ , which can be assigned to Ge-Ge peak.<sup>28–30</sup> Ge-Sn peaks cannot be observed with the 532 nm excitation. This is because that this laser wavelength excitation is far from the resonance condition with the  $E_1$  to  $E_1 + \Delta_1$  optical transitions of Ge-Sn mode as discussed in Ref. 29. As can be seen in Fig. 4(b), the Ge-Ge peaks of the  $Ge_{1-x}Sn_x/Si$  substrate and GeSnOI substrate shift toward lower wavenumbers and become broader as compared to that of the Ge (001) bulk substrate. The peak positions of the Raman spectra are obtained based on the maximum of the Exponentially Modified Gaussian (EMG) function fitted curves.<sup>29</sup> This agrees with the conventional definition of peak frequencies in semiconductor FIG. 4. (a) Raman spectrum of GeSnOI substrate shows the absence of Si-Si vibration mode. This indicates that Si from the donor wafer has been fully etched away. (b) Raman spectra of the GeSnOI, Ge<sub>1-x</sub>Sn<sub>x</sub> on Si, and Ge (001) bulk substrates. Using the Raman shift results, the compressive strain of GeSnOI substrate is calculated to be 0.10% which is smaller than 0.26% (calculated using Raman data) in the original Ge<sub>1-x</sub>Sn<sub>x</sub>/Si substrate.

alloys. The Ge-Ge peaks of the Ge<sub>1-x</sub>Sn<sub>x</sub>/Si substrate, GeSnOI substrate, and Ge (001) bulk substrate are 299.56 cm<sup>-1</sup>, 298.50 cm<sup>-1</sup>, and 301.52 cm<sup>-1</sup>, respectively. The Raman shift of the Ge-Ge peaks is determined by the difference of peak position between Ge<sub>1-x</sub>Sn<sub>x</sub> and Ge bulk substrate. The measured Ge-Ge peak shift can be expressed as<sup>30</sup>

$$\Delta \omega = \Delta \omega_{alloy} + \Delta \omega_{strain} = ax + b\varepsilon, \tag{5}$$

where  $\Delta \omega$  is measured Raman shift, *a* and *b* are constant parameters, *x* is the Sn composition, and *e* is the in-plane strain. The constant parameters of *a* and *b* are taken from Ref. 30. The relative Raman shifts of Ge<sub>1-x</sub>Sn<sub>x</sub> on Si substrate and GeSnOI substrate compared to Ge bulk substrate are  $-1.96 \text{ cm}^{-1}$  and  $-3.02 \text{ cm}^{-1}$ , respectively. Combining with the Sn composition calculated from XRD, the compressive strain is calculated to be 0.26% for the Ge<sub>1-x</sub>Sn<sub>x</sub> on Si substrate and 0.10% for the GeSnOI substrate using the measured Raman results. These results are consistent with HRXRD data and confirm that the compressive strain in the Ge<sub>1-x</sub>Sn<sub>x</sub> film decreases slightly after GeSnOI substrate formation.

The GeSn film quality of the formed GeSnOI substrate was also evaluated using spectroscopic ellipsometry. The measurements were carried out using J. A. Woollam's spectroscopic ellipsometer with the photo energy from 1 to 4.5 eV. The ellipsometric angles  $\Psi$  and  $\Delta$  were acquired at an incidence angle of 65°. Fig. 5 shows the complex dielectric function of the GeSn film from GeSnOI and GeSn-on-Si



FIG. 5. Complex dielectric function of the GeSn film from GeSnOI and GeSn-on-Si substrates. The sharp critical points  $E_1$ ,  $E_1 + \Delta_1$ ,  $E'_0$ , and  $E_2$  correspond to the optical response of the GeSn film in both the samples, and are consistent with the crystallinity of the GeSn films.

Reuse of AIP Publishing content is subject to the terms at: https://publishing.aip.org/authors/rights-and-permissions. Download to IP: 155.69.250.206 On: Thu, 04 Aug 2016

substrates. The slight shift in the dielectric function could be due to the slight change in compressive strain in the GeSn film.<sup>31</sup> The critical points  $E_I$ ,  $E_I + \Delta_I$ ,  $E'_0$ , and  $E_2$  correspond to the optical response of the GeSn films in both the samples.<sup>31</sup> These sharp critical points indicate that the single crystalline property is well-maintained after the GeSnOI formation process, which is consistent with HRXRD and TEM results.

In conclusion, GeSnOI substrate was fabricated using DWB technique. The substrate quality was investigated using AFM, TEM, HRXRD, Raman spectroscopy, and spectroscopic ellipsometry. The crystalline quality of the Ge<sub>1-x</sub>Sn<sub>x</sub> film is maintained after the DWB process. Based on HRXRD and Raman spectroscopy results, the magnitude of the compressive strain in the Ge<sub>1-x</sub>Sn<sub>x</sub> film was reduced to 0.10% after GeSnOI substrate formation. This GeSnOI substrate could offer a useful platform for monolithic integration of electronic and photonic devices using Group IV-only materials.

This project was supported by Singapore National Research Foundation through the Competitive Research Program (Grant No. NRF-CRP6-2010-4), NUS Trailblazer Grant (Grant No. R-263-000-B43-733), Ministry of Education (MOE) Academic Research Fund (Grant No. R-263-000-B50-112), and National Research Foundation Singapore through the Singapore MIT Alliance for Research and Technology's Low Energy Electronic Systems (LEES) IRG. The authors are thankful to V. R. D'Costa for valuable discussions on analysis of ellipsometry data.

- <sup>1</sup>G. Han, S. Su, C. Zhan, Q. Zhou, Y. Yang, L. Wang, P. Guo, W. Wang, C. P. Wong, Z. X. Shen, B. Cheng, and Y.-C. Yeo, Int. Electron Devices Meet. Tech. Dig. **2011**, 402–404.
- <sup>2</sup>S. Gupta, R. Chen, B. Magyari-Kope, H. Lin, B. Yang, A. Nainani, Y. Nishi, J. S. Harris, and K. C. Saraswat, Int. Electron Devices Meet. Tech. Dig. **2011**, 398–401.
- <sup>3</sup>X. Gong, G. Han, F. Bai, S. Su, P. Guo, Y. Yang, R. Cheng, D. Zhang, G. Zhang, C. Xue, B. Cheng, J. Pan, Z. Zhang, E. S. Tok, D. A. Antoniadis, and Y.-C. Yeo, IEEE Electron Device Lett. **34**, 339 (2013).
- <sup>4</sup>P. Guo, G. Han, X. Gong, B. Liu, Y. Yang, W. Wang, Q. Zhou, J. Pan, Z. Zhang, E.-S. Tok, and Y.-C. Yeo, J. Appl. Phys. **114**, 044510 (2013).
- <sup>5</sup>D. Lei, W. Wang, Z. Zhang, J. Pan, X. Gong, G. Liang, E.-S. Tok, and Y.-
- C. Yeo, J. Appl. Phys. 119, 024502 (2016).
- <sup>6</sup>G. He and H. A. Atwater, Phys. Rev. Lett. **79**, 1937 (1997).

- <sup>7</sup>P. Moontragoon, Z. Ikonic, and P. Harrison, Semicond. Sci. Technol. 22, 742 (2007).
- <sup>8</sup>J. Mathews, R. T. Beeler, J. Tolle, C. Xu, R. Roucka, J. Kouvetakis, and J. Menendez, Appl. Phys. Lett. **97**, 221912 (2010).
- <sup>9</sup>S. Su, B. Cheng, C. Xue, W. Wang, Q. Cao, H. Xue, W. Hu, G. Zhang, Y. Zuo, and Q. Wang, Opt. Express **19**, 6400 (2011).
- <sup>10</sup>Y. Dong, W. Wang, X. Xu, X. Gong, D. Lei, Q. Zhou, Z. Xu, W. K. Loke, S.-F. Yoon, G. Liang, and Y.-C. Yeo, IEEE Trans. Electron Devices 62, 128 (2015).
- <sup>11</sup>J. D. Gallagher, C. L. Senaratne, P. Sims, T. Aoki, J. Menendez, and J. Kouvetakis, Appl. Phys. Lett. **106**, 091103 (2015).
- <sup>12</sup>V. R. D'Costa, C. S. Cook, A. G. Birdwell, C. L. Littler, M. Canonico, S. Zollner, J. Kouvetakis, and J. Menendez, Phys. Rev. B 73, 125207 (2006).
- <sup>13</sup>S. Wirths, R. Geiger, N. von den Driesch, G. Mussler, T. Stoica, S. Mantl, Z. Ikonic, M. Luysberg, S. Chiussi, J. M. Hartmann, H. Sigg, J. Faist, D. Buca, and D. Grutzmacher, Nat. Photonics 9, 88 (2015).
- <sup>14</sup>S. Nakaharai, T. Tezuka, N. Sugiyama, Y. Moriyama, and S. Takagi, Appl. Phys. Lett. 83, 3516 (2003).
- <sup>15</sup>Y. Liu, M. D. Deal, and J. D. Plummer, Appl. Phys. Lett. **84**, 2563 (2004).
- <sup>16</sup>T. Akatsu, C. Deguet, L. Sanchez, F. Allibert, D. Rouchon, T. Signamarcheix, C. Richtarch, A. Boussagol, V. Loup, F. Mazen, J.-M. Hartmann, Y. Campidelli, L. Clavelier, F. Letertre, N. Kernevez, and C. Mazure, Mater. Sci. Semicond. Process. 9, 444 (2006).
- <sup>17</sup>K. Toko, N. Oya, N. Saitoh, N. Yoshizawa, and T. Suemasu, Appl. Phys. Lett. **106**, 082109 (2015).
- <sup>18</sup>H. Chikita, R. Matsumura, Y. Kai, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **105**, 202112 (2014).
- <sup>19</sup>M. Kurosawa, Y. Tojo, R. Matsumura, T. Sadoh, and M. Miyao, Appl. Phys. Lett. **101**, 091905 (2012).
- <sup>20</sup>M. Kurosawa, N. Taoka, H. Ikenoue, O. Nakatsuka, and S. Zaima, Appl. Phys. Lett. **104**, 061901 (2014).
- <sup>21</sup>Z. Liu, J. Wen, X. Zhang, C. Li, C. Xue, Y. Zuo, B. Cheng, and Q. Wang, J. Phys. D: Appl. Phys. 48, 445103 (2015).
- <sup>22</sup>T. Shimura, M. Matsue, K. Tominaga, K. Kajimura, T. Amamoto, T. Hosoi, and H. Watanabe, Appl. Phys. Lett. **107**, 221109 (2015).
- <sup>23</sup>J.-Y. J. Lin, S. Gupta, Y.-C. Huang, Y. Kim, M. Jin, E. Sanchez, R. Chen, K. Balram, D. Miller, J. Harris, and K. Saraswat, Symp. VLSI Technol. Dig, Tech. **2013**, T32–T33.
- <sup>24</sup>N. Bhargava, M. Coppinger, J. P. Gupta, L. Wielunski, and J. Kolodzey, Appl. Phys. Lett. **103**, 041908 (2013).
- <sup>25</sup>H. Tada, A. E. Kumpel, R. E. Lathrop, J. B. Slanina, P. Nieva, P. Zavracky, I. N. Miaolis, and P. Y. Wong, J. Appl. Phys. 87, 4189 (2000).
- <sup>26</sup>K. H. Lee, S. Bao, G. Y. Chong, Y. H. Tan, E. A. Fitzgerald, and C. S. Tan, J. Appl. Phys. **116**, 103506 (2014).
- <sup>27</sup>Y. Ishikawa, K. Wada, D. D. Cannon, J. Liu, H.-C. Luan, and L. C. Kimerling, Appl. Phys. Lett. 82, 2044 (2003).
- <sup>28</sup>H. Lin, R. Chen, Y. Huo, T. I. Kamins, and J. S. Harris, Appl. Phys. Lett. 98, 261917 (2011).
- <sup>29</sup>V. R. D'Costa, J. Tolle, R. Roucka, C. D. Poweleit, J. Kouvetakis, and J. Menendez, Solid State Commun. **114**, 240 (2007).
- <sup>30</sup>R. Cheng, W. Wang, X. Gong, L. Sun, P. Guo, H. Hu, Z. Shen, G. Han, and Y.-C. Yeo, ECS J. Solid State Sci. Technol. **2**, P138 (2013).
- <sup>31</sup>V. R. D'Costa, W. Wang, Q. Zhou, T. K. Chan, T. Osipowicz, E. S. Tok, and Y.-C. Yeo, J. Appl. Phys. **116**, 053520 (2014).