Graduate and Undergraduate Educational Methods for Microelectronics

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Abstract—**Methods applicable to teaching microelectronics at the undergraduate and graduate level in conjunction with an industrial fabrication capability are presented. Results of three semesters of teaching microelectronics at the graduate level with emphasis on both digital and analog circuits are summarized. Plans for teaching an undergraduate course utilizing the fabrication of integrated circuits are discussed.**

INTRODUCTION

MICROELECTRONICS is a dynamic and fast growing field of electrical engineering. In the past decade, microelectronics has directly contributed to the development and marketing of many products which have had a significant impact in our daily lives. It has been said that we are entering an age of electronic revolution similar in many respects to the energy revolution which spawned the industrial advancements of the last century [1]. It is without question that the microelectronic industry is on the verge of advances in technology and complexity that are hard to visualize even at this point in time. As a result circuits and systems implemented by microelectronic technology are becoming very complex. The design, development, and testing of such circuits and systems are quickly exhausting the available manpower resources. The size and complexity of such systems also aggravate this problem. Economic considerations require that these systems work with little or no modification the first time that they are built. Needless to say, these and similar other problems associated with microelectronics have provided a tremendous challenge to both industry and the university.

One thing that is very obvious from the trend in microelectronics is that the university, industry, and government will have to cooperate in order to meet the challenges of microelectronics. In many respects this cooperation is already active and is providing solutions to some of the problems posed by advances in technology. The integrated circuit at the very large-scale integration (VLSI) level or beyond is probably the best example of a very complex system found in the educational environment. It represents the opportunity to develop the skills and concepts to manage and design complex systems in a controllable environment, something which is not found in many other disciplines. Unfortunately, the fabrication of integrated circuits is a costly undertaking and requires skilled personnel, both of which are in short supply in the university. This leads to the primary mode of cooperation which presently exists between universities and industry and/or the government. Such a cooperative arrangement allows the university to concentrate on the educational aspects of microelectronics. This can lead to many benefits to all parties involved. The university can begin to address the problems of design methodology, automation, and many other questions concerning the philosophy and mechanics of the design of complex systems. Also, the relationship between the university and industry leads to the identification of pertinent research problems to which the university can devote its efforts.

The objective of this paper is to describe the results of teaching microelectronics at a university using industrial fabrication facilities. The focus will be primarily on the methods that have resulted based on the experience gained over a three-semester time frame. This cooperation has also led to growth in the research and development area of microelectronics, however these activities are not considered in this paper. The specific cooperative program on which this paper is based will be described. The objectives and necessary ingredients of such a program will be outlined. The experience in using this program to support graduate education in microelectronics will be summarized. This program has resulted in three multiple project chips. Plans to bring the microelectronic education associated with the fabrication down to the undergraduate level are described. The first course in this area will be given in the fall 1981 semester. The paper will conclude with an evaluation of the results to date and a description of future plans. The key aspect in this program is the flexibility to adapt to the changes and growth that are expected to be a routine occurrence in the field of microelectronics.

INDUSTRY-UNIVERSITY FABRICATION PROGRAM

A sequence of steps showing the process by which an integrated circuit is designed is given in Fig. 1. This illustration is transparent to technology and emphasizes the major steps in the design and implementation process. The primary steps are design, simulation, digitization, verification, mask generation, fabrication, and test and evaluation. At any point in this sequence the designer may return to some previous point in order to modify the design. The activities shown in Fig. 1 can be divided into three general areas. These areas are 1) design, 2) fabrication, and 3) testing and evaluation. In most situations, the design and testing and evaluation are accomplished in the university and the fabrication is accomplished in industry.

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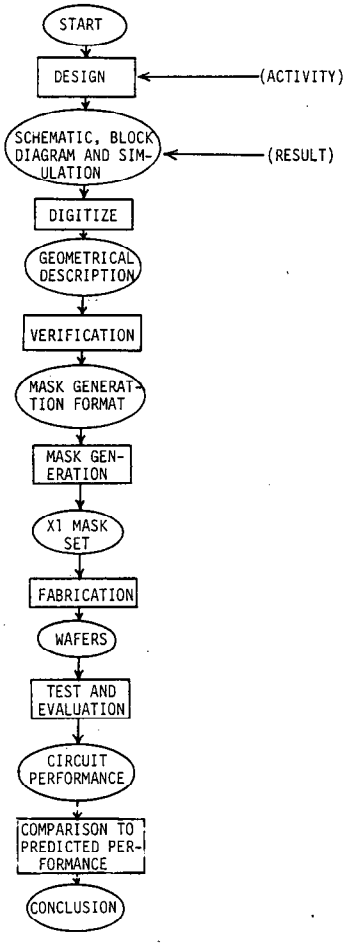

Fig. 1. Steps in the implementation of integrated circuit.

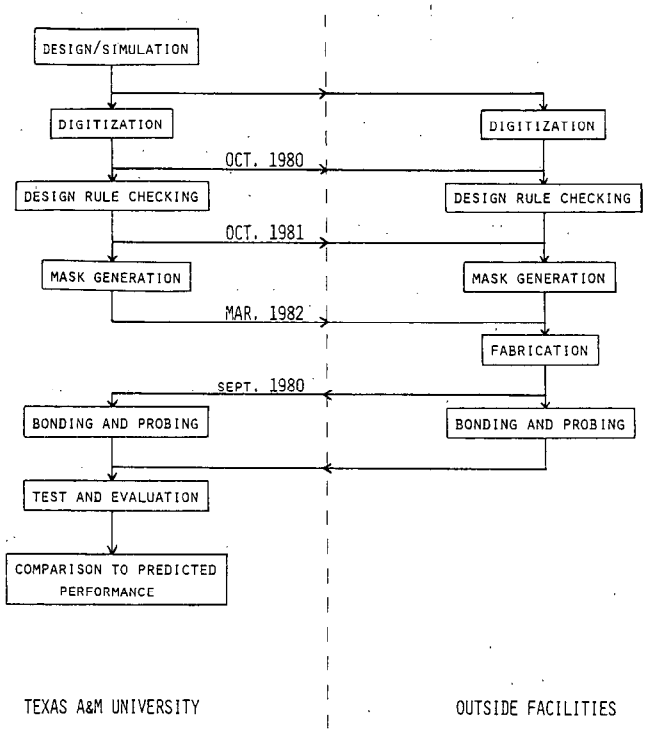

Fig. 2. Illustration of possible partitioning of the steps in Fig. 1 into the university and industrial environments. Dates in Fig. 2 indicate when this capability was developed at Texas A&M University.

The actual boundaries between the activities at the university and the activities in industry can become very fuzzy. These boundaries depend upon the capabilities and resources in both the university and industry. The optimum situation from a university viewpoint would be to accomplish as much as possible in the university environment. Fig. 2 illustrates the partitioning of these activities into the university and industrial environments.

The fabrication of university designs by industry may seem an unreality unless the need for cooperation is fully appreciated. It has become necessary to join together in helping each other meet mutual objectives. The typical objectives of industry in providing a fabrication capability for the university are 1) to enhance the reputation of the industry with the university students, 2) to have knowledge of and familiarity with qualified students as potential employees, 3) to improve the teaching of integrated circuit design, and 4) to encourage the student to pursue a career in integrated circuit design and/or fabrication. The typical objectives of the university in developing a microelectronic program which utilizes industrial fabrication are 1) to effectively teach microelectronics at the graduate and undergraduate level, 2) to have access to state of the art technologies, 3) to develop new circuits, design methodologies, and design aids, and 4) to develop closer relationships with industry. It is obvious that these objectives are for the most part very compatible.

In the summer of 1979, Texas Instruments, Inc. proposed the use of their corporate front end prototyping facility to fabricate integrated circuits for the students and faculty of the Department of Electrical Engineering at Texas A&M University. This proposal was inspired by the well-known arrangement between the California Institute of Technology and Xerox Research Laboratory in Palo Alto which has led to a government sponsored multiple project chip activity involving universities associated with the Department of Defense [2]. Texas A&M University responded in a positive manner resulting in a joint program to fabricate integrated circuits for our microelectronic program. At this date two multiple project chips, designated TEXAM 0180 and TEXAM 0280, have been designed, fabricated, and evaluated [3], [4]. A third multiple project chip, designated as TEXAM 0181, has been fabricated and is being evaluated. These multiple project chips will be described in more detail in the next section.

Some of the factors which allowed this program to flourish are described here. These factors in the university environment included a strong analog and digital circuits program and a well-equipped solid-state laboratory. In addition several of the faculty members had designed integrated circuits at Texas Instruments prior to this relationship. In the industrial environment, the key factors were a recognition of the difficulty in hiring sufficient quantities of qualified engineers and a farsighted commitment and a willingness to use their facilities to do something about this problem. Another key factor in the industrial side of this program was a coordinator who was willing to take the time and understand some of the peculiar constraints placed upon the university and to have the right amount of patience mixed with prodding. The attitude of Texas

Instruments was not "what did you build and did it work?" but rather "what did you learn by what you did?". Such an attitude by the industrial partner in a fabrication program was a key factor in the success of the program.

MICROELECTRONIC EDUCATION AT THE GRADUATE LEVEL

Integrated circuits and their design involves the principles of managing complex systems. The application of such principles is not constrained just to the field of microelectronics. The educational aspects of microelectronics offer a tremendous challenge to the university. Such a challenge includes questions on pedogogy, philosophy, and the implementation of such a program. Many of these questions will continue to be discussed while experience is gained. The program described in this paper has adopted the viewpoint that fabrication can be and is an essential part of teaching microelectronics. This viewpoint has been based on several important factors. The first is motivation. There is no substitute for the motivation of the student and faculty member who know that their circuit will be fabricated and they will eventually be responsible for determining its performance. The second factor is that the principles are often easily taught by doing. A third factor is that knowledge that the circuit will be fabricated forces one to seriously consider very important aspects such as design rule violations, testing and evaluating the circuits, packaging and pin out considerations, etc.

It is important to realize that the objective of fabricating an integrated circuit in an academic environment is for the purpose of information. It is more important for the student to know why a circuit does or does not work rather than to simply determine whether or not it was functional. Effort is made to "close the loop" and make the designer responsible for the entire aspects of the program including making provisions in his design and test evaluation for fabrication variations. The amount of time required to design, fabricate, and evaluate an integrated circuit exceeds a semester. A problem results in that the student may not have any more time than a semester to devote to such an activity. Approximately 80 percent of the projects thus far have some degree of follow-up after they have been designed in a prior semester. This follow-up rate is high due to the fact that most projects involve two or more students. One method which has been tried with good success is to assign the last semester's projects to be tested and evaluated by the present students. In this approach, the students are exposed to the mistakes committed by previous students and can learn from them.

The graduate microelectronic program is divided into one course per semester. The fall semester course emphasizes digital circuits and systems. The text is the *Introduction to VLSI Systems* by C. Mead and L. Conway [5]. The spring semester course emphasizes analog circuits and systems and uses the IEEE Press Reprint titled "Analog MOS Integrated Circuits" edited by P. Gray, D. Hodges, and R. Broderson [6] supplemented with a preliminary edition of "Switched Capacitor Circuits," by P. Allen and E. Sanchez-Sinencio [7]. The typical sequence of events involves getting the background necessary to accomplish integrated circuit design, proposing a project, providing a floorplan, designing and analyzing the project, digitization, and correcting the digitization. The project is ready for mask generation and fabrication at the termination of the semester. During these activities, lectures in the course provide the principles and background pertinent to the project. A report describing the project, its design, and proposed test and evaluation procedures is submitted at the end of the course. This report as well as the verified and corrected digitization constitute the project grade which is 30 percent to 40 percent of the course grade. Fig. 3 shows a typical chronological sequence of events in the cycle of a student IC design project.

The projects are usually undertaken by teams of students whose number varies from two to five depending upon the complexity of the project. During the semester, several group assignments are made which help prepare the students for the project. These assignments include characterization of actual metal-oxide semiconductor (MOS) devices, use of the SPICE computer program, and the layout of a given circuit graded in such a manner as to cause the students to achieve a compromise between the minimum areas and the number of design rule violations. Fig. 4 shows an example of this assignment given during the spring 1981 semester. The score for this assignment was calculated using the following formula

$$\text{SCORE} = \frac{500}{\left(\begin{array}{c}\text{minimum area of rectangle}\\ \text{A in mils of Fig. 4 which}\\ \text{just encompasses the active}\\ \text{circuits}\end{array}\right)} + \frac{5000}{\left(\begin{array}{c}\text{minimum area of rectangle B in}\\ \text{mils of Fig. 4 which just encom-}\\ \text{passes the entire circuit}\end{array}\right)} - 10 \times \left[\begin{array}{c}\text{number of computer flagged}\\ \text{design rule violations}\end{array}\right] \geqslant 0.$$

With a 0.2 mil minimum device geometry the scores ran from 84 to 97. This type of activity was well received by the students.

The projects began with the spring 1980 graduate course emphasizing analog circuits and systems. The multiproject chip (MPC) that resulted from this class and other research projects was called TEXAM 0180. A microphotograph of TEXAM 0180 is shown in Fig. 5. TEXAM 0180 contained 18 circuits, used a double-poly NMOS process and was 199 mils X 214 mils. A large array of matched transistors having different W/L ratios including both enhancement and depletion devices was included. This array has been extremely useful for breadboarding. The class projects included four NMOS op amps. The chip was submitted to Texas Instruments, Inc. on July 8, 1980 and returned on October 15, 1980. A typical process run includes 20 four-inch wafers. Seventeen of the circuits were tested and all but two were functional. Many of the

WEEK	ACTIVITY	ASSIGNMENTS
1	INTRODUCTION	
2	MOS CIRCUITS	
3		
4		GROUP ASSIGNMENTS
5	PROJECT EMPHASIS	
6		
7		
8	MECHANICS	
9	LECTURE	
10		PROJECT DEFINITION
11		PROJECT FLOORPLAN
12		PROGRESS REPORTS
13		
14		
15		PROGRESS REPORT AND DIGITIZATION
16	VERIFICATION AND CORRECTION	
20	CHIP COMMITTMENT	
28-32	CHIP FABRICATED	
32?	TEST AND EVALUATION	

Fig. 3. Chronological sequence of activities in a course where the students are designing circuits that will be fabricated.

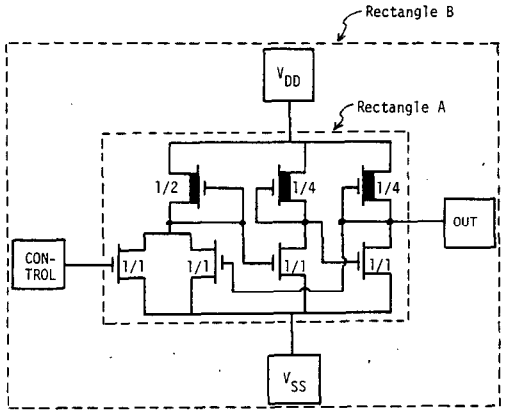

Fig. 4. Example of an assignment used to prepare the student for designing an integrated circuit. Ratio given by each active device corresponds to the W/L ratio in mils. The pad openings are defined as 4 mils X 4 mils.

functional circuits did not work as predicted due to design errors. Layout mistakes typically caused fatal errors whereas design mistakes typically caused nonfatal errors. While some of the wafers were diced and packaged at Texas Instruments, Inc., dicing, bonding, and packaging facilities were developed at Texas A&M University. These facilities permit quick turnaround and are a minimum cost to maintain. Experience with bonding internal and external connections showed that care must be taken in the location of pads in the layout.

The second MPC designated TEXAM 0280 was coordinated through the fall 1980 graduate course emphasizing digital circuits and systems. Fig. 6 shows a microphotograph of TEXAM 0280. Several lessons learned from TEXAM 0180 were applied to this MPC. Designers were given the choice of

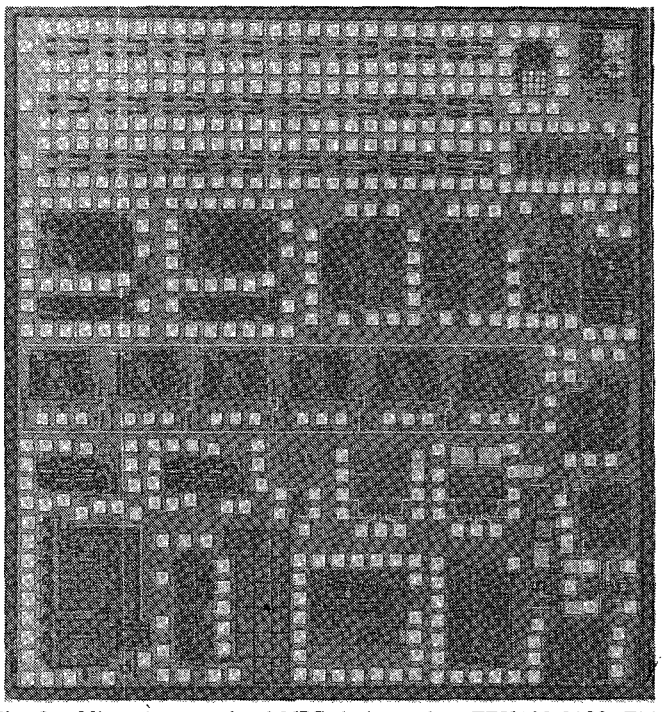

Fig. 5. Microphotograph of MPC designated as TEXAM 0180. This MPC was 199 mils X 214 mils and used a double-poly NMOS process.

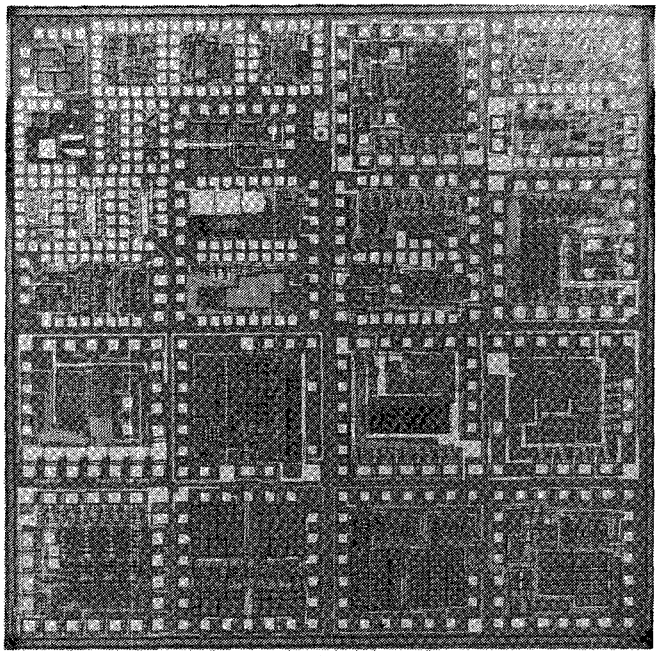

Fig. 6. Microphotograph of MPC designated as TEXAM 0280. This MPC was 300 mils X 300 mils and used a double-poly NMOS process. The projects included on this MPC are listed in Table I.

three layout formats with designated pad locations which could be probed by a standard probe card. The areas of these formats were 36 mils X 36 mils (20 pads), 36 mils X 72 mils (24 pads), and 72 mils X 72 mils (24 pads). In addition, the bar which is 300 mils X 300 mils, was designed to be quartered so that bonding pads were closer to the periphery of the quartered chip. This MPC was submitted for mask generation and fabrication on March 10, 1981 and the first batch was fabricated on April 13, 1981. A second batch was fabricated on June 4,

TABLE I
PROJECTS ON TEXAM 0280

CIRCUIT	FUNCTION/OBJECTIVE	DESIGNERS
ADDGH	This circuit is a very fast adder which is implemented as a self-timed system.	Gourley & Hodapp
BOTCH	This circuit is a 4 bit ALU.	Miller & White
CTILN	This circuit is a programmable PLA to be used in the undergraduate laboratory.	Ismail & Nguyen
DAC8	An 8 bit DAC using binary weighted capacitors with no capacitance ratio greater 16.	Allen & Taylor
EE457	Current mirrors. Test various geometries and different types.	Mays & Saldana
FBASS	Differential amplifier for undergraduate microelectronics course.	Bass
GRIM1	Data stack.	Grignoux & Morgan
HXPLA	4-bit binary 7-segment hex display-decoder and/or driver.	Kusnetz & Richardson
JWHCL	4-bit by 4 stack	Hardin & Lewis
KAPRT	Capacitance structures to test for the potential of using the laser to trim.	Allen & Fanini
LMFFO	A first-in, first-out 3x2 register.	Ledbetter & Mendez
MRSTT	Circuit to investigate the effect of holding capacitor and MOS transistor.	Geiger & Ngo
NLIEM	An analog building block for automated design considerations.	Allen & Nguyen
OPAMP	Three op amps. An improved version of HOPE. A TI op amp. A Bell Labs op amp.	Allen & Ismail
PTAIN	Integrator blocks using switched resistors.	Geiger & Ngo
QSTVF	Switched capacitor state variable filter.	Cantrell & Geiger
RANDY	Study of devices and the influence of a quasi depletion-enhancement device.	Geiger & Grignoux
SPLAC	Test of make-up, size, and speed for PLA	Strader
TEST2	A general test cell.	Allen & Woo
USFAN	63x1 bit static random access memory.	Fanini & Sridhar
VGP	Study of irregular shaped geometries.	Geiger & Grignoux
WABVA	Switched capacitor absolute value circuit.	Cantrell & Guynes
XMULT	Switched capacitor analog multiplier	Allen & Cantrell
YDPT2	Switched capacitor circuits using current amplifiers	Perdomo-Teran
ZTEST	A general test cell.	Allen & Woo

1981. TEXAM 0280 contained 25 projects and used the same double-poly NMOS process as the first MPC. These projects are summarized in Table I. Most of the circuits are digital as can be observed by the high degree of regularity. Approximately 50 percent of the circuits were digitized at Texas A&M University and the rest digitized at Texas Instruments, Inc. At this time 60 percent of the projects of TEXAM 0280 have been evaluated by their designers.

A third MPC, designated TEXAM 0181, has been designed and fabricated. Fig. 7 shows a microphotograph of TEXAM 0181. TEXAM 0181 is 338 mils X 338 mils and is designed to be diced into nine 108 mils X 108 mils sections. The purpose was to get a greater utilization of the chip area and to avoid long leads between the package pads and the chip pads. The project formats were expanded to include an area 72 mils X 108 mils with 30 pads and an area 108 mils X 108 mils with 36 pads. All digitization for the MPC was done at Texas A&M University. Some preliminary design rule and cell format checking was also done before sending the magnetic tape to Texas Instruments, Inc. Our in-house computer aid design capability supported by a VAX 11/780 was greatly improved during the development of this MPC. These improvements included data handling, verification, and circuit graphics. TEXAM 0181 was submitted for fabrication on August 17, 1981 and returned on October 5, 1981.

TEXAM 0181 was coordinated through the graduate course with emphasis on analog circuits and systems. The class project for this course was the design of an 8-bit high-speed analog-to-digital converter in an area of 108 mils X 108 mils. There were three 8-bit analog-to-digital converters included on TEXAM 0181. Table II summarizes all the projects that were included on TEXAM 0181. This table includes the class projects as well as other research and educational projects. The students prepared for the class project by undertaking several tasks which are pertinent to the background necessary to design an analog-to-digital converter. These tasks were assigned on a group basis. The groups consisted of those students who were planning to form a team to design the class project. This allowed the students to develop an effective team concept before undertaking the class project. These tasks included the evaluation of the SPICE parameters of the MOS device of TEXAM 0180, an evaluation of the MOSTEK 50808 analog-to-digital converter, and the evaluation of three NMOS op amps from TEXAM 0180. Four groups were formed from 17 students (only three of the four projects were fabricated). The design of each of the four analog-to-digital converters is described in more detail in a report on the class project [8].

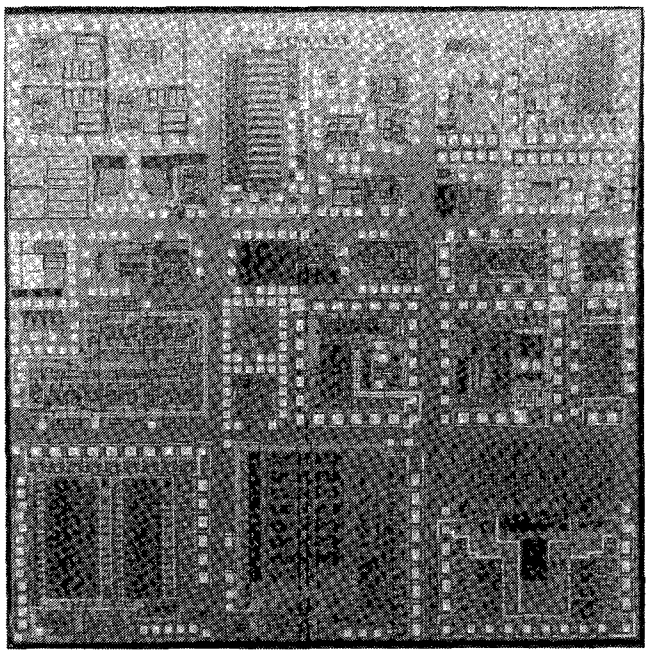

Fig. 7. Microphotograph of TEXAM 0181. This MPC is 338 mils X 338 mils and uses a double-poly NMOS process. Projects included on this MPC are listed in Table II.

The graduate program in microelectronics has benefitted immeasureably from the ability to conveniently fabricate integrated circuits using a state-of-the-art process. The program has tripled in the number of students taking courses. Disciplines which have normally remained separate have found a common ground in the microelectronic implementation of circuits. As a result of the motivation and enthusiasm, students are willing to undertake special projects devoted to the development of tools and techniques which make it more efficient to do the integrated circuit design. Many of the graduate research topics have been either directly or indirectly related to microelectronics. One of the difficulties here is to avoid coupling the successful performance of a circuit to the students' re-

TABLE II
PROJECTS ON TEXAM 0181

CIRCUIT	FUNCTION/OBJECTIVE	DESIGNERS
1PRAY	8 bit, two-step analog-to-digital converter using 30 comparators	Reese, Sridhar, Ferrell
2STEP	8 bit, two-step analog-to-digital converter using 15 comparators	Chaney, Fanini, Greaves, Richardson, and Weichold
3LOST	8 bit, analog-to-digital converter with 8 comparators	Bell, Hodapp, Homwongs, and Nguyen
ALAB1	Analog circuits for undergraduate microelectronic course	Fanini
BBLOK	Switched capacitor building block	Nguyen
CBSMX	Canonical bit-sequential digital multiplier	Becker, Vaglica
DLAB1	Digital circuits for undergraduate microelectronic course	Ledbetter
EATF1	Temperature to voltage converter	Tayefeh, Rybicki
EATF2	High frequency active filter	Tayefeh
EWION	Short channel transitional devices	Geiger
G5FIL	Fifth order switched capacitor, elliptic, low pass filter	Ismail
HSMUX	Bit-sequential multiplier based on (3:2) counter with shift control circuitry	Strader
IDPT3	Switched capacitor filter that utilizes a low power current amplifier as the active device	Perdomo-Teran
IDPT4	Switched capacitor filter utilizing current amplifiers	Perdomo-Teran
JIMB2	50KHz low pass switched resistor filter	Bass
QOTCH	4-bit ALU with two 4-bit registers and associated clock circuitry	White, Miller
SCOND	Input and output memory buffers	White
T1RD1	Test cell no. 1. Resistors and transistors	Nguyen
T2DA1	Test cell no. 2. Capacitance	Fanini
T3IOC	Test cell no. 3. Ring oscillator, inverter, and TI op amp.	Nguyen
T4ILT	Test cell no. 4. Inverter, alignment marks, identification	Fanini

search. Typically, the master's research is completed before the chip can be returned and evaluated.

MICROELECTRONICS EDUCATION AT THE UNDERGRADUATE LEVEL

It is clear that the microelectronic educational activity which now exists at the graduate level should be added to the undergraduate level. What is not clear is how to accomplish this objective. The undergraduate is not capable of the design and synthesis skills possessed by most graduate students. Consequently, this activity should be aimed at developing these skills for the undergraduate. It is also desirable to have the student associated with the technology and the integrated circuits so that he can begin to "close the loop." Another objective of teaching microelectronics at the undergraduate level is to teach the mechanics of designing integrated circuits. These mechanics include the use of the computer to analyze circuits at various levels of modeling, design rules, digitization procedures, verification, and testing.

The approach taken in the development of an undergraduate course in microelectronics which will be taught the first time in the fall 1981, is to use already designed and fabricated circuits to develop the design skills of the students. The approach will be to examine the principles involved in the operation and design of a particular circuit such as an inverter. This will be followed by computer analysis of the circuit to achieve its anticipated performance. Last, the student receives an integrated circuit which has been properly bonded and performs experimental measurements. It is hoped that from this

TABLE III
ANALOG INTEGRATED CIRCUIT LABORATORY CELL
(108 mils × 108 mils)

1. Voltage Reference: Show how to build voltage references independent of power supply and temperature.
2. Waveform Generator: Triangular and square wave generator.
3. Current Sinks/Sources: Depletion source and enhancement matching for current sinks.
4. Inverting Amplifier: The small signal performance of an inverter will be examined.
5. Differential Amplifier: The current sink will be used to bias a differential amplifier with depletion loads.
6. Operational Amplifier: Several NMOS op amps will be measured.
7. Switched Capacitor Filter: A first order, low pass filter will be examined. Development of non-overlapping clocks.
8. 4 Bit Digital-to-Analog converter

sequence the student will begin to develop the skills necessary for design. These activities will be accompanied by lectures on the principles of the circuits and how they were designed. In parallel, the course will introduce the mechanics of integrated circuit design referred to above. At the end of the course the students will be allowed to participate with a small project on the multiple project chip being fabricated that semester. At the termination of the course, the student should be in a good position to enter the microelectronic industry or to go on to graduate school and further develop his skills and knowledge in microelectronics.

The course content will emphasize MOS technology and cover both analog and digital circuits. Processing will be included as well as familiarization with the equipment used in the IC design process. All laboratory circuits have been fabricated on two 108 mil × 108 mil cells of TEXAM 0181. One of these cells is devoted to analog circuits and is the upper middle cell of Fig. 7. Table III gives a list of the circuits implemented on this cell. The other cell is the upper right cell of Fig. 7 and is devoted to digital circuits. Table IV indicates the circuits implemented on the digital laboratory cells. These two cells or chips will be extensively used in this course. In some cases, circuits on the cell can be used to assist in the testing of other circuits.

FUTURE PLANS

The future plans are exciting and filled with many challenges to both the student and the faculty. We plan to upgrade our capability to be able to interface with an industry such as Texas Instruments who is willing to fabricate our circuits. Approximately $200K has recently been spent to improve the computer capability including memory and graphics and the test and evaluation facilities. Many projects for improving our capability are underway. These projects include verification programs, mask generation using a laser system, and a flexible format allowing our intermediate form of digitization to be interfaced to other formats. Present plans also include the development of alternate methods of IC fabrication. Besides the industrial fabrication which already exists, other methods include making our own masks and to use a "silicon foundry," participating in government sponsored fabrication programs, or using our own solid-state laboratory for fabrication. The

TABLE IV
DIGITAL INTEGRATED CIRCUIT LABORATORY CELL
(108 mils X 108 mils)

1.	Inverter: The large signal characteristics of an inverter will be examined.
2.	Clock: A ring oscillator will be used to generate a clock. Transient time of an inverter will be measured. Two phase clock generator circuit
3.	Nand Gate: The characteristics of a Nand gate will be measured.
4.	Nor Gate: The characteristics of a Nor gate will be measured.
5.	Flip-Flop: The characteristics of a flip-flop will be measured. Several flip-flops will be used to divide the clock frequency.
6.	Registers: Four-stage shift register and a static/dynamic shift register.
7.	Programmable PLA: The use of PLA's to implement combinational logic will be examined.
8.	4 Bit Analog-to-Digital Converter

parallel ability to fabricate will permit a more efficient and effective use of the resources both within and without the university.

CONCLUSION

This paper has described some of the experiences of one university in the area of teaching microelectronics. We are not yet at the point where a teaching methodology for microelectronics can be proposed with confidence. The dynamic field of microelectronics would make this a risky proposition no matter how much experience was gained. The key seems to be an attitude of flexibility and the willingness to adapt and cooperate. The results so far have led to the development of a viable program in microelectronics. This program has resulted in a better prepared graduate for industry. A result of the program which is unmeasurable in its significance is the high degree of motivation and enthusiasm of those involved in it. This has resulted in a fresh insight into some of the problems that have existed in industry for some time. Another result of the program is an enhancement of university-industrial relationships.

The program has also identified many areas of weakness that need to be improved. Probably one of the more serious areas is the follow-up activity. At the present we select only those projects for fabrication which not only meet all the standards but have a strong possibility of follow-up. Another problem that can occur in a program such as this one is the use of an inadequate design procedure. By this we mean that because of time pressures and other factors, the problem is not well thought out and questions are answered by "let's try it and see" approach rather than making an effort to analyze and predict the results. Another problem that occurs when the university and fabrication facility are geographically separated is the need for a high-speed data link. Until such means are available, magnetic tape is the most reliable and convenient method of transporting the data bases describing the geometries.

The future holds some very interesting challenges to the university. Not only should the university strive to provide an appropriate education for the area of microelectronics but it should contribute to the state of the art in problems particularly suited for a university environment. One of these problems appears to be in the area of design methodology. The question of what the design process is in a complex circuit is one of the more challenging questions facing the educator. It is clear that since the exhaustion of present manpower for microelectronic design is a reality we must examine many of the fundamental processes which constitute design to look for areas of automation and efficiency.

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