Graphene Ambipolar Multiplier Phase Detector

Xuebei Yang, *Student Member, IEEE*, Guanxiong Liu, *Student Member, IEEE*, Masoud Rostami, *Student Member, IEEE*, Alexander A. Balandin, *Senior Member, IEEE*, and Kartik Mohanram, *Member, IEEE*

***Abstract*—We report the experimental demonstration of a multiplier phase detector implemented with a single top-gated graphene transistor. Ambipolar current conduction in graphene transistors enables simplification of the design of the multiplier phase detector and reduces its complexity in comparison to phase detectors based on conventional unipolar transistors. Fabrication of top-gated graphene transistors is essential to achieve the higher gain necessary to demonstrate phase detection. We report a phase detector gain of -7 mV/rad in this letter. An analysis of key technological parameters of the graphene transistor, including series resistance, top-gate insulator thickness, and output resistance, indicates that the phase detector gain can be improved by as much as two orders of magnitude.**

***Index Terms*—Ambipolarity, graphene, graphene field-effect transistor, phase detector.**

I. Introduction

SINCE its discovery in 2004 [1], graphene has attracted significant interest for electronics applications. Graphene has large intrinsic carrier mobility [2], excellent mechanical stability [3], and superior thermal conductivity [4]. Moreover, recent work has demonstrated graphene transistors with a cutoff frequency f_T of 26–300 GHz at a channel length on the order of 100 nm [5]–[7], and higher f_T is projected at smaller channel lengths. It has been also established that graphene transistors produce relatively low levels of $1/f$ noise [8], which contributes to the phase noise in the system via nonlinearity-induced upconversion. $1/f$ noise in top-gated graphene transistors is expected to be suppressed even further via proper design of the channel and contacts [9], with potential reductions in system noise levels. All these advantages have motivated significant interest and investment in the development of graphene as a potential candidate material for analog, mixed-signal, and radio-frequency (AMS/RF) systems.

Currently, most fabricated graphene transistors exhibit the ambipolar current conduction behavior [10]. By adjusting the gate–source and drain–source voltages, the ambipolar graphene transistor can be switched from n-type to p-type [10]–[12]. In analog electronics, this novel property has opened opportunities for increased functionality through nontraditional circuit architectures. For example, ambipolar graphene transistors have been used to demonstrate a frequency multiplier [13], [14], an RF mixer [15], and a triple-mode amplifier [16].

In this letter, we propose and experimentally demonstrate a multiplier phase detector utilizing a fabricated ambipolar top-gated single-layer graphene transistor. In comparison to the traditional implementation of the multiplier phase detector that requires multiple unipolar transistors, our proposed circuit requires only one transistor and one resistor, which greatly simplifies the design of the multiplier phase detector.

II. Graphene Multiplier Phase Detector

The multiplier phase detector is a vital component of the phase-locked loop, which is one of the most important building blocks in modern analog, digital, and communication circuits [17]. A multiplier phase detector takes two input signals, i.e., u_1 and u_2, and produces an output voltage that is proportional to the phase difference between u_1 and u_2. Usually, u_1 and u_2 are a sinusoidal signal and a square-wave signal, respectively [17]. Without loss of generality, we assume that

$$u_1(t) = U_{10}\ \sin(\omega_1 t + \theta_1) \text{ and } u_2(t) = U_{20}\,\mathrm{rect}(\omega_2 t + \theta_2) \tag{1}$$

where rect stands for rectangular, and U_{10} and U_{20}, ω_1 and ω_2, and θ_1 and θ_2 are the amplitudes, radian frequencies, and phases of u_1 and u_2, respectively. u_1 and u_2 are multiplied by the phase detector, and the high-frequency component of the result u_{out} is filtered out through a low-pass filter, leaving only the DC component u_{d}. If $\omega_1 = \omega_2$, u_{d} is given by

$$u_{\mathrm{d}}(t) = U_{10}U_{20}\frac{2}{\pi}\left(\sin(\theta_1 - \theta_2)\right) \approx K_{\mathrm{d}}\theta_{\mathrm{e}} \tag{2}$$

where K_{d} denotes the detector gain, and θ_{e} is the phase difference between the two input signals in radians.

Traditionally, u_1 and u_2 are multiplied by an analog multiplier built using multiple unipolar transistors. For example, a typical Gilbert cell analog multiplier [18] consists of six transistors and two resistors. However, in this letter, we leverage the ambipolarity of the graphene transistor to propose a simplified circuit structure requiring only a single top-gated graphene transistor and one resistor. The schematic of the graphene multiplier phase detector and an illustrative I_{DS}–V_{GS} curve of an ambipolar graphene transistor are presented in Fig. 1. In this proposed implementation of the multiplier phase detector, sinusoidal signal u_1 has a small amplitude. Square-wave signal u_2 serves as the bias voltage, and it is chosen so that the lower

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X. Yang and M. Rostami are with the Department of Electrical and Computer Engineering, Rice University, Houston, TX 77251-1892 USA (e-mail: xbyang@rice.edu; mrostami@rice.edu).

G. Liu and A. A. Balandin are with the Department of Electrical Engineering, University of California at Riverside, Riverside, CA 92521-0429 USA (e-mail: guliu@ee.ucr.edu; balandin@ee.ucr.edu).

K. Mohanram is with the Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA 15261 USA (e-mail: kartik.mohanram@gmail.com).

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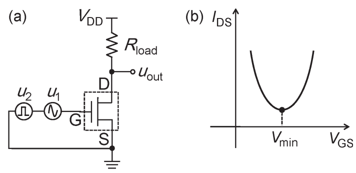

Fig. 1. (a) Schematic of the proposed graphene multiplier phase detector based on a single top-gated graphene transistor and an off-chip resistor R_{load}. u_{out} is the output of the phase detector. (b) Illustration of the typical ambipolar I_{DS}–V_{GS} curve. $V_{\min}$ is the voltage, where I_{DS} is the minimum.

and higher levels of u_2, denoted as V_{low} and V_{high}, satisfy $V_{\mathrm{low}} < V_{\min}$ and $V_{\mathrm{high}} > V_{\min}$, respectively. Here, $V_{\min}$ is the minimum conduction point of the ambipolar graphene transistor. When $u_2 = V_{\mathrm{low}}$ (V_{high}), I_{DS} of the graphene transistor decreases (increases) as the gate voltage increases, and the voltage drop across the resistor decreases (increases), thereby increasing (decreasing) u_{out}. Therefore, the voltage gain of the circuit $\partial u_{\mathrm{out}}/\partial u_1$ is positive (negative). As a result, the gain of the circuit G is also a square wave that switches between positive and negative values. Since $u_{\mathrm{out}} = G u_1$, the product of u_1 and u_2 has been transformed into the product of u_1 and G, which is inherently produced by the proposed circuit.

III. Graphene Transistor Fabrication

In this letter, the proposed multiplier phase detector is demonstrated using a fabricated top-gated graphene transistor. Our graphene flakes are exfoliated from a high-quality graphite source highly oriented pyrolytic graphite onto a Si/SiO_2 substrate, where the thickness of SiO_2 is 300 nm. The graphene flakes are selected by Raman spectroscopy through the 2D band deconvolution and $I(\mathrm{G})/I(\mathrm{2D})$ intensity comparison [19], where the Lorentzian fit gives full-width at half-maximum of 27.8 cm^{-1} for 2D peak. In this letter, a two-layer oxide fabrication method is used to grow a high-quality insulator on graphene [20]. The first layer serves as an adhesive layer between graphene and the following atomic layer deposition (ALD) oxide. This layer is self-oxidized AlO_x that is made by evaporation of a very thin layer of Al and stored at room temperature. The second layer is Al_2O_3 grown by ALD. Owing to the good adhesion of the first layer, the second ALD Al_2O_3 layer can uniformly grow. The total thickness of the top-gate oxide stack examined by AFM is about 23 nm. The source, drain, and top-gate electrodes are defined by e-beam lithography, followed by evaporation of Ti/Au (6/60 nm). The width and the length of graphene under the top gate are 2.98 and 1.28 μm, respectively. The top-gate insulator capacitance is evaluated to be approximately 360 nFcm^{-2}, the mobility is 2100 $\mathrm{cm}^2\mathrm{V}^{-1}\mathrm{s}^{-1}$, and the contact resistance is 5 k$\Omega\mu$m. The image of the fabricated graphene transistor and the electrical characteristics are shown in Fig. 2. All measurements were performed under ambient conditions.

IV. Graphene Multiplier Phase Detector

To demonstrate our proposed graphene multiplier phase detector in Fig. 1(a), R_{load} is set to 20 kΩ, V_{DD} to 1.8 V, and the frequency of both u_1 and u_2 to 100 kHz. In Fig. 3, we present the output u_{out} of the circuit at different phase differences θ_{e} between u_1 and u_2. Since I_{DS} of the graphene transistor is not identical at V_{low} and V_{high}, there will be a "stair" in the

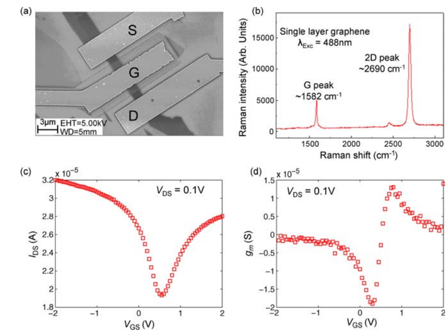

Fig. 2. (a) SEM image of a representative fabricated top-gated graphene transistor. (b) Raman spectrum of the single-layer graphene. (c) I_{DS}–V_{GS} characteristics of the graphene transistor for $V_{\mathrm{DS}} = 0.1$ V. (d) Transconductance g_m–V_{GS} characteristics for $V_{\mathrm{DS}} = 0.1$ V.

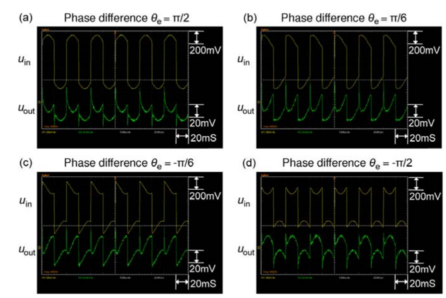

Fig. 3. Output u_{out} versus $u_{\mathrm{in}} = u_1 + u_2$ for (a) $\theta_{\mathrm{e}} = (\pi/2)$. (b) $\theta_{\mathrm{e}} = (\pi/6)$. (c) $\theta_{\mathrm{e}} = -(\pi/6)$. (d) $\theta_{\mathrm{e}} = -(\pi/2)$.

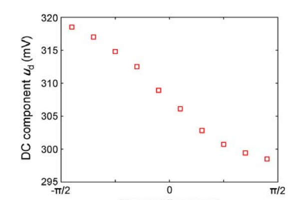

Fig. 4. DC component u_{out} at different θ_{e} between u_1 and u_2.

output u_{d} between the two halves in a cycle. However, this "stair" is caused only by u_2 and is not related to the phase difference between u_1 and u_2. Therefore, it will not affect the performance of the phase detector, which is the difference in the DC component u_{d} of u_{out} at different phase differences θ_{e}. In Fig. 3, it can be observed that at $\theta_{\mathrm{e}} = (\pi/2)$ rad, the circuit is biased in the negative gain condition for the positive half of u_1 and in the positive gain condition for the negative half of u_1. Hence, output u_{out} has the smallest DC component at $\theta_{\mathrm{e}} = (\pi/2)$ rad. In contrast, at $\theta_{\mathrm{e}} = -(\pi/2)$ rad, the circuit is biased in the positive gain condition for the positive half of u_1 and in the negative gain condition for the negative half of u_1. Hence, output u_{out} has the largest DC component at $\theta_{\mathrm{e}} = -(\pi/2)$ rad. The circuit voltage gain $\partial u_{\mathrm{out}}/\partial u_1$ is ≈ 0.1, which is approximately one order of magnitude larger than previous values reported in literature [13], [16]. This improvement in gain can be attributed to the use of top-gated graphene transistors in the design of the multiplier phase detector, and it directly leads to the increase in detector gain K_{d}. In Fig. 4, we have shown the DC component u_{d} at different θ_{e}. As the phase difference goes from $\pi/2$ to $-(\pi/2)$ rad, u_{d} increases from 298 to 319 mV, which corresponds to a detector gain $K_{\mathrm{d}} \approx -7$ mV/rad.

V. Discussion

Currently, due to the immature graphene transistor fabrication technology, the detector gain K_d of the proposed graphene multiplier phase detector is approximately two orders of magnitude lower than the detector gain of traditional multiplier phase detectors [21]. For the proposed graphene multiplier phase detector, K_d is directly proportional to the circuit voltage gain G, which is proportional to the transconductance g_m and R_total to the first order. Here, $R_\mathrm{total} = (R_\mathrm{load}R_\mathrm{O}/R_\mathrm{load} + R_\mathrm{O})$ is the parallel combination of the load resistance R_load and the output resistance R_O of the graphene transistor [16]. Here, we use the graphene transistor model in [22] to study the impact of improving g_m and R_total on detector gain K_d.

Improve g_m: g_m can be improved by reducing the contact resistance R_s and the thickness t_ins of the insulator Al_2O_3. Currently, $R_\mathrm{s} = 5$ k$\Omega\mu$m, and $t_\mathrm{ins} = 23$ nm for our graphene transistor. A recent study [23] has shown that by using the self-aligned fabrication technique, the top gate can completely cover the graphene sheet inside the channel, thereby reducing the access region resistance by as much as 10×. Our simulations indicate that reducing R_s by 10× can effectively increase g_m by 10×. However, as R_s further reduces, the improvement in g_m is marginal. In contrast, if $R_\mathrm{s} = 5$ k$\Omega\mu$m, reducing t_ins by 10× will not result in significant improvement of g_m, but if R_s has been reduced by 10×, reducing t_ins by 10× can further improve g_m by 10×, resulting in 100× improvement in g_m overall. Hence, we conclude that, currently, contact resistance R_s is the limiting factor for the improvement of g_m. As R_s is reduced, however, t_ins will dominate the value of g_m. Note that reducing t_ins and hence increasing the top-gate capacitance will not yield an unlimited increase in g_m, which is capped by the inherent quantum capacitance of graphene. However, the investigation of fundamental limitations of g_m is out of the scope of this letter.

Improve R_total: R_total is the parallel combination of R_load and R_O. Currently, R_O is on the order of kΩ, which is comparable to R_load. Since an increase in g_m leads to an increase in I_DS, the output resistance R_O and, hence, R_total are reduced as a result. Hence, although our simulations indicate that g_m can be potentially improved by 100× by reducing both R_s and t_ins by 10×, the circuit gain will only increase by 5×. In order to preserve the effect of improvements in g_m, the graphene transistor should be kept in the saturation region such that $R_\mathrm{O} \gg R_\mathrm{load}$, ensuring that the reduction in R_O due to improvements in g_m will not significantly decrease R_total. Under such conditions, the increase in g_m can be completely transformed into the increase in circuit gain.

VI. Conclusion

We have proposed and experimentally demonstrated a single-transistor graphene multiplier phase detector. By leveraging the in-field controllability of ambipolar conduction in the graphene transistor, the proposed circuit realizes phase detection with a detector gain of -7 mV/rad. Our analysis indicates that by 1) reducing the series resistance, 2) decreasing the gate insulator thickness, and 3) keeping the transistor in the saturation region, the detector gain can be potentially improved by 100×.

References

[1] K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric field effect in atomically thin carbon films," *Science*, vol. 306, no. 5696, pp. 666–669, Oct. 2004.

[2] K. Bolotin, K. J. Sikes, Z. Jiang, M. Klima, G. Fudenberg, P. K. J. Hone, and H. L. Stormer, "Ultrahigh electron mobility in suspended graphene," *Solid State Commun.*, vol. 146, no. 9/10, pp. 351–355, Jun. 2008.

[3] C. Lee, X. Wei, J. Kysar, and J. Hone, "Measurement of the elastic properties and intrinsic strength of monolayer graphene," *Science*, vol. 321, no. 5887, pp. 385–388, Jul. 2008.

[4] A. A. Balandin, S. Ghosh, W. Bao, I. Calizo, D. Teweldebrhan, F. Miao, and C. Lau, "Superior thermal conductivity of single-layer graphene," *Nano Lett.*, vol. 8, no. 3, pp. 902–907, Mar. 2008.

[5] Y. Lin, K. A. Jenkins, A. Valdes-Garcia, J. P. Small, D. B. Farmer, and P. Avouris, "Operation of graphene transistors at gigahertz frequencies," *Nano Lett.*, vol. 9, no. 1, pp. 422–426, Jan. 2009.

[6] Y.-M. Lin, C. Dimitrakopoulos, K. A. Jenkins, D. B. Farmer, H.-Y. Chiu, A. Grill, and P. Avouris, "100-GHz transistors from wafer-scale epitaxial graphene," *Science*, vol. 327, no. 5966, p. 662, Feb. 2010.

[7] L. Liao, Y.-C. Lin, M. Bao, R. Cheng, J. Bai, Y. Liu, Y. Qu, K. L. Wang, Y. Huang, and X. Duan, "High-speed graphene transistors with a self-aligned nanowire gate," *Nature*, vol. 467, no. 7313, pp. 305–308, Sep. 2010.

[8] Y.-M. Lin and P. Avouris, "Strong suppression of electrical noise in bilayer graphene nanodevices," *Nano Lett.*, vol. 8, no. 8, pp. 2119–2125, Aug. 2008.

[9] S. Rumyantsev, G. Liu, W. Stillman, M. Shur, and A. A. Balandin, "Electrical and noise characteristics of graphene field-effect transistors: Ambient effects, noise sources and physical mechanisms," *J. Phys.: Condens. Matter*, vol. 22, no. 39, p. 395302, Oct. 2010.

[10] F. Schwierz, "Graphene transistors," *Nat. Nanotechnol.*, vol. 5, no. 7, pp. 487–496, Jul. 2010.

[11] Y. Ouyang, Y. Yoon, and J. Guo, "Scaling behaviors of graphene nanoribbon FETs: A 3D quantum simulation," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2223–2231, Sep. 2007.

[12] Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, and J. Guo, "Performance comparison of graphene nanoribbon FETs with Schottky contacts and doped reservoirs," *IEEE Trans. Electron Devices*, vol. 55, no. 9, pp. 2314–2323, Sep. 2008.

[13] H. Wang, D. Nezich, J. Kong, and T. Palacios, "Graphene frequency multipliers," *IEEE Electron Device Lett.*, vol. 30, no. 5, pp. 547–549, May 2009.

[14] Z. Wang, Z. Zhang, H. Xu, L. Ding, S. Wang, and L.-M. Peng, "A high-performance top-gate graphene field-effect transistor based frequency doubler," *Appl. Phys. Lett.*, vol. 96, no. 17, p. 173104, Apr. 2010.

[15] H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-based ambipolar RF mixers," *IEEE Electron Device Lett.*, vol. 31, no. 9, pp. 906–908, Sep. 2010.

[16] X. Yang, G. Liu, A. A. Balandin, and K. Mohanram, "Triple-mode single-transistor graphene amplifier and its applications," *ACS Nano*, vol. 4, no. 10, pp. 5532–5538, Oct. 2010.

[17] J. A. Crawford, *Advanced Phase-Lock Techniques*. Norwood, MA: Artech House, 2008.

[18] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Hoboken, NJ: Wiley, 2001.

[19] I. Calizo, F. Miao, W. Bao, C. N. Lau, and A. A. Balandin, "Variable temperature Raman microscopy as a nanometrology tool for graphene layers and graphene-based devices," *Appl. Phys. Lett.*, vol. 91, no. 7, p. 071913, Aug. 2007.

[20] S. Kim, J. Nah, I. Jo, D. Shahrjerdi, L. Colombo, Z. Yao, E. Tutuc, and S. Banerjee, "Realization of a high mobility dual-gated graphene field-effect transistor with Al_2O_3 dielectric," *Appl. Phys. Lett.*, vol. 94, no. 6, p. 062107, Feb. 2009.

[21] B. Tzeng, C.-H. Lien, H. Wang, Y.-C. Wang, P.-C. Chao, and C.-H. Chen, "A 1–17-GHz InGaP–GaAs HBT MMIC analog multiplier and mixer with broad-band input-matching networks," *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 11, pp. 2564–2568, Nov. 2002.

[22] I. Meric, M. Y. Han, A. F. Young, B. Ozyilmaz, P. Kim, and K. L. Shepard, "Current saturation in zero-bandgap, top-gated graphene field-effect transistors," *Nat. Nanotechnol.*, vol. 3, no. 11, pp. 654–659, Nov. 2008.

[23] D. Farmer, Y.-M. Lin, and P. Avouris, "Graphene field-effect transistors with self-aligned gates," *Appl. Phys. Lett.*, vol. 94, no. 1, p. 013 103, Jul. 2010.