THESIS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

Graphene field-effect transistors and devices for advanced high-frequency applications

Fabrication, characterisation and analysis of limitations

MARLENE BONMANN

Department of Microtechnology and Nanoscience - MC2
CHALMERS UNIVERSITY OF TECHNOLOGY
Göteborg, Sweden 2019.

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ISBN 978-91-7905-237-9

Doktorsavhandlingar vid Chalmers Tekniska Högskola
Ny serie nr 4704
ISSN 0346-718X
Department of Microtechnology and Nanoscience - MC2
Chalmers University of Technology
SE-412 96 Göteborg
Sweden
Telephone: +46 (0)31-772 1000

Cover:
Top-left: Schematic cross section of a MOSFET or GFET with one gate finger. Top-right: Infrared image of a GFET. Bottom: SEM image of GFET.

Chalmers Reproservice
Göteborg, Sweden 2019.

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Abstract

New device technologies and materials are continuously investigated, in order to increase the bandwidth of high-speed electronics, thereby extending data rate and range of applications. The 2D-material graphene, with its intrinsically extremely high charge carrier velocity, is considered as a promising new channel material for advanced high frequency field-effect transistors. However, most fabrication processes introduce impurities and defects at the interface between graphene and adjacent materials, which degrade the device performance. In addition, at high drain fields, required for high transistor gain, the close proximity of the adjacent materials limits the saturation velocity, and there is a significant increase in the channel temperature caused by self-heating.

In this thesis, the influence of impurities and defects on charge transport, the limitations of the saturation velocity, and the effect of velocity saturation and self-heating on the transit frequency f_{T} and the maximum frequency of oscillation f_{max} of graphene field effect transistor (GFETs) are analysed. In addition, GFETs with state-of-the-art extrinsic $f_{\mathrm{T}} = 34\,\mathrm{GHz}$ and $f_{\mathrm{max}} = 37\,\mathrm{GHz}$, and an integrated 200-GHz GFET based receiver are presented. Also, through the development of a fabrication process of GFETs with a buried gate configuration, this work contributed to the direct nanoscopic observation of plasma waves in the GFET channel during terahertz illumination.

The study was conducted by (i) setting up a model describing the influence of impurities and defects on capacitance and transfer characteristics at low electric fields, (ii) by developing a method for studying the limiting mechanisms of the charge carrier velocity in the graphene channel at high electric fields and answering the question whether velocity saturation improves f_{max}, (iii) by developing a method to study the channel temperature and its effect on f_{T} and f_{max}. It was found that scattering by remote optical phonons limits the saturation velocity and charge carriers emitted from interface states at high fields are preventing the current to saturate and, hence, limiting f_{T} and f_{max}. Additionally, the study shows that the channel temperature in GFETs can increase significantly causing degradation of the high frequency performance due to the decrease of charge carrier mobility and velocity. In summary, this work shows that it is necessary to develop a GFET design and fabrication process providing clean and defect-free interfaces, to minimise parasitic effects, and to use materials with higher optical phonon energies and higher thermal conductivities than those used today. This will allow for realisation of GFETs with extrinsic f_{T} and f_{max} in the sub-terahertz range.

Keywords: graphene, field-effect transistors, microwave devices, saturation velocity, traps, impurities and defects, remote phonons, carrier transport, self-heating

List of publications

This thesis is based on the work contained in the following papers:

Paper A **M. Bonmann**, A. Vorobiev, J. Stake, and O. Engström. 'Effect of oxide traps on channel transport characteristics in graphene field effect transistors.' *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics: Materials, Processing, Measurement, and Phenomena* **35**, 01A115 (2017), doi:10.1116/1.4973904.

Paper B **M. Bonmann**, M. A. Andersson, A. Vorobiev, and J. Stake. 'Charge carrier velocity in graphene field-effect transistors.' *Applied Physics Letters* **111**, 233505 (2017), doi:10.1063/1.5003684.

Paper C **M. Bonmann**, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake. 'Graphene Field-Effect transistors With High Extrinisc f_{T} and f_{max}.' *IEEE Electron Device Letters* **40**, pp. 131-143 (2019), doi:10.1109/LED.2018.

Paper D **M. Bonmann**, M. Krivic, X. Yang, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, and J. Stake. 'Effects of Self-Heating on f_{T} and f_{max} Performance of Graphene Field-Effect Transistors.' submitted to the journal *IEEE Transactions on Electron Devices*, Aug., 2019.

Paper E P. Feijoo Guerro, F. Pasadas, **M. Bonmann**, M. Asad, X. Yang, A. Generalov, A. Vorobiev, L. Banszerus, C. Stampfer, M. Otto, D. Neumaier, J. Stake, and D. Jiménez, 'Does carrier velocity saturation help to enhance f_{max} in graphene field-effect transistors?' submitted to the journal *Nanoscale Advances*, Nov. 2019.

Paper F **M. Bonmann**, M. A. Andersson, Y. Zhang, X. Yang, A. Vorobiev, and J. Stake. 'An Integrated 200-GHz Graphene FET Based Receiver,' extended paper in *proceedings IRMMW-THz 2018*, doi:10.1109/IRMMW-THz.2018.8510069.

Paper G A. Soltani, F. Kuschewski, **M. Bonmann**, A. Generalov, A. Vorobiev, F. Ludwig, M. Wiecha, D. Čibaraitė, F. Walla, S. Kehr, L. Eng, J. Stake, and H. G. Roskos, 'Direct nanoscopic observation of plasma waves in channels of graphene field-effect transistors.' submitted to the journal *Light: Science & Applications*, Jul. 2019.

Nomenclature

$\hbar = 6.58 \times 10^{-16}$	[eV·s]	reduced Planck constant
$\hbar\omega_{\mathrm{OP}}$	[meV]	optical phonon energy
$k_{\mathrm{B}} = 8.62 \times 10^{-5}$	[eV·K^{-1}]	Boltzmann constant
τ	[s]	delay time
$\epsilon_0 = 8.85 \times 10^{-12}$	[F·m^{-1}]	vacuum permittivity
ϵ		relative permittivity
κ	[W·cm^{-1}·K^{-1}]	thermal conductivity
C_{ox}	[F·m^{-2}]	oxide capacitance
C_{g}	[F]	gate capacitance
C_{gd}	[F]	gate-drain capacitance
C_{gs}	[F]	gate-source capacitance
C_{PG} and C_{PD}	[F]	parasitic gate/drain pad capacitances
$e = 1.6 \times 10^{-16}$	[C]	elementary charge
$E_{\mathrm{DS,(int)}}$	[kV·μm^{-1}]	(intrinsic) electric field
E_{F}	[eV]	Fermi energy
E_{g}	[eV]	bandgap energy
$f_{\mathrm{max,(int)}}$	[Hz]	(intrinsic) maximum frequency of oscillation
$f_{\mathrm{T,(int)}}$	[Hz]	(intrinsic) transit frequency
g_{ds}	[S]	output conductance
σ_{ds}	[S]	output conductivity
g_{m}	[S]	transconductance
I_{DS}	[A]	drain current
l	[nm]	mean free path
L_{g}	[μm]	gate length
L_{a}	[μm]	access area length
μ_0	[cm^2·V^{-1}·s^{-1}]	low-field mobility
μ	[cm^2·V^{-1}·s^{-1}]	mobility
n	[m^{-2}]	charge carrier concentration
n_0	[m^{-2}]	residual charge carrier concentration
n_{imp}	[m^{-2}]	charged impurity concentration
n_{th}	[m^{-2}]	thermally generated charge carrier concentration
$P_{\mathrm{diss,(int)}}$	[mW]	(intrinsic) dissipated power
$P_{\mathrm{density,(int)}}$	[mW·μm^{-2}]	(intrinsic) dissipated power density
ρ_{C}	[$\Omega \cdot \mu$m]	specific width contact resistivity
R_{C}	[Ω]	contact resistance
R_{D}	[Ω]	drain resistance
R_{G}	[Ω]	gate resistance
R_{S}	[Ω]	source resistance
r_{i}	[Ω]	charging resistance of gate-source capacitance
R_{th}	[K·mW^{-1}]	thermal resistance

T	[K]	Temperature
t_b	[μm]	bottom oxide thickness
t_s	[μm]	substrate thickness
t_ox	[μm]	(top) oxide thickness
$v_\mathrm{F} \sim 10^6$	[m·s^{-1}]	Fermi velocity
v	[m·s^{-1}]	charge carrier velocity
v_sat	[m·s^{-1}]	charge carrier velocity
$V_\mathrm{GS,(int)}$	[V]	(intrinsic) gate-source voltage
$V_\mathrm{DS,(int)}$	[V]	(intrinsic) drain-source voltage
V_Dir	[V]	Dirac voltage
W_g	[μm]	gate width

Abbreviations

FET	field-effect transistor	BOE	buffered oxide etch
GFET	graphene FET	CVD	chemical vapor deposition
MOSFET	metal-oxide-seminconductor FET	rf	radio frequency
HEMT	high-electron-mobility transistor	R-V	resistance-voltage
SiO_2	silicon dioxide	I-V	current-voltage
hBN	hexagonal boron nitride	C-V	capacitance-voltage
S-parameters	scattering parameters		

Contents

Chapter 1

Introduction

The long-sighted goal of this work is to develop devices for advanced electronics applications in the emerging areas of high-speed communication, terahertz sensing, and imaging [1, 2]. The relevant frequency ranges in this context are the extended microwave frequency region (200 MHz to 300 GHz), where applications range from communication to radar, GPS and many more, and the field of terahertz frequencies (300 GHz to 10 THz), where applications are mostly limited to space applications, such as remote sensing and spectroscopy [3], because water in the Earth's atmosphere strongly attenuates THz radiation [4]. However, due to continued technology development the generated output power by THz sources has been increased [1]. This allows for utilisation of THz radiation in security imaging systems [5], in diagnostic tools in medicine and life sciences [6] and in high-speed communication networks [7]. An elementary component for the successful realisation of these applications are fast transistors, which are elementary components of all electronic devices.

The first bipolar transistor was based on the semiconductor material germanium. It was demonstrated in 1947 by Shockley, Bardeen and Brattain who were awarded the Nobel prize for their work. Today, transistors based on silicon, i.e. metal-oxide-semiconductor field-effect transistor (MOSFET), are the most common. The material is the second most abundant in the Earth's crust [8], and the technology is very mature. Other successful transistor technologies are high-electron-mobility transistors (HEMTs) based on gallium arsenide (GaAs) [9] or indium phosphide (InP) [10]. Over the past years, the gate length of MOSFETS has been continuously reduced to reach higher operating speeds. However, the scaling of the MOSFET technology is about to reach its fundamental limits. Therefore, new device technologies, such as nanowire MOSFETs [11] and vacuum channel transistors [12], and new materials with higher charge carrier velocities are explored for the application in transistors. The extremely high intrinsic charge carrier mobility and velocity in the 2D-material graphene, superior to those in the semiconductor counterparts, have attracted attention for using graphene as a potential channel material in high-frequency field-effect transistors (FETs). Furthermore, the atomical thickness of graphene helps to reduce short channel effects, which become more prominent as the gate length is scaled down, due to increased electrostatic control [13].

The band structure and electrical properties of a monolayer of graphite, i.e., graphene, was first theoretically described in 1947 by P.R. Wallace *et al.* [14]. However, it was not until 2004 that graphene was separated from graphite by K. S. Novoselov *et al.* [15] and its thermodynamic stability along with the electric field effect in graphene could be proven. Graphene is unique in that it combines high room-temperature charge carrier velocity (6×10^7cm/s on hBN [16]), high thermal conductivity (suspended graphene $(1-5.3)\times10^3$ W/m·K [17, 18]), mechanical strength, bendability and transparency in a single material. Graphene absorbs 2.3% of incident visible light [19]. This can be exploited in a number of emerging applications, such as transparent, stretchable electrodes [20, 21] and flexible

electronics [22].

The challenge of utilising graphene for transistor applications is its lack of a bandgap. It is not possible to achieve a high ratio between the on and off currents and a very small leakage current with graphene field-effect transistor (GFET), which makes it inapplicable for switching applications. Therefore, it is not possible to efficiently use graphene in logic circuits. Rather, research focuses on applications such as microwave amplifiers, mixers, power detectors and terahertz photonics [23, 24, 25, 26, 27, 28]. The first top-gated GFETs were developed in 2007 [29], followed by the development of subharmonic resistive mixers utilizing the symmetrical channel resistance vs. gate voltage characteristic of GFETs [30, 24] and a GFET amplifier operating at 1 GHz [23], leading to the demonstration of integrated components and circuits [31, 32], and the receiver composed by a graphene FET 200 GHz mixer and a 1 GHz intermediate frequency amplifier integrated on silicon substrate as presented in PAPER C. In PAPER G we report on the direct observation of plasma waves in the GFET channel under terahertz illumination.

For amplifier applications, power gain and current gain are important parameters of a transistor. The figures of merit related to the power and current gain are the maximum frequency of oscillation ($f_{\max}$) and the transit frequency (f_{T}), respectively. Another figure of merit is the noise figure which is not addressed in this work. The microwave noise characterization of graphene field effect transistors and terahertz detectors is analysed in [33, 34]. Figure 1.1 summarises the state-of-the-art f_{T} and $f_{\max}$ of different device technologies. It is important to distinguish between extrinsic and intrinsic parameters. Often intrinsic performances are presented, leading to miss-interpretation if they are compared with extrinsic performances of the devices. The intrinsic values are obtained by de-embedding the measurements to exclude the effects of the parasitic capacitance, resistance, and inductance associated with the contact pads of the transistors [51]. Figure 1.1 shows that GFETs compete well with other transistor technologies when comparing f_{T} at similar gate lengths. Values of $f_{\mathrm{T,int}}$ of 407 GHz was achieved in GFETs with a gate length of L_{g} =100 nm using bilayer graphene on a silicon carbide (SiC) substrate [49]. However, GFETs perform quite poorly in terms of $f_{\max}$ compared to transistors based on other material systems, such as InAs PHEMTs with $f_{\mathrm{T}} = 644$ GHz, $f_{\max} = 681$ GHz [42], GaAs mHEMT with $f_{\mathrm{T}} = 688$ GHz, $f_{\max} = 800$ GHz [43], and InP HEMT with $f_{\max} = 1$ THz [10]. For GFETs the highest $f_{\mathrm{max,int}}$ is 120 GHz with gate lengths of $L = 200$ nm [49].

This poor performance is due to the lack of a bandgap and the associated poor current saturation, which leads to a high drain conductance. Additionally parasitic capacitances and resistances degrade the performance. Attempts were made to induce a bandgap in graphene, but when inducing a bandgap, the carrier mobility rapidly decreases. In conclusion, in terms of mobility and for a given bandgap, graphene does not offer a distinct advantage over conventional semiconductors [52]. Current saturation can also be achieved when the velocity of the charge carriers saturates [53]. This work considers the development of this approach and the impact of velocity saturation on the high-frequency performance is studied in PAPER E. In PAPER C, the design, technology and fabrication of GFETs with state-of-the-art f_{T} and $f_{\max}$ and promising scaling down behaviour were demonstrated. At similar gate lengths, the values of extrinsic f_{T} and $f_{\max}$ are higher than those of the best published GFETs and comparable or even higher of the best published Si

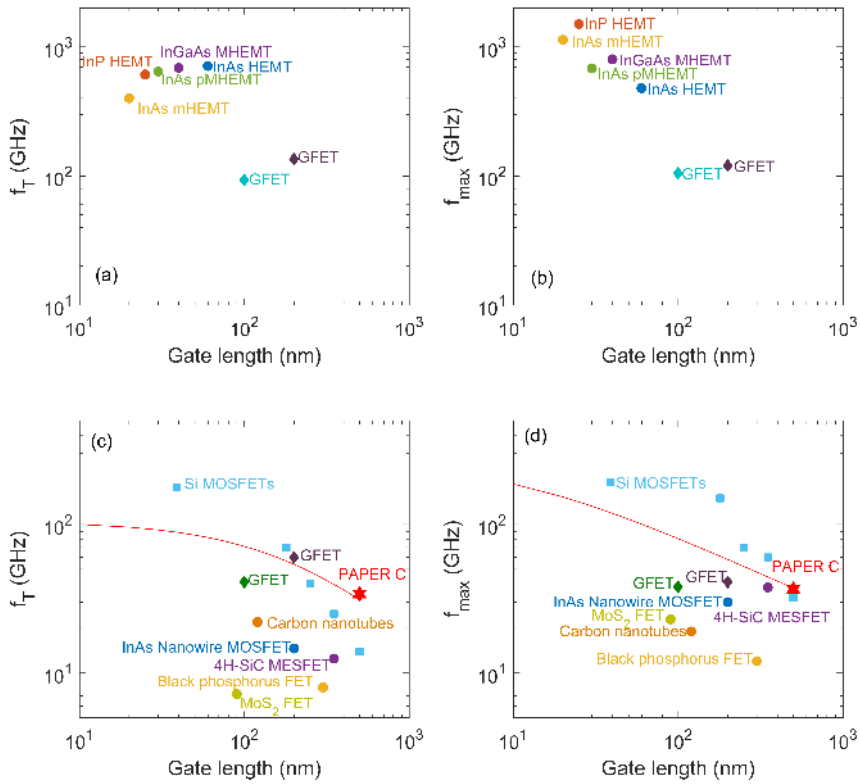

Figure 1.1: State-of-the-art intrinsic (a) f_T and (b) f_{max} and extrinsic (c) f_T and (d) f_{max} for different HEMT and FET technologies (circles) [10, 35, 36, 37, 38, 39, 40, 41, 42, 43, 11], Si MOSFETs (squares) [44, 45, 46, 47] and GFETs [48, 49, 50] (diamonds) as well as for the GFET presented in PAPER C (star).

MOSFETs, see Fig. 1.1. The theoretically achievable intrinsic high-frequency performance limit of a top-gated GFET has been estimated to be approximately $f_{T,int}$=640 GHz at a channel length of 100 nm and approximately 3.7 THz at a channel length of 20 nm [54].

A clean fabrication process and high-quality interfaces between graphene and adjacent materials are needed for high and reliable performance of GFETs. Critical steps are the growth of high-quality graphene, a clean transfer process from the growth substrate to the target substrate, and a clean fabrication process of the device. It remains challenging to achieve high conformity in performance between GFETs on the same substrate. It has been shown that super-clean graphene can actually reach the theoretically predicted mobility limit at cryogenic temperatures of $2\times10^5\,\mathrm{cm^2V^{-1}s^{-1}}$ [55], but as soon as graphene comes into contact with another material, its mobility degrades severely due to the inclusion of

impurities and remote phonon scattering [56, 57]. In GFETs, there is at least one substrate-graphene interface involved, when the transistor is backgated, and even two interfaces have to be considered for a top-gated GFET. Due to impurities and defects in the oxide and due to adsorbates at unprotected areas, the typical transfer and the capacitance versus gate voltage characteristics exhibit hysteresis [58, 59]. This is caused by charge transfer in and out of interface states associated with impurities. Therefore, it is important to study how impurities effect the charge transport in GFETs as is done in this work. In Paper A, a model was developed to describe how oxide traps affect the capacitance and transfer characteristics and it allows to study how these affect the extracted values of mobility, and residual charge carrier concentration, as well as to study how uncertainties in the parameters affect the extracted values. In Paper B, a model and method is presented for evaluation of the channel velocity in GFETs, via delay-time analysis, establishing relations between saturation velocity, extrinsic/intrinsic transit frequency, and concentration of charged impurities. This allows for understanding of the limitation of charge carrier velocity at high fields. Another limitation is the considerable increase of the channel temperature in GFETs operating under high drain bias, which is required for power gain. Self-heating at high fields as discussed in PAPER D, which provides a method to analyse the effect of self-heating on high-frequency performance of GFETs. In summary, this work contains the device modelling, fabrication, characterisation, and analysis of GFETs, with the aim to understand the limiting factors of the high-frequency performance of GFETs with the presented methods, and provide guidelines for further development.

1.1 Thesis outline

The following chapters serve as complementary background information for the content presented in the appended papers. In Chapter 2 the general working principle of FETs, the difference between GFETs and MOSFETs, and graphene properties for high-frequency FETs are explained. In Chapter 3 the fabrication process and device characterisation techniques are presented. The effect of impurities, defects and self-heating on f_{T} and f_{max} are discussed in Chapter 4. Finally, the main results are concluded in Chapter 5 with discussion of possible future pathways.

Chapter 2

Graphene field-effect transistors

In this chapter the operating principle of field-effect transistors and the figures of merit for current gain and power gain of rf transistors are introduced. The distinguishable features of graphene field-effect transistors compared to other transistor technologies are discussed and associated with graphene-specific properties.

2.1 Operation principle of FETs

Field-effect transistors are active electronic components that can be found in any electronic device. The name field-effect transistor arises from the utilisation of the field effect in this type of transistor [60]. The field effect entails the modulation of the current between a drain and source terminals with potentials of, V_{D} and V_{S}, respectively, through the application of an out-of-plane electric field on the gate terminal by applying a gate potential V_{G}. The current through the channel is either modulated by altering the channel height or by changing the charge carrier concentration in the channel. Junction field-effect transistors (JFETs) and metal-semiconductor field-effect transistors (MESFETs) belong to the former group, whereas in MOSFETs, HEMTs and GFETs, the carrier concentration is changed. In GFETs, it is even possible to change the majority charge carrier type in the channel due to lack of bandgap in graphene. Figure 2.1 shows a schematic cross section of a MOSFET structure.

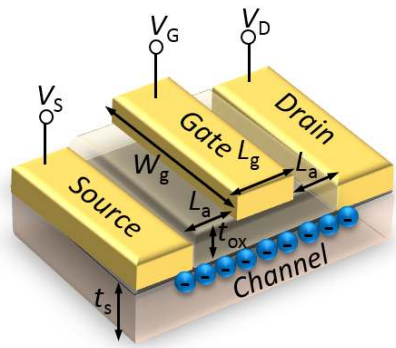

Figure 2.1: Schematic cross section of a MOSFET or GFET with one gate finger. The gate, drain and source contacts, the corresponding potentials, the gate width W_{g}, the gate length L_{g}, the ungated access area length L_{a}, the substrate thickness t_{s}, and oxide thickness t_{ox} are labeled and the channel region is illustrated with circles.

2.2 DC characteristics of GFETs vs MOSFETs

The current density in the channel of a field-effect transistor is expressed as:

$$J = e \cdot n \cdot v, \tag{2.1}$$

where e is the elementary charge, n is the charge carrier concentration, and v is the charge carrier drift velocity. The charge carrier concentration n is modulated by applying a gate voltage V_{GS} as explained in Section 2.4.2, whereas the charge carrier drift velocity depends on the in-plane electric field between the source and drain $E_{\mathrm{int}} = V_{\mathrm{DS,int}}/L_{\mathrm{g}}$, where $V_{\mathrm{DS,int}}$ is the applied intrinsic drain voltage. The charge carrier mobility μ is defined as $\mu = v \cdot E_{\mathrm{int}}$. μ is a measure of how well charge carriers can move through a material and is proportional to their mean free path. The field-dependent drift velocity is commonly modelled as follows [61]:

$$v = \frac{\mu_0 E_{\mathrm{int}}}{(1 + (\mu_0 E_{\mathrm{int}}/v_{\mathrm{sat}})^{\gamma})^{1/\gamma}}, \tag{2.2}$$

where μ_0 is the low-field mobility, v_{sat} is the saturation velocity of the charge carriers, and γ is a fitting parameter. At low electric fields Eq. 2.2 can be approximated by

$$v \approx \mu_0 E_{\mathrm{int}}. \tag{2.3}$$

At low-fields, μ_0 is used as a quality parameter of the material. The larger μ_0 the fewer scattering centers, i.e. imperfections and impurities, are apparent. At high fields, i.e., high V_{DS}, the drift velocity saturates and approaches v_{sat}. The scattering mechanism at low and high fields are different as discussed in Section 2.2.1. Therefore, v_{sat} is used to characterise transistors at high fields. Fig. 2.2 shows the typical output and transfer characteristics of GFETs and conventional semiconductor MOSFETs. It is apparent that the dc characteristics of the two devices differ significantly. Figures. 2.2(a) and (b) show the transfer characteristics of the GFET presented in PAPER C and of a MOSFET [62], respectively. In the transfer characteristic of the GFET the drain current I_{DS} is increasing with sweeping V_{GS} in both directions from the charge neutrality point V_{Dir}. At the charge neutrality point the Fermi level is at $E_{\mathrm{F}} = 0\,\mathrm{eV}$ and the conductance is defined by the residual charge carrier concentration n_0 which consists of thermally generated charge carriers n_{th} and charge carriers induced due to charged defects [56]. The effect of defects and impurities on the charge transport characteristics is discussed in Section 4.1 and analysed in PAPER A. Typically, the transfer characteristics of graphene are not symmetrical and the resistance increases when the majority charge carrier type changes from holes to electrons. Partly, this can be explained by the difference in scattering cross sections of holes and electrons, which can result in the ratio $\mu_{\mathrm{e}}/\mu_{\mathrm{h}}$=0.83 or 0.37 between the electron and hole mobilites, according to experimental and theoretical studies [63, 64]. Partly, the asymmetry can be explained by differing contact resistances of the source and drain sides of the GFETs due to formation of p-n junctions between the gated channel and the ungated regions [65]. In contrast, as can be seen in Fig. 2.2(b), the drain current I_{DS} of a semiconductor MOSFET reduces to approximately zero below the threshold voltage V_{T}. Figures 2.2(c) and (d) show the output characteristics of the GFET presented

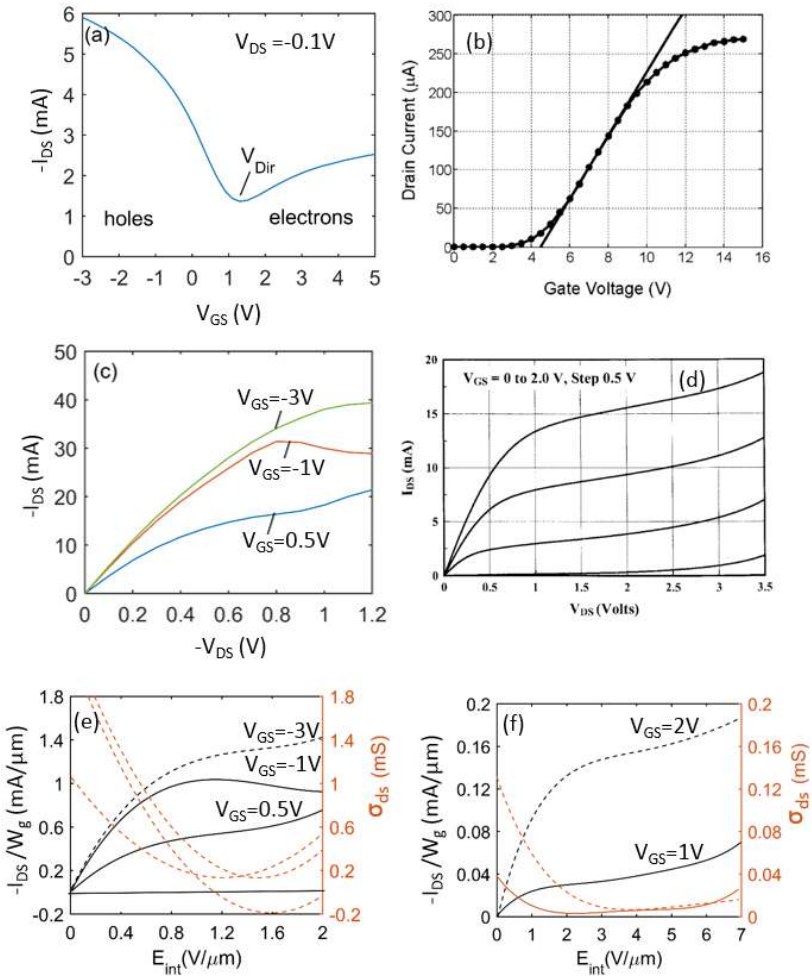

Figure 2.2: Comparison of the transfer and output characteristics of typical GFETs and MOSFETs. (a) Transfer characteristic of the GFET presented in PAPER C with $L_g = 0.5\,\mu$m and $W_g = 30\,\mu$m. The position of the charge neutrality point, i.e., the gate voltage for minimal conductance V_{Dir} is marked. (b) The transfer curve of a MOSFET [62]. In contrast to the GFET in (a) there is a threshold voltage V_T. For $V_{GS} < V_T$ the MOSFET is considered to be off. (c) The output characteristics of the GFET presented in PAPER C. The output curve at $V_{GS} = 0.5\,$V shows the "kink" where the charge carrier type in the channel changes from holes to electrons. (d) Output characteristics of a MOSFET with $L_g = 0.5\,\mu$m and $W_g = 100\,\mu$m [46]. The output characteristics exhibit current saturation over a wide bias range of the drain voltage V_{DS}. Drain current densities I_{DS}/W_g and the drain conductivity σ_{ds} versus intrinsic drain field E_{int} of the output characteristics of (e) the GFET and (f) the MOSFET in (c-d).

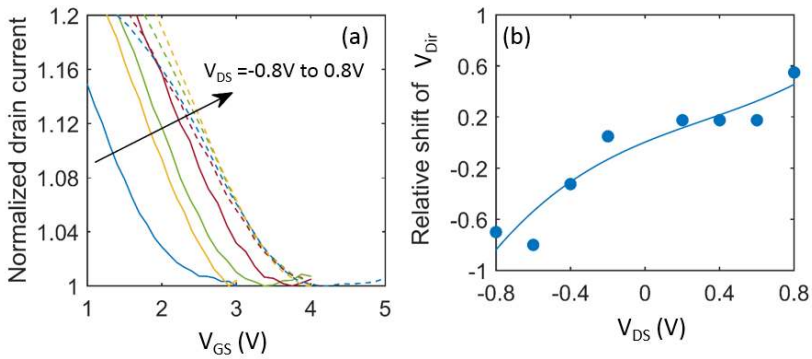

Figure 2.3: Illustration of how the gate voltage of minimum conductance, i.e., the Dirac voltage V_{Dir}, shifts with the applied drain voltage V_{DS}. (a) The normalized measured drain current versus gate voltage V_{GS}. The lines are at negative V_{DS}, the dashed lines are at positive V_{DS}. (b) The measured shift of $V_{\mathrm{Dir}}(V_{\mathrm{DS}})$ relative to $V_{\mathrm{Dir}}(V_{\mathrm{DS}} = 0\,\mathrm{V})$ versus applied V_{DS} (circles). The line is a polynomial fitting curve.

in PAPER C with $L_{\mathrm{g}} = 0.5\,\mu$m and $W_{\mathrm{g}} = 30\,\mu$m and a MOSFET with $L_{\mathrm{g}} = 0.5\,\mu$m and $W_{\mathrm{g}} = 100\,\mu$m [46]. Figure 2.2(d) shows that for the semiconductor MOSFETs the drain current saturates at high drain voltages (high electric fields). The current saturation in semiconductor MOSFETs is caused by velocity saturation and pinch-off of the channel. Figure. 2.2(c) shows that a saturation plateau, the so-called "kink", in the output characteristics of GFETs can be observed only for a small voltage range. The kink is obtained in a condition where the applied voltages effectively moves the Fermi level to the Dirac point at the drain side of the GFET channel, this is the point where the charge carrier concentration reduces to a minimum [66]. As illustrated in Fig. 2.3, this condition is approximately established, when $V_{\mathrm{DS}} = V_{\mathrm{GS}} - V_{\mathrm{Dir}}$. Because graphene has no bandgap, a further increase of the in-plane electric field changes the charge carrier type in the channel and the concentration increases. Therefore, the current continues increasing instead of saturating. At large V_{GS} the current will saturate before the drain voltage is large enough to fulfil the condition $V_{\mathrm{DS}} = V_{\mathrm{GS}} - V_{\mathrm{Dir}}$. As discussed in PAPER C and PAPER D the observed current saturation and even negative differential conductance are due to velocity saturation and due to the decrease of the saturation velocity caused by self-heating. Figure 2.2(e-f) compares the drain current densities $I_{\mathrm{DS}}/W_{\mathrm{g}}$ and the drain conductivity σ_{ds} versus intrinsic drain field $E_{\mathrm{DS,int}}$ of the output characteristics of the GFET and MOSFET in Fig. 2.2(c-d), where the drain conductivity is calculated as:

$$\sigma_{\mathrm{ds}} = g_{\mathrm{ds}} \cdot \frac{L_{\mathrm{g}}}{W_{\mathrm{g}}}. \tag{2.4}$$

The drain current density and hence the minimal drain conductivity are approximately ten times larger in the GFET than in the MOSFET, due to the lack of a bandgap. Due to the negative slope in the current density curve of the GFET at $V_{\mathrm{GS}} = -1\,\mathrm{V}$ the drain conductivity exhibits negative values at the corresponding drain fields.

2.2.1 Scattering mechanisms

Scattering of charge carriers in the graphene lattice can occur via different mechanisms, which are categorised into intrinsic and extrinsic scattering. Extrinsic scattering can be minimised by careful device design and an appropriate fabrication technology, whereas intrinsic scattering is inherent to the graphene lattice and sets an upper limit on the achievable performance of GFETs. Intrinsic scattering is due to lattice vibration, i.e., optical and acoustical phonons, and scattering between charge carriers within graphene. Extrinsic scattering mechanisms are scattering at neutral and charged impurities, scattering at defects and remote phonon scattering by adjacent materials. Experimentally, the dependencies of conductivity, of mobility, of the temperature, of the charge carrier concentration, and the electric field are often investigated to determine which are the dominating and limiting scattering mechanisms.

In graphene, at low fields and at room temperature elastic scattering mechanisms, i.e., resonant scattering, long range Coulomb scattering and scattering by surface polar phonons are most relevant. Every scattering mechanism has a specific mean free path, which is the distance that a mobile charge carrier can travel through an atomic lattice before it is scattered. The mean free path of resonant scatters (l_{RS}) and Coulomb scattering (l_{CL}) depend on charge carrier concentration as $l_{\mathrm{RS}}(n) \propto \sqrt{n}ln(\sqrt{n})^2$ and $l_{\mathrm{Cl}}(n) \propto \sqrt{n}$, respectively [67]. The mobility is proportional to l

$$\mu \propto \frac{el}{\hbar\sqrt{\pi n}}. \tag{2.5}$$

When several scattering mechanisms are active at the same time, μ is approximated as effective μ_{eff} using Matthiessen's rule [68]:

$$\frac{1}{\mu_{\mathrm{eff}}} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + ... + \frac{1}{\mu_{\mathrm{n}}}. \tag{2.6}$$

At high electric fields charge carriers gain enough kinetic energy to transfer energy to the material lattice. The relevant extrinsic scattering mechanism is inelastic soft optical phonon remote scattering by adjacent dielectrics. The dependence of the saturation velocity on charge carrier concentration and temperature is described by simplified models for the optical-phonon-scattering-limited saturation velocity model [69, 70, 71]

$$v_{\mathrm{sat}}(n,T) = \frac{2}{\pi}\frac{\omega_{\mathrm{OP}}}{\sqrt{\pi n}}\sqrt{1 - \frac{\omega_{\mathrm{OP}}^2}{4\pi n v_{\mathrm{F}}^2}}\frac{1}{N_{\mathrm{OP}}+1} \quad \text{or} \quad v_{\mathrm{sat}} \approx \frac{2}{\pi}\frac{\omega_{\mathrm{OP}}}{\sqrt{\pi n}}, \tag{2.7}$$

where $\hbar\omega_{\mathrm{OP}}$ is the optical phonon (OP) energy, and $N_{\mathrm{OP}} = 1/[exp(\hbar\omega_{\mathrm{OP}}/kT) - 1]$ is the phonon occupation. How charged impurity scattering affects v_{sat} is discussed in PAPER B and Section 4.2.1.

Ballistic transport

The scattering time relates to the mean free path l, which is the distance that a charge carrier can travel before it is scattered. When the mean free path is much smaller than

the channel length $l \ll L_g$ it is appropriate to consider diffusive transport. The condition $l \gg L_g$ is called ballistic transport. Ballistic-like transport can be achieved in devices with high-quality graphene and short gate length. For a device with the dimensions $L_g \times W_g$= $0.5\,\mu$m $\times 1.4\,\mu$m, the maximum ballistic mobility is $\sim 280000\,\mathrm{cm^2V^{-1}s^{-1}}$ at the charge carrier concentration $n \sim 4 \times 10^9\,\mathrm{cm^{-2}}$ [72]. Furthermore, ballistic transport has been observed at room temperature over a distance of $1\,\mu$m in Hall bar structures with graphene encapsulated in hexagonal boron nitride with $n \sim 10^{11}\,\mathrm{cm^{-2}}$ and $\mu > 100000\,\mathrm{cm^2V^{-1}s^{-1}}$ [73]. However, for the mobilities and gate lengths of the transistors considered in this work it is sufficient to assume diffusive transport. The fabrication process of GFETs unintentionally introduces impurities at the interfaces between the graphene layer and the adjacent substrate and the gate dielectric. Inevitably, these impurities act as scattering centres and shorten the scattering length.

2.3 RF characteristics of FETs

2.3.1 Figures of merit

To benchmark analog radio frequency (rf) applications the important figures of merit are the maximum frequency of oscillation ($f_{\max}$) and the transit frequency (f_{T}) for the characterization of the high-frequency performance. The maximum frequency of oscillation is the frequency at which the unilateral power gain U is unity, and the transit frequency is the frequency at which the short-circuit current gain h_{21} is unity (0 dB). $f_{\max}$ and f_{T} of a device are estimated from scattering parameters (S-parameters) measured by a vector network analyser, calculating and extrapolating U and h_{21} to 0 dB using the fact that they roll off at a slope of -20 dB/dec with frequency, as shown in Fig. 2.4. The unilateral gain is calculated in terms of the measured scattering parameter matrix S by [74]

$$U = \frac{|S_{12} - S_{21}|^2}{\det[\mathbf{1} - \mathbf{SS^*}]}, \tag{2.8}$$

where 1 is the unitary matrix and $*$ denotes the complex conjugate. The short-circuit current gain can be expressed via S-parameters as follows [75],

$$h_{21} = \frac{-2S_{21}}{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}. \tag{2.9}$$

Depending on the intended application, f_{T} and $f_{\max}$ should be at least three times larger than the operation frequency of the transistor [76]. Other important figures of merit are the minimum noise figure, output power and power-added efficiency [76] which are not part of the discussion in this work.

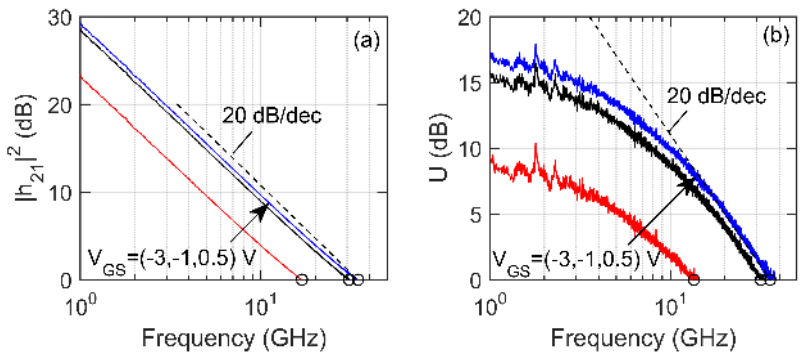

Figure 2.4: (a) Small-signal current gain ($|h_{21}|^2$), and (b) unilateral power gain (U) versus frequency at V_{DS}=-1.1 V and $V_{\mathrm{GS}} = (-3, -1, 0.5)$ V. The dashed line indicates the 20 dB/dec slope.

2.3.2 Equivalent circuit

Important tools for modelling and optimisation of the rf performance of full microwave circuits are the small-signal or large-signal equivalent circuits, which are representing FETs with lumped elements as shown in Fig. 2.5. The large-signal modelling requires consideration of non-linearities within the device when a large signal is applied to describe the behaviour of the transistor. A large-signal model of GFETs has been presented in [77] and is used for the analysis of the integrated mixer-amplifier circuit in PAPER F. In contrast, for small-signal modelling, the amplitude of the signal is assumed to be small enough such that the behaviour of the lumped elements can be linearised around the bias point. These circuits are used in the analysis of the GFETs in PAPER B-D.

The elements in the equivalent circuit correspond to actual physical effects in the transistor and can be extracted using dc measurements and S-parameter measurements [78, 79, 77]. The equivalent circuits consist of intrinsic and extrinsic elements. The intrinsic elements are the gate-source and gate-drain capacitances (C_{gs} and C_{gd}) and the charging resistance for the gate-source capacitance (r_{i}). Furthermore, the current source $g_{\mathrm{m}}V_{\mathrm{GSi}}$ and the drain conductance g_{ds} are parts of the intrinsic device, where g_{m} is the intrinsic transconductance. The intrinsic transconductance is defined as the derivative of the drain current (I_{d}) with respect to the intrinsic gate voltage (V_{GSi}):

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{GSi}}}\right|_{V_{DSi}=\mathrm{const.}}. \tag{2.10}$$

The drain conductance is the derivative of the drain current with respect to the intrinsic drain voltage (V_{DSi}):

$$g_{\mathrm{ds}} = \left.\frac{\partial I_{\mathrm{DS}}}{\partial V_{\mathrm{DSi}}}\right|_{V_{Gi}=\mathrm{const.}}. \tag{2.11}$$

The extrinsic elements are the parasitic drain, source and gate resistances (R_{D}, R_{S} and R_{G}), the bond and lead inductances (L_{D}, L_{S} and L_{G}), the parasitic pad conductances G_{PG} and G_{PD}, the parasitic pad capacitances C_{PG} and C_{PD}, the drain-source capacitance (C_{DS}), which is the junction capacitance of the parasitic diode formed at the drain side of a MOSEFET. Since, there is no real formation of a depletion region in the GFET channel due to the lack a bandgap in graphene, C_{DS} is mostly negligible. The intrinsic and extrinsic figures of merit, $f_{\mathrm{T,int}}$, $f_{\mathrm{max,int}}$ and f_{T}, f_{max}, respectively, can be approximated in terms of the small-signal equivalent circuit elements as [80, 81]

$$f_{\mathrm{T,int}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gs}}+C_{\mathrm{gd}})}, \tag{2.12}$$

$$f_{\mathrm{max,int}} = \frac{g_{\mathrm{m}}}{4\pi C_{\mathrm{gs}}} \times \frac{1}{\sqrt{g_{\mathrm{ds}}r_{\mathrm{i}}}}, \tag{2.13}$$

$$f_{\mathrm{T}} = \frac{g_{\mathrm{m}}}{2\pi(C_{\mathrm{gs}}+C_{\mathrm{gd}})} \frac{1}{1+g_{\mathrm{ds}}(R_{\mathrm{S}}+R_{\mathrm{D}})+\frac{C_{\mathrm{gd}}g_{\mathrm{m}}(R_{\mathrm{S}}+R_{\mathrm{D}})}{C_{\mathrm{gs}}+C_{\mathrm{gd}}}+\frac{C_{\mathrm{PG}}}{C_{\mathrm{gs}}+C_{\mathrm{gd}}}}, \tag{2.14}$$

$$f_{\mathrm{max}} = \frac{g_{\mathrm{m}}}{4\pi C_{\mathrm{gs}}} \frac{1}{\sqrt{g_{\mathrm{ds}}(r_{\mathrm{i}}+R_{\mathrm{S}}+R_{\mathrm{G}})+g_{\mathrm{m}}R_{\mathrm{G}}\frac{C_{\mathrm{gd}}}{C_{\mathrm{gs}}}}}. \tag{2.15}$$

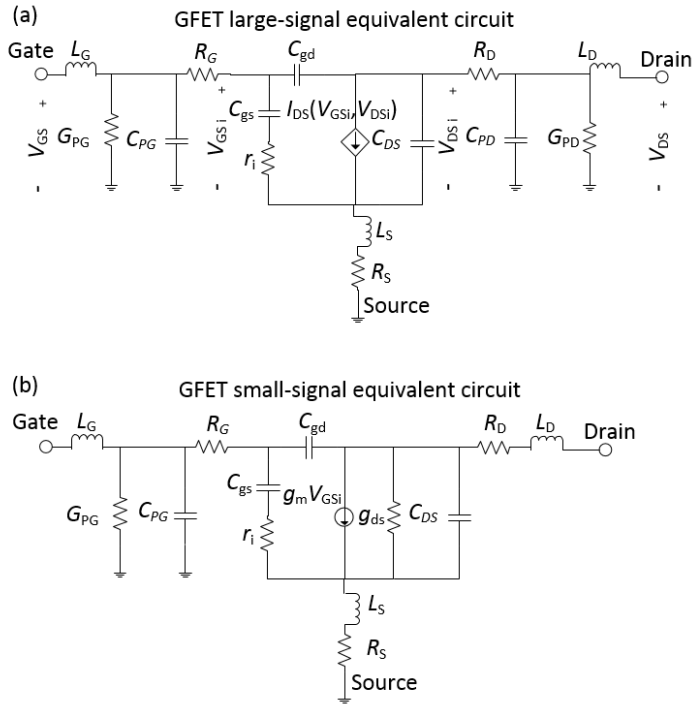

Figure 2.5: (a) Large-signal equivalent circuit of the GFETs used in the mixer and amplifier modelled in PAPER F. (b) Small-signal equivalent circuit of the GFETs modelled in PAPER B-D.

2.3.3 Dependencies of f_{T} and f_{max} on GFET design

Apparently, the values of the circuit elements are defined by the design of the transistor, and thus, f_{T} and f_{max} can be optimised by a careful transistor design. Analysis of Eqs. (2.14-2.15) suggests that g_{ds} and all parasitic elements, i.e., parasitic pad capacitances and gate, source and drain resistances, should be as small as possible, whereas g_{m} has to be maximized. As an example, Figure 2.6 illustrates how f_{max} and f_{T} of the GFET presented in PAPER C are affected by varying the gate length, the saturation velocity, the gate oxide thickness, and the gate width. For calculations, the values of the specific width contact resistivity ($\rho_{\mathrm{C}} = 3.3 \cdot 10^{-4}\,\Omega\mathrm{m}$), of the low-field mobility ($\mu_0 = 1800\,\mathrm{cm}^2/\mathrm{Vs}$), of the intrinsic electric field ($E_{\mathrm{int}} = 1.65\,\mathrm{V}/\mu\mathrm{m}$), and of the pad capacitance $C_{\mathrm{PG}} = 7\,\mathrm{fF}$ are taken from PAPER C. The resistances are calculated as $R_{\mathrm{C}} = \rho_{\mathrm{C}}/(2W_{\mathrm{g}})$ and $R_{\mathrm{S}} = R_{\mathrm{D}} = \rho_{\mathrm{C}}/W_{\mathrm{g}}$. To account for the dependence on saturation velocity (v_{sat}), the expression for the field-dependent velocity (Eq. 2.2) is used. The found effective velocity value (v) is then used to calculate $f_{\mathrm{T,int}}$ [82]:

$$f_{\mathrm{T,int}} = \frac{v}{2\pi L_{\mathrm{g}}}. \tag{2.16}$$

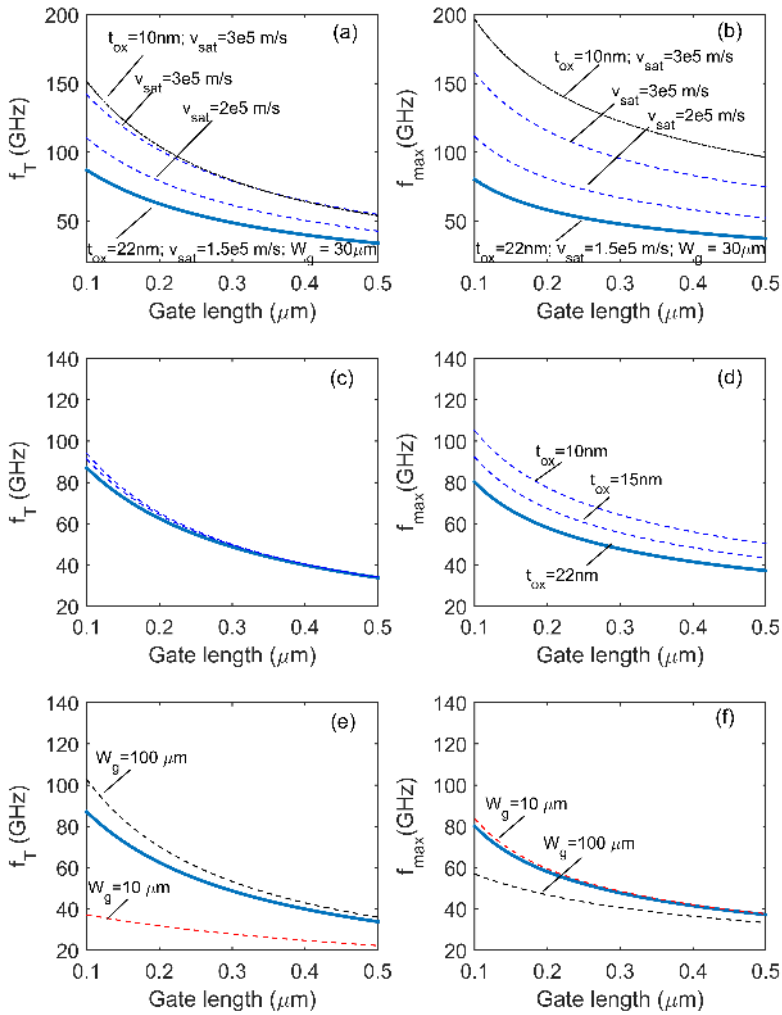

Figure 2.6: The modelled dependencies of f_{T} and f_{max} on different device parameters. The solid thick line in (a-f) is calculated for the original values of the GFET presented in PAPER C with the gate oxide thickness $t_{\mathrm{ox}} = 22\,\mathrm{nm}$, the saturation velocity $v_{\mathrm{sat}} = 1.5 \cdot 10^5\,\mathrm{m/s}$, and the gate width $W_{\mathrm{g}} = 30\,\mu\mathrm{m}$ and varying gate length L_{g}. (a) and (b) shows the effect of varying v_{sat}. The thin solid line is with $t_{\mathrm{ox}} = 10\,\mathrm{nm}$. (c) and (d) show the effect of varying t_{ox}. (e) and (f) show the effect of varying gate width W_{g}. The solid lines assume that the drain conductivity σ_{ds} scales with drain current, i.g., with W_{g}.

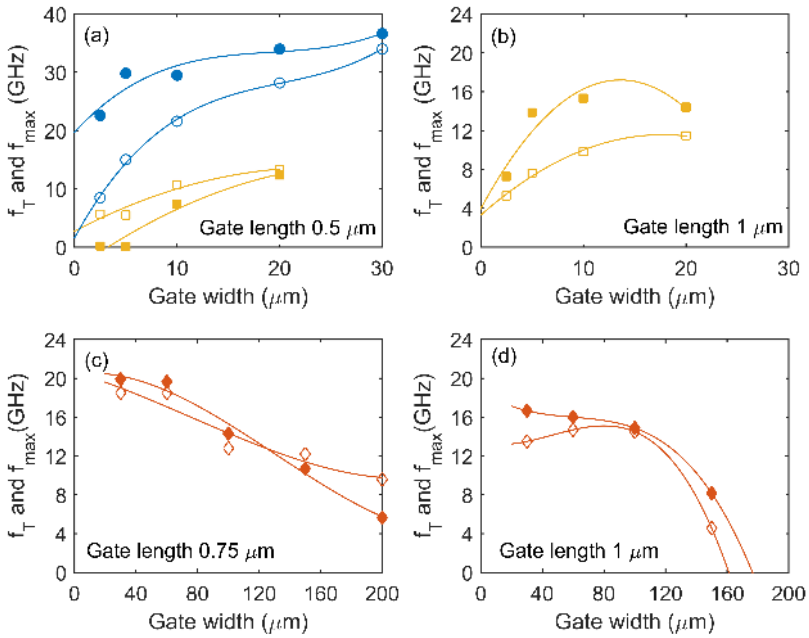

Figure 2.7: Gate width dependence of f_T (open symbols) and f_{max} (filled symbols) for different gate length and different device technologies. (a) The circles are the values of GFETs prepared as in PAPER C. The squares in (a) and (b) are the values of GFETs prepared in PAPER B. The diamonds in (c) and (d) are GFETs with graphene sandwiched between Al_2O_3.

Next, $f_{T,int}$ is used to estimate g_m using Eq. (2.12). The found value of g_m is then used to calculate the charging resistance $r_i = 1/(3g_m)$ [82]. The gate-source and gate-drain capacitances are scaled as in PAPER C, $C_{gs} = 0.5C_g$ and $C_{gd} = 0.2C_g$, where the gate capacitance $C_g = C_{ox}W_gL_g$ with the oxide capacitance $C_{ox} = \epsilon\epsilon_0/t_{ox}$. The relative permittivity of Al_2O_3 is $\epsilon = 7.5$. The gate resistance is calculated using the resistivity of gold ($\rho_g = 2.44\times10^{-8}\,\Omega$m) and the dimensions of the gate finger as $R_G = \rho_g W_g/(3L_g t_g N)$ [82], where $t_g = 300\,$nm is the thickness of the gate metal, and N the number of gate fingers. Note, that the width of the gate here is the length of the gate resistor. The drain conductance g_{ds} is calculated using the expression for the drain conductivity Eq. 2.4. Figure. 2.6 shows that increasing v_{sat} improves both f_T and f_{max}. Reducing the oxide thickness improves f_{max}, but has almost no effect on f_T. Varying the gate width has opposite effects on f_T and f_{max}. A larger W_g reduces the negative impact of C_{PG} and R_C, but R_G is increasing, hence, f_T is improved whereas f_{max} is worsen. Figure. 2.7 shows the gate width dependence of f_T and f_{max} for different GFET device technologies presented in this work. It appears as if there is fairly width independent performance between W_g =10-40 μm. Below and above this gate width the performance decreases

rapidly. The reduction with increasing W_g can be explained by the increase of R_G and with increasing probability of holes and imperfections in the graphene sheet, the reduction in performance with small width can be associated with a relatively larger impact of the parasitic pad capacitances.

2.4 Properties of graphene

The room temperature charge carrier velocity in graphene is larger than that in other semiconductor materials, which in combination with its unique high thermal conductivity and mechanical properties motivates the interest for using graphene in high-frequency electronic devices. The material properties of graphene and other common semiconductor materials are compared in Table 2.1. Note, the given values of thermal conductivity, mobility, and saturation velocity might vary in the literature depending on the measurement conditions.

2.4.1 Crystal structure and electronic band structure of graphene

Fig. 2.8(a) shows the orbital model of the carbon atoms in graphene. The three sp2 orbitals are equally spaced in the x-y-plane by an angle of 120° and form strong covalent σ bonds between the carbon atoms with a carbon-carbon bond length of approximately $a_{c\text{-}c} \approx 1.42\,\text{Å}$, which leads to the typical hexagonal arrangement as shown in Fig. 2.8(b) and explains the mechanical strength of graphene. The $2p_z$ orbital forms out-of-plane π bonds with the neighbouring carbon atoms, which allows electrons to move rather freely across the graphene sheet and is responsible for the notable electronic properties of graphene. The corresponding electronic band structure of graphene, which describes the allowed energy sates versus the momentum of electrons, is found by solving the Schrödinger equation. An approximate expression for the dispersion relation is found using the nearest-neighbor tight-binding model (NNTB) assuming electron-hole symmetry [24, 88] as

$$E(k)^{\pm} = \pm\gamma\sqrt{1 + 4\cos\Big(\frac{\sqrt{3}a}{2}k_x\Big)\cos\Big(\frac{a}{2}k_y\Big) + 4\cos^2\Big(\frac{a}{2}k_y\Big)}, \tag{2.17}$$

Table 2.1: Comparison of graphene properties at $T = 300\,\text{K}$ with conventional semiconductors. E_g is the energy bandgap, $m*/m_e$ is the electron effective mass, μ is the mobility, v_{sat} is the saturation velocity, and κ is the thermal conductivity [83, 16, 17, 84, 85, 86, 87].

Properties	Graphene	Si	GaAs	GaN	InAs	InP
E_g (eV)	0	1.12	1.42	3.44	0.35	1.34
$m*/m_e$	0 @V_{Dir}	0.98	0.06	1.5	0.02	0.08
μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	100000 (on hBN)	1450	900	9000	33000	5400
v_{sat} ($\times 10^7$ cm/s)	5 (on hBN)	1	0.7/2.7	1.4	0.9	0.7
κ ($\text{Wcm}^{-1}\text{K}^{-1}$)	1 (supported) 10 (suspended)	1.3	0.6	1.3	0.3	0.7

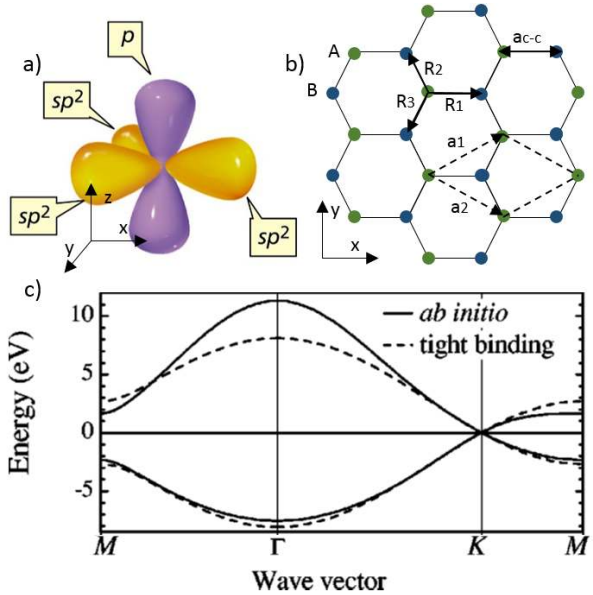

Figure 2.8: a) Orbital model of a carbon atom, [90]. b) The graphene lattice. The two inequivalent atom sites A (green dots) and B (blue dots) form the basis of the primitive unit cell indicated by the parallelogram (dashed lines). a_1 and a_2 are the primitive unit vectors (dashed arrows). R_1, R_2 and R_3 describe the separation between atom site A and its nearest-neighbour atoms. $a_{\text{c-c}} \approx 1.42\,\text{Å}$ is the carbon-carbon bond length. c) Comparison of the energy-momentum dispersion of ab initio calculations and the nearest-neighbour tight-binding approximation; adapted from [89].

where γ (typically between 2.7-3.1 eV) is the nearest neighbour overlap found by fitting Eq. 2.17 to ab initio calculations of the band structure at low energies (at the K point), as shown in Fig. 2.8(c) [89, 88]. k_{x} and k_{y} are the coordinate components of the wave vector. The + and - signs denote the signs for the conduction (π^*) and valence (π) bands, respectively.

The dispersion relation centred at the K point can be further simplified to the linear relation

$$E(k)^{\pm} = \pm\hbar v_{\text{F}} \sqrt{k\text{x}^2 + k\text{y}^2}, \tag{2.18}$$

where $\hbar$ is the reduced Planck's constant and $v_{\text{F}} = 3\gamma a_{\text{c-c}}/2 \approx 10^6\,\text{m/s} \approx c_0/300$, is the Fermi velocity, where c_0 is the speed of light in vacuum. The dispersion relation of conventional semiconductor materials, such as silicon and gallium arsenide, is approximated by a parabolic function and exhibits a band gap, whereas in graphene, the dispersion relation is linearly approximated, and the electron states are described by the Dirac equation, similar to weightless particles. This is the reason why the cone-like shape of the energy band structure is called a Dirac cone, and the point where the valence and conduction bands touch ($E = 0\,\text{eV}$) is called the Dirac point.

2.4.2 Charge carrier statistics

From the dispersion relation, the density of states (DOS) can be derived, which is the density of available states per energy interval. For graphene, the DOS has the following form [91]:

$$g(E) = \frac{2}{\pi(\hbar v_{\mathrm{F}})^2}|E|. \tag{2.19}$$

The DOS together with the Fermi-Dirac distribution

$$f(E_{\mathrm{F}}) = \frac{1}{1 + e^{(E-E_{\mathrm{F}})/kT}}, \tag{2.20}$$

where E_{F} is the Fermi energy, k is the Boltzmann constant and T is the temperature, is used to calculate the charge carrier concentration in the graphene sheet. For a given temperature and position of the Fermi level, the Fermi distribution describes the probability that an electron occupies an available energy state. The charge carrier concentrations of electrons, $n_{\mathrm{e}}(E_{\mathrm{F}})$, and holes, $n_{\mathrm{h}}(E_{\mathrm{F}})$, are derived as

$$n_{\mathrm{e}}(E_{\mathrm{F}}) = \int_0^\infty g(E)f(E, E_{\mathrm{F}})dE \tag{2.21}$$

and

$$n_{\mathrm{h}}(E_{\mathrm{F}}) = \int_{-\infty}^0 g(E)(1 - f(E, E_{\mathrm{F}}))dE. \tag{2.22}$$

The total charge carrier concentration $n_{\mathrm{g}}(E_{\mathrm{F}})$ is given by the sum of electrons and holes:

$$n_{\mathrm{g}}(E_{\mathrm{F}}) = n_{\mathrm{e}}(E_{\mathrm{F}}) + n_{\mathrm{h}}(E_{\mathrm{F}}). \tag{2.23}$$

The total charge is given by the difference between electrons and holes times the elementary charge:

$$Q_{\mathrm{g}}(E_{\mathrm{F}}) = e(n_{\mathrm{h}}(E_{\mathrm{F}}) - n_{\mathrm{e}}(E_{\mathrm{F}})) = -e \cdot \mathrm{sign}(E_{\mathrm{F}})\frac{4\pi E_{\mathrm{F}}^2}{(hv_{\mathrm{F}})^2}. \tag{2.24}$$

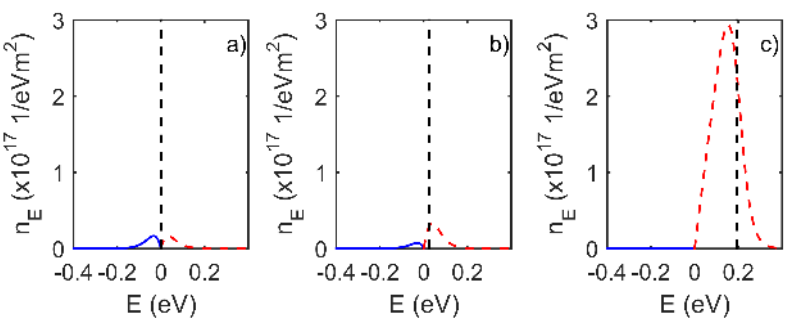

Figure 2.9: Charge carrier concentration of holes (solid line) and electrons (dashed line) for different positions of the Fermi level as indicated by the vertical dashed line.

For $E_F = 0\,\text{eV}$, the density of occupied states per unit volume and energy (n_E) for holes and electrons is the same as that shown in Fig. 2.9(a). The area below the curves is equal to the charge carrier concentrations of electrons and holes derived by Eqs. 2.21 and 2.22. As soon as the Fermi level is shifted to more positive energies, the charge carrier concentration will be dominated by electrons (Fig. 2.9(b-c)). The position of the Fermi level is tuned by either doping graphene with impurity atoms or via the field effect by electrical gating [15].

2.4.3 Quantum capacitance

Due to the low density of states in graphene, a small shift in the Fermi level noticeably changes the charge carrier concentration. For material systems with low DOS, the so-called quantum capacitance (C_q) [92] needs to be considered. C_q is defined as the derivative of the total charge (Q_g) in graphene with respect to the local electrostatic channel potential $V_{ch} = E_F/e$, and for pristine graphene, it can be expressed as follows [93, 94]:

$$C_q = \frac{\partial Q_g}{\partial V_{ch}} = \frac{8\pi e^2 kT}{(hv_F)^2} ln\Big[2 + 2\cosh\Big(\frac{E_F}{kT}\Big)\Big]. \tag{2.25}$$

In GFETs the total gate capacitance (C_t) will be reduced due to the quantum capacitance (C_q) acting in series with the geometrical capacitance $c_{ox} = \epsilon/t_{ox}$:

$$C_t = \frac{C_{ox}C_q}{C_{ox} + C_q}. \tag{2.26}$$

However, in the case that one of the capacitances is substantially lager than the other capacitance, the total capacitance can be approximated by the smaller capacitance, for example, when the gate oxide thickness is relatively large then

$$C_q \gg C_{ox} \rightarrow C_t \approx C_{ox}. \tag{2.27}$$

In PAPER A we consider the quantum capacitance for ideal graphene, but one needs to keep in mind that any distortion of the ideal graphene lattice that influences the electronic properties will affect the quantum capacitance since C_q is directly related to the density of states. Distortions can be generated by doping with impurity atoms, by forming nanoribbons (graphene strips with a width of a few nanometres) or by inducing strain [95, 96, 97, 98]. Also, charged defects introduce potential fluctuations across the graphene sheet. In that case, the quantum capacitance can be modelled assuming a Gaussian distribution of the potential [99].

Chapter 3

Fabrication and characterisation of GFETs

In this work, GFETs are designed and fabricated with the aim to achieve as high as possible f_T and f_{max}. Therefore, we developed a new fabrication process for GFETs, which is used in PAPER C-E, and is presented in this chapter together with the previous fabrication process used in PAPER A, B and F. For PAPER G a buried gate configuration of the detector was developed and is presented here. Furthermore, in this chapter, techniques for material quality and device characterization are explained.

3.1 GFET design and fabrication

The GFETs that have been reported in literature (Fig. 1.1) with high values of intrinsic and/or extrinsic f_T and f_{max} have been fabricated utilising a fabrication process with self-aligned T-gate structures with the aim to reduce the ungated access area length and, simultaneously, reduce the gate resistance [49, 48, 50]. Additionally, most GFETs were fabricated on SiC since it has superior optical phonon energy compared to SiO_2 [49, 48, 50]. However, the self-aligned technique does not necessary reduce L_a. Some of the reported values are still in the range of $\sim 100\,\text{nm}$ [49, 48], which is similar to that of the GFET design in this work (see description below). Also the charge carrier concentration in graphene on SiC can be larger than that of samples prepared on SiO_2 due to charge transfer from the SiC substrate to graphene [100]. The large charge carrier concentration strongly degrades the saturation velocity according to Eq. 2.7 and entails reduction of f_T and f_{max}. Other fabrication techniques employ buried gates electrodes, followed by transfer of exfoliated hBN and exfoliated graphene [101]. The highest intrinsic $f_T = 427\,\text{GHz}$ has been reported for transferable nanowire gate stacks on silicon glass at 67 nm [51]. However, simultaneously, due to high parasitic resistances, these devices perform extremely poorly in terms of f_{max} of only 8 GHz at $L_g = 46\,\text{nm}$.

The design of the GFETs used in this work is shown in Fig. 3.1. Figure. 3.1(a) shows a micrograph of the top view of a double-finger GFET. The metal pads for probing the GFET constitute the largest part. Figure 3.1(b) shows a schematic magnification of the gate-stack structure. The important layout parameters are the gate length Lg, the gate width W_g, the top-oxide thickness t_{ox}, and the bottom gate thickness t_b. Figure 3.1(c) shows a SEM image of the GFET in PAPER C. In the inset the un-gated access length $L_a = 0.1\,\mu\text{m}$ between the gate and the source/drain contacts is indicated. Figure 3.1(d) shows a SEM image of the graphene channel of the terahertz detector fabricated in PAPER G. The fabrication steps of the GFETs in PAPER A-E are illustrated in Fig. 3.2 and a detailed recipe of the new fabrication process described below can be found in the

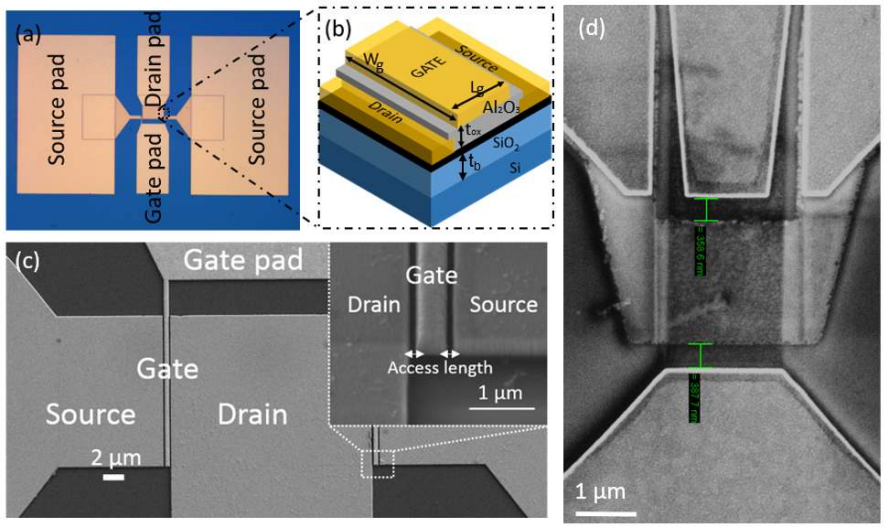

Figure 3.1: General two-finger gate layout of the GFETs used in this work. (a) The micrograph shows the top view of a GFET. (b) The schematic is a magnification of the gate-stack structure indicating the gate width W_g, gate length L_g, top-oxide thickness t_{ox}, and substrate material. (c) SEM image of the GFET in PAPER C. (d) SEM image of the terahertz detector fabricated in PAPER G.

APPENDIX. For the development of the new fabrication process the previous process used in PAPER A, B and F was modified to achieve better high-frequency performance. This was achieved by using high quality CVD graphene grown on copper transferred onto the substrate using an transfer method assisted by hBN instead of polymethylmethacrylate (PMMA) [83]. The latter usually leaves polymer residuals on the graphene sheet. Secondly, by depositing a protective Al_2O_3 layer as a first processing step after the graphene transfer instead of first patterning the graphene mesa, and thirdly, by using a thicker SiO_2 layer (1 μm instead of 300 nm) which reduces the parasitic pad capacitances. As discussed in PAPER C, the new fabrication sequence resulted in cleaner interfaces, which allowed for realisation of extremely low specific width contact resistivity of $\rho_C \sim 90\,\Omega\mu$m. ρ_C was measured by transfer-length method.

In all papers high bulk resistivity (10 kΩcm) Si substrate with 500 μm (PAPER A-E) or 280 μm (PAPER F) thickness was used, with the exception of PAPER A, where lithium niobate ($LiNbO_3$) substrate was used. The seed layer and the protective Al_2O_3 layers were formed by repeating deposition of 1 nm Al by e-beam evaporation and subsequent oxidation in air at 60 °C four times. The full oxide thickness was obtained by deposition of 15 nm Al_2O_3 using atomic layer deposition in thermal mode at 300 °C. The mesa, the drain, source and gate contacts were defined by E-beam lithography. Buffered oxide etch (BOE:water=1:10) was used to remove the Al_2O_3 layer in the areas intended for the the ohmic contacts and O_2 plasma etch was used to remove graphene in the mesa pattering step. The drain, source and gate metallisation was deposited by e-beam evaporation

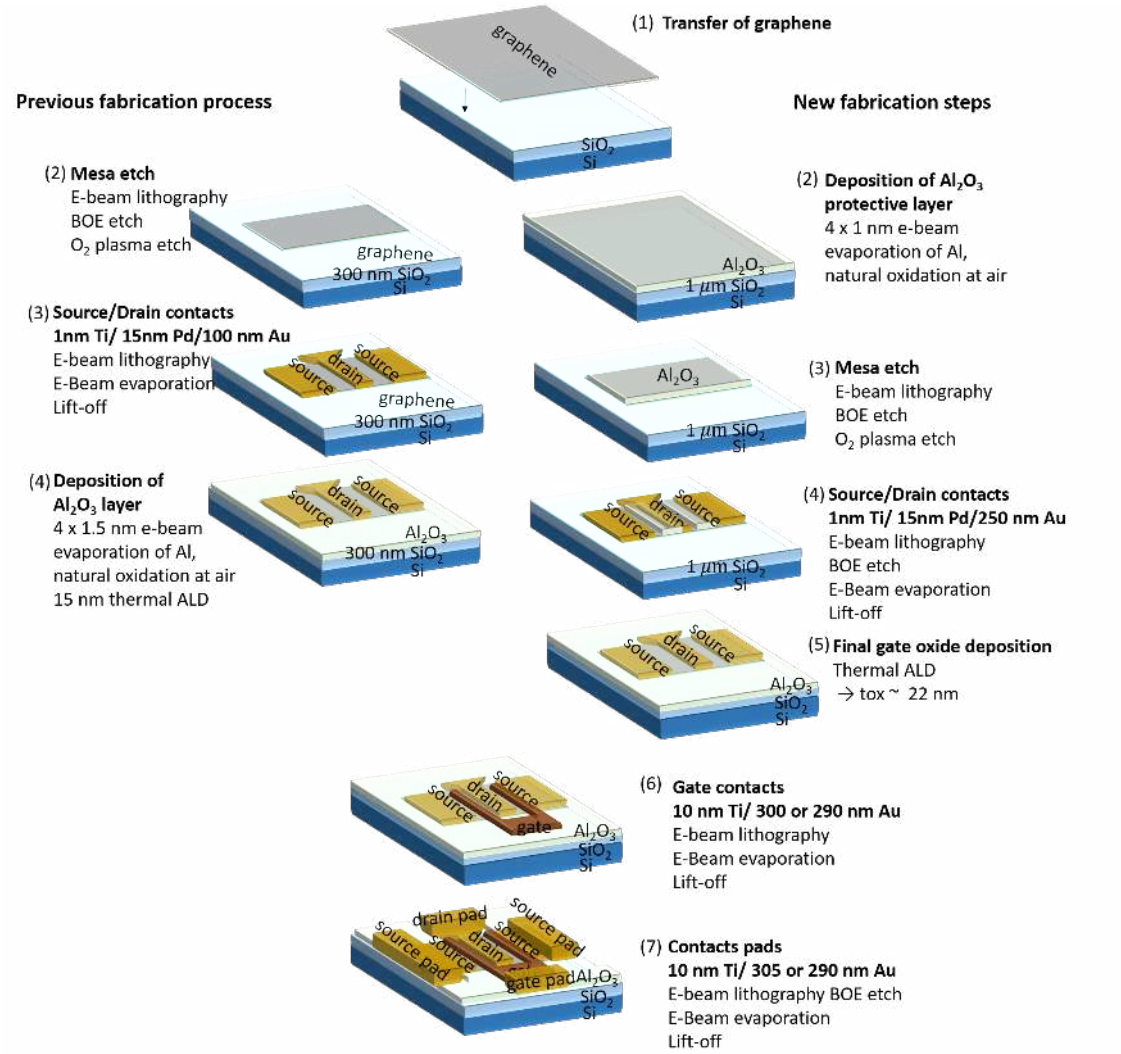

Figure 3.2: Fabrication processes of the GFETs in this work. The previous fabrication process was used in PAPER A, B and F. The new fabrication process was used in PAPER C-E.

followed by lift-off. Fabrication of the receiver presented in PAPER F was not part of this work. In short, the amplifier GFETs and the mixer GFETs were first fabricated together onto the silicon substrate following the previous fabrication process, and, subsequently, the coplanar waveguide circuitry, including the band pass filters and matching networks, were formed around the GFETs. The SiO_2 thickness is 90 nm.

Figure 3.3 shows the fabrication steps for the GFET in PAPER G, which were the following. The buried gate was patterned by e-beam lithography followed by the deposition

of 2 nm of Ti and 20 nm of Au by e-beam evaporation and lift-off. Two versions of the buried gate were fabricated. One version with vertical sidewalls of the burried gate, and one with sloped sidewalls. Vertical sidewalls were obtained by standard e-beam evaporation of the gate metal and lift-off. Sloped sidewalls were obtained evaporating the gate metal onto the substrate while tilting the substrate 20° and rotating it. The deposition rate is 0.8 Å/s with 4 revolutions per second. Next, the gate oxide was deposited by atomic layer deposition of Al_2O_3 in thermal mode at 300 °C with the final oxide thickness of 25 nm Fig. 3.3(2). After that, "Easy Transfer" graphene from Graphenea was transferred onto the Al_2O_3 layer following the company's recommended transfer method from a sacrificial polymer layer onto the substrate [102]. Patterning of the graphene channel was conducted by e-beam lithography and O_2 plasma etch (Fig. 3.3(4)). The parts of the bow-tie antenna which constitute the drain/source contacts and the contact pads were formed by e-beam lithography followed by e-beam evaporation of 2 nm Ti /10 nm Pd/150 nm Au and lift-off (Fig. 3.3(5)). In the final step, the gate contact pads were formed by e-beam lithography, followed by BOE etch to provide electrical contact to the buried gate. The gate contact metal was deposited by e-beam evaporation of 4 nm Ti and 270 nm Au followed by lift-off (Fig. 3.3(6)).

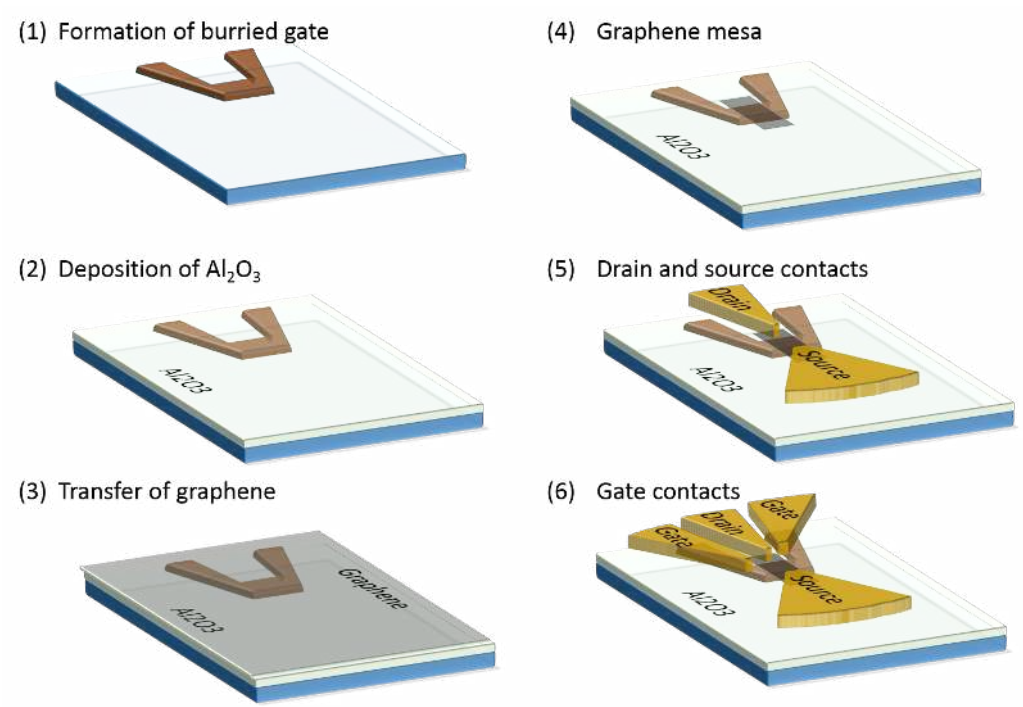

Figure 3.3: Fabrication process of the GFET in PAPER G. In contrast to the fabrication process of the GFETs in Fig. 3.2, the gate was formed first. This way the graphene is accessible for the near-field terahertz nanoscopy.

3.2 Synthesis of graphene and characterization of material quality

3.2.1 Synthesis of graphene

Originally, graphene was obtained by mechanical exfoliation from graphite using adhesive tape [15]. Graphite consists of stacked layers of graphene that adhere to each other by van der Waals forces. Using adhesive tape and repeatedly folding and unfolding the tape, the graphene layers can be detached from each other, until only one layer of graphene remains.

Following the first mechanical exfoliation of graphene, other synthesis processes have been developed. Graphene can be grown by chemical vapour deposition (CVD) on a catalyst material (most commonly copper) [103]. Another technique is the formation of graphene by intercalation on a silicon carbide crystal (SiC). This is performed under ultrahigh vacuum and at high temperatures, which are sufficient to sublimate silicon from the surface and leave the carbon-rich surface layer to transform to graphene [104]. Furthermore, graphene can be obtained by liquid exfoliation from graphite powder in a solvent using ultrasonication or sheer forces applied by a mixer to separate the graphene sheets [105, 106]. The graphene quality in terms of mobility has been highest in mechanically exfoliated graphene because it had less defects and impurity residuals, and did not include grain boundaries. However, advances in the growing and transfer technology of CVD graphene has been improved so that CVD graphene encapsulated in hexagonal boron nitride (hBN) can reach moblities up to $10{\times}10^4\,\mathrm{cm^2V^{-1}s^{-1}}$ at room temperature and, at cryogenic temperatures, similar mobilites as suspended graphene [83, 55]. At cryo-temperatures, suspended graphene reaches the theoretical intrinsic mobility limit of $2{\times}10^5\,\mathrm{cm^2V^{-1}s^{-1}}$ [55]. On SiO_2 the mobility is approximately in the order of $1{\times}10^4\,\mathrm{cm^2V^{-1}s^{-1}}$, limited by elastic scattering of the charge carriers by remote polar optical phonons of the substrate [107, 108]. Considering the combination of price for large-scale production and quality, the CVD graphene is the most promising. The CVD graphene can be grown at large scales and then be transferred onto arbitrary substrates. The bottleneck is the necessity to develop a clean transfer method that results in an ultra-clean and atomically flat graphene layer that does not exhibit wrinkles or holes.

3.2.2 Characterisation of material quality

Raman spectroscopy

Raman spectroscopy is a fast and nondestructive characterisation tool that provides structural and electronic information about graphene sheets. Raman spectroscopy is often used after transferring graphene onto the substrate to identify the graphene quality. The shape, intensities and positions of the characteristic peaks in the Raman spectrum provide information about any structural damage, unwanted dopants or chemical modifications of the graphene [110]. Fig. 3.4 shows the Raman spectra of CVD graphene provided by Graphenea after transfer onto SiO_2. The Raman spectra are measured using a Horiba scientific spectrometer with a 638 nm laser. The characteristic G peak and 2D peak are

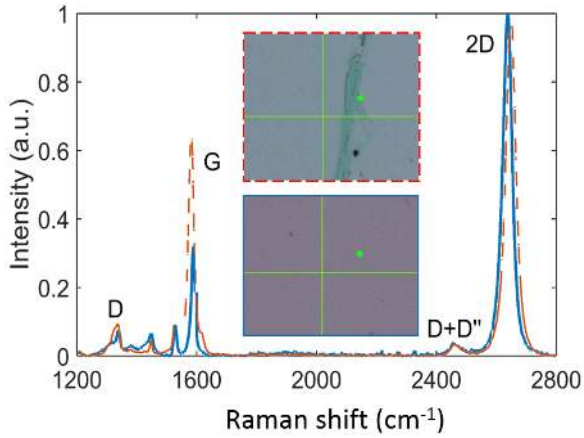

Figure 3.4: Raman spectra of graphene ("Easy Transfer" CVD graphene from Graphenea) at two different positions on the SiO_2 substrate. The Raman spectra are measured on single layer graphene (solid line) and on folded multi-layer graphene (dashed line). The position of measurements are indicated on the inset images. Both spectra are exhibiting the characteristic G and 2D peaks, and the D and D' peaks, which appear when defects are present. The G peak can be larger because of higher charge carrier concentration [109].

present in the Raman spectrum. The 2D to G peak intensity ratio, and the position of the G peak is a strong function of the charge carrier concentration and can be utilized to estimate the residual charge carrier concentration [109]. The full width half maximum of the G-peak is related to the number of graphene layers [111]. Since defects are present, the D peak and D' peak appear in the spectrum. As disorder increases the intensity ratio of the D and G peak increases and all peaks widen. Additionally, the shape of the D peak also depends on the number of graphene layers [110]. Another peak that is related to interlayer coupling and that can be used to estimate the number of graphene layers is the C peak; however, this peak is not shown in Fig. 3.4.

Characterisation of gate oxide

Imperfections in the gate oxide give rise to the formation of traps in the oxide and at the interface between graphene and the oxide. The schematic of traps, i.e., energy states between the conduction and valence bands of the oxide that are available for charge carriers in graphene, is illustrated in Fig. 3.5. There are different types of traps depending on their energy levels and physical location in the oxide [112]. A-type and b-type traps are so-called interface traps/interface states, which originate from defects and impurities or dangling bonds at the interface. The difference between a-type and b-type interface states is in the energy level. A-type interface states are likely to trap and de-trap charge carriers, whereas b-type interface states are too high or too low in energy to contribute to the fast trapping dynamics. However, both types of traps contribute to

charged defect scattering. C-type traps are commonly oxygen vacancies that lay in the bulk oxide. After fabricating the GFETs it is important to characterise the gate oxide. A high-quality oxide is important for good device performance. The effect of imperfections in the oxide on the transport characteristics is discussed in Section 4.1 and in Paper A. A commonly used method is analysing capacitance versus gate voltage (CV) measurements at different frequencies or temperatures to find relevant material parameters, such as the gate dielectric thickness, the dielectric constant, the oxide charge, and the doping profile of the substrate. CV measurements are a good tool for characterising interfaces between materials and to find the interface state density [113]. Charge carriers moving in and out of interface states contribute to the total capacitance as an in-series with the gate oxide acting capacitance. When measuring the capacitance at low frequencies, all interface states contribute to the total capacitance; at higher frequencies, the trapping-detrapping cannot follow the voltage variations fast enough, and the contribution of the interface capacitance is negligible. From the difference between the total capacitance at low and high frequencies, estimates of the interface state density can be made. Another method for characterising a gate oxide is presented in [114]. Dedicated parallel-plate capacitor test structures are characterised, using graphene on polyethylene terephthalate (PET) as a bottom electrode and gold as a top electrode. The measurement of the leakage current and the capacitance is used to for finding the dielectric constant of the oxide and for determining the origin of losses. To obtain further insights into the origin, distribution, and capture and emission rates of interface states, various analysis methods are available, such as conductance measurements [115], capacitance frequency spectroscopy [116], and multiparameter admittance spectroscopy [117].

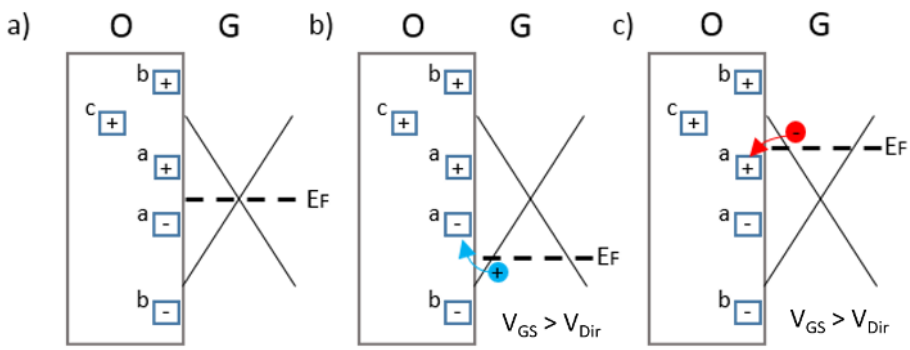

Figure 3.5: a) Schematic of different types of traps within the band diagram of an oxide (O) and graphene (G) system. A-type traps lay close to the oxide/graphene interface at relatively low energy levels. B-type traps are positioned close to the interface but have much higher or much lower energy levels than a-type traps. C-type traps lay deep in the bulk oxide [112]. b) Emptying and c) filling of traps when $V_{GS} < V_{Dir}$ and $V_{GS} > V_{Dir}$, respectively.

3.3 Device characterisation

3.4 Measurement set-ups

To characterise the dc performance and the rf performance of the fabricated GFETs, transfer and output characteristics, capacitance-voltage (C-V) characteristics, and scattering parameters (S-parameters) were measured and analysed. Figure 3.7 summarises the different experimental setups used in PAPERs A-E. The I-V and C-V characteristics of the GFETs were measured using an Agilent B1500A semiconductor device analyzer or a Keithley 2604B dual-channel source meter. In the first setup, cascade microtech dc probes were used. In the second setup, 67A-GSG Picoprobe microwave probes were used. The S-parameters were measured using an Agilent N5230A or Agilent E8361A vector network analyzer together with a Signatone S-1160 or Cascade probestation, respectively. Measurements were conducted in the frequency ranges from 100 MHz up to 50 GHz. The rf measurement system was calibrated at the ground-signal-ground microwave probe tips using TRL structures on a CS-5 standard calibration substrate. Figure 3.6 shows the measured S-parameters between 1 GHz and 50 GHz at $V_{GS} = 0.5\,V$ and $V_{DS} = -1.1\,V$ of the GFET presented in PAPER C. To study the S-parameters under different bias conditions, the drain and the gate voltages were swept using the Keithley 2604B dual-channel source meter. Isolation between the rf and dc equipment was ensured via bias-Ts. A PC was used to control the equipment via a GPIB link. A QFI InfraScope was used to visualize the heating of the GFET using the dual-channel Keithley Source Meter 2604B for biasing. In this set-up ground-signal-ground dc probes were used. External heating was provided by a Temptronic TP03215B ThermoChuck System.

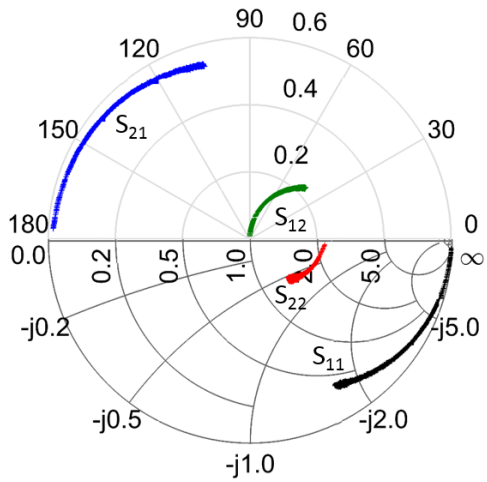

Figure 3.6: Smith chart with measured S-parameters between 1 GHz and 50 GHz at $V_{GS} = 0.5\,V$ and $V_{DS} = -1.1\,V$ of the GFETs presented in PAPER C.

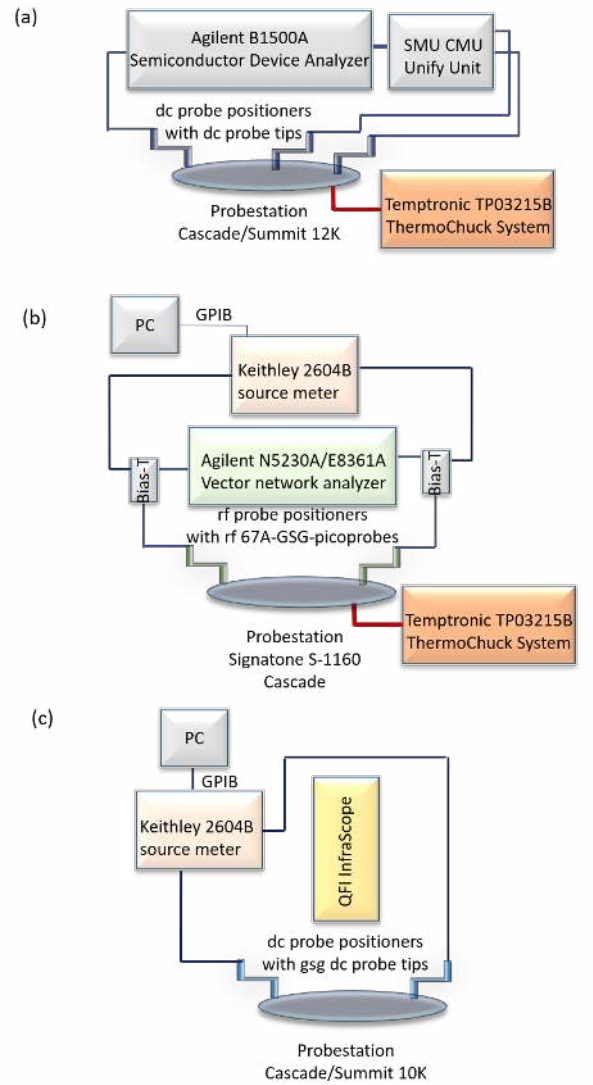

Figure 3.7: Measurement set-ups used in PAPER A-E. (a) Set-up used to measure transfer and capacitance characteristics in PAPER A. The SMU CMU Unify Unit allows measureing I-V and C-V characteristics with the same set-up. The ThermoChuck is used in PAPER D to supply external heating during measurements of transfer and output characteristics. (b) Set-up used for dc and rf characterisation used in PAPER B-E. The vector network analyzer Agilent N5230A was used in PAPER B, C, and E and Agilent E8361A was used together with the ThermoChuck in PAPER D. (c) Set-up used in PAPER D for IR microscopy imaging by QFI InfraSCope.

The measured transfer characteristics were used to extract the contact resistance, the low-field mobility and residual charge carrier concentration as described below in Section 3.4.2 and discussed in PAPER A. For analysis in PAPER B-E, the measured scattering parameters were used to calculate f_{T} and f_{max} using Eqs. (2.8)-(2.9) and extrapolation to zero gain. Together with the measured output characteristics, f_{T} was used to analyse the charge carrier velocity in GFETs in PAPER B.

3.4.1 Evaluation of charge carrier mobility

Different mobility definitions and corresponding methods can be applied for evaluating the mobility in graphene. The most commonly used methods are [118]

- the Hall effect mobility: $\mu_{\mathrm{H}} = |R_{\mathrm{H}}|/\rho$, where $\rho = 1/(\mu n e)$ is the resistivity and $R_{\mathrm{H}} = -1/(ne)$ is the Hall coefficient. To evaluate μ_{H} the fabrication of so-called Hall bars or van der Pauw structures are required. These structures are used to measure ρ and R_{H}.

- the conductivity mobility: $\mu = \sigma/(ne)$. The mobility is found from a conductivity measurement vs drain voltage, followed by dividing the measured conductivity by the charge carrier concentration estimated from the approximation

$$n \approx \frac{|V_{\mathrm{GS}} - V_{\mathrm{Dir}}|C_{\mathrm{ox}}}{e}, \tag{3.1}$$

  which is valid when $V_{\mathrm{GS}} > V_{\mathrm{Dir}}$ and $C_{\mathrm{q}} \gg C_{\mathrm{ox}}$. When $C_{\mathrm{q}} \gg C_{\mathrm{ox}}$ the total gate capacitance per unit area can be approximated as $C_{\mathrm{t}} \approx C_{\mathrm{ox}}$.

- the field-effect mobility. The field-effect mobility is defined by the transconductance g_{m} as $\mu = \frac{L_{\mathrm{g}} g_{\mathrm{m}}}{W_{\mathrm{g}} C_{\mathrm{ox}} V_{\mathrm{DS}}}$ and can be evaluated as the slope of the conductivity curve.

- fitting the drain-source resistance model [119] to the measured data. This method is described below.

It is important to note which method is used to extract the mobility because the found mobilities are not necessarily equal. Mobility degrades during fabrication and the mobility measured on complete GFETs is lower than that by the Hall effect since graphene is exposed to different external factors during the fabrication of specific test structures introducing additional scattering mechanisms associated with the top dielectric/interface.

3.4.2 The drain-source resistance model

Fitting of the drain-source resistance model to the measured resistance versus gate voltage (R-V) curve, obtained from the measured transfer characteristics at small V_{DS}, are used to find the contact resistance R_{C}, the low-field mobility μ_0, and the residual charge carrier concentration n_0, which are used as fitting parameters [119]. The drain-source resistance model has the form:

$$R_{\mathrm{DS}} = 2R_{\mathrm{C}} + \frac{L_{\mathrm{g}}}{W_{\mathrm{g}} e \mu_0 \sqrt{n^2 + n_0^2}}, \tag{3.2}$$

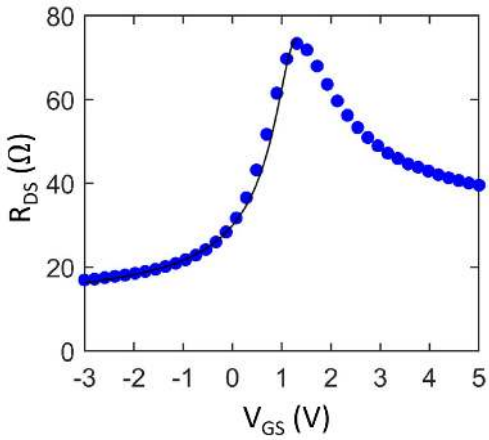

Figure 3.8: Measured drain-source resistances (R_{DS}) versus gate voltage (V_{GS}) (circles) together with modelled drain-resistance curve [PAPER C].

where $R_{\mathrm{C}} = R_{\mathrm{S}} = R_{\mathrm{D}}$ is the contact resistance. Note, in the appended papers $R_{\mathrm{C}} = R_{\mathrm{S}} + R_{\mathrm{D}}$ was used instead. The drain/source contact resistances consist of the sum of the gate metal-graphene contact resistance R_{mg} and the ungated access length resistance R_{acc}:

$$R_{\mathrm{D,S}} = R_{\mathrm{mg}} + R_{\mathrm{acc}}. \tag{3.3}$$

The gate induced charge carrier concentration n is estimated using the expression

$$|V_{\mathrm{GS}} - V_{\mathrm{Dir}}| = \frac{e}{C_{\mathrm{ox}}} n + \frac{\hbar v_{\mathrm{F}} \sqrt{\pi n}}{e} \tag{3.4}$$

or as $n = C_{\mathrm{ox}}|V_{\mathrm{GS}} - V_{\mathrm{dir}}|/e$ for the case when $C_{\mathrm{g}} \approx C_{\mathrm{ox}}$. The drain resistance approach is used throughout this work. The motivation of use, limitations and the applicability of this method is discussed in PAPER A and Supplementary material in PAPER B. As an example, Figure 3.8 shows the measured drain-source resistance versus gate voltage taken from PAPER C together with the modelled curve. There is an asymmetry between the hole branch and the electron branch of the R-V characteristic as shown in Fig. 3.8. For $V_{\mathrm{GS}} < V_{\mathrm{Dir}}$, the majority charge carriers are holes, and for $V_{\mathrm{GS}} > V_{\mathrm{Dir}}$, the majority charge carriers are electrons. The asymmetry in R-V characteristics can be explained, firstly, by the change in R_{D} and R_{S} due to formation of p-n junctions between the n-type gated channel and the p-type ungated regions at $V_{\mathrm{GS}} > V_{\mathrm{Dir}}$ [120, 121]. Second, assuming charged impurity scattering to be the dominant scattering mechanism, the scattering cross sections for holes and electrons are different, and thus the ratio between the mobility values of holes and of electrons can be as high as ≈ 2. [63].

Residual charge carrier concentration

Close to the Dirac point, the minimum conductivity depends on the charged impurity concentration, defects in the gate oxide and thermally generated charge carriers. The

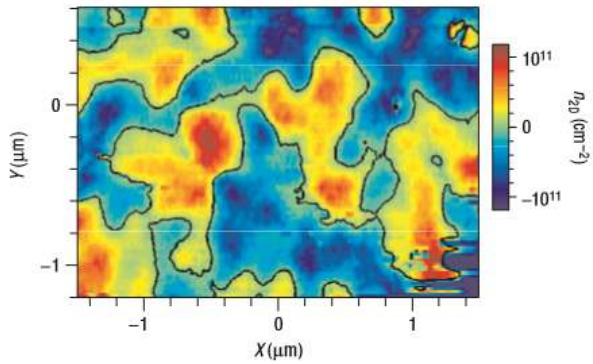

Figure 3.9: Colour map of the spatial concentration variations in a graphene flake extracted from surface potential measurements. The blue regions correspond to holes, and the red regions correspond to electrons. The black contour lines mark the zero concentration contour; adapted from [122].

higher the charged impurity and defect concentration, the higher the conductivity minimum because the charged impurities induce potential fluctuations across the graphene sheet, which lead to the formation of electron-hole puddles, as has been observed by a scanning single-electron transistor shown in Fig. 3.9. The relation between the concentration of charged impurities n_{imp} and n_0 is found using a self-consistent approximation of the screening between impurities and carriers [56]. At low temperatures ($T \approx 20\,\mathrm{K}$), the measured dependence between conductivity and residual charge carrier concentration, conductivity minima width and the shift of the Dirac point have been well described by the self-consistent approximation [107]. With a higher charged impurity concentration, the conductivity minima width and the shift of the Dirac point increase. Although the conductivity minima increases, the conductivity for $|V_{\mathrm{GS}}| > V_{\mathrm{Dir}}$ decreases with higher charged impurity concentrations as $\sigma \propto n/n_{\mathrm{imp}}$ because the mobility is reduced by charged impurity scattering. Because long-range scattering, i.e. scattering by charged defects, which is also named as Coulomb scattering, is generally the dominant scattering mechanism in fabricated GFETs, the conductivity measurements at low temperatures, exhibit a linear dependence with carrier concentration. That is because the mobility governed by this scattering mechanism does not depend on the carrier concentration [67]. In cases where the concentration of charged impurities is low, the conductivity exhibits a sub-linear behaviour with a crossover from long-range to short-range dominant scattering when moving from lower to higher charge carrier concentrations [123].

3.4.3 Evaluation of saturation velocity

The saturation velocity can be found by fitting the field-dependent velocity model, Eq. 2.2, to the measured velocity versus electric field curves and using the low-field mobility μ, the saturation velocity v_{sat} and γ as fitting parameters. The velocity versus electric field curves are found from measured values of f_{T} versus V_{DS} using delay time analysis, as

explained in PAPER B and in the APPENDIX. Delay time analysis allows for estimation of $f_{\mathrm{T,int}}$ and then Eq. 2.16 is used to calculate $v = 2\pi f_{\mathrm{T,int}}$. The limitation of v_{sat} by optical phonon scattering is studied in PAPER B using Eq. 2.7.

3.4.4 Near-field terahertz nanoscopy

The visualisation of plasma waves in the GFET channel under terahertz illumination was enabled by the unique combination of a free electron laser, which serves as a powerful THz source, and scanning scattering near-field optical microscopy (s-SNOM). Figure 3.10 illustrates the measurement principle [124]. Similar to atomic force microscopy, the s-SNOM setup utilizes a cantilever with a probe tip to scan the spacial electric field distribution in the GFET detector channel. The 2 THz beam is focused onto the probe tip, scattered and detected by a detector. The near-field signal, which depends on the local electric field, is found via demodulation of the detector signal at the second harmonic of the cantilever's oscillation frequency.

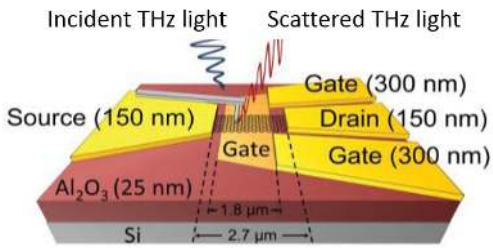

Figure 3.10: Illustration of the s-SNOM setup [124].

Chapter 4

Effects of imperfections and self-heating on f_{T} and f_{max}

The dc and rf performance of GFETs is affected by extrinsic factors, such as interface states at the interfaces between the graphene layer and the adjacent material layers, charged impurities and defects, parasitic resistances and capacitances, and self-heating. In this chapter, the main results concerning these issues which were studied in the appended PAPERS A-E are presented together with additional insights and discussions.

4.1 Effect of imperfections on transport characteristics

4.1.1 C-V and R-V characteristics

One main consequence of the presence of interface states and deep oxide traps is the observation of hysteresis due to trapping and de-trapping of charge carriers. Figure 4.1 shows a typical measured gate-source capacitance versus gate voltage (C-V) and a drain-source resistance versus gate voltage (R-V) characteristics of a GFET. To be able to observe the capacitance minimum in the C-V characteristic, i.e., contribution of the quantum capacitance, it is necessary to use a non-conducting substrate, such as polyethylene terephthalate (PET), $LiNbO_3$ or sapphire. On silicon, the gate capacitance is overshadowed by the large parasitic capacitance of the contact pads (Fig. 3.1). For this reason, the measurement results presented in Fig 4.1 are from a GFET on a PET substrate and in PAPER A we utilized $LiNbO_3$ substrate. In the presented C-V and R-V characteristics, one can observe that the forward and backward sweeps ($V_{\mathrm{GS}} = -2$ to $3\,\mathrm{V}$ and $V_{\mathrm{GS}} = 3$ to $-2\,\mathrm{V}$, respectively) in the C-V and R-V characteristics do not coincide; but they exhibit hysteresis. The hysteresis appears in two different ways, depending on the sweep rate and temperature of the system. An increase in the minimum capacitance gate voltage during the back sweep can be explained by charge carriers being trapped by traps formed at the gate oxide gate and/or adsorbents on graphene [58]. A negative shift in the minimum capacitance gate voltage is due to capacitive gating. Fast interface traps, which can follow the ac current when conducting the C-V measurements at typical frequencies of approximately $1\,\mathrm{MHz}$, contribute with an interface capacitance, whereas slower traps are responsible for the shift of the capacitance minimum and resistance maximum between the forward and backward sweeps. Fully covering graphene by a high-quality protective oxide layer helps to reduce or completely eliminate the hysteresis. Thereby, the device performance can be stabilised for weeks [125]. This approach is not applied for fabrication of devices in this work, since a relatively thin gate oxide is needed

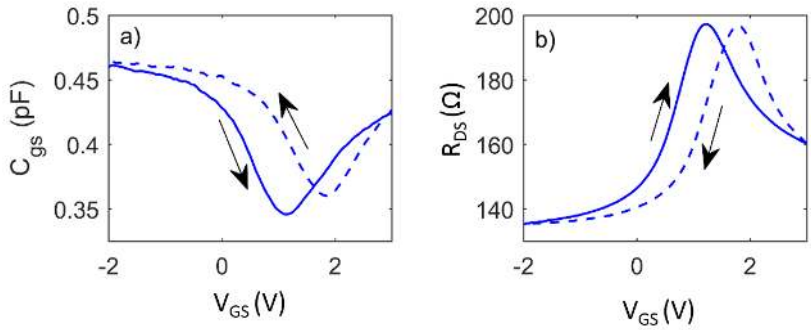

Figure 4.1: a) Gate-source capacitance versus gate voltage and b) resistance versus gate voltage for a GFET fabricated on polyethylene terephthalate with a gate length of $L_g = 1\,\mu$m, gate width of $W_g = 2 \times 30\,\mu$m (two-finger gate) and 15 nm Al_2O_3 gate oxide. Solid lines are forward sweeps of the gate voltage $V_{GS} = -2$ to 3 V, and dashed lines are backward sweeps $V_{GS} = 3$ to -2 V.

to allow for top-gating the device. If no conservation measures are undertaken, with ageing or stressing the gate oxide with a gate voltage and/or high drain voltage will lead to the C-V and R-V characteristics changing in shape, and shifting the position of the Dirac point due to detrapping or trapping of charges into the oxide. As shown in Fig. 4.2(a), the capacitance curves are reproducible when the gate voltage sweeps are repeated immediately after each other. In contrast, when the gate voltage is swept after keeping the gate voltage at a constant $V_{GS} = 1$ V for 10 minutes, the measured minimum capacitance is decreasing and the minimum capacitance voltage is increasing, as shown in Fig. 4.2(b). In PAPER A, a model was presented describing the influence of interface states on C-V and R-V characteristics. It was found that neglecting interface states in

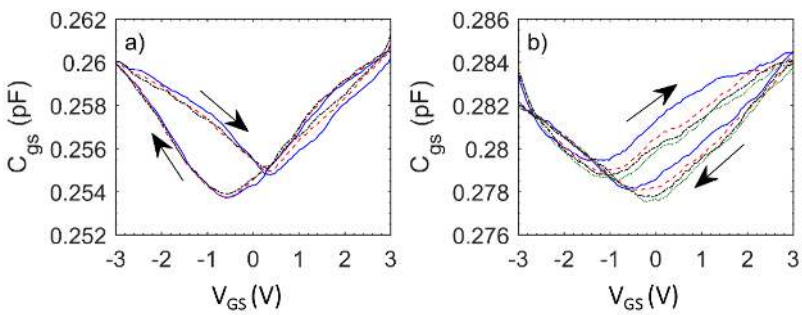

Figure 4.2: C-V characteristics of a GFET on $LiNbO_3$ with a) gate voltage sweeps repeated immediately and b) holding the gate voltage at $V_{GS} = 1$ V for 10 minutes after every sweep. Solid line - first sweep; dashed line - second sweep after 10 minutes; dashed dotted line - third sweep after 20 min; and dotted line - fourth sweep after 30 min.

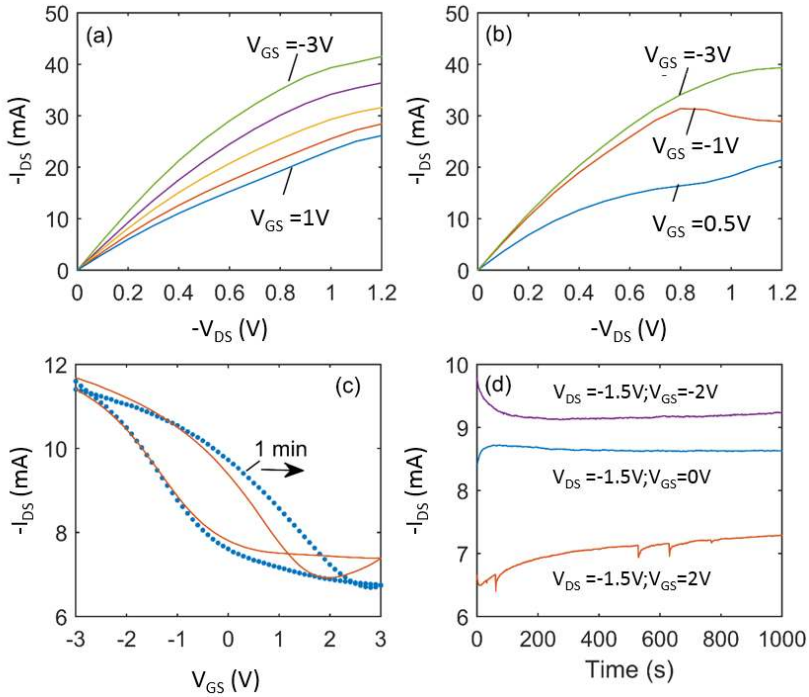

Figure 4.3: Effect of sweeping rate of V_{DS} and V_{GS} on measurements. Output curves measured with (a) 0 s delay time and (b) 30 s delay time per bias point. (c) Transfer curves with 0 s delay time (line) and 1 s delay time per bias point (circles). (d) Transient measurement of I_{DS} at $V_{\mathrm{DS}} = -1.5\,\mathrm{V}$ and different V_{GS}.

the resistance model presented in Section 3.4.2 significantly affects the extracted values of μ_0 and n_0. However, the interplay of charge carrier trapping and detrapping is rather complex. Therefore, Eq. 3.2 is used throughout the thesis to allow for relative comparison of the extracted values of μ_0 and n_0.

4.1.2 Output characteristics

Figure 4.3 shows how output and transfer characteristics are affected by charge trapping when using different sweeping rates of the drain and gate biases. In Fig. 4.3(a) the delay time between measurement points is 0 s, whereas in Fig. 4.3(b) the delay time is 30 s. The output characteristics have distinctive different shapes. While the "kink" effect is apparent at low V_{GS} and long delay time, the "kink" in Fig. 4.3(a) is not visible, due to charge de-trapping caused by Poole-Frenkel mechanism [126] at positive V_{GS} on time scales below ~ 1 min, which increases the current, instead of saturating. Also the transfer curves shown in Fig. 4.3(c) for slow and a fast sweeping rate of V_{GS} is affected by trapping/de-trapping. The trapping/de-trapping of charge carriers can be observed when measuring a transient curve, as shown in Fig. 4.3(d). This implies to measure I_{DS}

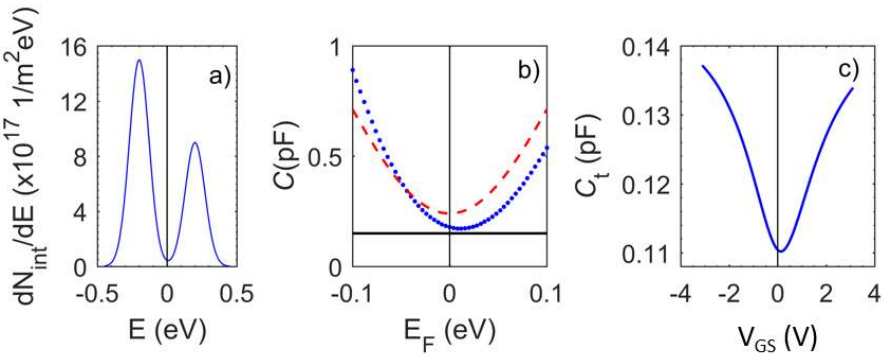

Figure 4.4: a) Gaussian interface state density distribution. b) Quantum capacitance (dashed line), interface capacitance for the interface state density distribution in (a) (dotted line), and oxide capacitance (solid line). c) The total capacitance of the capacitance in (b) calculated using Eq. 4.1.

versus time while keeping V_{DS} and V_{GS} constant. Depending on the bias condition, the drain current increases or decreases rather strongly within the first minute after starting the transient measurements and stays approximately constant after two minutes. Clearly, the instability of the GFETs is a challenge for characterisation and commercialisation. Therefore, for characterisation of GFETs in this work a delay of 30 s at each bias point was chosen. To be useful in commercial applications, the devices need the ability to provide the same output at the same bias conditions used.

4.1.3 Effect of interface state density distribution

The trapping and de-trapping of charges in interface states contribute to the total capacitance consisting of the oxide capacitance C_{ox} in series with quantum capacitance C_{q} and interface capacitance C_{int} connected in parallel

$$C_{\mathrm{t}} = \frac{C_{\mathrm{ox}}(C_{\mathrm{int}} + C_{\mathrm{q}})}{C_{\mathrm{ox}} + C_{\mathrm{int}} + C_{\mathrm{q}}}. \tag{4.1}$$

In PAPER A a constant interface state density was assumed. Figure 4.4 illustrates how the interface state density distribution affects the shape of the total capacitance, assuming that the interface state density distribution for the donor-like and acceptor-like interface states was Gaussian like, as shown in Fig. 4.4(a), rather than having a uniform distribution. The quantum capacitance, the interface capacitance for the interface state density distribution in Fig. 4.4(a) and the oxide capacitance are shown in Fig. 4.4(b). The interface capacitance is not constant, and its minimum is shifted away from $E_{\mathrm{F}} = 0$. This affects the shape of the total capacitance versus gate voltage dependence shown in Fig. 4.4(c). The curve is not symmetric around the minimum and is shifted away from $V_{\mathrm{GS}} = 0$.

4.2 Effect of saturation velocity on f_{T} and f_{max}

The analysis of the velocity in GFETs in Paper B-D is relevant for amplifier applications at high electric fields since the charge carrier velocity is directly affecting $f_{\mathrm{T,int}}$ and $f_{\mathrm{max,int}}$ via [126]:

$$f_{\mathrm{T,int}} = \frac{v}{2\pi L_{\mathrm{g}}} \quad \text{and} \quad f_{\mathrm{max,int}} = \sqrt{\frac{f_{\mathrm{T,int}}}{8\pi R_{\mathrm{G}} C_{\mathrm{GD}}}} \tag{4.2}$$

According to the analysis in PAPER B, C, and E, the velocity, and thus v_{sat}, should be as high as possible to achieve improved high-frequency performance.

4.2.1 Velocity limitations at high electric field

As discussed in Section 2.2, the saturation velocity is the most adequate parameter to describe transport at high fields. A number of different theoretical approaches can be used for analysis of the high-field behaviour of GFETs. The reported theoretically achievable saturation velocities range between 0.2 and $0.8v_{\mathrm{F}}$ depending on the calculation method, the considered scattering mechanisms, and substrate [57, 71, 127, 128]. According to [129, 71, 128], impurity scattering does not significantly affect high-field transport, whereas in [69] a strong effect of charged impurity scattering is predicted. In PAPER B we show that by applying delay time analysis the saturation velocity is limited by the optical

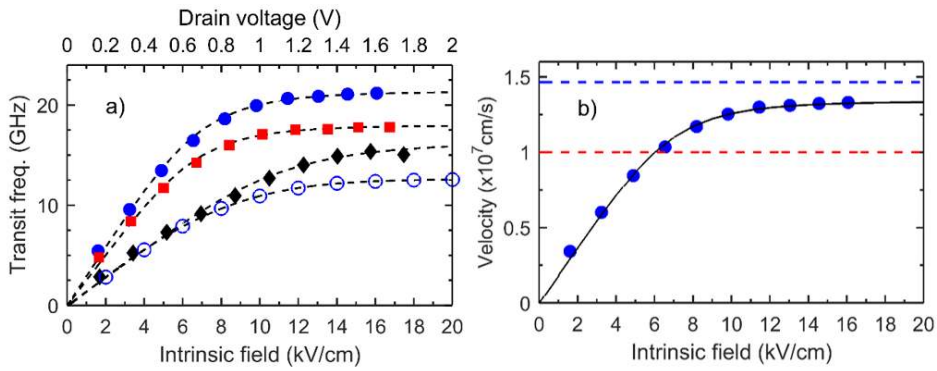

Figure 4.5: a) Intrinsic transit frequency vs electric field in the channel for devices with $n_0 = (1.7, 1.9, 2.8) \times 10^{12}\,\mathrm{cm}^{-2}$ (circles,squares,diamonds) at $V_{\mathrm{g}} = -2\,\mathrm{V}$. The extrinsic transit frequency vs drain voltage for the device with $n_0 = 1.7 \times 10^{12}\,\mathrm{cm}^{-2}$ is indicated in the same graph by open circles. Dashed lines are polynomial fitting curves and serve as a guide for the eye. (b) Carrier velocity for the device with $n_0 = 1.7 \times 10^{12}\,\mathrm{cm}^{-2}$ calculated using Eq. 4.2 and fitted by the empirical expression of Eq. 2.2 (solid line) using $\gamma = 3$, $\mu_0 = 1920\,\mathrm{cm}^2/\mathrm{Vs}$ and $v_{\mathrm{sat}} = 1.4 \times 10^7\,\mathrm{cm/s}$ vs electric field in the channel. The effective saturation velocities for graphene with SiO_2 optical phonons (dashed) and graphene with SiO_2 and Al_2O_3 phonons (dashed-dotted) are also shown.

phonons in SiO_2 and impurities only contribute through the emission of additional charge carriers reducing v_{sat} which is explained by the charge carrier concentration dependence in Eq. 2.7. In Fig. 4.5(a) the measured and intrinsic transit frequencies are compared. The measured transit frequency is lower due to the contribution of the extrinsic and parasitic parts. Furthermore, the transit frequency is lower for higher residual charge carrier concentrations. From $f_{T,int}$, the charge carrier velocity is found using Eq. 4.2, and the field-dependent velocity model, Eq. 2.2, is fitted to the measurement to find v_{sat}. Figure 4.5(b) shows the measured charge carrier velocity versus intrinsic electric field in the channel together with the fit of the model. Another explanation of the dependence of saturation velocity on charge carrier concentration is suggested in [130, 131]. The simulations assume increasing impurity scattering with increasing carrier concentration, since the applied gate voltage will fill interface traps, charge them and thus introduce more scattering centres, or that local potential scattering (atomic scale defect scattering and dislocation scattering) explains the dependence of saturation velocity on charge carrier concentration at high fields.

4.3 GFET with state-of-the-art extrinsic f_T and f_{max}

Figure 4.6 compares the values of extrinsic f_T and f_{max} of the GFETs fabricated with the old fabrication process used for the GFETs presented in PAPER B and with the new fabrication process which was used in PAPER C. Indeed, high quality graphene in combination with reducing C_{PG} and R_C allows for improving the GFET f_T and f_{max} performance from ∼10 GHz up to ∼30 GHz with a promising scaling behavior with gate length which predicts extrnisc values of up to 100 GHz at $L_g = 60$ nm. The reported state-of-the-art extrinsic f_T and f_{max} performance was achieved thanks to the modified fabrication process presented in this work. Also shown are values of extrnisc f_T and f_{max}

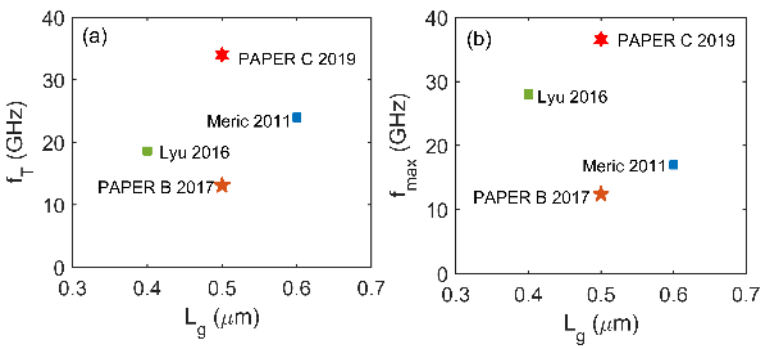

Figure 4.6: Values of extrinisc f_T and f_{max} versus gate length L_g for GFETs presented in PAPER C fabricated by the new fabrication process compared to the performance of GFETs fabricated by the previous fabrication process in PAPER B. The fabrication processes are presented and compared in Chapter 3.1. Additionally, the perfromance is compared to GFETs with similar gate length [132, 101].

reported in the literature for GFETs with similar gate length [132, 101].

4.4 Effect of self-heating on $f_{\mathbf{T}}$ and $f_{\mathbf{max}}$

4.4.1 Self-heating

An electrical current that flows through a conductor with a finite resistance causes Joule-heating. In a transitor, the dissipated heating power $P_{\mathrm{diss}} = I_{\mathrm{DS}} V_{\mathrm{DS}}$ leads to a rise of the channel temperature ΔT proportional to the dissipated power and the thermal resistance R_{th} of the device:

$$\Delta T = R_{\mathrm{th}} \cdot \Delta P_{\mathrm{diss}}. \tag{4.3}$$

In graphene sheets on a SiO_2/Si substrate a considerable increase of the temperature, up to a several hundred Kelvin, has been observed via infrared microscopy and Raman spectroscopy at power densities above $0.1\,\mathrm{mW}/\mu\mathrm{m}^2$ [133, 134, 135, 136, 137]. As can be seen in Fig. 4.7, these power densities are typical for GFETs being developed for current and power amplification applications [136, 137, 135, 133, 138, 101, 139].

However, many of the temperature studies consider larger device dimensions than those practical for a high-frequency transistor with typical dimensions of the gate length $L_{\mathrm{g}} \ll 1\,\mu\mathrm{m}$ and gate widths W_{g} in the micrometer range [135]. Figure 4.8 reveals that the channel temperature of the GFETs used in this work increases with V_{DS}. The temperature was measured by means of IR microscopy imaging and, hence, is underestimated, since the resolution of the IR microscope is approximately $1.6\,\mu\mathrm{m}$ per pixel which is larger than the gate length L_{g}=$0.5\,\mu\mathrm{m}$. Therefore, it is important to study the effect of self-heating on the GFET performance. Some of the results are presented in PAPER D. Additionally, the analysis showed it is important for future device and circuit development to establish thermal resistance models that are applicable for GFETs. The thermal resistance model and the thermo-sensitive electrical method to find the thermal resistance of GFETs used in PAPER D are explained in detail below. Figure. 4.9, which is taken from Paper D, shows f_{T} and f_{max} versus intrinsic dissipated power density and different external temperatures. The values of f_{T} and f_{max} decrease rapidly starting from $P_{\mathrm{density,int}} = 1\,\mathrm{mW}/\mu\mathrm{m}^2$ which can be fully explained by self-heating.

4.4.2 Thermal resistance and temperature models

Knowing the thermal resistance of a device structure allows for evaluation of the temperature rise in the graphene channel with dissipated power $P_{\mathrm{diss}} = I_{\mathrm{DS}} \cdot V_{\mathrm{DS}}$ using Eq. 4.3. Establishing a thermal resistance model based on the device structures allows for optimization of the device dimensions, such as substrate thickness, separation of the gate fingers, gate length and gate width, as well as substrate material and number of gate fingers. Generally, the thermal resistance of a layered structure can be estimates as

$$R_{\mathrm{th}} = \frac{t}{A \cdot \kappa}, \tag{4.4}$$

where t is the thickness of the sample and A the cross-sectional area. However, Eq. 4.4 is only applicable if L_{g}, $W_{\mathrm{g}} \gg L_{\mathrm{H}}$, t_{ox}, where $L_{\mathrm{H}} \approx 0.1\,\mu\mathrm{m}$ is the thermal healing length and

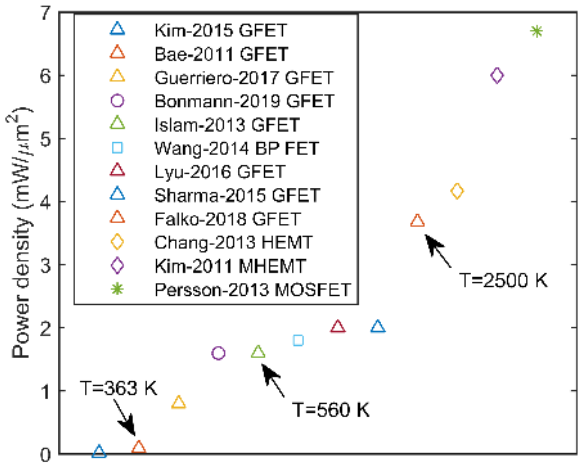

Figure 4.7: Power densities typical for different transistors technologies. The channel-temperature for GFETs reported in the literature is indicated in the plot [136, 133, 140, 139, 138, 141, 132, 142, 143, 144, 145, 146].

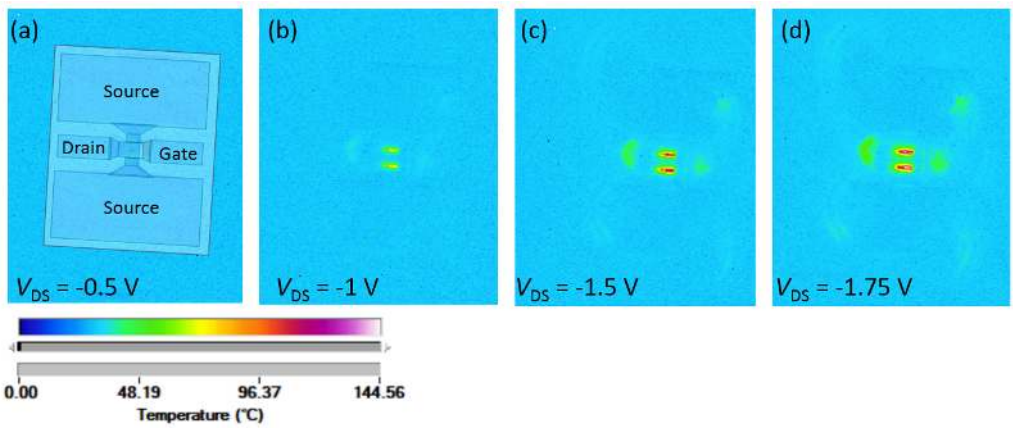

Figure 4.8: Infrared images of a GFET on 1 μm/300 μm SiO_2/Si substrate with gate length $L_g = 0.5\,\mu$m and gate width $W_g = 2 \times 15\mu$m at the same gate-source bias $V_{GS} = 1.5\,V$ and different drain-source biases of (a) $V_{DS} = -0.5\,V$, (b) $V_{DS} = -1\,V$, (c) $V_{DS} = -1.5\,V$, and (d) $V_{DS} = -1.75\,V$. A QFI InfraScope is used to visualize the heating of the GFET. In the IR microscope setup the dual-channel Keithley Source Meter 2604B is used for biasing.

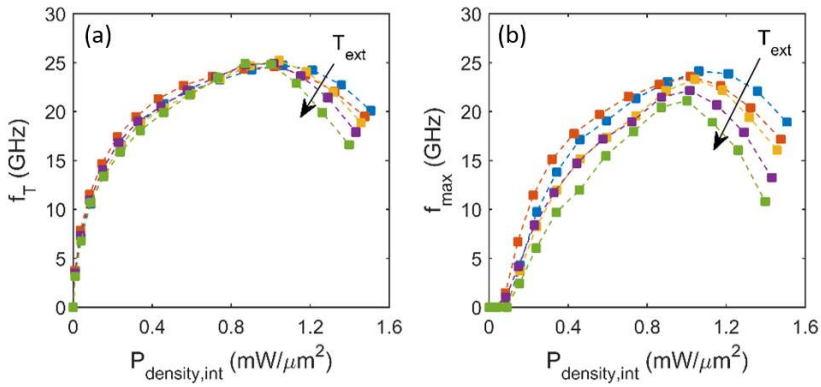

Figure 4.9: Effect of external temperatures $T_{\text{ext}} = (60, 70, 80, 90, 100)\,^{\circ}\text{C}$ and self-heating on f_{T} and f_{max} for a GFET with $L_{\text{g}} = 0.5\,\mu\text{m}$ and $W_{\text{g}} = 2 \times 15\,\mu\text{m}$ on $1\,\mu\text{m}$ $SiO_2/300\,\mu\text{m}$ Si substrate. (a) f_{T} and (b) f_{max} versus intrinsic dissipated power density $P_{\text{density,int}}$.

t_{ox} the gate oxide thickness [147]. Additionally, thermal coupling between the gate fingers of the GFET needs to be taken into account [148, 149]. Theoretical models of thermal resistance have been developed for semiconductor device technologies, such as HEMTs and diodes. However, they either require the knowledge of the thermal conductivities [148, 149] or temperature-dependent current-voltage dependencies [150]. For the latter, the current-voltage dependencies of graphene differ from other semiconductor materials due to its lack of a bandgap. Figures 4.10(a-b) show the measured and calculated channel temperatures and thermal resistances using different temperature models. The considered models are Eq. 4.3 and two models which have been developed for multi-finger HEMTs presented in Refs. [148] and [149], The application of the model in [149] is explained in the APPENDIX. Figure 4.10(a) shows that all models are overestimating the measured channel temperature by IR microscopy imaging. This can be explained by the limited resolution of the QFI InfraScope. The temperature $T \sim 500\,\text{K}$ reported for corresponding power densities at $P_{\text{diss,density}} \sim 1.5\,\text{mW}/\mu\text{m}^2$ in Fig. 4.7 agrees with the temperature calculated by the method presented in Ref. [148], whereas at $P_{\text{density}} \sim 3.5\,\text{mW}/\mu\text{m}^2$ the temperature calculated using Eq. 4.3 agrees well with the reported temperature $T \sim 2500\,\text{K}$. The reported measured temperatures in Fig. 4.7 are based on graphene sheet sizes much larger than in GFETs intended for high-frequency applications and therefore Eq. 4.4 and Ref. [148] are applicable. Figure 4.7(c) shows the thermal resistance estimated by the method of thermo-sensitive electrical parameters, which is used in PAPER E and explained below in the APPENDIX. The analysis in PAPER E suggest that there is a strong non-linearity of the thermal resistance, which is possible to model by the method in Ref. [149] taking the nonlinear thermal conductivities into account. However, Fig. 4.10 shows that the non-linearity can only be reproduced by using $\alpha_{\text{SiO2}} = 2$ (black dotted line) instead of $\alpha_{\text{SiO2}} = 0.2$ (dashed line) in the model (APPENDIX). It is the task for future work to find the physical origin of the dependency of R_{th} on P_{density} in GFETs.

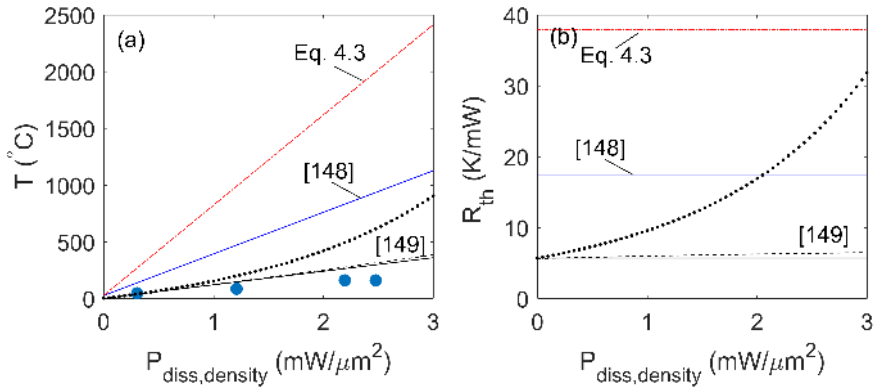

Figure 4.10: Comparison of different thermal resistance models. (a) Channel temperature of a GFET with $L_g = 0.5\,\mu$m and $W_g = 2 \times 15\,\mu$m measured by QFI InfraScope (circles) and calculated by different temperature models: (black line) and (black dashed line) using the linear and non-linear temperature model from Ref. [149] (explained in APPENDIX), (blue line) using the model from Ref. [148], (red dots) calculated using Eq. 4.3. (b) The corresponding thermal resistance R_{th}. The (black dots) values are calculated using model from Ref. [149] but using $\alpha_{SiO2} = 2$ instead of 0.2. (c) Thermal resistance R_{th} estimated by the TSEP method using Eq. 7.12 versus intrinsic dissipated power P_{int} for three different external chuck-temperatures T_{ext}. The lines are polynomial fitting curves and serve as guide for the eye [PAPER E].

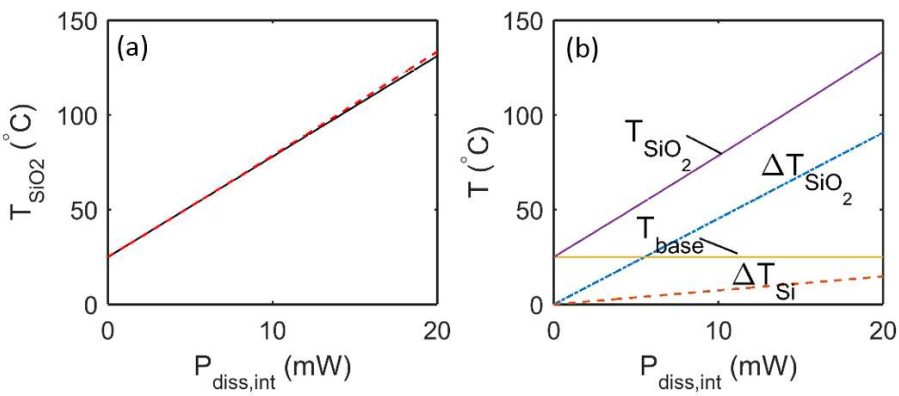

Figure 4.11: (a) Graphene/SiO_2 interface temperature T_{SiO2} versus dissipated power P_{diss} estimated by the linear (solid line) and non-linear (dashed line) thermal resistance model [149]. (b) The non-linear (solid line) temperature T_{SiO2} together with the temperature increase across SiO_2 (ΔT_{SiO2}, dashed dotted line) and across the silicon substrate (ΔT_{Si}, dashed line) versus dissipated power P_{diss}. The base temperature T_{base} is also indicated.

4.4.3 Effect of substrate on $f_{\mathbf{T}}$ and $f_{\mathbf{max}}$

Figure 4.11(a) shows the graphene/SiO_2 interface temperature T_{SiO2} estimated using the analytic thermal resistance model for the linear and the non-linear case. For the linear case the non-linearity of the thermal conductivity (Eq. (7.10)) is not taken into account and $T_{lin} = T_{base} + \Delta T_{Si} + \Delta T_{SiO2}$. Figure 4.11(b) shows the base temperature T_{base} and the non-linear channel temperature T_{SiO2} together with the contributions of the temperature rise across Si and SiO_2, respectively. Clearly, the temperature rise across SiO_2, ΔT_{SiO2} dominantly contributes to the observable total rise in channel temperature due to the low thermal conductivity SiO_2 compared to Si. Therefore, it is important to choose a substrate with high thermal conductivity. Table. 4.1 summarizes the values of κ, optical phonon eneregies and the corresponding v_{sat} calculated using Eq. 2.7 for some materials relevant for the fabrication of GFETs. Clearly, hBN and SiC provide the highest values of κ and OP energies to enhance the GFET high-frequency performance.

Table 4.1: Comparison of thermal conductivites κ [151, 18, 152, 153, 154, 155], optical phonon energies [156, 157, 158, 69, 159, 160] and the corresponding calculated saturation velocity using Eq. 2.7 for $n = 2 \times 10^{16}\,\mathrm{m}^{-2}$ and $T = 300\,\mathrm{K}$.

Material	Graphene	Si	SiC	diamond	Al_2O_3	SiO_2	hBN
κ ($\mathrm{Wcm^{-1}K^{-1}}$)	∼1-10	1.3	5	30	0.018	0.014	3 (in plane)
OP energy (meV)	160	-	100	165	87	55	102
v_{sat} $\times 10^5$(m/s)	5.5	-	3.6	5.5	3.1	1.9	3.6

Chapter 5

Conclusions and future outlook

In this work, methods were developed to study factors and phenomena that are limiting the GFETs' high-frequency performance. Among the studied factors are (i) parasitic capacitances, (ii) device dimensions, (iii) impurities, (iv) saturation velocity and (v) self-heating. In summary, the conducted analysis allows for outlining ways for further device development. (i) The analysis of GFETs in PAPER C suggests that the thickness of the SiO_2 on the Si substrate needs to be relatively large to minimize the effect of parasitic pad capacitances. (ii) The width of the gate fingers needs to be optimised, so that the parasitic gate resistance, which is proportional to gate width, is not suppressing $f_{\max}$, and scaling the gate length will substantially improve f_T and $f_{\max}$. (iii) It is necessary to obtain high-quality interfaces between graphene and the adjacent materials to keep the interface state density as low as possible and thereby minimise hysteresis and charge carrier emission at high fields as it has been discussed in PAPER A and PAPER B. (iv-v) Analysis in PAPER B, C and E indicates that for further improvement of f_T and $f_{\max}$ another substrate material needs to be utilized which offers higher optical phonon energies and thermal conductivity. Higher optical energies will increase the saturation velocity, which was found to be limited by remote phonon scattering associated with the materials adjacent to the graphene channel (PAPER B). Higher saturation velocity entails higher charge carrier velocities which entails higher values of f_T and $f_{\max}$ according to the results in PAPER E. According to Tabel 4.1 hBN is the best choice in terms of OP energy and κ.

GFETs with graphene encapsulated between sheets of hBN have been demonstrated with enhanced saturation velocity [16]. However, there are no reports which present high-frequency perfromance for such structures. Apparently, the fabrication process of hBN encapsulated graphene is not yet mature enough to be incorporated in the high-frequency GFET technology and parasitic elements may suppress the possible high performance. Therefore, Al_2O_3 is first tested in our laboratory as an alternative substrate. It has the advantage to be scalable since Al_2O_3 can be deposited by atomic layer deposition and, additionally, Al_2O_3 can be selectively etched which simplifies the formation of drain and source contacts on graphene. For GFETs with hBN encapsulated graphene only side contact can be formed [161]. Preliminary results of GFETs with a graphene layer encapsulated with Al_2O_3 seem promising, but will be presented elsewhere. Another way, to reduce the self-heating effect could be to decrease the bottom oxide thickness. However, one reason for the increased device performance presented in PAPER C was the increase of the bottom oxide thickness from 300 nm to 1 μm, which reduced the parasitic pad capacitance.

One can conclude that the $f_{\max}$ of GFETs has been improved a factor of two during the last five years from 20 GHz to nearly 40 GHz at $L_g = 0.5\,\mu$m, which was partly enabled by the development of a clean transfer techniques of CVD graphene [83] and the development of the fabrication technique presented here. Other groups reported ~ 30 GHz

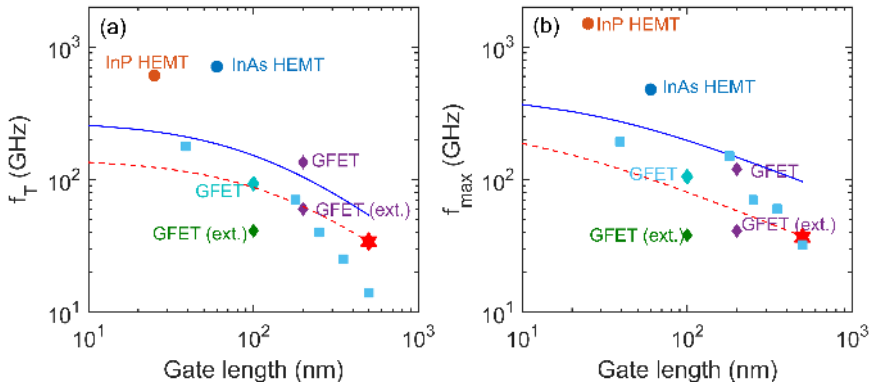

Figure 5.1: Calculated values of extrinsic f_T and f_{max} at $v_{sat} = 3 \times 10^5$ m/s, corresponding to graphene, sandwiched between Al_2O_3, and the gate dielectric thickness $t_{ox} = 10$ nm (blue line) compared to $v_{sat} = 1.5 \times 10^5$ m/s corresponding to graphene on SiO_2, and the gate dielectric thickness $t_{ox} = 22$ nm as in PAPER C (red dashed line), compared to intrinsic and extrinsic GFETs (diamonds) [51, 48, 50, 49], extrinsic MOSFETs (squares) [44, 45, 46, 47] and intrinsic HEMTs (circles) [40, 10]. For calculations, Eq. 2.14 and Eq. 2.15 in Section 2.3.2 were used.

at $L_g = 0.4\,\mu$m in 2016 [132] and 15 GHz at $L_g = 0.8\,\mu$m [140]. Figure 5.1 shows the calculated performance of GFETs if saturation velocity $v_{sat} = 3 \times 10^5$ m/s, corresponding to graphene, sandwiched between Al_2O_3, and $t_{ox} = 10$ nm can be realized. For that case, extrinsic values of f_T and f_{max} beyond 300 GHz can be achieved for device scaling down to $L_g = 100$ nm. This performance would be superior to the reported intrinsic and extrinsic reported performances of GFETs and to the MOSFET performance. However, to compete with the high-frequency performance of HEMTs, the saturation velocity needs to be further enhanced. High extrinsic f_T and f_{max} performance of the GFETs will allow for improving the performance of the receiver presented in PAPER F and for extending the circuit with a low noise frontend rf amplifier.

Another task for future work is the development of a thermal resistance model which can be utilised in device simulators and for optimisation of the device dimensions for minimising the effects of self-heating. Furthermore, in this work, specific graphene terahertz detector test structures, allowing for direct access to the channel by means of near field optical scanning microscopy, have been designed and fabricated. These test structures allowed for direct observation of the plasma wave phenomena in the graphene channel during terahertz illumination. This may open up for exploration of plasma waves in new terahertz applications.

In conclusion, it is possible to further improve the high-frequency performance of GFETs by careful choice of the substrate, the gate oxide materials, and the device dimensions. However, the bottleneck is the graphene quality and the development of a fabrication process that allows minimising defects and impurities at interfaces and in the oxide materials. These imperfections are preventing reliable device performance and are

limiting the performance and are, hence, preventing the application of GFETs in advanced high-frequency applications. Only if this issue can be solved, there is a real chance for graphene in high-frequency transistors and to live up to the original expectations that were put on it since it was first exfoliated.

Chapter 6

Summary of appended papers

Paper A

Effect of oxide traps on channel transport characteristics in graphene field-effect transistors

In this article, the effect of oxide traps on the charge transport in GFETs was studied by including an interface capacitance and interface charge in the capacitance-gate voltage and resistance-gate voltage models. The models allow us to find the interface state density, the mobility, the contact resistance, and the residual charge carrier concentration and to study the effects of uncertainties in material parameters on the extracted values. It was found that, if oxide traps, i.e., interface states, are neglected, then the mobility values are underestimated. Additionally, the value of the Fermi velocity strongly influences the extracted mobility.

My contribution: IV and CV measurements of the graphene-field effect transistors, development of the proposed model, analysis, interpretation of the results, and writing the article.

Paper B

Charge carrier velocity in graphene field-effect transistors

In this work, a method was developed to analyse the mechanisms limiting the charge carrier velocity in GFETs. The analysis of the saturation velocity is of particular interest since drain current saturation via velocity saturation is a possible approach to overcome the zero bandgap issue and to achieve higher $f_{\max}$. The S-parameters of transistors with different residual charge carrier concentrations were measured, and the respective transit frequencies for different bias conditions of V_{GS} and V_{DS} were found. At the same time, the dc current was measured to calculate the charge carrier concentration. The transit frequencies were used in delay-time analysis to estimate the intrinsic transit frequency, which is directly related to the velocity of the charge carriers. Using a field-depended velocity model and a phonon-limited saturation velocity model, we found that the saturation velocity is limited mainly by remote phonons in SiO_2 and intrinsic phonons of graphene. The phonon-limited saturation velocity is inversely proportional to the charge carrier concentration. Additionally, it was shown that a higher impurity concentration leads to a higher charge carrier concentration in the channel due to the emission of charge carriers from traps at high fields, thereby resulting in reduction of the saturation velocity.

My contribution: Conducting the measurements and application of the suggested method to analyse the charge carrier velocity and its limitations in the graphene field-effect transistors at high drain fields, writing the article.

Paper C

Graphene field-effect transistors with high extrinsic $f_{\mathbf{T}}$ and $f_{\mathbf{max}}$

In this work, graphene field effect transistors with state-of-the-art extrinsic high frequency performance of $f_{\mathrm{T}} = 34\,\mathrm{GHz}$ and $f_{\mathrm{max}} = 37\,\mathrm{GHz}$ are presented. The outstanding performance was achieved due to the application of high quality graphene and an optimised fabrication process which resulted in extremely low source/drain contact resistances and reduced parasitic pad capacitances. The scaling behavior is analysed using velocity, saturation velocity and a small-signal equivalent circuit models. Extrapolation predicts extrinsic f_{T} and f_{max} above 100 GHz for a gate length of 50 nm.

My contribution: Device fabrication, dc and high-frequency characterization of the devices, analysis of the high-frequency performance in respect to device dimensions, applying models via expressions of f_{T} and f_{max} derived from the corresponding small-signal equivalent circuit as well as writing the article.

Paper D

Effect of self-heating on $f_{\mathbf{T}}$ and $f_{\mathbf{max}}$ performance of graphene field-effect transistors

In this work, a method is developed to study the actual temperature increase in the GFET channel and its influence on the high-frequency performance. Theoretical expressions for f_{T} and f_{max} based on small-signal parameters are used in combination with models for the field-dependent velocity, and the temperature-dependent and charge carrier concentration-dependent mobility and saturation velocity to find the channel temperature. Our method does not require the estimation of the charge carrier concentration derived from the applied gate voltage and, hence, is free from uncertainties associated with trapping and de-trapping in the gate oxide. Comparison of the found values of the thermal resistance to those obtained by a model based on the solution of Laplace's equation, and obtained by thermosensitive electrical parameters shows good agreement. This work is giving valuable insights for further device optimisation considering heat development in GFETs for high-frequency applications.

My contribution: Device fabrication and development of a method how to assess the effect of self-heating on the high-frequency performance of graphene field-effect transistors and evaluate the channel temperature, interpretation of the results and writing the article.

Paper E

Does carrier velocity saturation help to enhance $f_{\max}$ in graphene field-effect transistors?

In this work, a self-consistent simulator is applied, which solves the drift-diffusion equation coupled with the two-dimensional Poisson's equation to accurately fit the measured dc characteristics of graphene-field effect transistors in combination with a small-signal model of the GFET composed by parameters extracted from linearisation around a bias point of the dc simulations guaranteeing charge conservation and assuming non-reciprocal capacitances. The analysis of the dc and ac measurement results via applying the corresponding models allow for finding material parameters, such as the saturation velocity and low-field mobility and device parameters, such as the contact resistance and capacitances. Thereby, we obtain insight of which physical mechanisms, e.g., velocity saturation, self-heating, are governing the measured transistor performance and, additionally, find regions of RF stability. Based on these insights it is possible to conclude that there is a complex interplay between charge carrier concentration and velocity that influences the value of $f_{\max}$, but that a larger charge carrier velocity increases $f_{\max}$.

My contribution: Device fabrication, support with experimental data, such as dc and high frequency measurements, as well as supporting the interpretation of the modelling results, and supporting writing the article.

Paper F

An integrated 200-GHz graphene FET based receiver

In this article, a millimeter wave integrated receiver composed by a graphene FET 200-GHz mixer and a 1-GHz intermediate frequency amplifier integrated on silicon substrate was demonstrated. The receiver was modelled, fabricated and characterized. The receiver conversion loss is 25 dB across the 185-205 GHz band, which is in good agreement with the circuit simulations. The simulations show that the conversion loss can be reduced by reducing the contact resistance and increasing the charge carrier mobility.

My contribution: Characterization and simulations of the receiver, data analysis and writing the paper. The design of the amplifier, mixer and integrated receiver circuit was not performed as part of this work.

Paper G

Direct nanoscopic observation of plasma waves in the channels of graphene field-effect transistors

In this work direct observation of plasma waves inside a channel of graphene FET

terahertz detector is demonstrated experimentally. Graphene FETs with a buried gate electrode were employed together with near-field THz nanoscopy at room temperature to observe the plasma waves directly on the exposed graphene FET channel. Mapping of the field distribution and establishing an electric-field model enables us to determine the decay length and propagation speed of the plasma waves as a function of gate voltage. The experimental gate voltage dependence of the propagation speed is in good agreement with the model, proving that we successfully visualized plasma waves in a FET channel. The results indicate that plasma waves can be further exploited for THz electronics and photonics.

My contribution: Device fabrication and dc characterization of the devices, as well as supporting the measurements conducted with the free-electron laser in Dresden, supporting the interpretation of results, and supporting writing of the article.

Chapter 7

Appendix

7.1 Fabrication of graphene field-effect transistors

The fabrication process of graphene FETs starts with preparation of 20 mm x 20 mm high bulk resistivity (10 kΩcm) Si substrate which is covered with 1 μm SiO_2 grown by wet thermal oxidation. High quality graphene is transferred on top of the substrate covering an area of ca 10x10 mm^2. The graphene transfer was performed by our collaboration partners [83]. The details of the further fabrication steps, shown in Fig. 3.2, are as follows.

1. Evaporation of Al seed layer
   a) E-beam evaporation of 10 Å Al (at deposition rate 0.5 Å/s)
   b) Oxidation on hotplate for 5 min at 160 °C
   c) Repeat a)-b) four times
2. E-beam lithography of alignment marks
   a) Spin MMA (8.5) EL10, 1 min, 3000 rpm (∼400 nm); Bake 5 min on hotplate at 160 °C
   b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (∼150 nm); Bake 5 min on hotplate at 160 °C
   c) Exposure with e-Beam, dose 350 $\mu C/cm^2$, 35 nA
   d) Developer: 1. N-Amylacetate 45 s + blow dry with N_2, 2. MIBK:IPA 1:1, 120 s + blow dry with N_2
   e) Remove resist using oxygen plasma etching (50 W for 10 s)
   f) Remove Al_2O_3 in buffered oxide etch (BOE:H_2O 1:10) for 5 s
   g) Remove graphene using oxygen plasma etching (50 W for 10 s)
   h) E-beam evaporation of 40 Å Ti\700 Å Au
   i) Lift-off: acetone for 10 min at 65 °C; rinse in acetone; rinse in isopropanol
3. Mesa lithography
   a) Spin man2403, 1 min, 3000 rpm (∼300 nm); Bake 1 min on hotplate at 90 °C
   b) Exposure with e-Beam, dose 170 $\mu C/cm^2$, 10 nA
   c) Developer: MF-24A 45 s; wash in H_2O
   d) Remove resist using oxygen plasma etching (50 W for 10 s)

e) Remove Al_2O_3 in buffered oxide etch (BOE:H_2O 1:10) for 5 s

f) Remove graphene using oxygen plasma etching (50 W for 10 s)

g) Wash off resist in acetone and isopropanol

4. Ohmic contact lithography

a) Spin MMA (8.5) EL10, 1 min, 3000 rpm (∼400 nm); Bake 5 min on hotplate at 160 °C

b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (∼150 nm); Bake 5 min on hotplate at 160 °C

c) Exposure with e-Beam, dose 360 $\mu C/cm^2$, 10 nA

d) Developer: 1. N-Amylacetate 45 s + blow dry with N_2, 2. MIBK:IPA 1:1, 120 s + blow dry with N_2

e) Remove Al_2O_3 in buffered oxide etch (BOE:H_2O 1:10) for 5 s

f) E-beam evaporation of 10 Å Ti\150 Å Pd\2500 Å Au

g) Lift-off: acetone for 10 min at 65 °C; rinse in acetone; rinse in isopropanol

5. Formation of gate oxide

a) Atomic layer deposition in thermal mode at 300 °C → total Al_2O_3 thickness ∼22 nm

6. Gate contact lithography

a) Spin MMA (8.5) EL10, 1 min, 2800 rpm (∼420 nm); Bake 5 min on hotplate at 160 °C

b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (∼150 nm); Bake 5 min on hotplate at 160 °C

c) Exposure with e-Beam, dose 390 $\mu C/cm^2$, 10 nA

d) Developer: 1. N-Amylacetate 45 s + blow dry with N_2, 2. MIBK:IPA 1:1, 120 s + blow dry with N_2

e) E-beam evaporation of 100 Å Ti\2900 Å Au

f) Lift-off: acetone for 10 min at 65 °C; rinse in acetone; rinse in isopropanol

7. Contact pads lithography

a) Spin MMA (8.5) EL10, 1 min, 2800 rpm (∼420 nm); Bake 5 min on hotplate at 160 °C

b) Spin ARP 6200.13 1:1, 1 min, 3000 rpm (∼150 nm); Bake 5 min on hotplate at 160 °C

c) Exposure with e-Beam, dose 390 $\mu C/cm^2$, 35 nA

d) Developer: 1. N-Amylacetate 45 s + blow dry with N_2, 2. MIBK:IPA 1:1, 120 s + blow dry with

e) Remove resist using oxygen plasma etching (50 W for 10 s)

f) Remove Al_2O_3 in buffered oxide etch (BOE:H_2O 1:10) for 5 s

g) E-beam evaporation of 100 Å Ti\2900 Å Au

h) Lift-off: acetone for 10 min at 65 °C; rinse in acetone; rinse in isopropanol

7.2 Delay-time analysis

The delay-time analysis utilized in PAPER B was developed based on the methodologies in [162, 81, 163]. The extrinsic f_T of a field-effect transistor is inversely proportional to the total delay (τ_{tot}) of the device. Rewriting Eq. 2.14 and using $R_{ds} = 1/g_{ds} = R_{DS} - R_C$ the total delay time can be expressed as:

$$\tau_{tot} = \frac{1}{2\pi f_T} = \frac{C_{gs} + C_{gd}}{g_m} \cdot \left(1 + \frac{R_C}{R_{ds} - R_C} + \frac{C_{gd} g_m R_C}{C_{gs} + C_{gd}} + \frac{C_{PG}}{C_{gs} + C_{gd}}\right). \tag{7.1}$$

The τ_{int} is associated with the transit time of the electrons through the channel and is expressed through the intrinsic transit frequency $f_{T,int}$ as:

$$\tau_{int} = \frac{1}{2\pi f_{T,int}} = \frac{C_{gs} + C_{gd}}{g_m}. \tag{7.2}$$

Using Eq. 7.2 and $C_{gd} = 0.5 \cdot C_{ox} W_g L_g$, Eq. 7.1 can be written as

$$\tau_{tot} = \tau_{int} + \tau_{int} \frac{R_C}{R_{ds} - R_C} + 0.5 \cdot C_{ox} W_g L_g R_C + \frac{C_{PG}}{g_m} = \tau_{int} + \tau_{ext} + \tau_{pad}. \tag{7.3}$$

Apparently, τ_{tot} is the sum of τ_{int}, the extrinsic delay time τ_{ext} associated with the charging delays caused by R_C and C_{gs}, and the parasitic pad delay $\tau_{pad} = C_{PG}/g_m$. By

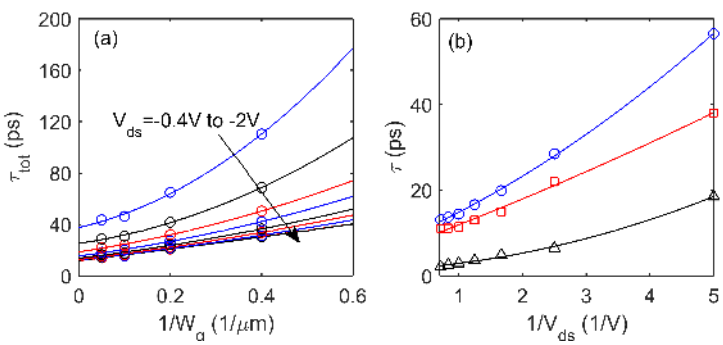

Figure 7.1: a) Delay-time versus the reciprocal of the gate width $W_g = (2.5, 5, 10)\mu$m for drain bias from top to bottom $V_{DS} = 0.2$ to 2 V in steps of $\Delta V_{DS} = 0.2$ V. b) Measured delay-time τ_{tot} (open circles) of the device with $W_g = 20\,\mu$m, delay-time minus gate pad delay $\tau_{tot} - \tau_{pad}$ (open squares) and gate pad delay τ_{pad} (open triangles) versus reciprocal of the drain-source voltage.

increasing the width of the device, the effect of the pad capacitance can be minimized. This dependence is utilized in PAPER B. By measuring τ_{tot} for devices with the same L_{g} and with similar n_0 but different $W_{\mathrm{g}} = (2.5, 5, 10, 20)\,\mu$m and plotting τ_{tot} versus the inverse of the device width $1/W_{\mathrm{g}}$, as shown in Fig. 7.1, the y-intercept gives the delay time (τ) without the contribution of τ_{pad}. This procedure is performed for different drain biases. τ_{pad} versus drain bias is found by subtracting τ at the y-intercept from τ_{tot}, as shown in Fig. 7.1(b). As soon τ_{pad} is found, all parameters that are needed to calculate the τ_{int} are known. R_{ds} is calculated using measured output characteristics and R_{C} is extracted using fitting of the drain-source resistance model to measured transfer characteristics. τ_{int} is used to calculate the intrinsic transit frequency:

$$f_{\mathrm{T,int}} = \frac{1}{2\pi\tau_{\mathrm{int}}}. \tag{7.4}$$

7.3 Analytic thermal resistance model

The analytic thermal resistance model is based on that presented in Ref. [149] and has been originally developed for channel temperature analysis of GaN HEMTs with nonlinear thermal conductivity. We adapt the model for our GFET design. Figure 7.2 shows the geometric parameters of the GFET and the cross section with the corresponding temperature gradient between the different layers.

The total temperature rise ΔT across all involved layers is

$$\Delta T = \Delta T_{\mathrm{SiO2}} + \Delta T_{\mathrm{Si}}, \tag{7.5}$$

where the temperature rise in the SiO_2 layer is ΔT_{SiO2} and in the silicon substrate layer is ΔT_{Si}, which are given by

$$\Delta T_{\mathrm{SiO2}}(T_0) = \frac{P_{\mathrm{mm}}}{\pi k_{\mathrm{SiO2}}(T_0)} ln\left(\frac{4t^*_{\mathrm{SiO2}}}{\pi\rho L^*_{\mathrm{g}}}\right), \tag{7.6}$$

and

$$\Delta T_{\mathrm{Si}}(T_0) = \frac{P_{\mathrm{mm}}}{\pi k_{\mathrm{Si}}(T_0)} ln\left(\frac{f(1/2t^*_{\mathrm{SiO2}})}{f(\sqrt{1+(1/s^*)^2-(t^*_{SiO2}/s^*)^2})}\right) + \frac{\sqrt{2}P_{\mathrm{mm}}}{\pi s^* k_{\mathrm{Si}}(T_0)} ln\left(\frac{h((1/t^*_{Si})^2-(2t^*_{SiO2}/t^*_{Si})^2)}{h((1/s^*)^2-(2t^*_{SiO2}/s^*)^2)}\right), \tag{7.7}$$

respectively, where

$$f(x) = \frac{\sqrt{x+1}+\sqrt{x-1}}{\sqrt{x+1}-\sqrt{x-1}}, \tag{7.8}$$

and

$$h(x) = \sqrt{\frac{\sqrt{x+1}+1}{\sqrt{x+1}-1}}, \tag{7.9}$$

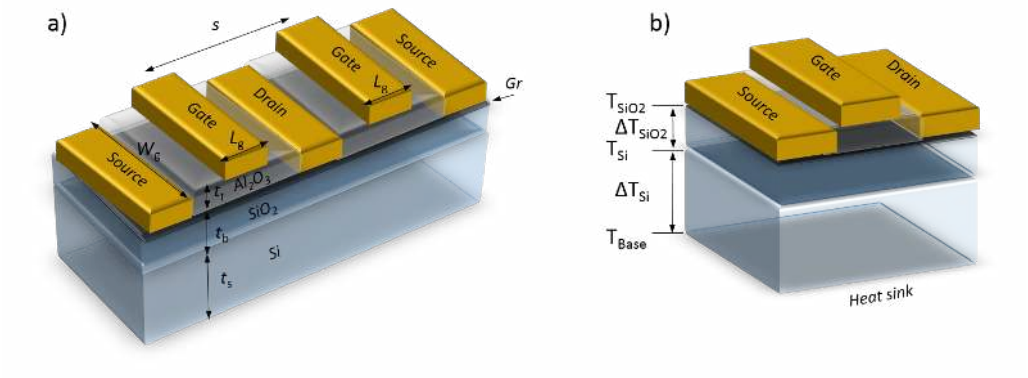

Figure 7.2: (a) GFET geometric parameters. Graphene is placed on a 1 μm thick SiO_2 layer grown on 300 μm thick Si substrate. Gate parameters are the gate length L_g, the gate width W_g, and the gate spacing s. (b) Cross section of the GFET showing the temperature and temperature gradient between the different layers.

and $t^*_{SiO2} = \rho t_{SiO2}/W_g$, $t^*_{Si} = \pi t_{Si}/W_g$, $s^* = s\sqrt{2}/W_g$, $L^*_g = L_g/W_g$, $P_{mm} = P_{diss}/(NW_g)$, $\rho = 4k_{SiO2}/(\pi^2 k_{Si})$, where N is the number of gate fingers, T_0 is a reference temperature, P_{diss} is the total dissipated power, P_{mm} is the dissipated power density in Watts per mm of gate width, k_{SiO2} is the SiO_2 thermal conductivity, and k_{Si} is the silicon thermal conductivity.

The temperature dependent thermal conductivity is

$$k(T) = k_{T0}\left(\frac{T}{T_0}\right)^{\alpha}, \tag{7.10}$$

where $\alpha \neq 1$ when taking phonon-phonon interactions in the crystal into consideration, and k_{T0} is the thermal conductivity at T_0. Using Kirchhoff's transformation the heat equation may be solved as

$$T_{\text{non-lin}}(\Delta T_{lin}, T_0, \alpha) = T_0\left(1 + (1-\alpha)\left(\frac{\Delta T_{lin}}{T_0}\right)^{\frac{1}{1-\alpha}}\right), \tag{7.11}$$

where $T_{\text{non-lin}}$ is the temperature accounting for non-linear thermal conductivity, and T_{lin} is the linear temperature increase calculated for the different layers using Eqs. (7.6-7.7).

The channel temperature T_{SiO2}, which effectively is the expected channel temperature of the GFET, is calculated as follows:

- Assume base temperature $T_{Base} = 300$ K, since connected to a heat sink;
- Calculate temperature increase in the silicon substrate ΔT_{Si} using Eq. 7.7 with $T_0 = T_{Base}$, and $k_{Si} = 140$ W/mK [164];
- Calculate T_{Si} using Eq. 7.11 with $\Delta T_{lin} = \Delta T_{Si}$, $T_0 = T_{Base}$, and $\alpha_{Si} = 1.3$;

- Calculate temperature increase in SiO_2 ΔT_{SiO2} using Eq. 7.6 with $T_0 = T_{Si}$, and $k_{SiO2} = 1.4\,\mathrm{W/mK}$ [165];
- Calculate T_{SiO2} using Eq. 7.11 with $\Delta T_{lin} = \Delta T_{SiO2}$, $T_0 = T_{Si}$, and $\alpha_{SiO2} = 0.2$ [165].

7.4 Thermo-sensitive electrical parameters

The method of thermo-sensitive electrical parameters [166, 167] is used in PAPER E to estimate the thermal resistance R_{th} based on the differential of the gate leakage current I_g with respect to the increase of the dissipated power and the temperature as

$$R_{th} = (\partial I_g / \partial P_{diss}) \cdot (\partial T / \partial I_g). \tag{7.12}$$

The measurements were conducted with dc probes using only one finger of the GFET, therefore, $W_g = 15\,\mu\mathrm{m}$ instead of $W_g = 2 \times 15\,\mu\mathrm{m}$. Figure 7.3(a-b) shows the measured drain current I_{DS} and gate leakage current I_{GS} versus drain-source voltage V_{DS} for different external chuck-temperatures. I_{DS} increases with V_{DS} but decreases with elevated temperatures as discussed in PAPER D, whereas I_{GS} increases with $P_{density,int}$ and T_{ext} due to external heating and self-heating in agreement with the most probable conduction mechanisms [168, 169]. From the measured IV characteristics the intrinsic dissipated power is calculated as $P_{diss,int} = I_{DS} \cdot (V_{DS} - R_C I_{DS})$, where R_C is the contact resistance extracted from the drain-source resistance versus gate voltage measurements as described above. Figure. 7.3(c) shows I_{GS} versus external chuck-temperature for different V_{DS} together with exponential fitting curves. The fitting curves are used to estimate the partial derivative of I_{GS} with respect to T_{ext}. Figures. 7.3(d-e) show I_{GS} versus $P_{diss,int}$ and $\partial I_{GS}/\partial P_{diss,int}$, where the derivative is based on the exponential fitting curves in Fig. 7.3(c). The results from Figs. 7.3(d),(f) are used in Eq. (7.12) to calculate R_{th}.

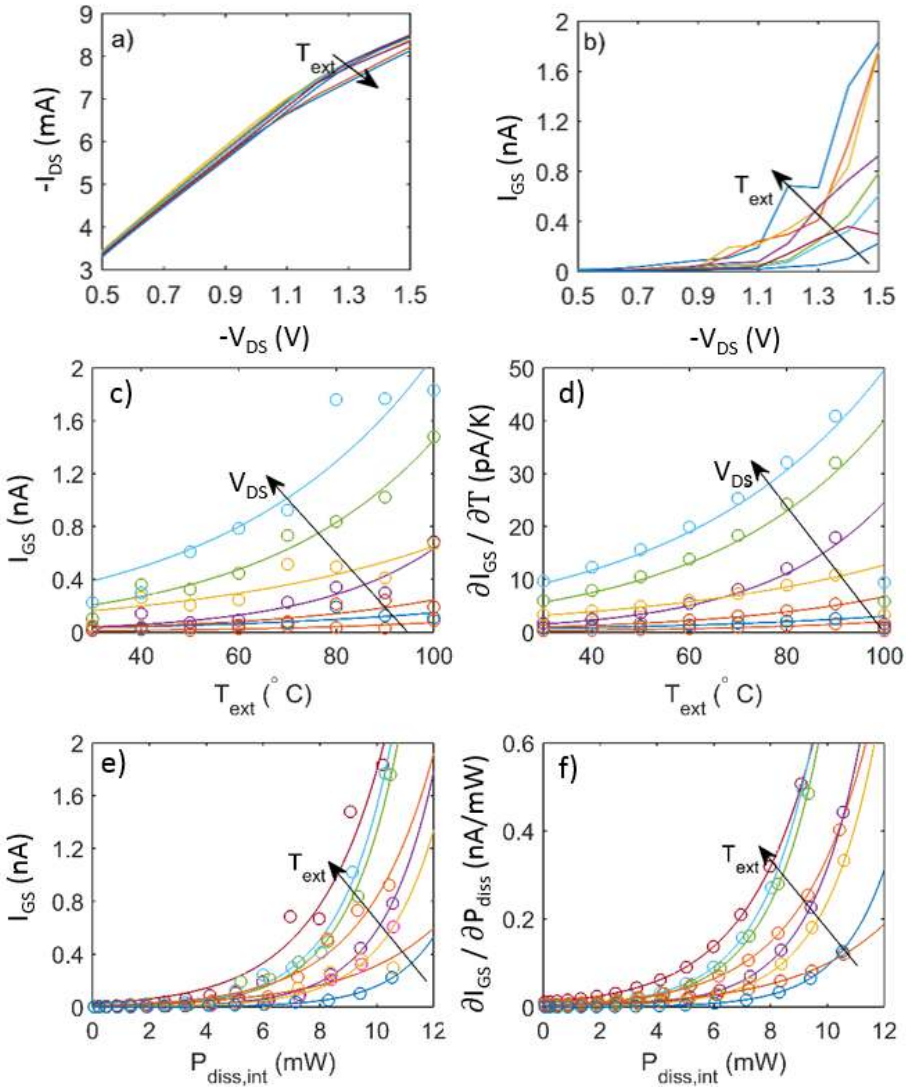

Figure 7.3: (a) Drain current I_{DS} and (b) gate-leakage current I_{GS} versus drain-source bias V_{DS} at different external chuck-temperatures $T_{\mathrm{ext}} = (25, 60, 70, 80, 90, 100)\,^{\circ}\mathrm{C}$ for a GFET with L_{g}=0.5 μm and $W_{\mathrm{g}} = 2 \cdot 15\,\mu$m. The applied gate bias is $V_{\mathrm{GS}} = -1\,\mathrm{V}$. (c) Gate-leakage current I_{GS} versus T_{ext} and (d) the corresponding derivative $\partial I_{\mathrm{GS}}/\partial T$ for different V_{DS}. (e) I_{GS} versus intrinsic dissipated power $P_{\mathrm{diss,int}}$ and (f) corresponding derivative $\partial I_{\mathrm{GS}}/\partial P_{\mathrm{diss,int}}$ for different T_{ext}.

ACKNOWLEDGEMENTS

Hereby, I want to express my sincere gratitude to a number of people which supported me on my path towards the PhD degree.
First, I would like to thank Jan Stake, the head of the Terahertz and Millimetre wave Laboratory (TML), to employ me and giving me the chance to make this experience.
Furthermore, I would like to acknowledge Andrei Vorobiev, my main supervisor, for always being available for discussions and giving his advice.

A big thank you to all my office mates and ex office mates, Andrey Gerneralov, Muhammad Assad, and Michael Andersson, for the pleasantly shared time and discussions, whether it was work related and not. A special thanks to my office mate Xinxin Yang who shared the PhD experience with me all the way and helped to make it an enjoyable time.

I would also like to thank the rest of the former and current Master students, PhD students and post docs at the TML and MEL laboratories for being a nice group to have around and do after work activities together, Juan Cabello, Nooshien Laderian, Narendra Acharya, Anis Moradikouchi, Eunjung Cha, Divya Jayasankar, Stella Bevilacqua, Ahmed Adel Hassona, Dhecha Nopchinda, Isabel Harrysson Rodrigues, Junjie Li, and Marijana Krivic. Not less I want to thank my senior colleagues at TML, Kjell Jeppson, Helena Rodilla, Serguei Cherednichenko, Mats Myremark, Vladimir Drakinskiy, Josip Vukusic, Tomas Bryllert, Peter Sobis, for being supportive when needed.

In addition, a thank you to Dr. Johan Liu, Yifeng Fu, Per Hyldgaard, Zhibin Zhang for the collaboration. I am thankful to Antonio Lombardo and the Graphene Centre for exchanging ideas, to Daniel Neumaier and Christoph Stampfer and their teams for supplying material and valuable knowledge, and to Olof Engström for a fruitful collaboration. I would also like to thank Jasper Ruhkopf and Max Lemme for supporting my measurements at the University of Siegen, and Samina Bidemshkipour for the support during device fabrication in the beginning of my PhD time.

I am grateful to the cleanroom staff for all your help and the support.
Also, I would like to thank Debora Perlheden for her support in coordinating the administrative work.

Above all, I am extremely thankful to my family, Vedad and Ervin, my parents, my brothers, my family in law and my friends for always being there for me and supporting me in good and in bad times!

This work was supported in part by the Swedish Research Counsel (VR) under Grant Nos. 2012-4978, 2014-5470 and 2017-04504, in part by the Swedish Foundation for Strategic Research (SSF) under Grant No. SE13-0061, and in part by the European Union's Horizon 2020 research and innovation programme Graphene Flagship under grant agreement Nos. 696656 and 785219.

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