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Graphene integration with Nitride semiconductors for high power and high frequency electronics

F. Giannazzo[1], G. Fisichella[1], G. Greco[1], A. La Magna[1], F. Roccaforte[1], B. Pecz[2], R. Yakimova[3], R. Dagher[4,5], A. Michon[4], Y. Cordier[4]

[1] CNR-IMM, Strada VIII, 5, Zona Industriale, 95121 Catania, Italy.
[2] Institute for Technical Physics and Materials Science Research, Centre for Energy Research, HAS, Budapest, Hungary
[3] Department of Physics Chemistry and Biology, Linköping University, Linköping, Sweden
[4] CRHEA-CNRS, Rue Bernard Gregory, 06560 Valbonne, France
[5] Université de Nice Sophia-Antipolis, 28 Av. Valrose, 06103 Nice, France

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* Corresponding author: e-mail: filippo.giannazzo@imm.cnr.it, Phone: +39 095 5968242, Fax: +39 095 5968312

Group III Nitride semiconductors (III-N), including GaN, AlN, InN, and their alloys, are currently the materials of choice for many applications in optoelectronics (light-emitting diodes, laser diodes), and high-power and high-frequency transistors. Due to its attractive electrical, optical, mechanical and thermal properties, graphene (Gr) integration with III-N technology has been considered in the last few years, in order to address some of the major issues which still limit the performances of GaN-based devices. To date, most of the studies have been focused on the use of Gr as transparent conductive electrode (TCE) to improve current spreading from top electrodes and light extraction in GaN-LEDs. This paper will review recent works evaluating the benefits of Gr integration with III-N for high power and high frequency electronics. From the materials side, recent progresses in the growth of high quality GaN layers on Gr templates and in the deposition of Gr on III-N substrates and templates will be presented. From the applications side, strategies to use Gr for thermal management in high-power AlGaN/GaN transistors will be discussed. Finally, recent proposals of implementing new ultra-high-frequency (THz) transistors, such as the *Gr Base Hot Electron Transistor* (GBHET), by Gr integration with III-N will be highlighted.

1 Introduction

Group III–Nitride semiconductors (III-N), including GaN, AlN, InN and their alloys (AlGaN, InGaN), are key technological materials for optoelectronics devices, such as light-emitting diodes (LEDs) and laser diodes (LDs) [1,2]. Furthermore, the continuous improvement of the material quality has recently opened new perspectives also in the fields of high power and high frequency applications. In particular, GaN and related Al-based alloys ($Al_xGa_{1-x}N$) are outstanding electronic materials for the next generation of high power and high frequency devices. In fact, due to the presence of spontaneous and piezoelectric polarization, a two-dimensional electron gas (2DEG) is generated at the AlGaN/GaN interfaces, with typical sheet carrier densities n_s in the order of $\sim 1\times10^{13}$ cm^{-2}, and high values of the carrier mobility (1000–2000 cm^{2}V^{-1}s^{-1}) [3]. These unique features, combined with the high critical electric field (3.3 MV/cm) and electron saturation velocity (2.5×10^7 cm/s) of GaN, enable the fabrication of high electron mobility transistors (HEMTs) operating up to several tens of GHz and with a high-power handling capability [4].

In spite of these great promises, some issues still limit the performances of GaN-based HEMTs. As an example, self-heating due to inefficient power dissipation currently represents one of the main problems for the high-power operation of these devices. In fact, the high electric field at gate edge of GaN transistor and the resulting non-uniform distribution of dissipated power can lead to the formation of

hotspots near the device channel. These can be responsible of a degradation of the drain current, an increase of the gate-leakage current and a poor reliability.

	Si	GaN	Graphene
Bandgap (eV)	1.12 Indirect	3.4 Direct	0
Intrinsic carrier conc. (cm^{-3}) at 300K	1.5×10^{10}	1.9×10^{-10}	
2DEG carrier density (cm^{-2})		10^{13}	10^{11} - 10^{13} (tunable by field effect or doping)
Electron mobility ($cm^2V^{-1}s^{-1}$) at 300 K	1350	900 (bulk GaN) 1000 – 2000 (AlGaN/GaN 2DEG)	10^3 - 10^5
Saturation electron velocity (10^7 cm/s)	1.0	2.5	3
Critical electric field (MV/cm)	0.3	3.3	
Thermal conductivity ($Wm^{-1}K^{-1}$)	150	150 - 210	2000 (bulk graphite) 5000 (Graphene)

Table I. Comparison of the electronic properties of Si, GaN and graphene.

Due to its excellent electrical, optical, thermal and mechanical properties, graphene (Gr) [5] has been the object of several scientific and technological interests in the last years. This interest has been supported by the development of many synthesis methods allowing to grow large area of Gr. The epitaxial growth of Gr on SiC by controlled high temperature graphitization [6], initiated in the mid 70's [7], has been further developed to grow high quality Gr at the wafer scale in a rather simple way [8,9,10]. More recently, the direct growth of Gr on SiC has been demonstrated using both molecular beam epitaxy (MBE) [11,12] and chemical vapor deposition (CVD) [13,14] set-up. The catalytic chemical vapour deposition (CVD) allows to grow Gr on various surfaces, from monocrystalline substrate [15] to polycrystalline thin film [16] or foil [17], the catalytic growth surfaces being mainly transition metals (Cu, Ni…), including precious metal (Pt, Ir…), or possibly metalloid such as Ge [18]. From a technological point of view, the interest of catalytic CVD lays in its ability to grow large area of Gr on low costs surfaces [19] and in the possibility to transfer Gr on arbitrary substrate.

Integration of Gr with III-N semiconductor technology has been recently considered, with the aim to improve the performances of GaN based optoelectronics or high power devices. Furthermore, new device concepts can arise from the combination of the outstanding physical properties of these two classes of materials. A summary of the main electronic and thermal properties of hexagonal GaN and of Gr is reported in *Table I*. The properties of Si, the most commonly used semiconductor in electronics, have been also included for comparison.

To date, most of the efforts to integrate Gr with III-N semiconductors have been performed in connection with the GaN-based LED technology [20]. Gr has been evaluated as a transparent conductive electrode (TCE) both for the p-GaN top layer in the lateral LEDs on sapphire substrates and for the n-GaN layer in the vertical LEDs architecture [21]. In most of the studies, single or multilayers Gr membranes grown by chemical vapour deposition (CVD) on catalytic metals (Ni, Cu,..) and transferred to the target substrates have been used. The primary requirement for a TCE is the combination of high optical transparency (Tr) and low sheet resistance (R_{sh}). Several progresses have been performed in the last years to optimize the trade-off between Tr and R_{sh} in the case of Gr [22]. As an example R_{sh} ≈8.8 Ω/sq and Tr≈84% have been obtained intercalating multilayers of Gr with $FeCl_3$ [23]. Bae et al. [19] reported the roll-to-roll production and wet- chemical doping of large area monolayer Gr films grown by CVD onto flexible Cu substrates, reaching a low R_{sh}≈125 Ω/sq and Tr≈97.4%. Besides the high Tr and low R_{sh}, another key requirement for the TCE is the formation of a low contact-resistance Ohmic contact to p-GaN (in the case of lateral LEDs) or to n-GaN (in the case of vertical LEDs). This generated several studies on the vertical current transport across the Gr/GaN heterojunctions [24,25,26,27], as discussed in more details in the *Section 2* of this paper.

Other literature studies have considered the integration of Gr with Nitrides for high power and high frequency applications. As an example, due to its excellent thermal conductivity of up to 5000 $W\ m^{-1}K^{-1}$ (the highest of all known materials) [28], Gr has been suggested as a suitable candidate for solving self-heating problems in high-power HEMT devices based on AlGaN/GaN heterostructures [29], as well as in high power solid state optoelectronic devices [30]. Proof of concept experiments for using few layers of Gr as heat spreaders for local thermal management in AlGaN/GaN based transistors will be discussed in the *Section 3* of this paper.

Due to its excellent carrier mobility, Gr has been used as channel material for high frequency (RF) transistors with cut-off frequencies up to 300 GHz [31,32]. However, the zero bandgap in the Gr energy bandstructure gives rise to transfer characteristics (I_D-V_G) with a low on/off current ratio (typically lower than 10) and an high I_{off}. Clearly, the low I_{on}/I_{off} makes Gr FETs unsuitable for logic applications. Furthermore, the high I_{off} represents a serious concern in terms of power efficiency of the devices. Finally, the poor saturation behaviour of the output characteristics (also due to the lack of a bandgap) has a negative impact on the power gain of Gr RF transistors [32]. In this context, alternative 2D materials with a bandgap, such as the transition metal dichalcogenides (MoS_2, $MoSe_2$, WS_2, WSe_2,..)

[33] and phosporene [34], are currently under investigation for next generation thin film transistors for logic and/or high frequency applications. In particular, MoS_2 has been the object of several studies, due to its natural abundance and high stability in ambient conditions, in addition to sizable bandgap (1.8 eV direct bandgap for single layer and 1.2 eV indirect bandgap for multilayers), and reasonable mobility values (~200 $cm^2V^{-1}s^{-1}$) [35]. Very promising performances, such on/off current ratio $>10^7$ and nearly ideal subthreshold swing (≈70 mV/decade) have been already demonstrated for top gated monolayer MoS_2 transistors with high-k gate dielectrics [35]. Furthermore, operation at GHz frequency (with comparable values of the cut-off frequency f_T=6 GHz and maximum frequency of oscillation f_{max}=8.2 GHz) has been demonstrated for few layers MoS_2 transistors [36]. In spite of these great promises, several issues need to be addressed to fully exploit the potentialities of MoS_2 and other transition metal dichalcogenides. As a matter of fact, most of the demonstrated device prototypes with these materials have been fabricated using small flakes exfoliated from bulk crystals, although CVD deposition methods are also rapidly developing [37]. Other critical issues under investigation are the formation of low resistance contacts [38,39,40], controlled doping [41,42], interface with dielectrics [43,44].

As a matter of fact, the state-of-the-art Gr growth methods are much more mature than the currently available synthesis methods of alternative 2D materials. Hence, the use of Gr can guarantee superior reproducibility of devices performances on wafer scale. To overcome the above discussed limitations of Gr related to the lack of a bandgap, novel vertical device concepts, such as the Gr base hot electron transistor (GBHET) [45,46] have been proposed and demonstrated on silicon in the last years, showing I_{on}/I_{off} current ratios ($>10^4$) not reachable by conventional lateral Gr FETs and the potentiality of operating at ultrahigh frequencies (THz) [47]. The possibility of implementing such device concepts using Gr heterostructures with SiC and III-N semiconductors is under investigation by various research groups. The most recent developments in this advanced research field will be illustrated at the end of *Section 3*, whereas recent studies on the electrical properties of Gr/AlGaN/GaN heterojunctions (one of the building blocks of a perspective GBHET) will be discussed in the *Section 2*.

To date, most of the Gr/III-N heterostructures investigated for proof-of-concept devices demonstration have been fabricated by transfer of Gr layers exfoliated from graphite or grown by CVD on metals. However, the transfer procedure needs to be carefully optimized, since it can cause damage to Gr, contaminations by polymers or metal residues. Furthermore, the final device structure can suffer from a lack of robustness, due to adhesion problems between transferred Gr and the III-N substrate. Clearly, the direct deposition of Gr on the surface of Nitride semiconductors and/or the growth of III-N films on Gr could represent the best solution for the realization of Gr/III-N heterostructures. However, several challenges must be addressed to achieve this goal. The most recent progresses in this research field will be finally reviewed in the *Section 4* of this paper.

2 Electronic transport in graphene/III-N heterostructures

2.1 Gr contacts on GaN. Motivated by the technological interest for LED technology, several experimental investigations have been reported so far to understand the charge transport mechanisms across Gr contacts to n- and p-type doped GaN [24,25,26,27]. Single and multilayer Gr contacts to GaN have been shown to exhibit a rectifying behaviour. Typically, the Schottky barrier height (SBH) Φ_B has been extracted by fitting the forward bias I–V curves of Gr/GaN diodes using the thermionic emission equation:

$$I = AA^{*}T^{2}\exp\left(-\frac{q\Phi_B}{kT}\right)\exp\left[\frac{q(V-IR_s)}{nkT}\right]$$

where A is the Gr contact area, A* is the Richardson constant (26.4 $Acm^{-2}K^{-2}$ for n-GaN and 96.1 $Acm^{-2}K^{-2}$ for p-GaN), k is the Boltzmann constant, T is the temperature, R_s is the series resistance and n is the ideality factor.

	Ideal	I-V	XPS
$\Phi_{B,n}$ (eV)	0.7	0.33±0.01 [26] 0.36±0.01 [27] 0.73 [25]	0.57 [27]
$\Phi_{B,p}$ (eV)	2.7	0.36±0.01 [26] 0.49±0.02 [25]	2.08 [27]

Table II. Literature values of the Schottky barrier height for Gr contacts on n- and p-type GaN, obtained by thermionic emission fitting of forward bias I-V curves and XPS analyses. For comparison, the ideal values obtained as the difference of Gr workfunction and GaN electron affinity are also reported.

Table II summarizes the obtained SBH values $\Phi_{B,n}$ and $\Phi_{B,p}$ measured by different groups on n- and p-type GaN, respectively. For comparison, the ideal value of the SBH (calculated as the difference between the Gr workfunction W_{Gr} and GaN electron affinity χ_{GaN}) and the value obtained by XPS measurements are also listed [27].

Typically, the $\Phi_{B,n}$ and $\Phi_{B,p}$ values obtained from I-V measurements are rather lower than the corresponding theoretical values. On the other hand, the SBH values obtained by XPS fall between the ideal values and those evaluated by I-V analyses. *Zhong et al.* [26] recently proposed the following theoretical model to describe the SBH at the Gr/GaN interface. The band alignments of Gr with n-type and p-type GaN when the two materials are separated and after the contact formation are schematically illustrated in Fig.1.

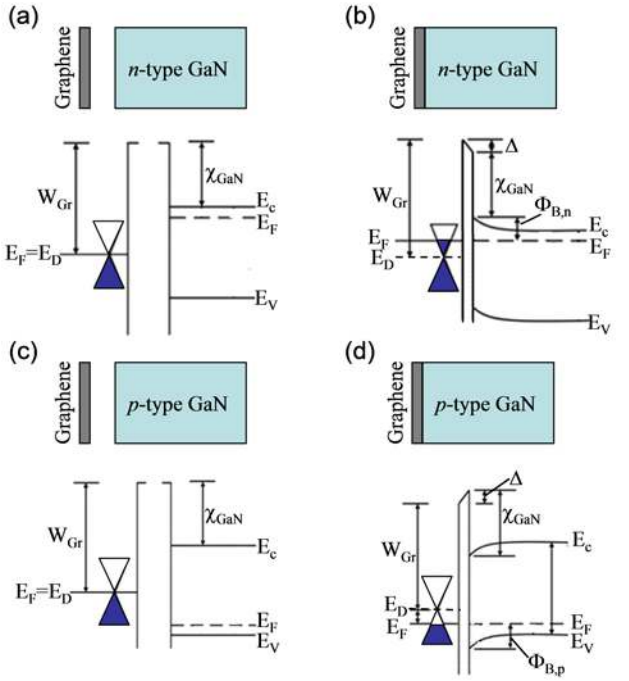

Figure 1 Schematic representation of the energy band diagram of Gr and n-type GaN before (a) and after contact formation (b). Energy band diagram of Gr and p-type GaN before (c) and after contact formation (d). The model is discussed more in details in Ref. [26].

Before contact formation, (Fig.1(a) and (c)) Gr is assumed to be neutral, i.e. the Fermi level is coincident with the Dirac point (E_F=E_D). Due to the linear dependence of the density of states on energy in Gr, when the Gr/semiconductor contact is formed, a shift of Gr Fermi level is induced by the charge transfer at the interface. In particular, electron are transferred into (out of) Gr when it contacts with n-GaN (p-GaN), resulting in a shift of E_F in the conduction (valence) band. Hence, both $\Phi_{B,n}$ and $\Phi_{B,p}$ result to be lower than the difference between the work-function of neutral Gr (W_{Gr}) and χ_{GaN}, as illustrated in Fig.1(b) and (d). In addition to this effect, which depends on the peculiar density of states of Gr, the presence of GaN surface states was also found to affect the SBH measured by I-V characteristics. The effect of surface states, which is illustrated in the band diagrams in Fig.1(b) and (d) considering an ultrathin insulating layer at the interface between Gr and GaN, further reduces the SBH. It can be very important in the case of Gr/p-GaN interface, where the $\Phi_{B,p}$ values obtained by I-V analyses are typically much lower than the ideal ones. Finally, defects (such as screw-type threading dislocations) in GaN epilayers are known to work as preferential current path from GaN surface to the bulk and can also be partially responsible of the reduced SBH obtained by I-V measurements. On the other hand, *Kumar et al.* obtained a Gr/GaN diode with 0.6-0.72 eV barrier height which is found to have lower level of barrier inhomogeneities than conventional Ni/GaN diode [48].

2.2 Gr contacts onto AlGaN/GaN heterostructures. Differently than for Gr/GaN contacts, fewer studies have been reported to date on the electrical behaviour of Gr contacts to AlGaN/GaN heterostructures. Furthermore, these studies show quite different results. As an example, it has been shown that Gr insertion between a metal and AlGaN gives rise to a Schottky contact with low barrier height, i.e., ranging from ~0.4 to ~0.6 eV depending on the metal workfunction [49]. Another work indicates that a Gr interlayer between a metal (Cr) and AlGaN provides an Ohmic contact to AlGaN/GaN heterostructures [50]. These differences can depend on several factors, including the structural properties (thickness, composition, defectivity, etc.) of the AlGaN barrier layer.

Recently, *Pandit et al.* [51] investigated current transport mechanism in Gr/AlGaN/GaN heterostructures with different Al mole fractions, demonstrating the dependence of the SBH on the AlGaN barrier layer composition.

Fisichella et al. [52,53] employed conductive atomic force microscopy (CAFM) for the nanoscale electrical characterization of Gr contacts to AlGaN/GaN heterostructures, focusing on the role of the microstructure of the AlGaN barrier layer on the formation of rectifying or Ohmic contacts. Two $Al_{0.25}GaN_{0.75}$/GaN heterostructures with the same thickness (~24 nm thick) and different structural quality were compared: (i) a reference sample with a very low defect density in the AlGaN layer (LD sample) and (ii) a sample with a high density of characteristic defects (V-defects) [54,55] in the AlGaN layer (HD sample). Gr grown on copper by CVD was transferred to the AlGaN surface using a procedure consisting in the electrochemical delamination from the Cu foil, followed by the thermo-compression printing to the target surface [56].

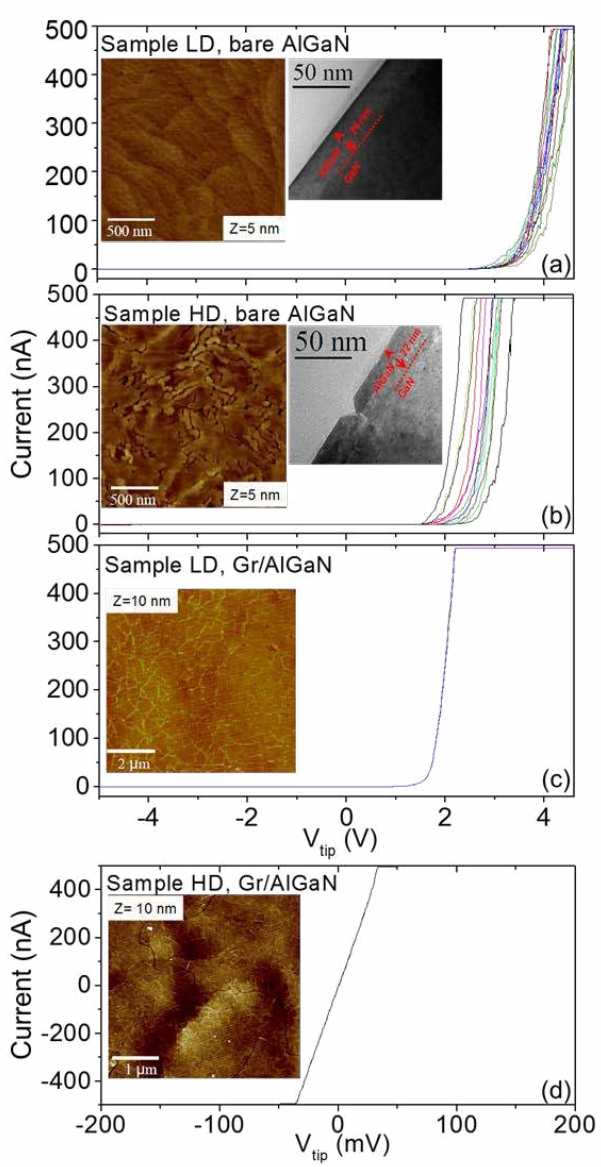

Figure 2 I-V curves on the reference AlGaN/GaN samples LD (a) and HD (b) and on the Gr-coated samples LD (c) and HD (d). Representative AFM and cross-sectional TEM images of the bare AlGaN surface of the LD and HD samples are reported in the inserts of (a) and (b). AFM images of the Gr-coated samples LD and HD are reported in the inserts of (c) and (d). Panels (a), (b), (c) and (d) have been modified and reprinted with permission from [52], copyright from AIP 2014.

Two representative atomic force microscopy (AFM) and cross-sectional transmission electron microscopy (TEM) images of the bare AlGaN surface of the LD and HD samples are reported in the inserts of Fig.2(a) and (b), respectively. The LD sample exhibits an atomically smooth surface with low roughness (RMS=0.85nm), corresponding to a uniform and defects-free AlGaN layer with ~24 nm thickness. Conversely, the presence of the V-shaped defects in the HD sample (see TEM image in Fig.2(b)) causes a local reduction of the AlGaN layer thickness, resulting in a higher roughness (RMS=1.21nm). Two typical AFM images of Gr transferred to the AlGaN surface of the LD and HD samples are reported in the inserts of Fig.2(c) and (d) respectively. In both cases, a very uniform Gr coverage with a low level of cracks can be observed. Local current-voltage (I-V) measurements by CAFM were carried out using an Au coated tip at several positions of the two samples. In Fig.2(a) and (b) are reported the I-V characteristics measured at the different positions on bare AlGaN in the two samples, respectively. For both samples all the I-V curves exhibit a rectifying behaviour and, for each tip position, the Au/AlGaN SBH was calculated using the thermionic emission model [49]. From the statistic on the SBH values measured at different positions, Φ_B=0.95±0.12 eV and Φ_B=0.63±0.17 eV have been evaluated for the LD and HD sample, respectively. The lower average value and the larger standard deviation in the case of the HD sample can be ascribed to the presence of the V-shaped depressions in the AlGaN barrier layer, acting as preferential current paths from the metal tip to the 2DEG. The I-V characteristics measured at different surface positions of the Gr-coated LD sample are reported in Fig.2(c). In this case, all the characteristics also exhibit a rectifying behaviour, but a very limited spread was found between curves measured at different positions. This indicates a superior lateral homogeneity of the Gr/AlGaN contact, that can be ascribed to some peculiar properties of a Gr membrane with respect to a common metal contact, such as the conformability to the substrate surface and the higher electron mean free path l (l~100 nm for Gr [57,58] against l=1-10 nm for common metals). Noteworthy, the SBH values in the presence of Gr onto AlGaN were significantly lower (Φ_B=0.41±0.04 eV) with respect to the values measured with the AFM tip onto bare AlGaN. Furthermore, this SBH value is much lower than the theoretical one (~1.8 eV) expected according to the Schottky-Mott theory. Starting from these experimental results, *Fisichella et al.* proposed a model of the Gr/AlGaN/GaN contact considering the role of AlGaN surface states [49]. These cause a pinning of the Gr Fermi level at the interface with AlGaN. Furthermore, charge transfer from these surface states is responsible of the high n-type doping (~10^{13}cm^{-2}) of Gr residing onto AlGaN [49]. The energy band diagram for the Gr/AlGaN/GaN heterostructure is illustrated in Fig.3.

Finally, the I-V characteristics measured at different surface positions of the Gr-coated HD sample are reported in Fig.2(d). Noteworthy, in this case all the curves reveal an Ohmic behaviour, which can be explained considering the combination of several effects. The local thinning of the AlGaN barrier layer at the V-defects positions, combined to the low values of the Gr/AlGaN SBH, give rise to many low resistance conduction paths between Gr and the AlGaN/GaN 2DEG. It can be supposed that the Gr electrode connects in parallel several of these vertical conductive paths, since the V-defects separation is similar or even

lower than the typical Gr electron mean free path (see AFM in the insert of Fig.2(b)). This would also explain the highly homogeneous Gr Ohmic contact even in the presence of a high density of V defects in the AlGaN.

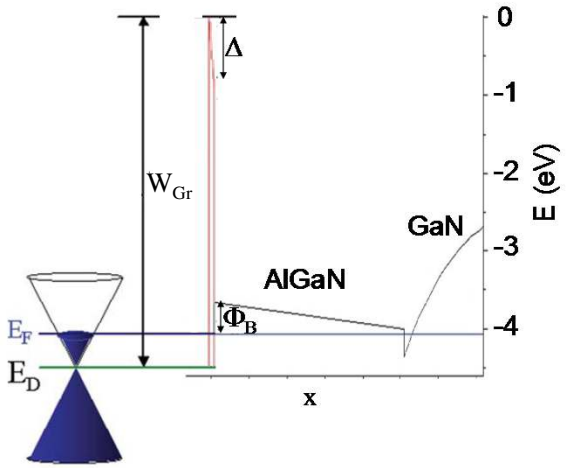

Figure 3 Energy band diagram for a Gr/AlGaN/GaN heterostructure.

3 Applications of Gr/III-N heterostructures in high power and high frequency electronics

3.1 Thermal management. A large number of methods have been used to improve heat removal from GaN devices. Conventional sapphire substrates with low thermal conductivity K=30Wm^{-1}K^{-1} at room temperature (RT) have been replaced with SiC substrates with a higher thermal conductivity K=100–350 Wm^{-1}K^{-1} at RT. However, even in GaN transistors on a SiC substrate, self-heating can lead to temperature rises ΔT above 180 °C. This is due to the high electric field induced at the gate edge while increasing the drain bias of the transistors. In this context, solutions for the local thermal management of high-power density devices, specifically targeting the hotspots at nanometre and micrometre scale are highly desirable.

Yan et al. [29] showed that the local thermal management of AlGaN/GaN transistors can be substantially improved via introduction of additional heat-escaping channels, represented by top-surface heat spreaders made of few layer Gr (FLG). FLG films present many advantages as heat spreaders with respect to ordinary metals films. In fact, heat conduction in FLG films is ruled by phonon transport and it is preserved even reducing film thickness down to a single layer of Gr. On the contrary, the thermal conductivity of metals is dominated by electron transport and it becomes significantly lower than the bulk value for thin films with thickness comparable to the electron mean free path [59]. Beside the thermal conductivity, another important parameter for heat spreaders is the *thermal boundary resistance* (TBR) at the interface with other materials. Noteworthy, the TBR at the interface between Gr or graphite and various substrates is relatively small, in the order of ~10^{-8} Km^{2}W^{-1} at RT, and does not strongly depend on the interfacing material [60,61,62].

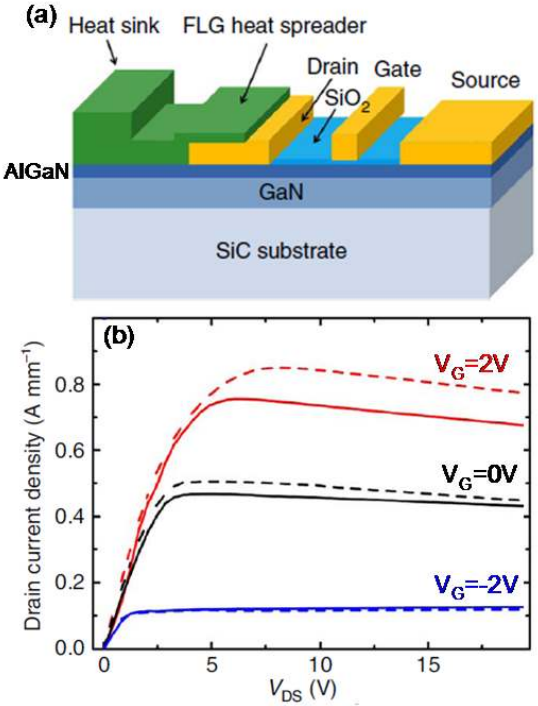

Figure 4 (a) Scheme of an AlGaN/GaN heterostructure transistor with FLG flakes transferred on top of it as surface heat spreaders. (b) Comparison of the I-V characteristics of the transistor without (solid lines) and with (dashed lines) Gr heat spreaders. Panels (a) and (b) have been modified and reprinted with permission from [29], copyright from Nature Publishing Group 2012.

In the proof-of-concept experiment performed by Balandin's group, FLG films were exfoliated from highly-oriented pyrolytic graphite (HOPG) and transferred in contact with the drain of AlGaN/GaN devices on a semi-insulating 4H–SiC substrate. Fig.4(a) illustrates the structure of a tested $Al_{0.2}Ga_{0.8}N$ (30nn)/GaN (0.5 μm) transistor with FLG flakes transferred on top of it as heat spreaders. Fig.4(b) shows a direct comparison between the output characteristics (I_D-V_D) of the device without (solid lines) and with FLG heat spreaders (dashed lines). A significant increase in the output current I_D (12% at V_G=2 V and 8% at V_G=0 V) can be observed as a result of better heat removal with the local FLG heat spreaders.

The temperature rise ΔT due to self-heating in the channel region of operating (i.e. biased) AlGaN/GaN transistors was also monitored in situ by micro-Raman spectroscopy. The laser probe was focused between the gate and the drain (closer to the gate), where ΔT is expected to be the highest, and ΔT was evaluated from the shift of the posi-

tion of the characteristic Raman peak at 567 cm^{-1} associated to the E_2 mode of GaN [63]. As an example, at a power density of 12.8 W/mm, ΔT for the AlGaN/GaN transistor with and without Gr heat spreaders was 92 and 118 °C, respectively. Those experiments presented a direct evidence of the improvement in the device performance with the top-surface FLG heat spreaders.

Although these proof-of-concept experiments were performed using FLG exfoliated from graphite, practical applications of Gr heat spreaders could be enabled by the progress of Gr CVD growth directly on GaN and Nitride semiconductors. Since the FLG quality for heat spreaders does not need to be as high as that for the electronic applications, probably this could represent the first application of CVD grown Gr on Nitrides. Furthermore, recent demonstration of direct low-temperature growth of synthetic diamond on GaN [64] can lead to the development of heterogeneous FLG-diamond lateral heat spreaders, where the diamond layers provide electrical insulation and additional heat spreading [65].

3.2 Hot electron transistors. The *Gr Base Hot Electron Transistor* (GBHET) is a new vertical device concept very promising for ultra-high frequency applications [66]. It is a three terminal device, consisting of a Gr base (B) terminal separated from the emitter (E) and collector (C) terminals by an emitter–base (EB) barrier and a base–collector (BC) barrier, respectively.

Fig.5(a) and (b) illustrate the schematic band diagrams of a GBHET in the off- and on-state biasing conditions, respectively. In the on-state, electrons are injected into the Gr base, either by Fowler–Nordheim (FN) tunnelling through the EB barrier or by thermionic emission (TE) over the EB barrier. When these electrons have energies well above the Fermi level of the Gr base and the collector barrier height (hot electrons), they can pass through the atomically thin Gr base and overcome the collector barrier, contributing to the collector on-current. In order to minimize the parasitic base current and maximize current gain, emitter–base emission of cold electrons, mainly due to defect mediated electron transfer mechanisms and direct tunnelling, should be prevented. In fact, those electrons with energies comparable to the Gr Fermi level can easily be backscattered from the base–collector barrier and contribute to the undesirable parasitic base current.

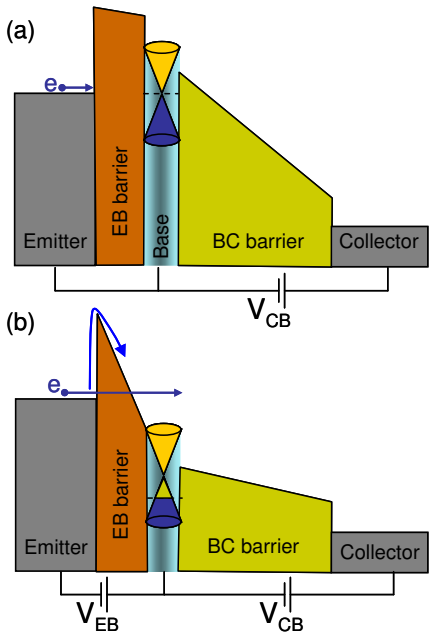

Figure 5 Schematic band diagrams of a GBHET in the off-state (a) and on-state (b) biasing conditions

The first GBHET demonstrators have been realized using a metal/high-k/Gr/SiO_2/Si stack, where Si, Gr and the metal work as the *E*, *B* and *C*, respectively, and the SiO_2 and the high-k dielectrics as the EB and BC barrier layers [45,46]. However, these first demonstrators suffered from a poor collector current density and current gain, mainly due to the inefficient current injection in Gr by tunnelling from the Si emitter through the SiO_2 EB barrier. In the last years several solutions have been considered to improve the device performances. As an example, alternative dielectrics with properly tailored electron affinity, such as a thulium silicate/titanium dioxide bilayer, have been proposed as E-B barrier layer on a Si n^+ emitter, whereas Si was considered as B-C barrier on top of Gr [67]. This combination of layers yields an improvement of the collector current density of more than a factor 10^5 with respect to the first prototypes [45]. The possibility of implementing GBHETs by Gr integration with semiconducting materials different than silicon has been recently considered. As an example, the use of Silicon Carbide or III-Nitrides is expected to be extremely beneficial to achieve GBHETs with extremely low power dissipation in the off-state and high on-state currents, thanks to the very low intrinsic carrier concentration and superior electron saturation velocity of these wide-bandgap semiconductors.

Recently, a GBHET system based on a metal/AlN/Gr/SiC stack has been demonstrated [68], where SiC works as the collector, epitaxial Gr grown on SiC(0001) works as the base and a thin AlN films grown on Gr works as emitter-base barrier layer [82]. As discussed in the *Section 4* of this paper, the direct growth of high quality single crystalline Nitride films on Gr requires the use of proper functionali-

zation treatments that minimally degrade the Gr quality. Vertical current transport across the Gr/SiC system crucially depends on the peculiar structural properties of the interface [69,70,[71]] and can be tailored by intercalation of proper atomic species (such as hydrogen) under Gr [72] and/or by molecular doping [73].

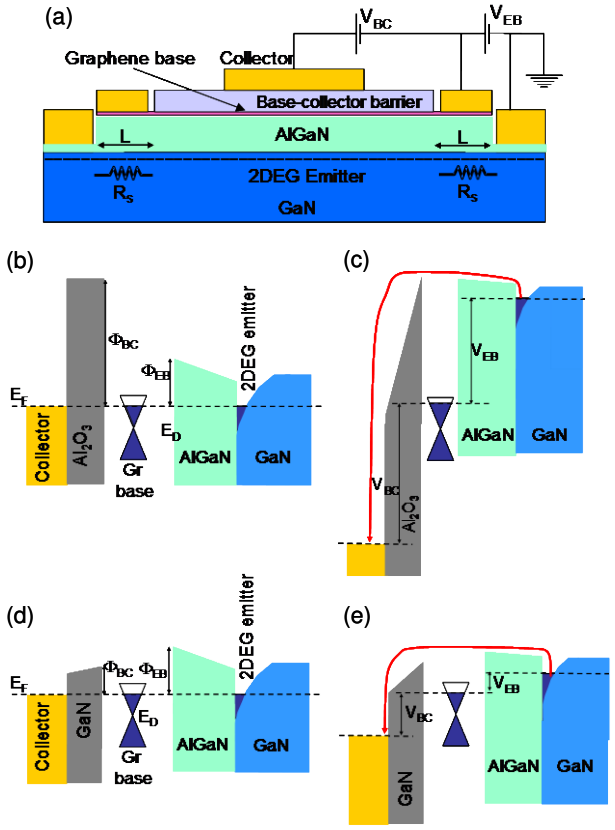

Figure 6 Schematic representation of the cross-section of a GBHET based on the AlGaN/GaN heterostructure (a). Energy band diagram of a device implementation using a thin Al_2O_3 film as base-collector barrier under equilibrium conditions (V_{EB}=0, V_{BC}=0) (b) and in the on-state. (c) Energy band diagram of a device implementation using a thin GaN film as base-collector barrier under equilibrium conditions (V_{EB}=0, V_{BC}=0) (d) and in the on-state (e).

A GBHET scheme based on a Gr/AlGaN/GaN heretostructure has been also recently proposed by different groups [74,75]. Fig.6(a) shows a cross-sectional schematic of such transistor, where the 2DEG at AlGaN/GaN interface works as the emitter contact, the AlGaN layer as the emitter-base barrier. Current injection into the Gr base is expected to be very efficient, due to the high carrier density of the emitter and to the current transport mechanism from the AlGaN/GaN 2DEG to Gr, i.e. thermionic emission over the barrier [49], as discussed in the *Section 2*. Furthermore, a low series resistance R_s is expected for the access region between the emitter contacts and the active region (see schematic in Fig.6(a)), thanks to the low sheet resistance of the 2DEG. A high-k dielectric film (Al_2O_3) [76] or even a thin GaN layer deposited on Gr have been considered as possible base-collector barrier layers in this device structure.

The energy band-diagrams under equilibrium conditions (V_{EB}=0, V_{BC}=0) for two AlGaN/GaN GBHETs with Al_2O_3 and GaN as base-collector barriers are depicted in Fig.6(b) and (d), respectively. The energies of the emitter-base barrier (Φ_{EB}) and base-collector barrier (Φ_{EB}) are in scale. In particular, Φ_{EB} is the value of the Gr/AlGaN Schottky barrier (~0.41 eV) from Ref. [49], while the Φ_{BC} values of the Gr/Al_2O_3 and Gr/GaN barrier are taken from Refs. [45] and [26], respectively. The energy band diagrams for the two devices in the on-state (V_{EB}>0, V_{BC}>0) are depicted in Figs.6(c) and (e), respectively. Clearly, the band alignment depicted in Fig. 6 suggests that a thin GaN layer deposited on Gr can represent the optimal choice as base-collector barrier layer, to minimize back-reflection of hot electrons at this barrier and, hence, to maximize the collector current.

Pioneering research activities aimed at the growth of high quality GaN thin films on Gr for these vertical transistors applications are in progress within different groups.

4 Growth of graphene/III-N heterostructures

This section will provide an overview on the state of the art about the growth of thin films of Nitride semiconductors on Gr by different techniques, such as metal-organic-chemical-vapour-deposition (MOCVD), molecular beam epitaxy (MBE), atomic layer epitaxy (ALE). Furthermore, the results of the first studies on the chemical vapour deposition (CVD) of Gr on Nitride thin films will be reviewed.

4.1 Growth of III-N films on graphene. In the first studies, Gr was considered simply as an intermediate layer to grow c-plane GaN on arbitrary substrates [77]. Due to its hexagonal six-fold symmetry, Gr should be effective for forming an epitaxial relationship with the c-plane of GaN. However, the lack of dangling bonds on the surface of pristine Gr makes the direct growth of III–Nitrides challenging, as there are no sites to promote bonding with foreign atoms [78]. As a result, various functionalization methods have been employed to modify the Gr surface in order to promote bond formation.

K. Chung et al. [77] first evaluated the growth of GaN on oxygen-plasma treated Gr, which resulted in a polycrystalline GaN layer with a rough and irregular surface. Subsequently, they explored the use of vertically aligned ZnO nanowalls as an intermediate layer on oxygen plasma treated Gr, obtaining GaN films with excellent optical characteristics at room temperature, such as stimulated emission. LEDs with strong photoluminescence emission were fabricated on these GaN layers and easy transfer to

foreign substrates, including flexible ones, was demonstrated [79].

More recently, Gr has been proposed as a compliant layer to improve the quality of GaN grown on Si (100) substrates [80], which would be desirable to realize monolithic integration between mature Si-based electronic devices on Si(100) and GaN-based optoelectronic devices. Owing to the different symmetries of hexagonal (0001) GaN and cubic (100) Si, the quality of GaN films grown on these substrates is typically poor. To obtain a better quality growth, (111) oriented Si wafers are commonly used as substrates for GaN heteroepitaxy. *Araki et al.* [80] used Gr grown by CVD on Cu and transferred onto Si(100) as a substrate for GaN growth by radio-frequency plasma-excited molecular beam epitaxy (RF-MBE). The comparison between thick (~400 nm) GaN films grown on Si(100) without and with the Gr interlayer showed in both cases a columnar structure, but with significantly larger grains in the presence of Gr/Si(100) substrate. Furthermore, X-ray diffraction measurements showed that the GaN columns grown on Gr/Si(100) have a c-axis-oriented hexagonal wurtzite structure. However, cross-sectional TEM analyses showed a high density of stacking faults and the presence of cubic (111) GaN inclusions within the columnar GaN grains, especially in the interface region with Gr.

In the above mentioned works, Gr was used just as an intermediate layer for GaN growth on arbitrary substrates, without specific attention to preserve Gr quality. As a matter of fact, chemical treatments (such as oxidation) on Gr, used to promote GaN growth, strongly affect the electrical/thermal properties of Gr. On the other hand, for novel applications where Gr and III-N properties must be jointly exploited, more refined strategies of Gr pre-functionalization and/or of III-N films growth are required in order to preserve Gr physical properties.

Motivated by the possibility of using a Gr interfacial layer between the SiC substrate and GaN to alleviate self-heating problems in GaN-based high power electronic devices, *Kovacs et al.* [81] recently demonstrated the MOCVD growth of GaN layers on patterned epitaxial Gr on 6H–SiC (0001), without need of any pre-functionalization. Few layers of Gr (FLG) were grown on a SiC wafer by high-temperature sublimation [8].

The continuous Gr film was patterned by e-beam lithography and Ar/O_2 plasma etching, with the aim to obtain a periodic pattern of alternating uncovered and Gr covered SiC areas, as schematically illustrated in Fig.7(a). In the reality, it was found that small Gr islands remained in the regions subjected to Ar/O_2 plasma etching. Then, a 100 nm thick AlN buffer layer was deposited onto the patterned Gr/6H-SiC surface, followed by the deposition of 300 nm thick $Al_{0.2}Ga_{0.8}N$ and 1.5 µm thick GaN layers. Fig.7(b) shows a low-magnification bright-field TEM image of the heterostructure. Vertical arrows mark the regions where the Gr layers were partially etched away in 1 µm wide stripes. The GaN layer contains semicircular polycrystalline regions above the intact Gr layers. The vertical dark lines are inversion domains, which travel straight to the surface from regions where the AlN/GaN grows directly on the SiC. The dislocation density in this sample was determined to be $\approx 3\times10^9$ cm^{-2}. A reference sample without Gr layers was grown using identical parameters and had a dislocation density of 2×10^9 cm^{-2}.

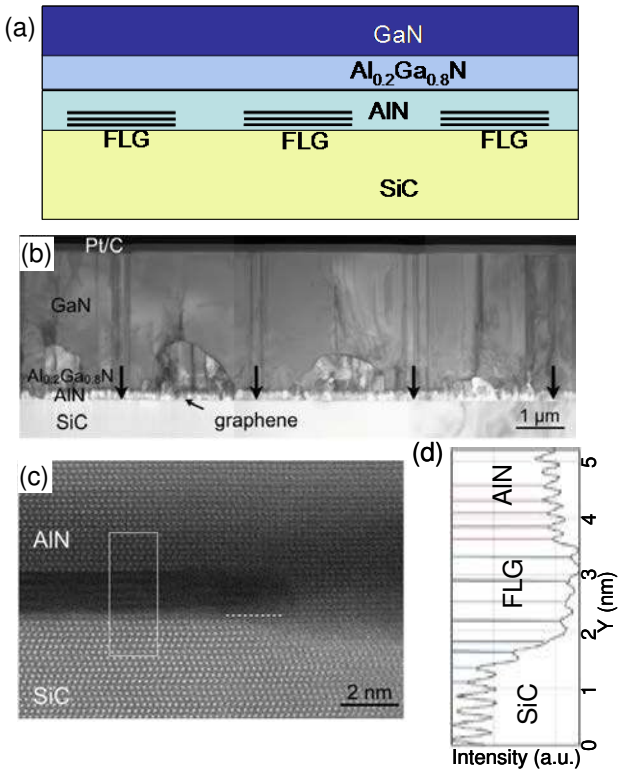

Figure 7 (a) Scheme of the deposited layer sequence to grow GaN on patterned epitaxial Gr on SiC. (b) Low-magnification bright-field TEM image of the heterostructure. Vertical arrows mark the regions where the Gr layers were partially etched away. (c) HAADF STEM image of the heterostructure in a partially etched Gr/SiC interface. Dashed line marks the uppermost SiC layer. (d) Integrated intensity scan across the interface with peak-to-peak distances recorded from the region marked by rectangle in (c). Panels (b), (c) and (d) have been modified and reprinted with permission from [81], copyright from Wiley 2015.

Fig.7(c) shows a high-resolution HAADF-STEM image of AlN grown on a FLG island that remained on the etched surface of the SiC. Bright spots correspond to atomic columns of Si and Al in the 6H-SiC and AlN layers, respectively. Fig.7(d) shows integrated intensity lines scan obtained across the SiC, Gr and AlN, with the well-defined peaks corresponding to Si, C, and Al layers. On the right side of the image in Fig.7(c), the Gr layers have been etched away completely and the white-dashed line indicates the uppermost SiC layer. The image suggests that the

AlN nucleated epitaxially and started to grow on the 6H-SiC and then overgrew the Gr layers laterally.

Nepal et al. [82] recently demonstrated that high quality thin (~10 nm) AlN layers can be grown on epitaxial Gr on SiC by atomic layer epitaxy (ALE) at low temperatures (280 °C) after a fluorine functionalization using xenon difluoride (XeF_2) gas at room temperature. Such a fluorination method was used in the past also to functionalize the epitaxial Gr surface for dielectric deposition, with little or no degradation of the Gr lattice [83]. The chemisorption of a fluorine atom forms a semi-ionic C–F bond rather than a covalent bond to the Gr surface. This allows the structural and electrical integrity of the Gr to be preserved, while providing sufficient nucleation sites for subsequent high-quality layer deposition. Low temperature ALE was employed to grow the thin AlN layer instead of conventional molecular beam epitaxy (MBE) or metal organic chemical vapor deposition (MOCVD) conditions at higher temperatures (500–1300 °C), in order to avoid the complete desorption of the fluorine adatoms from Gr. The inherent kinetics of ALE allows the growth of crystalline materials at greatly reduced temperatures relative to standard epitaxial techniques such as MOCVD. Currently, the exact mechanism of AlN nucleation is unclear. Probably the reaction of TMA molecules with surface fluorine semi-ionically bonded to Gr results in the substitution of Al for F and the creation of a reaction site for subsequent AlN growth.

The ultrathin AlN layer on epitaxial Gr on SiC has been recently used as the emitter-base barrier layer of a metal/AlN/Gr/SiC hot electron transistor, as discussed in the *Section 3* of this paper. The AlN layer was also used as a buffer layer for the subsequent growth of a thick (800 nm) unintentionally doped GaN layer by standard MOCVD. The authors showed that the resulting quality of the GaN layer is similar to that obtained by traditional growth methods on III–N substrates [82].

In all the above discussed growth approaches, a modification of Gr structure (pre-patterning, functionalization,..) was required before III-N films deposition. Recently, *Kim et al.* [84] explored the possibility of performing the direct van der Waals epitaxy (vdWE) of high-quality single-crystalline GaN films on Gr. Epitaxial Gr grown on SiC (0001) was used as a template because it retains a unique orientation over the entire substrate.

Fig.8(a) shows the AFM surface morphology of as-grown epitaxial Gr on SiC. It exhibits parallel and nearly equally spaced steps originating from the SiC step bunching phenomenon occurring during high temperature graphitization. Step edges were demonstrated to play a key role to obtain a uniform and single crystalline GaN layer on Gr using MOCVD with careful control of the growth kinetics. Such a result was obtained under proper growth conditions which allowed preferential GaN nucleation along the periodic step edges and then lateral (2D) growth and coalescence of GaN nuclei.

This was demonstrated comparing different deposition conditions: (i) a two-step deposition, with nucleation at low temperature of 580 °C and growth at 1150 °C; (ii) a one-step deposition at 1100 °C; and (iii) a two-step deposition, with nucleation at high temperature 1100 °C and growth at 1250 °C. Fig.8(b)–(d) show three plan-view SEM images of GaN films grown on Gr under those different conditions. The two-steps deposition with low temperature nucleation resulted in the formation of 3D faceted GaN clusters (Fig.8(b)), which was attributed to the limited atomic mobility at 580 °C resulting in a low density of nuclei randomly formed on Gr on SiC terraces. The one-step deposition at 1100 °C resulted in the formation of continuous GaN stripes aligned along the SiC vicinal steps (Fig.8(c)), which was explained in terms of the increased mobility of adatoms, allowing nucleation at the energetically favourable step edges. Finally, the two-step deposition, with high temperature nucleation at 1100 °C and growth at 1250 °C, resulted in the formation of continuous and smooth GaN films (Fig.8(d)). This was attributed to the faster lateral growth at an increased growth temperature of 1250 °C from the GaN nuclei along the periodic terrace edges formed at 1100 °C. The final thickness of the GaN film grown under these optimal conditions was ~2.5 μm. A high resolution AFM morphology of the GaN grown under these optimal conditions is reported in Fig.8(e) to illustrate the low roughness (RMS ~0.3 nm) of GaN surface. The threading dislocation density for this film was $\sim 4\times10^8$ cm^{-2}. These results indicated that, even without using any buffer layer, GaN crystalline quality comparable with that typically obtained via conventional AlN-buffer-assisted GaN epitaxy on SiC or sapphire substrates can be obtained on Gr.

III-N thin films commonly present the wurtzite crystal structure with tetrahedral sp^3 coordination of the atoms. However, theoretical studies and some preliminary experimental investigations indicated that ultra-thin films of AlN or GaN can be thermodynamically stable also in the hexagonal graphitic-like structure with planar sp^2 coordination of the atoms, for film thickness ranging from a monolayer up to 10 layers. To date, the experimental evidence of graphitic AlN films have been obtained by plasma assisted MBE on a catalytic Ag(111) substrate [85]. Recently reported ab-initio calculations evaluated the stability and electronic properties of Van der Waals stacks of few-layer graphitic AlN with Gr [86]. Furthermore, an experimental activity is in progress for the realization of heterostructures of graphitic AlN with epitaxial Gr on SiC(0001). at ultrathin GaN films with a 2D buckled structure can be obtained at the interface between SiC (0001) and epitaxial Gr by a process consisting in the intercalation of Ga and N atoms [87].

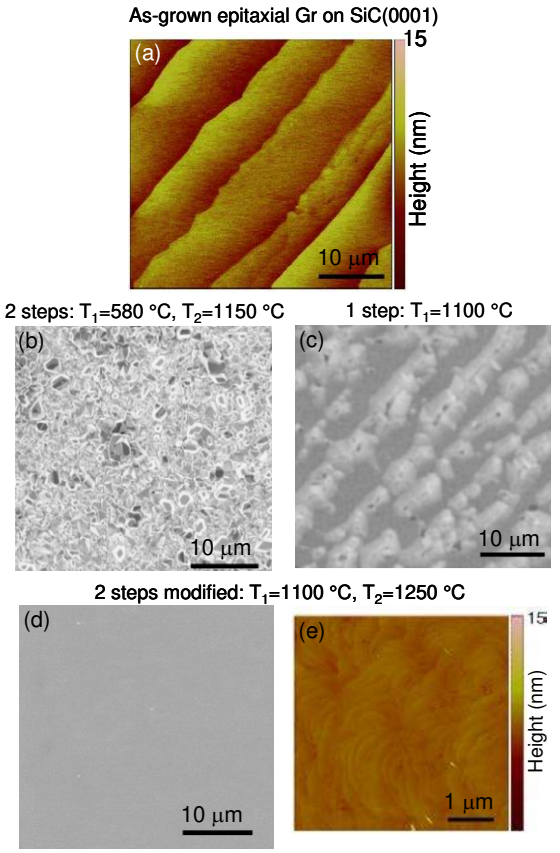

Figure 8 (a) AFM surface morphology of as-grown epitaxial Gr on SiC(0001). Plan-view SEM images of GaN films grown on Gr under different conditions: (b) 2-steps deposition with nucleation at low temperature 580 °C and growth at 1150 °C, (c) 1-step deposition at 1100 °C, and (d) modified 2-steps deposition with nucleation at high temperature 1100 °C and growth at 1250 °C. (e) High resolution AFM morphology of GaN grown under the optimal conditions as in panel (d). Panels (a), (b), (c), (d) and (e) have been modified and reprinted with permission from [84], copyright from Nature Publishing Group 2014.

4.2 Growth of graphene on III-N. The growth of Gr using CVD on non-metallic surfaces has been demonstrated simultaneously on SiC [13,14] and oxide substrates such as Al_2O_3 [13] and MgO [88], hence opening a potential way for graphene growth on Nitrides. Recently, *Michon et al.* [89] demonstrated the possibility of growing Gr on AlN films on a Si(111) substrate. The AlN films (200 nm thick, with a dislocation density $>2\times10^{11}/cm^2$ and an average crystal grain size of ~30 nm) were grown on Si(111) by MBE using ammonia as the nitrogen source. Gr was grown on AlN using CVD with propane as the carbon source, and a 50% hydrogen/50% nitrogen mixture as the carrier gas. This optimal carrier gas mixture was found to reduce the hydrogen etching effect on the AlN template during Gr growth. Different Gr growth temperatures of 1150, 1250, and 1350 °C (i.e., below the melting point of Si) were evaluated. Furthermore, both on-axis and 2° off-axis Si(111) substrates were considered for these experiments, but the off-axis template appeared slightly more favourable for Gr growth on AlN.

Fig.9(a) and (b) shows AFM images of the Gr grown on AlN at 1250 and 1350 °C, respectively. The most evident difference from the comparison of these morphological images is the presence of pits on the sample grown at 1350 °C, probably associated to etching mechanisms which are known to develop strongly with the temperature. Raman spectra of the Gr samples grown at these temperatures are reported in Fig.9(e). For all the growth temperatures, the Raman spectra present the characteristic peaks of a graphitic phase (D, G, and 2D located near 1350, 1590, and 2690 cm^{-1} respectively), indicating that growth occurred at both temperatures. The presence of the D, D', and D+D' peaks revealed the presence of defects, especially for the lower growth temperature. The average few layer Gr thickness, deduced both from the normalised integrated intensity of the G band and from reflectivity measurements, was evaluated between 1 and 3 layers for 1250 °C growth temperature and about 10 layers for the sample grown at 1350 °C. The 2D bands appear as single Lorentzian, indicating a decoupling of stacked Gr layers. This rotational disorder between the layers, also evidenced by low energy electron diffraction (LEED) patterns (Fig. 9(c) and (d)), is consistent with the observation of small wrinkles on high magnification of AFM image. A compressive strain of the layers was also deduced from the shift of both G and 2D peaks positions with respect to the case of unstrained Gr. The Gr domains size, as estimated from the D/G intensity ratio, was ~5–6 nm for samples grown at 1250 °C. For the sample grown at 1350 °C the Gr domain size increased to ~30 nm, a value comparable to the average grain size of the AlN template. This latter observation suggests that the structural quality of CVD grown Gr on AlN/Si(111) at high temperature can be limited by the structural quality of the AlN film. This finally indicates that high-quality Gr could be obtained on bulk AlN substrates, thanks to a lower density of defects and to the possibility of further increasing deposition temperatures above the silicon melting point.

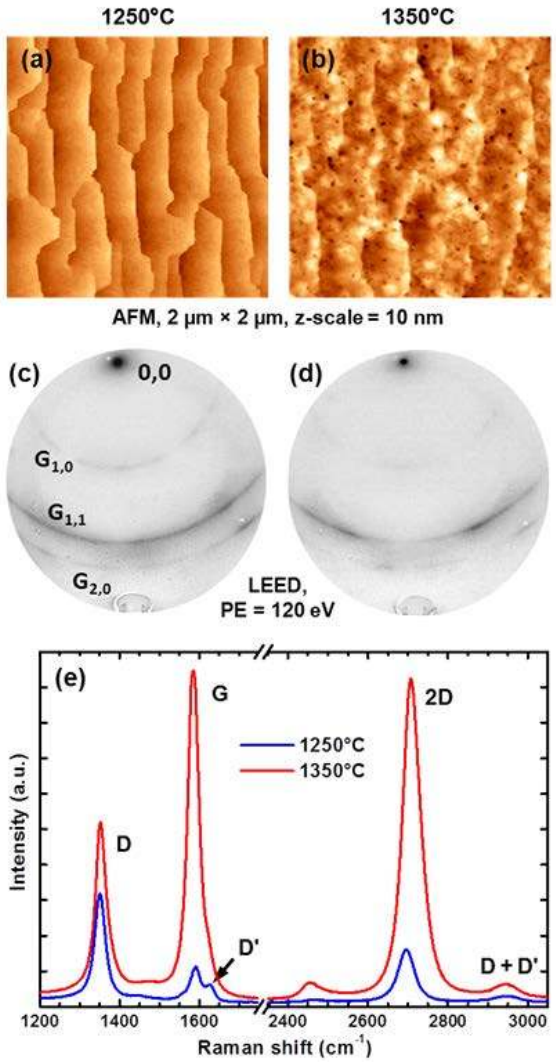

Figure 9 Characterizations of Gr films grown by CVD at 1250°C and 1350°C on AlN/Si(111) templates. (a) and (b): AFM morphology for Gr growth temperature of 1250 and 1350°C, respectively; (c) and (d): corresponding LEED pattern; (e) Raman spectra. Panels (a), (b), (c) (d) and (e) have been modified and reprinted with permission from [89], copyright from AIP 2014.

More Recently, *Dagher et al.* [90] have studied Gr growth on polar faces of bulk AlN using CVD. In contrast with AlN templates, where etching effects have to be reduced, hydrogen etching of bulk AlN substrate during annealing at 1400°C allows to improve AlN surface, which can finally present atomic terraces without defects. The growth of Gr on the N-face of annealed AlN substrate is clearly established by the observation of large wrinkles by AFM together with a sp^2 peak on XPS spectra (Fig.10 (a) and (b)). Gr growth is also evidenced on the Al-face from XPS spectra, but no wrinkles are observed by AFM. *Dagher et al.* have also studied Gr growth using CVD on AlN templates grown by MBE on SiC and on sapphire. The lower density of defects and the good morphology of AlN templates on SiC even after annealing at temperature up to 1450°C make them ideal templates for Gr growth. Gr growth on AlN template on SiC is reported at temperature of 1450°C on the basis of AFM and XPS observations (Fig.10(c) and (d)), but further works are required to characterize Gr on AlN templates on SiC.

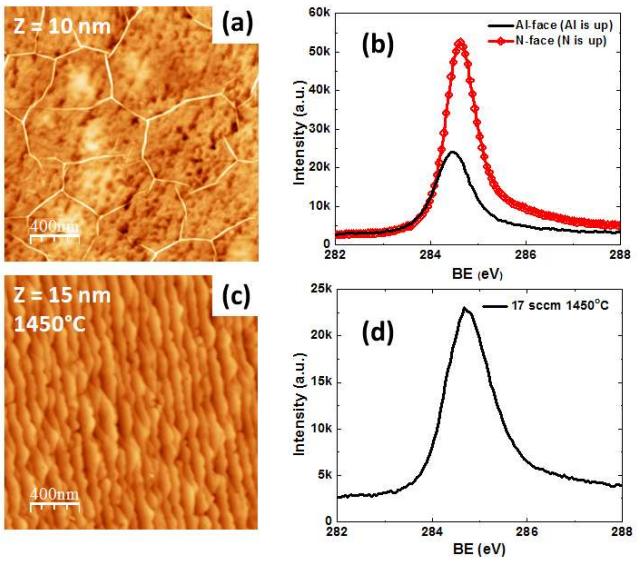

Figure 10 (a) and (b): AFM morphology and XPS spectra of Gr films grown at 1350°C by CVD on the N-face of bulk AlN substrate. (c) and (d): AFM morphology and XPS spectra of Gr films grown at 1450°C by CVD on AlN/SiC template.

From these studies, bulk AlN appears as the more favourable surface for high-quality Gr growth. However, beyond the problem of the limited sizes of bulk AlN substrates, Gr growth on AlN templates may offer more possibilities of integration with current nitride devices. From this point of view, Gr growth on AlN on SiC template could be an ideal trade-off in terms of substrate size and quality of Gr and Nitride.

5 Summary To conclude, recent literature results on the integration of Gr with Nitride semiconductors for high power and high frequency electronics have been reviewed. Investigations on the electronic transport properties through Gr/GaN and Gr/AlGaN/GaN interfaces have been presented. Strategies to use Gr for thermal management in high-power AlGaN/GaN transistors have been discussed. Furthermore, we highlighted recent proposals for the implementation of new ultra-high-frequency (THz) transistors, such as the *Gr Base Hot Electron Transistor* (GBHET), by Gr integration with III-N. Finally, recent progresses in the growth of high quality GaN layers on Gr templates and in the deposition of Gr on III-N substrates and templates have been presented.

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