SCIENTIFIC REPORTS

OPEN

SUBJECT AREAS:
SENSORS AND BIOSENSORS
NANOSENSORS
ELECTRONIC PROPERTIES AND DEVICES

Received
2 May 2014

Accepted
6 June 2014

Published
7 July 2014

Correspondence and requests for materials should be addressed to Z.Y.Z. (zyzhang@pku.edu.cn) or L.-M.P. (lmpeng@pku.edu.cn)

Graphene/Si CMOS Hybrid Hall Integrated Circuits

Le Huang[1], Huilong Xu[1], Zhiyong Zhang[1], Chengying Chen[2], Jianhua Jiang[2], Xiaomeng Ma[1], Bingyan Chen[1], Zishen Li[1], Hua Zhong[1] & Lian-Mao Peng[1]

[1]Key Laboratory for the Physics and Chemistry of Nanodevices and Department of Electronics, Peking University, Beijing 100871, China, [2]ASIC and System Department, Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, China.

Graphene/silicon CMOS hybrid integrated circuits (ICs) should provide powerful functions which combines the ultra-high carrier mobility of graphene and the sophisticated functions of silicon CMOS ICs. But it is difficult to integrate these two kinds of heterogeneous devices on a single chip. In this work a low temperature process is developed for integrating graphene devices onto silicon CMOS ICs for the first time, and a high performance graphene/CMOS hybrid Hall IC is demonstrated. Signal amplifying/process ICs are manufactured via commercial 0.18 um silicon CMOS technology, and graphene Hall elements (GHEs) are fabricated on top of the passivation layer of the CMOS chip via a low-temperature micro-fabrication process. The sensitivity of the GHE on CMOS chip is further improved by integrating the GHE with the CMOS amplifier on the Si chip. This work not only paves the way to fabricate graphene/Si CMOS Hall ICs with much higher performance than that of conventional Hall ICs, but also provides a general method for scalable integration of graphene devices with silicon CMOS ICs via a low-temperature process.

Graphene is a two-dimensional material with sp^2 structure that has been considered as an outstanding functional material for constructing high-performance nanodevices such as radio frequency (RF) transistors[1–3], photo-detectors[4], flexible electronics[5], gas sensors[6] and magnetic field detectors[7,8]. Although graphene has many excellent physical properties such as extremely high intrinsic carrier mobility, ultrathin body, long mean-free-path, great thermoelectric property and stability[9–14], this material also suffers from some major drawbacks. One of the vital intrinsic shortcomings of graphene is that the material has a zero band gap. This problem leads to small current on/off ratio and no stable saturation region in output characteristics of graphene transistors, limiting the applications of graphene in some mainstream fields such as digital electronics and amplifiers[1,14]. Instead of modifying the intrinsic drawbacks of graphene intentionally, graphene has also been used in such fields as sensors[4–8] and ambipolar electronics[15,16] which can take full advantages of its excellent properties while avoiding intrinsic drawbacks. Therefore an advisable and feasible route for graphene devices is to integrate them complementarily with the mainstreaming silicon CMOS circuits to construct more powerful hybrid integrated circuits (ICs) or systems, in which both graphene devices and Si CMOS circuits can do what they are good at. To realize such a hybrid ICs, one has to overcome the challenge as to how to integrate these two kinds of heterogeneous devices on the same chip, and this work aims to develop exactly this technique, i.e. a graphene device fabrication process that is compatible with Si CMOS technology to spread the applications of graphene devices and to extend the functions of Si CMOS ICs.

Previously graphene has been demonstrated as an ideal material for constructing graphene Hall element (GHE)[7,8,17], which takes full advantage of graphene's excellent properties such as high carrier mobility, ultrathin body, low noise and great stability, while avoids the main shortcoming, *i.e.* zero band gap. In particular, GHE has exhibited great advantages over commercial Silicon and even III-V compounds Hall sensors in many key figures of merits, e.g. sensitivity, linearity, resolution and temperature stability[7,8,17]. Moreover, a scalable fabrication process has been developed which might promise commercial applications of GHE in the future[18].

In most applications, the output Hall voltage from a Hall element is very small, and Hall ICs composed of Hall elements and cascaded signal amplifying/processing circuits are widely used in advanced applications. Until now, silicon based Hall ICs remain the mainstream since silicon CMOS technology is the most mature and advanced technology for realizing advanced signal amplifying/processing circuits[19]. Although individual Hall sensors made from III-V compounds may outperform silicon based Hall element, these high performance Hall sensors are hardly used in Hall ICs since it is hard to fabricate signal amplifying/processing ICs using III-V semiconductors[20,21]. Ideally we would want to combine the best Hall elements with the most advanced ICs, but it is

difficult to integrate the III-V based high-performing Hall sensors with advanced Silicon CMOS ICs on the same chip due to the complicated and demanding heterogeneous fabrication processes[22–24]. The situation becomes very different when graphene is considered. Several works have been demonstrated to utilize graphene as interconnects and integrate them with Si CMOS IC[25–27]. Although it remains challenging to fabricate digital ICs or amplifier using graphene, GHEs may in principle be fabricated on silicon CMOS ICs as well. This is because only low temperature processes are involved in graphene transfer and sensor fabrications. The excellent combination between GHE and Si CMOS ICs should further improve the performance of Hall ICs.

In this work, we develop a low-temperature process for fabricating graphene devices which is compatible with Si-based CMOS technology, and demonstrate the integration of GHEs with Si CMOS ICs on the same chip. Signal amplifying/processing ICs are manufactured via commercial 0.18 μm silicon CMOS technology, and GHEs are fabricated on top of the passivation layer of the Si CMOS chip via a low-temperature micro-fabrication process. The hybrid ICs work well, exhibiting full function of the Hall ICs at a low supply voltage of 3.3 V, i.e. the GHE can convert a magnetic signal to electrical signal which can then be processed/amplified by the Si CMOS ICs. In addition, this work also provides a general method for scalable integration of graphene devices and silicon CMOS ICs.

The graphene/silicon CMOS hybrid IC to be demonstrated here is a widely-used linear Hall IC, and its function diagram is depicted in Figure 1a. This IC contains five components, *i.e.* a buffer, a voltage amplifier, a bandgap, a voltage regulator and a Hall element. The Hall element used here is fabricated using graphene as the channel material[7,8,17]. The other four blocks are amplifying and assistant IC modules, and are realized via matured 0.18 μm silicon CMOS technology. The output signal from the GHE is first transmitted to the CMOS buffer module with storage and modulation functions, and is then inputted to the amplifier module. This module is designed to amplify the input AC signal with two optional amplifications (35 and 50 at 1 kHz) via setting the level of the pin named S0 (#7) and S1 (#8) respectively (Figure 1a). The bandgap module works as a power reference, which supplies a constant current (DC 10 μA) to power the buffer, amplifier and voltage regulator; and a constant voltage (DC 1.25 V) for the voltage regulator. The regulator, controlled by the pin named EN (#15), outputs a constant voltage (DC 3 V), which is an alternative power supply for the GHE. The pin named V_{CM} (#5), biased with DC 1.65 V, offers a common mode reference voltage for the buffer and amplifier. The Si CMOS IC contains totally 98 transistors, and is designed to run at a direct current (DC) voltage of 3.3 V (the standard supply voltage for 0.18 um ICs). In contrast to conventional linear Hall ICs, the GHE in the hybrid Hall ICs works in voltage mode[8], and the complex module for supplying constant current for energizing Hall element in current mode may thus be saved. This simplification profits from the highly linear response of the GHE in voltage mode, which is another important advantage of the GHE when compared with other conventional Hall elements.

Silicon based CMOS ICs were first fabricated via commercial 0.18 μm Si CMOS technology. Figure 1b shows a typical optical image of an as-fabricated chip with an overall size of 5 mm × 5 mm and an active area of 820 μm × 1030 μm. Totally 18 pins enclosed by solid green line in Figure 1b are arranged around the chip as interconnecting ports. The area for fabricating the GHE is enclosed by the dashed blue square. This region is on top of the Si_3N_4 passivation layer above the silicon devices, and hybrid graphene/Si CMOS IC is thus a three-dimensional IC[28].

The GHE was fabricated on top of the Si_3N_4 passivation layer of the finished Si CMOS chip via a scalable micro processing technology, and detailed fabrication process flow is shown in Figure 2a. The structure of the completed graphene/silicon hybrid Hall IC is depicted in Figure 2b. Since the GHE is fabricated on the passivation layer above the Si CMOS circuits, no additional chip area is needed. The construction method demonstrated here is in fact a transistor stacking three-dimensional integrating method[28], which is a big challenge in conventional semiconducting technology since the temperatures required for building another layer of high-performing semiconductor devices would destroy any metallic interconnection wire and cause migration of transistor dopants on previous layers. However, this problem is avoided in the construction of our

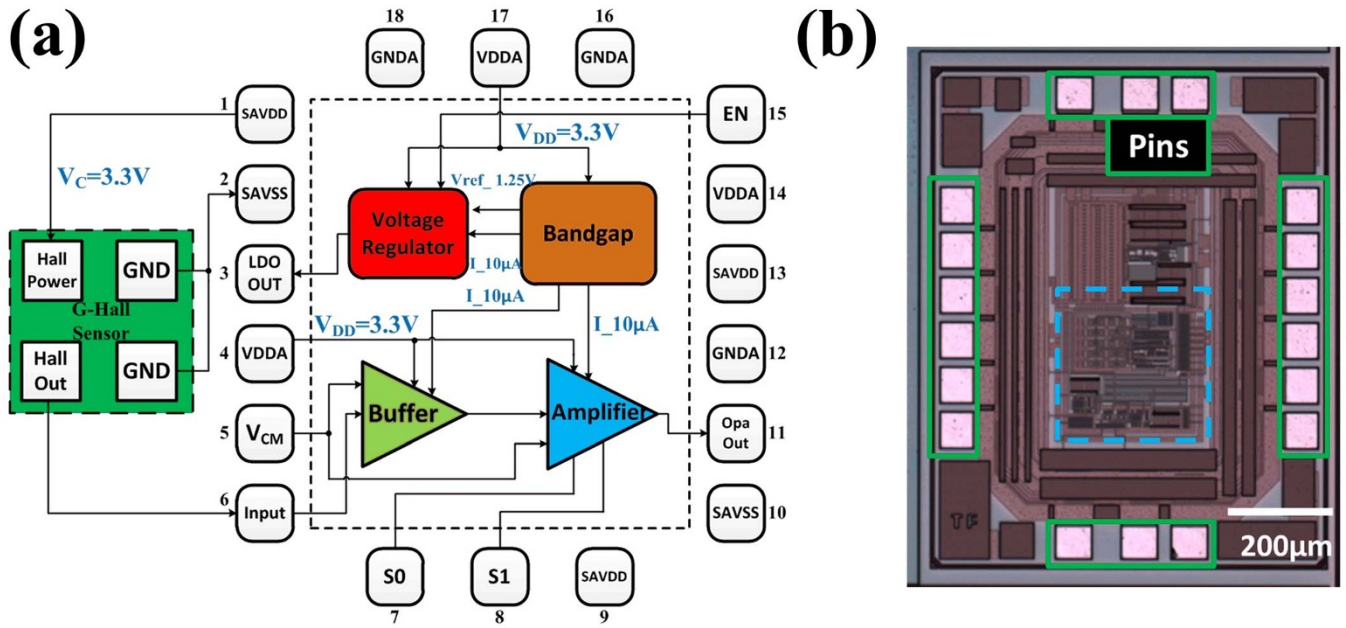

Figure 1 | Silicon based CMOS chip before the integration of GHE. (a) Circuit diagram of the graphene-silicon hybrid chip. The pins named SAVDD (#1) and VDDA (#17) denote In/Out (IO) power supply and analogue power supply respectively, which are identical in this work (DC 3.3 V). The pins named SAVSS (#2) and GNDA (#16) denote IO ground and analogue ground respectively, which are also identical. (b) Typical optical image showing the unprocessed CMOS chip. Totally 18 pins of the chip are marked by the solid green frame. The dashed blue square denotes the area where the GHE is to be fabricated.

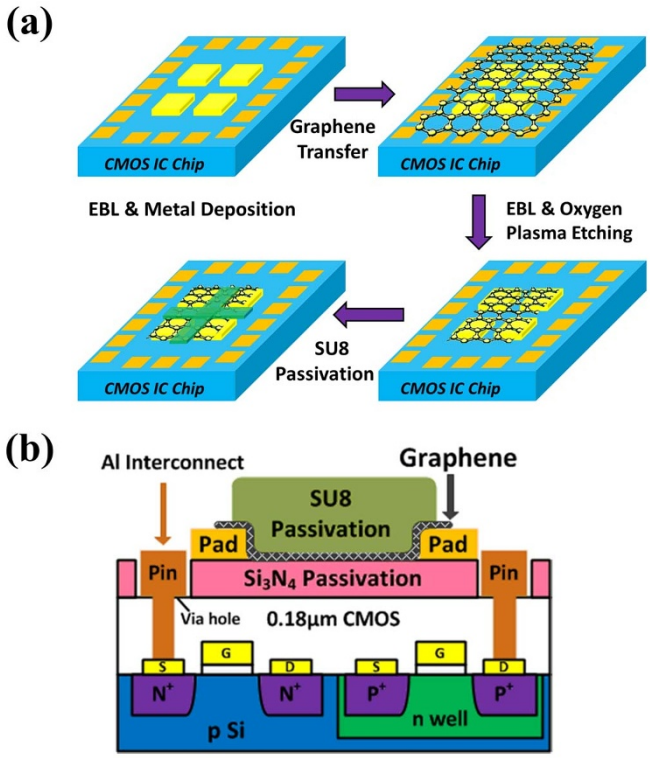

Figure 2 | Fabrication process flow and structure of the graphene-Silicon hybrid Hall chip. (a) Process flow showing the fabrication of a GHE on the Si CMOS chip. All processes are carried out via micro fabrication technology based on EBL. (b) Depicted side-view of the completed graphene-Silicon hybrid chip. The chip is fabricated by using 0.18 μm technology based on conventional Silicon CMOS structure. The GHE is fabricated on the passivation layer of the Si chip.

graphene/Si hybrid ICs, since no high-temperature process is required, *i.e.* both material transfer and fabrication of graphene devices on top of the Si chip are carried out at temperature no more than 180°C.

Before being connected to the Si CMOS ICs, the GHE fabricated on Si_3N_4 passivation layer of the Si chip was characterized and results are shown in Figure 3. It should be noted that graphene is not visible under optical microscope since the beneath Si_3N_4 layer is not designed with the right thickness to contrast graphene visible[29]. Instead scanning-electron-microscope (SEM) is used to observe graphene and device structures here. SEM image of a typical GHE after oxygen plasma etching process (but before being passivated by SU8) is shown in Figure 3a, in which we can readily distinguish the active graphene channel from the etched graphene area by the contrast of the image. The square shaped graphene channel remains uniform and complete on top of the Si_3N_4 passivation layer, suggesting that our modified transfer process of graphene works well. The graphene on Si CMOS chip is further characterized via Raman spectroscopy, and a typical Raman spectrum is shown in Figure 3b. The 2D/G peak ratio of about 3 indicates that the graphene is monolayer as well as high-quality, suggesting that our fabricating process is almost harmless to graphene. It should be noted that the Raman spectrum shown in Figure 3b was obtained by subtracting the substrate (Si_3N_4) signal from the total signal (Figure S1, Supplementary information), since the graphene is located on the surface of Si_3N_4 passivation layer of the chip. The final GHE after passivation is shown in Figure 3c, where the graphene layer is hardly visible because of the limited contrast between the substrate chip and graphene.

The magnetic response of the GHE was measured via a Hall probe station. When a magnetic field is applied normal to the channel of the GHE which is biased with a constant voltage or current over the electrodes V_{C1} and V_{C2}, a Hall voltage is generated over the other two opposite electrodes V_{H1} and V_{H2}. The magnetic field dependent Hall voltages are measured in constant voltage (V_C=3.3 V, which is consistent with the operating voltage of the CMOS ICs) mode, and results are shown in Figure 3d. It is obvious that Hall voltage increases linearly with increasing magnetic field, and the linearity error is smaller than 2% over a large magnetic field range from −0.4 T to 0.4 T, showing excellent linearity of the GHE. As a comparison, the typical linearity error is about 10% for high-performance two-dimensional electron gas (2DEG) Hall elements at magnetic field of less than 0.1 T[23]. The excellent linearity of the GHE over a wide magnetic field range in voltage mode enables us to use it in voltage mode. As a result, the complex constant current source widely used in conventional Hall ICs can be saved and the hybrid graphene/Si Hall ICs can be significantly simplified.

The slope of the V_H-B curve in Figure 3d reflects the absolute sensitivity S_A of the GHE, *i.e.* about 0.335 V T^{-1}. The voltage related sensitivity S_V is then retrieved to be 0.10 T^{-1}, yielding a carrier mobility of about 1000 $cm^2\ V^{-1}\ s^{-1}$ for the graphene channel. This mobility is much smaller than those of the GHE on SiO_2/Si substrate, which have typical values of 6000 $cm^2\ V^{-1}\ s^{-1}$ [8,17]. Nevertheless, the achieved voltage related sensitivity is still higher than that of silicon based Hall sensors fabricated via CMOS technology, which have typically a sensitivity of about 0.07 T^{-1} owing to the lower carrier mobility in Si[20]. The low graphene channel mobility is mainly attributed to the scattering and charge impurities introduced by Si_3N_4 substrate and SU8 passivation layer since fabricating process and structure of the GHE are both far from optimized. It is expected that the performance of the integrated GHE on Si chip can be greatly improved by perfecting the fabrication process, device geometry and substrate preparation or treatment conditions. On the other hand, if the GHE is stimulated by a constant current of 100 μA (Figure S2, Supplementary information), the current related sensitivity is derived to be 200 V $A^{-1}\ T^{-1}$, which is again much larger than that of typical silicon based Hall sensor, *i.e.* 100 V $A^{-1}\ T^{-1}$ [20].

After fabrication and characterization on the GHE were finished, the silicon CMOS ICs and GHE were wire-bonded to a printed circuit board (PCB) for further IC function and integration test (Figure S3, Supplementary information). Output signals of the hybrid Hall ICs under an alternating magnetic field were measured using a test circuitry as shown in Figure 4a. During the test, the input signals of the chip were selected either from an Agilent function waveform generator 33220A or the GHE output, which correspond to IC function test and integrated system test respectively. We first tested the functions of the Si CMOS ICs. As a reference, a sinusoidal wave (generated by the function waveform generator 33220A) with a frequency of 15 Hz and a peak-to-peak voltage of 25 mV was inputted into the Si CMOS amplifier, and its output signal was observed by an oscilloscope (Agilent DSO7054A). Figures 4b and 4c show the input and output signals in amplification mode S1 and S0 respectively. It is evident that the silicon ICs can function normally at low frequency with amplifications of about 7.2 in S1 and 4.8 in S0, which are about one seventh of those at 1 kHz (Figure S4a and S4b, Supplementary information). The damping of amplification at low frequency is resulted from the coupling and shunt capacitances of the ICs at low frequency outside the band width of the amplifier (Figure S4c and S4d, Supplementary information).

In performing graphene/Si hybrid Hall ICs system test, the GHE and CMOS ICs are biased with one constant power supply of 3.3 V, and the hybrid ICs chip is measured under an alternating magnetic field which is generated by rotating a magnet using an electro-motor. The magnetic field at the measurement position varies periodically following the position of rotating magnet with amplitude of 21.7 mT and a frequency of 15 Hz (Figure S5, Supplementary information). As a magnetic sensor, the GHE on the chip should convert the

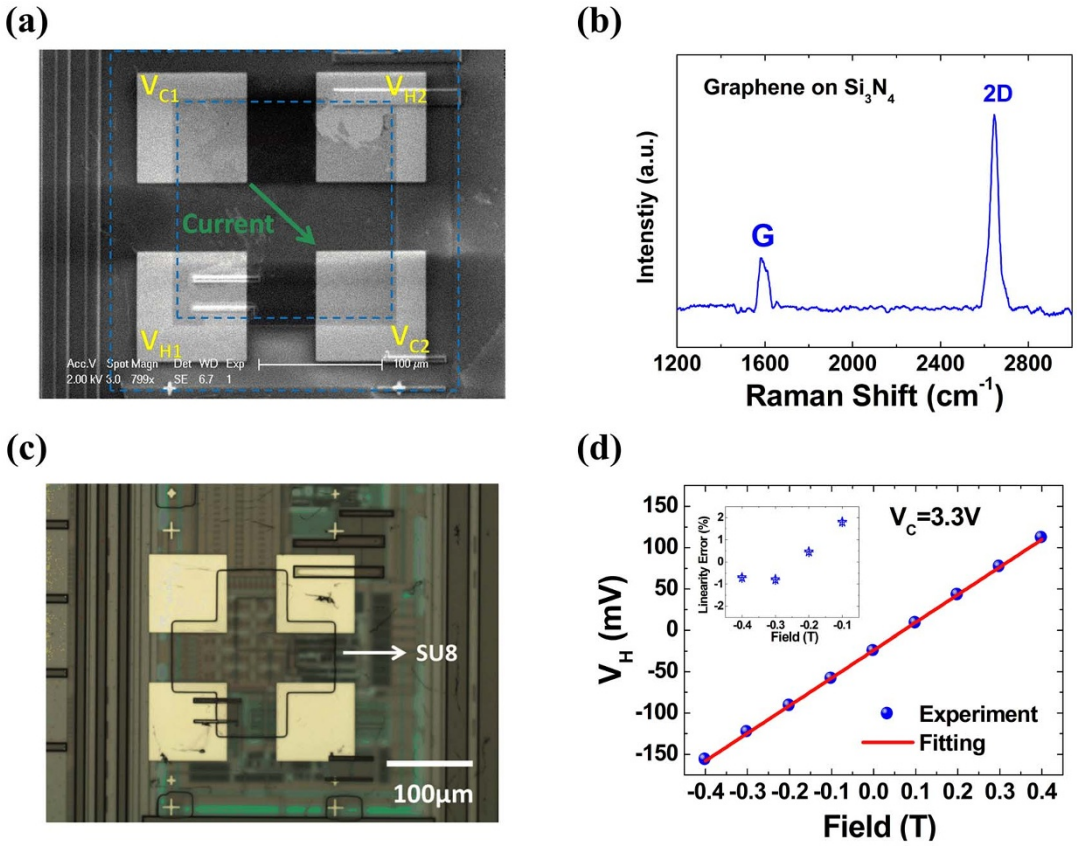

Figure 3 | Characterization of the as-fabricated GHE on silicon CMOS chip. (a) SEM image showing the GHE on the chip. The image is taken after completing the oxygen plasma etching process. The area enclosed by the two blue dashed squares is the place where graphene is etched away. The green arrow denotes current flow from electrode V_{C1} to electrode V_{C2}. (b) Typical Raman spectrum obtained from the CVD graphene on top of the Si_3N_4 passivation layer of the Si chip. The wavelength of the excitation laser is 633 nm. (c) An optical image showing the GHE after the device is passivated by a cross shaped SU8 layer, which is marked in the image by a white arrow. (d) A typical linear fitting of the Hall voltage versus magnetic field in voltage mode. Inset: linearity error of the GHE in a magnetic field ranging from −0.4 T to −0.1 T.

alternating magnetic field into an alternating Hall voltage signal. The alternating output signal of the GHE is then sent to the Si CMOS IC which amplifies the Hall voltage with optional amplification S1 or S0, and the final output signals are shown in Figure 4d and 4e respectively. It should be pointed out that the noise in the final result is mainly resulted from the low frequency 1/f noise of the device which dominates the measurement system at 15 Hz. This represents the upper limit of the alternating magnetic field frequency that we can realize in this work. It should be noted that the Si CMOS chip is designed to work at high frequency of above 1 kHz, which is much higher than the maximum alternating magnetic field frequency of 15 Hz used here. In principle, the signal/noise ratio of our Hall ICs can be significantly improved if the Hall measurements were carried out at higher frequency, e.g. at 1 kHz. Nevertheless, the output signals of the hybrid ICs follow the same 15 Hz frequency of the rotating magnet, suggesting that the output signals of the hybrid ICs is stimulated by the external magnetic field. The voltage amplitude of the output signal is 47 mV in mode S1 and 33 mV in mode S0, yielding an absolute sensitivities of the integrated Hall ICs of 2.17 V T^{-1} and 1.52 V T^{-1} respectively. These values are much higher than that of the as-fabricated GHE before being integrated to Si CMOS ICs. The increased sensitivity of the Hall ICs may be attributed to the silicon amplifying module in the Si CMOS ICs, and the actual amplifications is 6.6 in S1 and 4.6 in S0 respectively, which are very close to the measured values of 7.2 and 4.8 from Figure 4b and 4c. In the same way the voltage related sensitivity of the Hall ICs is also improved by the silicon amplifier and reaches 0.66 T^{-1} in mode S1 and 0.46 T^{-1} in mode S2, which are 6.6 and 4.6 times higher than that of the GHE in mode S1 and S2 respectively. It should be noted that the best performance of the hybrid Hall ICs cannot be fully demonstrated at very low operating frequency here because it falls outside the designed bandwidth of the Si CMOS ICs. Nevertheless the graphene/Si hybrid CMOS Hall ICs work well, demonstrating certain advantages of the hybrid Hall ICs, *i.e.* the sensitivity of the fabricated GHEs is higher than that of silicon Hall elements and can be further increased directly by the integrated Si CMOS amplifier on the chip. Although the final sensitivity of the hybrid Hall ICs is still lower than that of the best commercial silicon Hall ICs[30], there remains a huge space to optimize the hybrid Hall ICs. Among other factors, the carrier mobility of graphene is many times higher and the temperature stability of the GHE is much better than that of Si. We thus expect that via further optimizing the fabrication process of GHEs and the silicon amplifying circuits, the graphene/Si CMOS Hall ICs might eventually outperform all conventional Hall ICs.

In conclusion, we have developed a low-temperature process for fabricating graphene Hall sensors and integrating them with silicon CMOS ICs. Signal amplifying/processing ICs are manufactured via commercial 0.18 μm silicon CMOS technology, and GHEs are fabricated on the passivation layer of the Si CMOS chip via a low-temperature micro-fabrication process. The hybrid ICs work well and fully exhibit the function of Hall ICs at a low supply voltage of 3.3 V, *i.e.* GHE converts a magnetic signal to electrical signal which can be further amplified by Si CMOS ICs. The as-fabricated GHE on CMOS chip exhibits higher sensitivity than that of silicon Hall element, and the sensitivity can be further improved by the cascaded Si CMOS amplifier. This work not only paves the way for fabricating

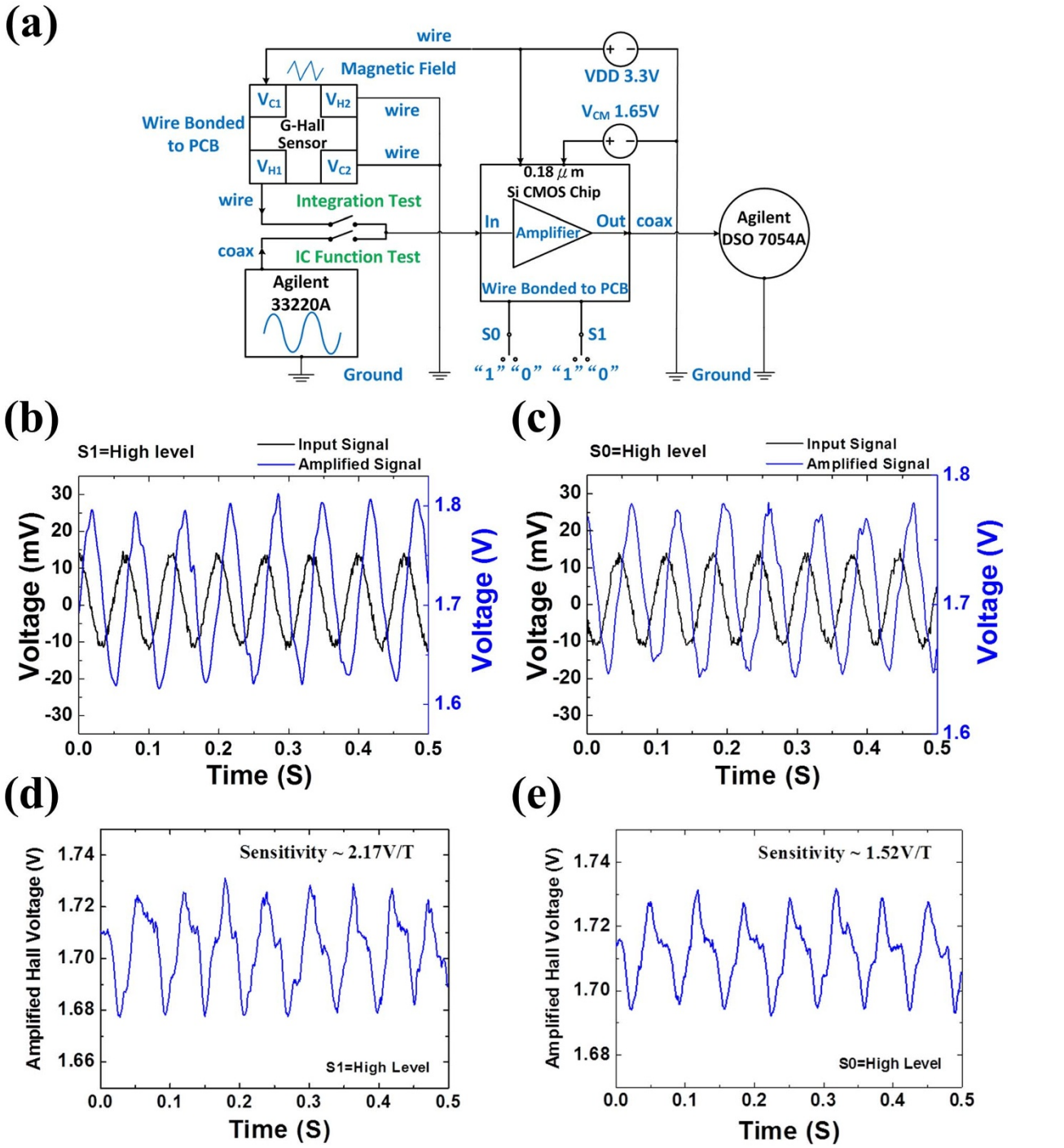

Figure 4 | Electronic measurements of the hybrid Hall IC. (a) Measurement circuitry. IC function test results showing the input and output signals when the amplifier is selected as (b) Amplification S1 and (c) Amplification S0. The input signals of (b) and (c) are sinusoidal waves with a frequency of 15 Hz and a peak-to-peak voltage of 25 mV, which are produced by the function waveform generator. Test results for the Hall IC under an alternating magnetic field when the amplifier is selected as (d) Amplification S1 and (e) Amplification S0. The input signals of (d) and (e) are collected from the output of the GHE.

graphene/Si CMOS Hall ICs with much higher performance than that of conventional Hall ICs, but also provides a general method for scalable integration of graphene devices and silicon CMOS ICs.

Methods

Fabrication of GHE devices on Si-CMOS chip. (1) Ti/Au (10/90 nm) metal contacts and alignment marks for next patterning process are patterned using electron-beam lithography (EBL) based on PMMA, and deposition is made by electron beam evaporator, followed by a standard lift-off process in acetone. Before the exposure, PMMA 200k is spun onto the chip at a speed of 4000 round per minute, and then the chip is baked on the hotplate at 180°C for 3 minutes. (2) Chemical vapor deposition (CVD) graphene is synthetized on a Pt foil and transferred to the Si chip via a well-developed bubbling method[31]. (3) The Si_3N_4 surface of the Si chip is pre-cleaned through oxygen plasma and functionalized with 3-aminopropyltriethoxysilane (APTES) before transferring graphene[8,18]. This step is crucial to keep the transferred graphene complete and stable on Si_3N_4 surface due to the strong interaction between APTES and graphene, which is harmless to graphene sample[18]. Moreover, our previous work has proven that GHE with APTES modification exhibites higher transconductance and smaller Dirac point voltage compared with that without modification[8]. (4) The transferred graphene is patterned to form a channel for the Hall element through another EBL on PMMA 200k, followed by an oxygen plasma

etching process under power of 100 w for 40 seconds. (5) The finished GHE is passivated by covering it with a layer of negative photoresist SU8 (with a thickness of about 1 μm), which is patterned via an additional EBL and reinforced through a hard bake process at 150°C on a hot plate for one hour. It is worth mentioning that the SU8 passivation layer can prevent graphene from usual contaminants and help to improve the stability of the GHE in air[17,32], which is essential for the integration test of the hybrid graphene/Si Hall ICs. In Addition, SU8 causes minimum damage to the carbon lattice of graphene[32] and contributes to the negligible hysteresis in transfer curve of GHE[17].

The supplementary information contains detailed descriptions of graphene characterization, Hall measurements, and graphene/Si CMOS hybrid Hall ICs.

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Acknowledgments

This work was supported by the Ministry of Science and Technology of China (Grant Nos. 2011CB933001 and 2011CB933002), National Science Foundation of China (Grant Nos. 61322105, 61271051, 61376126, 61321001 and 61390504), and Beijing Municipal Science and Technology Commission (Grant Nos. Z131100003213021 and 20121000102).

Author contributions

Z.Z. and L.M.P. designed the experiment, L.H., H.X., X.M., B.C., Z.L. and H.Z. performed the growth and transfer of graphene, device fabrication and characterization. L.H., C.C. and J.J. designed the silicon CMOS ICs. L.H., Z.Z. and L.M.P. analyzed the data and co-wrote the manuscript. All authors discussed the results and commented on the manuscript.

Additional information

Supplementary information accompanies this paper at http://www.nature.com/scientificreports

Competing financial interests: The authors declare no competing financial interests.

How to cite this article: Huang, L. *et al*. Graphene/Si CMOS Hybrid Hall Integrated Circuits. *Sci. Rep.* **4**, 5548; DOI:10.1038/srep05548 (2014).