

Graphite based Schottky diodes formed on Si, GaAs, and 4H-SiC substrates

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We demonstrate the formation of semimetal graphite/semiconductor Schottky barriers where the semiconductor is either silicon (Si), gallium arsenide (GaAs), or 4H-silicon carbide (4H-SiC). Near room temperature, the forward-bias diode characteristics are well described by thermionic emission, and the extracted barrier heights, which are confirmed by capacitance voltage measurements, roughly follow the Schottky–Mott relation. Since the outermost layer of the graphite electrode is a single graphene sheet, we expect that graphene/semiconductor barriers will manifest similar behavior. © 2009 American Institute of Physics. [doi:10.1063/1.3268788]

Metal-semiconductor contacts are ubiquitous in semiconductor technology not only because they are unavoidable, but also because the associated (Schottky) barriers to electronic transport across the metal-semiconductor interface can be tuned by judicious choice of materials and processing techniques.¹ The most prominent property of a Schottky barrier is its rectifying characteristic; the barrier acts like a diode with large currents flowing for forward bias and significantly smaller currents flowing for reverse bias.² If low resistance and “ohmic” (linear) I - V characteristics are desired, then materials and/or processing techniques are chosen to assure that the Schottky barrier height (SBH) ϕ_B is small compared to temperature (i.e., $\phi_B \ll k_B T$). Semimetal rather than metal electrodes can also be used. For example, epitaxial ErAs/InAlGaAs diodes fabricated by molecular beam epitaxy have barrier heights that can be tuned over a wide range by adjusting composition and doping.³

Here we report on the use of highly oriented pyrolytic graphite (HOPG) as the semimetal in semimetal/semiconductor Schottky barriers. We demonstrate rectifying characteristics on three different n -type semiconductors each of which is uniquely suited to specific applications: namely, Si with its robust oxide, to field-effect transistors, GaAs with its direct band gap, to spintronic and optical applications, and SiC with its high thermal conductivity and breakdown strength, to high power/frequency devices. Advantageously the HOPG contact, which can be applied at room temperature, causes minimal disturbance at the semiconductor surface for two reasons: the graphene sheets of the graphite are robustly impervious to diffusion of impurity atoms⁴ and the van der Waals force of attraction is relatively weak. Since ϕ_B is related to an interfacial dipole layer associated with bond polarization,¹ we infer that barrier properties are determined primarily by the outermost layer of the HOPG contact, i.e., a single-layer graphene (SLG) sheet. Accordingly, our results anticipate similar phenomenology using two-dimensional graphene rather than three-dimensional graphite. Other examples demonstrating SLG-like properties in graphite include angle resolved photoemission spectroscopy (ARPES) evidence for the precursor influence of K-point Dirac fermions⁵ and a pronounced temperature-dependent upturn

in the in-plane resistivity (ρ_{ab}) in the 300 K $< T <$ 900 K temperature range where the next-to-nearest neighbor couplings can be ignored so that the graphite can be described as a stack of graphene bilayers.⁶

We have used commercially available n -type Si and GaAs with $1 \times 10^{15} \text{ cm}^{-3}$ phosphorus (P) and $3 \times 10^{16} \text{ cm}^{-3}$ silicon (Si) doping densities respectively. The 4H-SiC wafers are layered, comprising a 5 μm thick layer of doped epilayer ($1 \times 10^{16} \text{ cm}^{-3}$) deposited onto an insulating 4H-SiC substrate. The substrates are thoroughly cleaned to remove any native oxide and/or contaminants. Ohmic contacts are made on the substrates using existing ohmic contact recipes.⁷⁻⁹

The HOPG contacts are made to the semiconductors using three related techniques: (1) spring loaded bulk HOPG, (2) van der Waals adherence of cleaved HOPG flakes, or (3) HOPG “paint.” In the first technique a relatively large ($\sim 1 \text{ mm}^2$) piece is gently pressed onto the substrate. In the second cleavage technique, mechanically exfoliated HOPG sheets are landed on the semiconducting substrates. Occasionally, relatively large area ($\sim 0.5 \text{ mm}^2$) HOPG flakes flatten out with strong adherence to the substrate due to van der Waals attraction. In the paint technique, graphite powder/flakes are sonicated in residue-free 2-butoxyethyl acetate and octyl acetate and the painted contacts allowed to air dry. All of these “soft-landing” techniques give similar results when the applied currents are normalized with respect to contact area.

The three panels of Fig. 1 show the measured current density versus Voltage (J - V) room-temperature characteristics of HOPG paint contacts on Si, GaAs, and 4H-SiC substrates. These data represent a subset of 27 different samples, all giving similar results independent of the method of application of the HOPG electrode. As seen from Fig. 1, graphite based junctions show good rectification at room temperature. For all of the junctions the rectification is preserved down to 20K.

When electron transport over the barrier height is dominated by thermionic emission, the semilogarithmic J - V curves usually display a sufficiently linear portion in the forward-bias region from which estimates of the zero bias barrier height ϕ_{B0} and the ideality constant η can be extracted. The extraction is based on the Richardson equation

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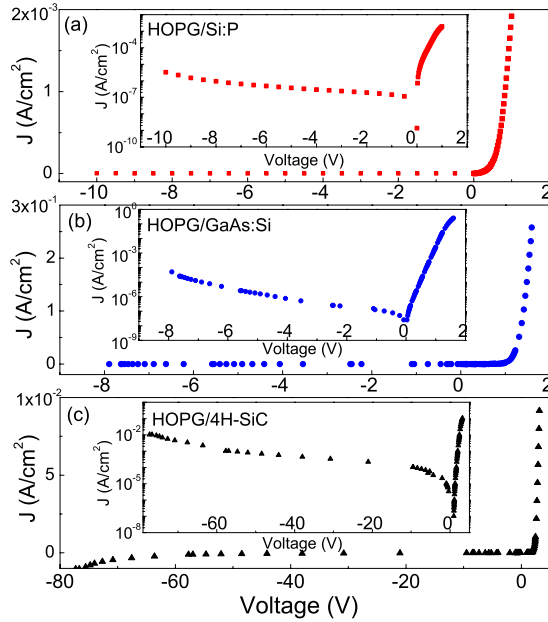


FIG. 1. (Color online) Plots of the room-temperature current density J with respect to applied bias V on (a) n -type Si/graphite (red squares), (b) n -type GaAs/graphite (blue circles), and (c) n type 4H-SiC/graphite junctions (black triangles). Insets: J - V plots on semilogarithmic axes.

$$I = I_s(T) [\exp(qV/\eta k_B T) - 1], \quad (1)$$

where $I_s = AA^* T^2 \exp(-q\phi_{B0}/k_B T)$ is the saturation current, $q\phi_{B0}$ is the zero bias SBH, A^* is the Richardson constant, T is the absolute temperature, and V is the voltage across the ohmic and HOPG contacts. As shown in the panel insets of Fig. 1, the HOPG/Si junctions displayed 2–3 decades of linearity in the semilogarithmic J - V curve while the HOPG/GaAs and HOPG/4H-SiC junctions displayed, respectively, 6 and 4 decades of linearity. The deviations from linearity can be attributed to the existence of more than one transport process, such as space-charge limited emission at low voltages and series resistance effects at higher voltages.

Extraction of a reliable value for ϕ_{B0} from Eq. (1) requires knowledge of the electrically active area A . For the HOPG paint contacts, A is not accurately known due to the unknown contact areas of the randomly distributed graphite pieces/flakes on the semiconductor. We remedy this situation by plotting semilogarithmic isothermal I - V curves, rather than the J - V curves shown in Fig. 1, and then use extrapolation from the linear regions to $V=0$ to determine $I_s(T)$. Analysis is facilitated by writing the equation for $I_s(T)$ in the form

$$\ln[I_s(T)/T^2] = \ln(AA^*) - (q\phi_{B0}/k_B T), \quad (2)$$

where the unknowns A and ϕ_{B0} now appear in separate terms. Typical Richardson activation energy plots of $\ln[I_s(T)/T^2]$ versus T^{-1} are shown in Fig. 2 over the temperature range 250–330 K for HOPG/Si:P (red squares) and HOPG/GaAs:Si (blue circles) junctions. The effective SBHs are calculated from the slopes to be 0.40(1) eV and 0.50(1) eV for Si and GaAs, respectively, (Table I) with ideality factors (η) spanning from 1.25 to 2.0 for the paint samples shown in Fig. 1. The ideality factors (η) of the graphite flake samples ($1.12 \leq \eta \leq 1.50$) are found to be typically smaller than those of the samples prepared by the paint and pressure-contact methods.

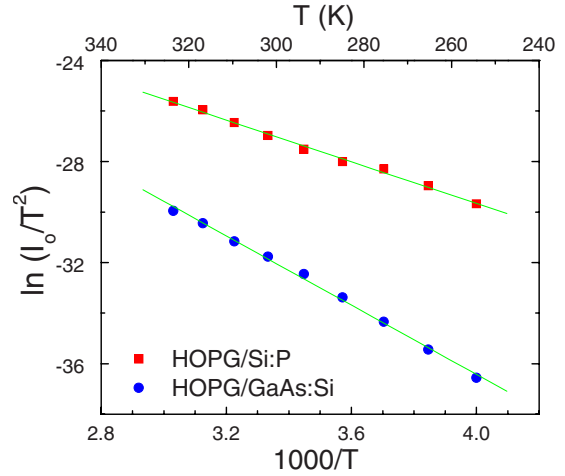


FIG. 2. (Color online) Richardson activation plots, i.e. $\ln(I_s/T^2)$ as a function of T^{-1} from 250 K up to 330 K on (a) HOPG/Si:P (red squares) and (b) HOPG/GaAs:Si junctions (blue circles).

Values of η greater than unity are generally attributed to bias dependent SBHs, generation-recombination, thermally assisted tunneling, and image force lowering.¹ These effects can be quantitatively taken into account by finding the flat band zero-electric-field SBH, ϕ_{BF} , where surface states, if they exist, are depleted of charge and tunneling and image force lowering effects are not present. Theoretical arguments supported by experimental data for η in the range $1.05 \leq \eta \leq 2.2$ validate the relation^{10,11}

$$\phi_{BF} = \eta\phi_{B0} - (\eta - 1)(k_B T/e) \ln(N_C/N_D), \quad (3)$$

where N_D and N_C are respectively the doping density and the effective density of states in the conduction band. Using this expression, the calculated ϕ_{BF} values are found to be larger than ϕ_{B0} and are closer to the SBH values determined by the C - V measurements (Table I).

Using the Schottky–Mott relation, $\phi_{BF,B0} = \phi_m - \chi$, which relates SBH to the metal work function ϕ_m and the semiconductor electron affinity χ , together with the assumption that the Fermi levels of the semiconductors are not pinned, we calculate the HOPG contact work function (ϕ_{HOPG}) to be in the range 4.40–4.80 eV (Table I). Although the HOPG/4H-SiC junctions do not reveal comparable linearity in the activation energy plots, we can still estimate SBHs using Eq. (1)–(3) and with the contact area and theoretical value of the Richardson constant by fitting the J - V curves in panel (c) of Fig. 1 (Table I). Our values of ϕ_{HOPG} determined separately on Si, GaAs and 4H-SiC are in good agreement with the theoretically and experimentally determined values (ranging from 4.4 to 4.8 eV) reported in the literature.^{12–14}

As shown in Fig. 3, we have also used capacitance (1 kHz)-voltage (C - V) measurements plotted in the form $1/C^2$ versus V_R , where V_R is the reverse bias voltage, to

TABLE I. Extracted SBHs, doping densities, and corresponding graphite work function values on various graphite/semiconductor junctions.

Junction type	ϕ_{B0} (eV)	ϕ_{BF} (eV)	ϕ_{C-V} (eV)	N_D^{C-V} (cm ⁻³)	N_D^{Hall} (cm ⁻³)	ϕ_{HOPG} (eV)
HOPG/ n Si	0.40	0.60	0.70	1.2×10^{15}	1.0×10^{15}	4.60
HOPG/ n GaAs	0.60	0.78	0.76	3.6×10^{16}	3.0×10^{16}	4.78
HOPG/ n 4H-SiC	1.15	1.60	1.84	1.2×10^{16}	1.0×10^{16}	4.80

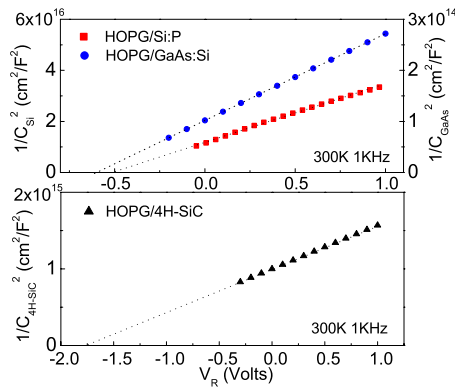


FIG. 3. (Color online) Inverse square of capacitance per unit area measured at 1 kHz as a function of reverse bias at room temperature: (top panel) HOPG/Si:P (red squares, right hand axis) and HOPG/GaAs:Si (blue circles, left hand axis); (bottom panel) HOPG/4H-SiC (black triangles).

characterize our junctions at room temperature. The observed linearity suggests that gap states are absent and that the surface density of states is small.¹⁵ Linear extrapolation (dotted lines) to the intercept with the abscissa identifies the built-in potential V_{bi} , which is related to SBH via the expression, $\phi_{C-V} = V_{bi} + (E_c - E_F)$, where E_c is the conduction band edge and E_F the Fermi energy. In like manner, the dopant densities of each semiconductor can be calculated from the slopes. The values for ϕ_{C-V} and N_D extracted from the linear dependences shown in Fig. 3 are listed in Table I. Although the values for N_D are in good agreement with Hall data, the values for ϕ_{C-V} are observed to be slightly higher than the values extracted from $I-V$ measurements. This trend might be attributed to the presence of a very thin oxide layer at the metal-semiconductor interface causing V_{bi} , and hence ϕ_{C-V} , to be overestimated by $C-V$ measurements.¹

In conclusion, we have demonstrated the formation of Schottky contacts using a “soft-landing” HOPG contact on n -type Si, GaAs, and 4H-SiC semiconducting substrates. Fabrication can be as easy as allowing a dab of HOPG paint to air dry on any one of the investigated semiconductors. The extracted values of SBH from $I-V$ and $C-V$ measurements

roughly obey the Schottky–Mott relation with inferred graphite work functions agreeing well with literature values. Our results not only provide unexpected insights into the nature of the graphite/semiconductor interface but also anticipate applications where single-layer graphene is directly contacted to a semiconductor substrate rather than isolated by an insulating oxide¹⁶ or grown directly on undoped insulating semiconductors.¹⁷

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