Grid integration and coordinated control of voltage source inverters with energy storage systems

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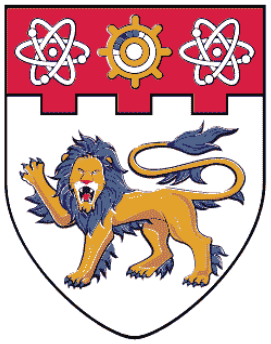

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

GRID INTEGRATION AND COORDINATED CONTROL OF VOLTAGE SOURCE INVERTERS WITH ENERGY STORAGE SYSTEMS

QI YANG

INTERDISCIPLINARY GRADUATE SCHOOL
ENERGY RESEARCH INSTITUTE @ NTU

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QI YANG

Interdisciplinary Graduate School
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A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2021

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

20 Jun 2020

Date

QI Yang

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accordance with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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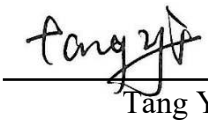
Tang Yi

Authorship Attribution Statement

This thesis contains material from four papers published in the following peer-reviewed journals where I was the first author.

Chapter 2 is published as Y. Qi, J. Fang, and Y. Tang, "Utilizing the Dead-time Effect to Achieve Decentralized Reactive Power Sharing in Islanded AC Microgrids," *IEEE J. Emer. Sel. Topics Power Electron.*, doi: 10.1109 /JESTPE. 2019.2904077.

The contributions of the co-authors are as follows:

I prepared and wrote the manuscript draft, established the hardware prototype, and performed the experimental test.

Dr. J. Fang assisted me in developing the control scheme, performing stability analysis, revising the original manuscript, and writing the response letter.

Prof. Y. Tang was responsible for revising and proofreading the manuscript.

Chapter 3 is published as Y. Qi, Y. Tang, K. R. R. Potti, and K. Rajashekara "Robust power sharing control for parallel three-phase inverters against voltage measurement errors," *IEEE Trans. Power Electron.*, doi: 10.1109/ TPEL.2020. 2993290,

The contributions of the co-authors are as follows:

I prepared the manuscript draft and performed the experimental tests.

Dr. K. R. R. Potti helped me to build the hardware prototype at the University of Houston.

Prof. Y. Tang and Prof. K. Rajashekara were responsible for revising and proofreading the manuscript.

Chapter 4 is published as "Y. Qi, P. Lin, Y. Wang, and Y. Tang, "Two-Dimensional Impedance-Shaping Control with Enhanced Harmonic Power Sharing for Inverter-Based Microgrids," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11407-11418, Nov. 2019.

The contributions of the co-authors are as follows:

I prepared and wrote the manuscript draft, performed the experimental tests.

Dr. P. Lin assisted me in building the hardware setup and performing stability analysis.

Dr. Y. Wang provided valuable advice on the development of a distributed control algorithm.

Prof. Y. Tang provided the original idea of this manuscript and helped me to revise and proofread the manuscript.

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Abstract

Recent advances in power-electronics technologies facilitate the integration of distributed generations (DGs), such as renewable energy resources (RESs) and distributed energy storage systems (DESSs). The “microgrid” concept is formed when a number of DGs and loads are coupled together through power electronics converters. To maintain the power balance of a microgrid and perform the grid-forming function, DESSs should be properly controlled through the interfaced power converters. This thesis aims to analyze and overcome several issues regarding the coordination and control of DESSs, with the focus on the following aspects: fundamental power sharing among DESSs, unbalanced power sharing among DESSs, harmonic power sharing among DESSs, and the synchronization stability of Voltage source inverter (VSI) with DESSs. The detailed descriptions will be respectively provided hereinafter.

In an islanded AC microgrid, DESSs are usually integrated to the microgrid through voltage source inverters (VSIs). To improve the operation efficiency and avoid the undesired overloading, it is expected that multiple VSIs, which operate in parallel with each other, can share active and reactive power according to their power ratings. Though the active power can always be accurately shared by the frequency droop control, it is difficult to achieve the reactive power sharing as desired due to mismatched grid impedances and voltage sensor scaling errors. To address this problem, a decentralized reactive power control scheme is proposed through the inherent pulse-width modulation (PWM) dead-time effect. More specifically, a supplementary control is incorporated into the voltage control loop, which utilizes the dead-time effect to equalize the power factors of all the VSIs. As a consequence, the reactive power sharing can be accurately shared in a fully decentralized manner. Finally, simulation and experimental results are provided for verification.

In addition to the reactive power sharing, the unbalanced power introduced by negative-sequence load currents should also be accurately shared among DESSs based on the power ratings of VSIs. It is revealed that even small voltage measurement scaling errors may deteriorate the power sharing accuracy by

injecting positive- and negative-sequence circulating currents. Such a negative impact cannot be avoided given that the voltage-feedback control is well designed to have excellent tracking ability. To address this problem, a hybrid feedback and feedforward impedance-shaping control is developed, which makes the power-sharing performance robust against voltage measurement errors. The feedforward control is implemented to reshape the VSI impedances at the fundamental frequency such that the reactive and unbalanced power-sharing performance can be ensured. Meanwhile, conventional voltage-feedback control is also implemented to compensate for voltage distortions and improve the harmonic power-sharing performance. Since no communications and prior sensor error knowledge are required, the proposed control algorithm provides a simple but effective solution for decentralized power sharing among parallel three-phase VSIs. Finally, both simulation and experimental results are provided to verify the effectiveness of the proposed control strategy.

Due to the proliferation of nonlinear loads, considerable harmonic currents are injected into the microgrid, leading to severe power quality issues. In view of this challenge, it is expected that DESSs can cooperatively share the harmonic currents and contribute to the total harmonic distortion (THD) reduction of the point of common coupling (PCC) voltage. It is widely accepted that the harmonic currents of nonlinear loads are distributed among parallel VSIs according to their effective harmonic impedances, i.e., the sums of VSI impedances and grid impedances. Since grid impedances are unknown and could be mismatched, the VSI output impedance should be reshaped to improve the harmonic power-sharing accuracy. However, as conventional techniques only regulate VSI output impedances in one dimension, only one degree of freedom (DOF) is provided for the impedance shaping. It is found that such measures can hardly fulfill the proper harmonic power-sharing requirement under complex grid impedance situations. As a result, circulating harmonic currents will occur and produce additional power losses even if the harmonic power has been accurately shared. To solve this problem, a two-dimensional impedance-shaping control is developed, which can adaptively regulate VSI output resistances and inductances at the same time. The proposed control strategy requires no prior grid impedance knowledge and

can eliminate the circulating harmonic currents for arbitrary grid impedances, as verified by experimental results.

Another important aspect related to the VSI operation is the synchronization stability, which is not only influenced by VSI control parameters but also affected by grid structure, feeder impedances, and etc. Seen from the perspective of a local VSI, it is difficult to obtain the complete grid information. As a consequence, unpredicted low-frequency angle oscillations and even loss of synchronization may occur and pose a significant threat to the system. To overcome this issue, a design-oriented analysis is proposed for grid-connected VSIs. To be specific, by comparing the frequency-power characteristic (FPC) of the VSI and that of the power grid, clear insights are gained into the synchronization dynamics. Moreover, a frequency response identification (FRI) approach is further proposed to acquire the grid FPC without requiring grid information. Through this effort, low-frequency oscillations can be easily identified and damped through reshaping the FPC of VSI. Finally, the experimental results of a grid-connected VSI are provided for verification.

In summary, the overall research problem of this thesis is load power sharing and stability analysis of VSIs with the distributed energy storage system. This thesis analyzes the reasons for inaccurate power sharing and proposes control schemes that can improve the active, reactive, unbalanced, and harmonic power sharing in decentralized or distributed manners. Besides, the synchronization stability has also been studied and analyzed.

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List of Abbreviations

DESS	Distributed Energy Storage System
RES	Renewable Energy Source
RoCoF	Rate of Change of Frequency
CAES	Compressed Air Energy Storage
MW	Megawatt
VSI	Voltage Source Inverter
PWM	Pulse Width Modulation
UPS	Uninterruptable Power Supply
PLL	Phase-Locked Loop
SOC	State of Charge
THD	Total Harmonic Distortion
APF	Active Power Filter
GM	Gain Margin
PM	Phase Margin
KVL	Kirchhoff's Voltage Law
DOF	Degree of Freedom
SCR	Short Circuit Ratio
HIC	Harmonic Impedance Controller
GNC	Generalized Nyquist Criterion
FPC	Frequency Power Characteristic
FRI	Frequency Response Identification

Nomenclature

V_0	Nominal AC voltage magnitude
V_{pcc}	PCC voltage magnitude
ω_0	Nominal AC frequency
V_i	Voltage magnitude of *i*# VSI
u_{dc}	DC-input voltage
L_g	Line inductance
L_f	Filter inductance
r	Inductor ESR
C_f	Filter capacitance
R_g	Line resistance
Z_g	Line impedance
R_o	VSI output impedance
R_L	Load resistance
X_L	Load reactance
Z_L	Load impedance
m	*P-f* droop coefficient
n	*Q-V* droop coefficient
ω_f	Power filter cut-off frequency
P	Active power
Q	Reactive power
S^h	Harmonic power
S	Apparent power
P_L	Active power of load
S_N	Rated apparent power
Δk	Sensor scaling error
X_{dc}	Sensor DC offset
h	Harmonic order
k_p	Proportional gain
k_i	Resonant gain
k_c	Current-loop control gain
H_{SM}	Inertia coefficient
D	Damping coefficient
f_{sw}	Switching frequency
t_{sw}	Switching period
t_d	Dead-time duration

Chapter 1 Introduction

This chapter introduces the background related to the research topic of this thesis, including renewable energy sources (RESs), distributed energy storage systems (DESSs), and AC microgrids. Besides, the fundamentals of power-electronic converters and the associated control strategies will be elaborated. The motivations and objectives of this thesis are highlighted. Finally, the detailed organization of this thesis is provided.

1.1. Background

1.1.1. Renewable Energy Sources

For centuries, fossil-based power plants have contributed to the majority of electrical power generation. However, the combustion of fossil fuels, such as coal and oil, would inevitably result in massive consumption of carbon dioxides, which speed up the global warming process and contaminate the air. To effectively reduce the carbon footprint and greenhouse gas emission, environmental-friendly RESs will be increasingly deployed in the future power system. Fig. 1.1 illustrates the share of renewables of power generation capacity. It is seen that the renewable generation share has exceeded 50% during the past decade and this penetration level will be likely to grow in the coming years.

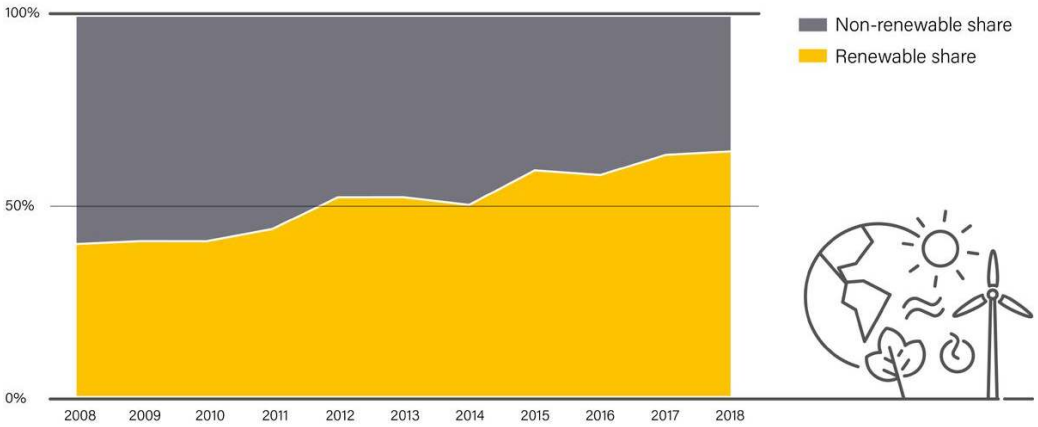


Fig. 1.1. Share of renewables in net annual addition of power generation capacity [1].

Generally, RESs include solar photovoltaic (PV), wind power, hydropower, and other types of resources. Among these RESs, hydropower remains dominant and contributes to around 16% of the total electricity production [1]. The hydropower plant harvests the gravitational energy of falling water and converts it into electricity. Due to affluent hydropower resources, countries such as Canada, New Zealand, Brazil, Switzerland, and Venezuela generate the majority of electricity through hydropower stations. However, the installation of hydropower plants may lead to detrimental impacts, mostly on aquatic ecosystems [2].

Alternatively, solar PV panels and wind turbines also provide promising solutions for electrical power generation. Fig. 1.2 illustrates the annual addition of renewable power capacity. It can be seen that solar PV and wind power are increasing rapidly as compared with hydropower and other RESs. Particularly, the annual PV power capacity increment

has approached 100 Gigawatts in the year 2018. It should be noted that countries like Ireland, Denmark, Costa Rica, and Germany have ambitiously deployed the RES-based power generations, with a penetration level of more than 20% [3].

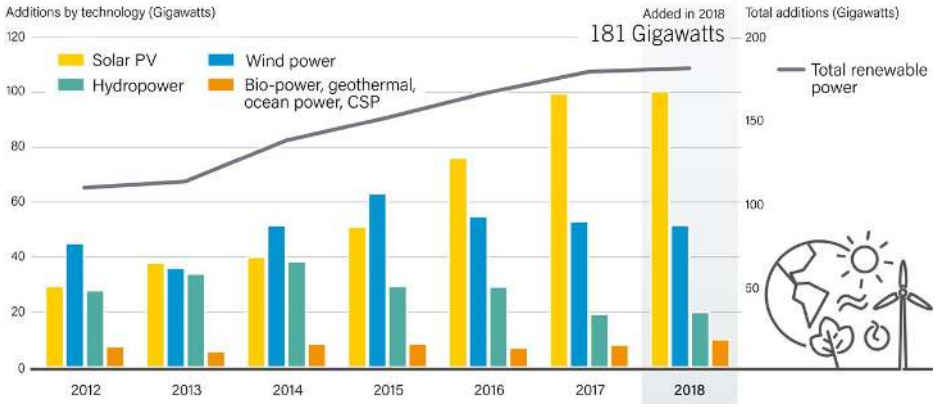


Fig. 1.2. Annual additions of renewable power capacity, by technology and total. [1]

Despite the effective reduction of carbon footprint, operating power systems with a high penetration level of RESs may fundamentally change the characteristics of the grid and pose significant threats to the power grid operation. Different from the conventional fossil-based synchronous generators that provide steady output powers, the outputs of RESs heavily depend on the environment condition and could be highly fluctuating. For example, the frequently-passing clouds would result in severe variations of solar PV panel output powers and the intermittency rate, in most cases, falls in the time scale of several seconds [4]. Similar things happen for wind power generation systems. There will be more wind power during the night hours than during the daytime since the wind direction changes more frequently during the night hours. Moreover, considerable ramp-rate power may occur as a consequence of sudden weather changes across geographical areas. It is widely believed that the intermittency caused by RESs will lead to a number of serious consequences, including system frequency deviations, voltage derivations, curtailment of power generations, load shedding, and etc.

Apart from the aforementioned issues, the grid integration of RESs is usually achieved through fast-response power-electronics converters. These converters do not possess the mechanical inertia attribute and hence may fail to accommodate the grid frequency regulation requirements [5]. When the majority of power generation has been achieved through inertialess power converters, the system frequency will be prone to instability, which is usually characterized by a frequency nadir as well as the rate of change of frequency (RoCoF) [6]. Consequently, the power grid frequency may easily exceed the

acceptable operation range, which subsequently leads to the tripping of synchronous generators, cascading failures, and even a system-level blackout. One recent example is reported as the South Australia power outage in September 2016, which has affected millions of people and caused considerable economic losses [7]. It is believed that the reduction of power system inertia would be one of the main reasons behind this accident [7].

Although massive integration of RESs contributes to the reduction of carbon footprint, it also introduces significant challenges to the security and operation of modern power systems. The aforementioned issues have already been reported in some small-scale microgrids and will soon be faced by large power systems that pursue a 100% renewable penetration level. In this regard, many countries have set a limit for the renewable penetration level. For example, the maximum allowable capacity of renewable power generation is capped at 600 MW in Singapore, which is much smaller than the 7000 MW peak load [8]. In this regard, the power grid decarbonizing process will be hindered and the system operator must be cautious about setting renewable energy targets.

1.1.2. Energy Storage Systems

To mitigate the adverse influences caused by RESs and improve the quality of power supply, energy storage systems (ESSs) are widely deployed together with RESs. An ESS is essentially an "energy buffer" that can absorb the redundant power at one time and release it later. Fig. 1.3 illustrates the functions of ESSs in terms of peak shaving and load leveling. During the low demand period when the total power generation is larger than the load consumption, the surplus electrical power will be stored by ESSs in the forms of electrochemical, gravitational potential, kinetic, thermal energy, etc. For the high demand period when the total power generation is smaller than the load consumption, the previously-stored energy will be converted into electrical power again, which helps to compensate for the imbalance between the power generation and the load consumption.

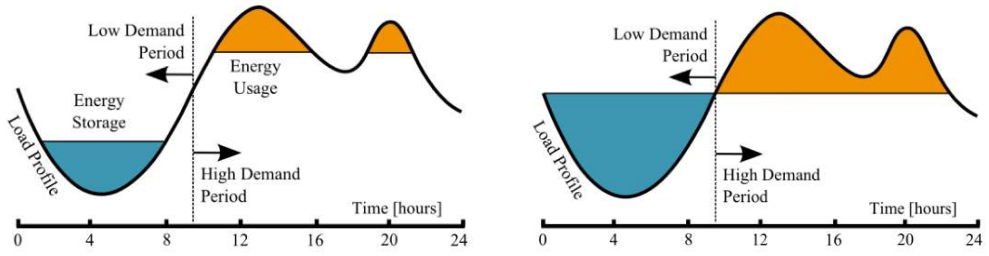


Fig. 1.3. Functions of ESS in terms of peak shaving and load leveling.

Presently, there are different types of energy storage technologies, including batteries, supercapacitors, flywheels, compressed air energy storage (CAES). A brief introduction to these technologies will be provided hereinafter and their respective disadvantages and advantages will also be evaluated.

a.) *Battery energy storage*

Batteries are considered as one of the most effective and promising ESSs, which can be utilized to shift load peaks, compensate reactive power, and improve power quality. Batteries are further classified according to the electrode materials. Lead-acid batteries are already commercialized and have a comparatively low material cost. Nevertheless, lead-acid batteries are bulky in size and their characteristics are sensitive to temperature changes. Compared with lead-acid batteries, lithium-ion batteries exhibit overwhelming advantages such as high energy density and high open-circuit voltages. Moreover, the performance of a lithium-ion battery will not degrade even after hundreds of charging and discharging cycles. However, lithium-ion batteries are seldom used for large-scale ESSs, as the current density of lithium-ion battery is limited due to physical constraints.

b.) *Supercapacitor energy storage*

The supercapacitor is an emerging energy storage technology. Compared with BESS, the supercapacitor has a larger power density, which means that it can be charged and discharged in a very short amount of time. Moreover, it is very convenient for operation since little maintenance works are required for the operation of supercapacitors. Despite this merit, low energy density is an inherent limitation of the supercapacitor and hinders its wide application.

c.) *Flywheel energy storage*

The flywheel energy storage system is a mechanical energy storage technology that converts electrical power into the kinetic power of a rotating flywheel [9]. Flywheel energy storage systems have advantages such as high efficiency and long operation lifetime. It is a very competitive storage technology except for high maintenance costs.

d.) *Compressed air energy storage* (*CAES*)

Compressed air energy storage utilizes electrical energy to compress air and store it in an underground reservoir. The compressed air has extremely high pressure and can be subsequently released to drive a turbine generator to generate electricity. Currently, two MW-level compressed air energy storage plants have been installed in Huntorf and McIntosh, respectively [10].

In summary, Fig. 1.4 compares the features of various energy storage technologies. Generally, the evaluation is made from two perspectives. The first index is power density, which refers to the ability of the ESS to absorb/release the power in a certain amount of time. The second index is energy density, which is related to ESS capacity and determines the charging/discharging time at the rated power. Among all the energy storage approaches, CAES and pumped hydro techniques have the largest power rating but a slower response time. Therefore, they could be assigned to compensate for significant power fluctuations over a long time period. In contrast, battery energy storage systems have a comparatively smaller power rating but are distributed at different places of a power system. The coordination control strategy would prefer battery energy storage systems to compensate for the power fluctuations near their locations. Lastly, ESSs like the supercapacitors have the smallest power rating but the fastest response. Due to this characteristic, they could be properly controlled to improve the transient response of the coordinated control strategy (by releasing and absorbing energy with a high ramp rate).

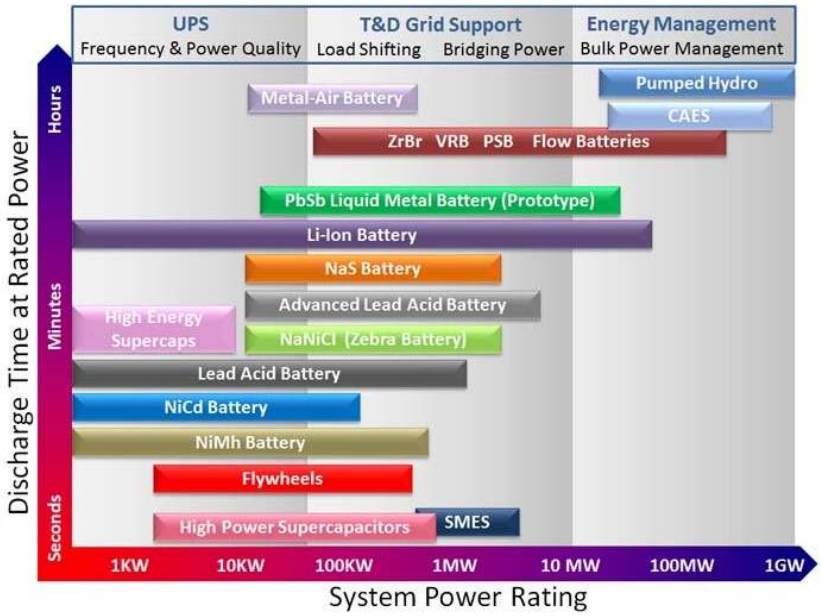
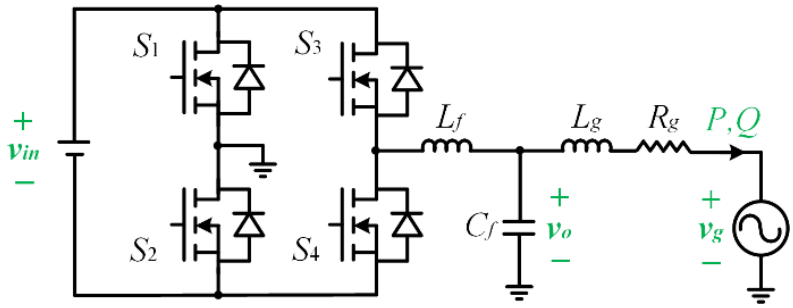


Fig. 1.4. Grid energy storage technologies and applications. [11]

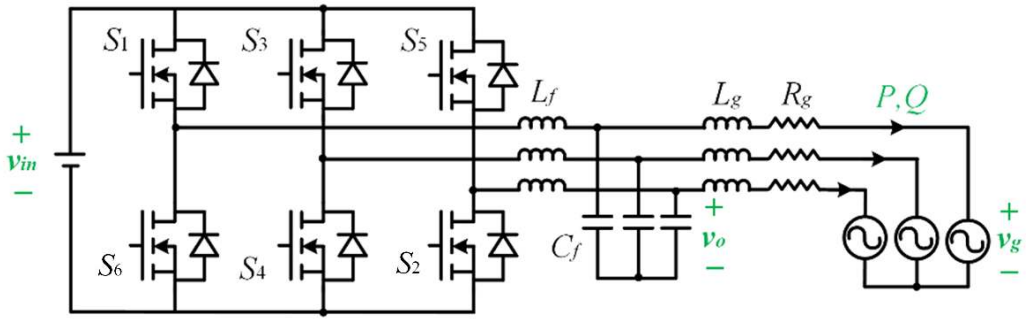
1.1.3. Power Electronic Converters

Usually, DESSs including batteries and supercapacitors have DC output voltages. To transform the DC energy into grid-compatible AC electricity, a power-electronics device called “inverter” is needed. Fig. 1.5 shows the typical circuit configuration of the single-phase and three-phase voltage source inverter (VSI). It should be mentioned that current source inverters [12] and multi-level inverters [13], [14] are also implemented in some

specific applications. This thesis, however, mainly focuses on the control and operation of the two-level VSIs, which are commonly adopted in various applications.



(a)



(b)

Fig. 1.5. Circuit configuration of a two-level VSIs. (a) Single phase. (b) Three phase.

As illustrated in Fig. 1.5, the overall DC/AC power conversion stage contains several components. Initially, power semiconductor switches S_i (i=1,2,3,4…) are controlled by pulse-width modulation (PWM) waves and alternatively turned on/off. Consequently, the inverter AC terminal outputs high-frequency square waves that contain the desired fundamental frequency voltage component. However, since considerable switching harmonics are also included, directly connecting the inverter AC terminal with the power grid will lead to serious power quality issues.

To overcome this problem, passive filters are normally installed at the output ports of the inverter. One straightforward approach is to deploy a single inductor, namely, the L filter, in series with the inverter. Although the L-filter is simple to implement, it enlarges the circuit size and increases the weight of the hardware prototype [15]. Alternatively, high-order filters such as the LC-filter and LCL-filter are usually preferred with a lighter weight and better harmonic attenuation ability [16], [17]. The filtered AC output voltage

v_o is coupled to the power grid voltage v_g through grid impedances R_g and L_g. For some applications, the power grid may not be available and the inverter is expected to operate as an uninterruptable power supply (UPS) and supplies power to critical loads [18], [19]. The bidirectional power flow is expected, which can be achieved through the control of VSI.

Next, VSI control strategies will be briefly introduced. Although there have been a number of controllers for the grid integration of ESSs, they can be generally classified into the grid-feeding type and grid-forming type [20]. Fig. 1.6 illustrates a typical circuit and control block diagram of the grid-feeding VSI.

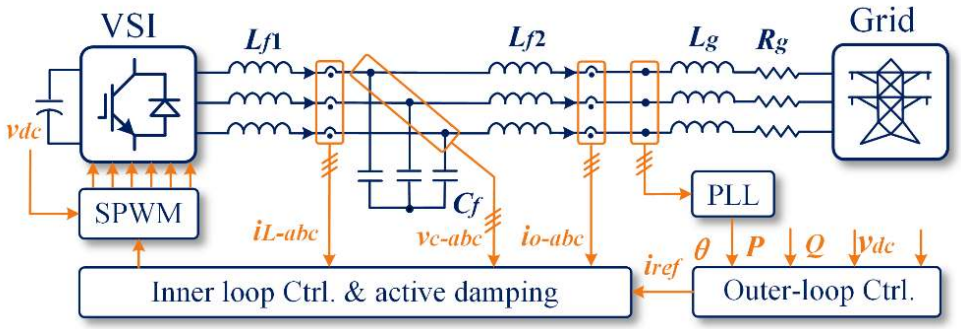


Fig. 1.6. Circuit and control block diagram of the grid-feeding VSI.

The grid-feeding inverter can be modeled as a current source, which injects active power P and reactive power Q to the power system. The overall control structure in Fig. 1.6 contains an outer power-control loop and an inner current control loop. Between them, the outer power-control loop is responsible for tracking the power references and determines the current reference i_{ref}. It should be mentioned that if the DC-input of the inverter is not supplied by a constant voltage source, the DC-link voltage v_{dc} must be maintained via the dynamic active power exchange between the VSI and power grid. In the meantime, the inner current-loop tracks the inverter output currents i_{o_abc} with the reference values. In addition, a phase-locked loop (PLL) is normally implemented for the grid synchronization and the *abc*/*dq* transformation through the provision of phase angle θ. It should be noted that the grid-feeding inverters behave like current sources and must work cooperatively with the AC power grid or grid-forming inverters.

Unlike the grid-feeding inverter, a grid-forming inverter behaves like a voltage source. The typical circuit and control block diagram of a grid-forming inverter are illustrated in Fig. 1.7. Similarly, the entire control architecture includes an outer power-control loop as well as an inner control loop. Based on sensor measurement results, the power-control

loop calculates the active and reactive power and subsequently generates the reference voltage v_{ref} through pre-designed relationships such as the frequency droop control [21]–[25], the virtual synchronous generator control [26]–[30], and the power synchronization control [31], [32]. In the meantime, the inner control loop is responsible for eliminating the voltage tracking error between VSI output voltage and the reference voltage. Besides, either the inductor current i_L or the capacitor current i_c, or the combination of both, are utilized as feedback to provide the active damping [33], [34]. It should be mentioned that the grid-forming inverter can run autonomously during the islanded operation mode, i.e., it can supply power to the load without relying on the utility grid. Moreover, during the grid-connected operation mode, the grid-forming inverter plays an important role in stabilizing the power grid frequency and voltage, just like the conventional synchronous generator [35], [36]. This attractive merit makes the grid-forming inverter be a promising solution for the 100% power-converter-based system.

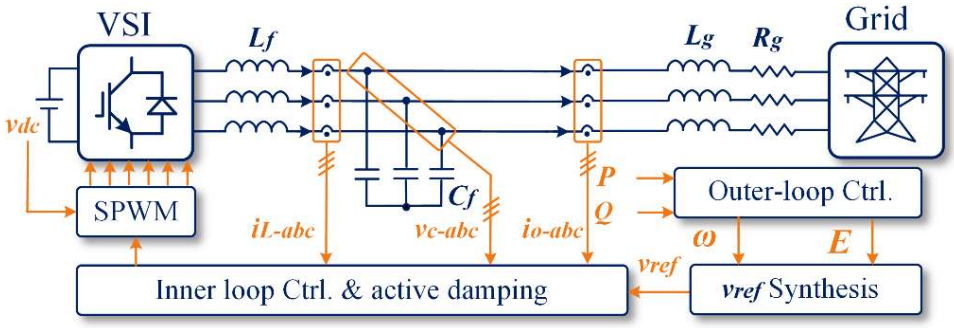


Fig. 1.7. Circuit and control block diagram of a grid-forming VSI.

For both grid-feeding VSIs and grid-forming VSIs, the controllers should be properly designed to fulfill certain requirements. First and foremost, it is necessary to ensure the stability of power converters. During the past decades, instability issues due to the high penetration of power converters were frequently reported in both industrial applications and literature [37]. This is especially true when a number of power converters operate in parallel, the interactions among which are very complicated and would probably trigger resonances.

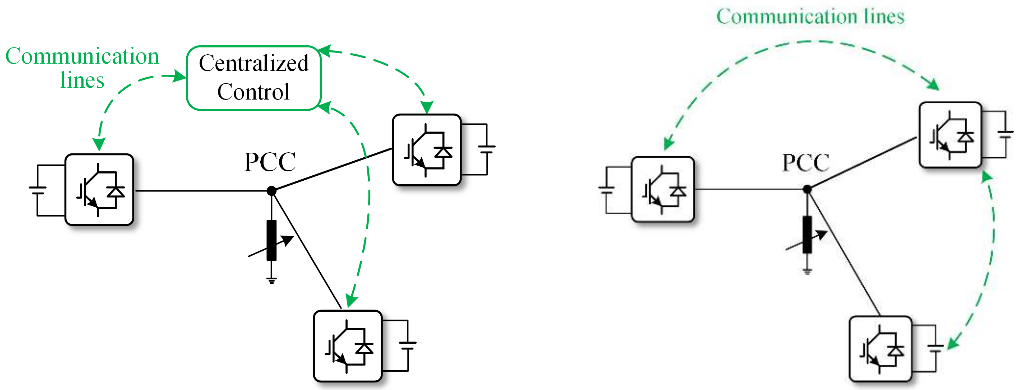
In addition to this, the VSI output voltage and current must satisfy the power quality standards, for example, IEEE and IEC [38], [39]. To be specific, the individual harmonic voltage/current distortion should be less than 3% of the fundamental magnitude. Besides, the total harmonic distortion (THD), which is defined as the ratio of the sum of the powers of all the harmonic components to the power of the fundamental frequency component, should be no more than 5%. It is known that the increasing use of power

converters inevitably introduces both low-frequency and high-frequency harmonics [40]. To ensure good power quality, VSI controller and passive filters must be designed to have effective harmonic attenuation abilities.

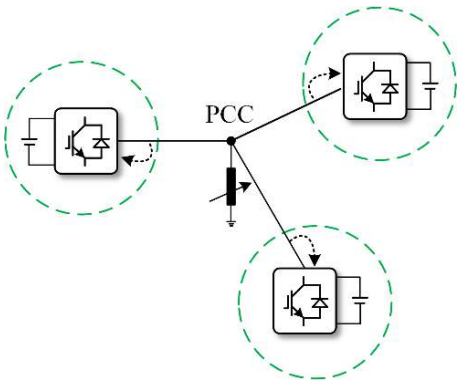
1.1.4. Microgrid with DESSs

The concept of a microgrid is formed when a number of RESs, ESSs, and loads are coupled together as a single controllable entity with respect to the grid [41]. Generally, a microgrid offers prominent advantages in terms of flexibility and expandability. It can either operate with the main grid in the grid-connected mode or just run autonomously in the islanded mode [42]. Between them, the islanded mode is highly preferred for small utilities or rural/remote areas, where the cost of building transmission lines overwhelms its practical efficacy. In the islanded mode, the power balance between the synchronous generator power generation and the load consumption is maintained by multiple VSIs, cooperatively. Therefore, it is of importance to coordinate them.

One important aspect would be the load power sharing among multiple parallel VSIs. It is desired that the total load power shall be proportionally allocated among VSIs based on their respective power ratings. The inaccurate load power sharing, on one hand, does not fully utilize the VSI capacities, while on the other hand, it may overload some of the VSIs. In view of this challenge, various control strategies have been proposed to achieve this objective. Generally, they are classified into centralized controls, decentralized controls, and distributed controls [43]. Fig. 1.8 respectively illustrates the principles of various control algorithms.



(a) (b)



(c)

Fig. 1.8. Various power management algorithms. (a) Centralized control. (b) Distributed control. (c) Decentralized control.

a.) *Centralized control algorithms*.

To implement centralized control algorithms, a central controller is normally required to exchange information with all the power controllers through communication channels. One typical example is the master-slave power management strategy, which assigns one specific power converter as the "master" unit and the rest as the "slave" units [44], [45]. Just as the literal meaning indicates, the master unit is responsible for supporting the microgrid operation, while the slave units are required to follow the commands sent from the master. Note that the "master" VSI operates in the grid-forming mode, which determines the microgrid frequency and voltage. Meanwhile, the rest of the "slave" VSIs are controlled as current sources with grid-feeding capabilities. Their reference currents are provided by the master VSC through a controller area network (CAN) bus such that the accurate power sharing among VSCs can be ensured.

b.) *Distributed control algorithms.*

It has to be mentioned that the microgrid under a centralized control algorithm is prone to the single-point communication line failures. To further enhance system reliability, distributed control algorithms are also proposed [46]–[48]. In these control techniques, power converters only need to share the information with their neighbors so that the use of a central controller can be avoided. In this case, the information required for power management would be adjacent rather than global. As a consequence, system reliability and flexibility have been greatly improved.

c.) *Decentralized control algorithms.*

For both centralized and distributed control algorithms, communication links must be required for information exchange. The dependency on communications, however, also brings many other issues, including the increased cost and infrastructure requirements, degraded reliability due to communication failures, degraded system stability caused by the communication delays [49], and vulnerability against malicious cyber attacks [50]. To overcome such limitations, decentralized control algorithms have also been proposed to facilitate power management wirelessly.

Inspired by the experience of paralleling multiple synchronous generators, one major technical milestone is reached as the active power-frequency (*P-f*) droop and the reactive power-voltage magnitude (*Q-V*) droop are innovatively implemented for the load power sharing. The major contribution behind this invention is allowing the VSI to emulate the characteristics of synchronous generators so that the microgrid power management issue can be effectively addressed by the methods that electrical engineers are already familiar with. The distinctive feature of decentralized droop control is that only local information is required for the power-sharing purpose, which is easy to achieve and does not require a communication link. In addition to this, the decentralized control algorithms also make it easier for VSIs to plug and play, which greatly improves the microgrid flexibility and scalability.

In some cases, the initial state of charges (SOCs) of ESSs are different and need to be balanced through the coordinated control of VSIs. To achieve this target, the SOC value can be incorporated into the frequency droop control to dynamically equalize the SOCs of different DESSs. The general idea is to link the VSI frequency with the SOC of ESS. As the frequency is a globally uniformed variable in the steady state, the consensus of SOC will also be reached for all DESSs. To this end, the active power-frequency (*P-f*) droop control will be replaced by the SOC-frequency droop control with a similar principle. The corresponding implementation has been well documented in the literature and hence will not be repeated [51]–[54]. For clarification, one research hypothesis of the thesis is that all the DESSs have the same initial SOC. Given that the active power is accurately shared among DESSs, their SOCs that are related to the integration of active power over time will inherently be balanced.

1.2. Motivations and Objectives

Though decentralized droop control provides a promising solution to microgrid power management. It still suffers from several drawbacks.

a.) *Inaccurate Reactive Power Sharing.*

The conventional droop control links the VSI active power with the voltage frequency. Since all the VSIs within a microgrid will reach the same frequency in the steady state, the total active power will be accurately shared according to the inverse of VSI droop coefficients, or in other words, VSI power ratings. Nevertheless, the same principle does not work for reactive power sharing. This is because reactive powers are linked with the VSI output voltage magnitudes, which will not reach a consensus even in the steady state. There are many factors that would degrade the reactive power sharing accuracy, such as mismatched grid impedances [55], the uneven distribution of inductive/capacitive loads, and voltage sensor measurement errors [56]. It is therefore challenging to eliminate the reactive power sharing error through the decentralized control algorithm since VSIs do not know the reactive power information of their peers.

b.) *Voltage and Frequency Deviations.*

One straightforward solution towards the above issue is to set a large droop coefficient so that the reactive power sharing error could be reduced to some extent. However, large droop coefficients also lead to severe voltage magnitude deviations at the same time [57]. Consequently, the point of common coupling (PCC) voltage magnitude deviation might go beyond the normal operating range. In this regard, there is, inevitably, a compromise between voltage magnitude deviation and the reactive power sharing accuracy. Similarly, the microgrid frequency should also comply with certain requirements. For example, the maximum frequency deviation should be maintained less than ± 0.2 Hz while the largest RoCoF value should be maintained less than 0.125 Hz/*s* (given that there might also be synchronous generators in the microgrids). Accordingly, the frequency droop coefficient, as well as the time constant of the power filter (which is equivalent to the inertia constant according to [58]) must be carefully tuned to ensure the satisfactory primary frequency regulation performance.

c.) *Unbalanced and Harmonic Power Sharing.*

Another technical challenge would be the sharing of unbalanced and harmonic powers, which is an important aspect due to the proliferation of power-electronics converters. It is well known that the conventional droop control only takes effect at the fundamental positive-sequence domain. Hence, the negative-sequence and harmonic currents cannot be properly shared by the classical droop control. The uneven distribution of unbalance and harmonic powers results in significant circulating currents among multiple VSIs and will cause distortions on the VSI output currents and the PCC voltage [59].

d.) *Stability Issues.*

In addition, stability is another issue for the microgrid operation. This is particularly the case when there are multiple VSIs within a microgrid and their interactions could be very complicated. Consequently, both high-frequency resonances (which are affected by the inner-loop controllers, passive filters, and grid impedances [60]) and subsynchronous resonances (which are mostly influenced by outer-loop controllers and grid impedances [61]) may be triggered, resulting in poorly-damped oscillations and even instability. To ensure the normal operation of a microgrid, VSI controllers must be carefully designed with adequate stability margins.

The aforementioned issues call for effective power management schemes on multiple parallel VSIs, which will facilitate the deployment of DESS and subsequently accelerate the decarbonization process. The overall objective of the thesis is to improve the power-sharing performance of VSI-interfaced DESSs, effectively compensate for the harmonic unbalanced voltages, and ensure the stable operation of the microgrid. Moreover, several research hypotheses are listed below

1.) The reactive, unbalanced, and harmonic power may not be accurately shared among multiple parallel VSIs by the conventional frequency droop control.
2.) Line impedance values and voltage sensor errors could affect the load power sharing accuracy. Power-sharing performance could be improved by reshaping VSIs output impedance and compensating voltage sensor errors.
3.) The dead-time effect may be used as an indicator of reactive power sharing accuracy.
4.) Synchronization stability depends on the frequency power characteristic of VSIs.

1.3. Thesis Organization

This thesis has six chapters. The corresponding contents are respectively discussed as listed below:

Chapter 1 introduces the fundamental knowledge of RESs, DESSs, and DC/AC power conversion techniques. Followed by this introduction, various control strategies of VSI and microgrids are respectively discussed. Then, several technical difficulties for the deployment of DESSs are discussed and the solutions towards these problems will serve as the major contributions of this thesis. The primary research objective of this thesis is to properly share load power among VSIs supplied by DESSs. Generally, the load power includes active, reactive, unbalanced, and harmonic power.

It is well known that the active power is always accurately shared by the frequency droop control, while some reactive power sharing errors exist. In view of this challenge,

Chapter 2 provides an in-depth analysis of the reactive power sharing among multiple parallel VSIs. It clearly explains how the dead-time effect is related to reactive power sharing and how to utilize this characteristic to eliminate the reactive power sharing error. A dead-time-based reactive power-sharing control strategy is then proposed, which is fully decentralized and does not require specific microgrid configuration, line impedance values, and locations of VSIs/loads.

However, the developed method as well as the conventional droop control only takes effect at the fundamental positive-sequence domain and cannot deal with unbalanced and harmonic power sharing. Chapter 3 reveals that even small voltage sensor voltage measurement errors may result in considerable positive-sequence and negative-sequence circulating currents among multiple VSIs. To address this issue, a hybrid feedback and feedforward control scheme is developed, which neutralizes the effects of voltage measurement errors at the fundamental frequency and facilitates the harmonic current sharing at selective harmonic frequencies. The proposed control algorithm is implemented in a decentralized manner and robust against sensor measurement errors.

In addition, Chapter 4 studies the harmonic current sharing among multiple parallel VSIs. The accurate harmonic current sharing condition is derived. On this basis, a two-dimensional impedance shaping strategy is proposed, which simultaneously regulates the resistive and inductive parts of VSI o impedances. Through this effort, the circulating harmonic currents among multiple VSIs are eliminated, regardless of the complex and unknown line impedances.

Lastly but most importantly, one important premise of AC load power sharing is that VSIs can well synchronize without any stability concerns. To guarantee synchronization stability, Chapter 5 presents a design-oriented analysis for the synchronization stability of VSI. Through the injection of small disturbances and the observation of associated responses, the power grid characteristic can be acquired, which facilitates the VSI controller design and helps to guarantee good synchronization stability. A case study is presented for verification, where a grid-forming VSI operates in parallel with a synchronous machine.

Chapter 6 concludes the main contributions of the thesis and also presents several new perspectives regarding the grid integration of DESSs. Firstly, system-level stability is considered to be an emerging research issue, especially for large-scale power systems formed by heterogeneous power generation units. Other research directions are the reliability improvement and cyber-physical security of the microgrid. It is envisioned

that future power converters would be smarter and providing many ancillary services to the power grid.

Chapter 2 Decentralized Reactive Power Sharing through Inherent PWM Dead-time Effect

As discussed in Chapter 1, active and reactive powers are expected to be proportionally shared among parallel VSIs according to their respective power ratings. In this chapter, the reactive power sharing will be analyzed and studied. To eliminate the reactive power-sharing error, a dead-time-related control strategy is proposed and its principle will be elaborated. As compared with the existing research approaches, the proposed control strategy can accurately share the reactive power in a fully decentralized manner.

2.1. Introduction

In islanded AC microgrids, DESSs are normally coupled to the grid through VSIs. To improve the VSI operation efficiency and avoid overloading, it is expected that VSIs can share active and reactive power in proportion to their respective power ratings. Although accurate active power sharing can be easily guaranteed by frequency droop control, it is difficult to share the reactive power as desired. The state-of-the-art analysis shows that in order to share the load power is proportional to VSI power ratings, the VSIs should have the same per-unit impedance value [24]. However, this condition can be hardly achieved in practical situations since line impedances are usually mismatched and unknown. Due to this reason, reactive power sharing error inevitably exists.

To improve reactive power sharing accuracy, virtual impedance controls are proposed to compensate for line impedance mismatch through the feedback of VSI output current [62], [63]. The virtual impedance value can either be tuned inversely proportional to the VSI power rating or adaptively regulated according to the delivered reactive power [64], [65]. However, this passive compensation technique requires virtual impedance value to be much larger than line impedances and hence will lead to severe voltage magnitude deviations in weak microgrids. Besides, some other control strategies are also proposed to enhance the reactive power sharing performance without causing significant voltage drops. In [66], [67], the impacts of mismatched grid impedances are ameliorated through measuring the PCC voltage. Nevertheless, PCC voltage information is not available for the VSIs that are distributed far away. In [68], an online slope estimation approach is proposed, and the slope estimated during the grid-connected mode is utilized to adjust the reactive power sharing during the islanded mode. A similar method is also reported in [69], which can effectively enhance the reactive power sharing performance through a pre-estimation of the VSI equivalent impedance. However, such an estimation approach requires prior knowledge of physical line impedances.

Alternatively, communication-based approaches can also be implemented to deal with this issue. In [70]–[72], a microgrid central controller is deployed, which can exchange reactive power information with an individual VSI. To avoid the centralized structure and improve system reliability, distributed consensus control algorithms are developed. In [73]–[74], a secondary distributed averaging term is added to the primary Q-V droop control so that reactive power can be proportionally shared in the steady state. Similarly, a distributed averaging term is also used in [75] to dynamically adjust virtual inductance

values. By doing so, the same control objective can be achieved, as the virtual inductance adjustment is equivalent to the voltage magnitude adjustment [76].

The implementation of the communication-based control strategies can eliminate the power-sharing error and the performance is robust against mismatched grid impedances as well as sensor errors. Despite all these advantages, these control strategies will bring additional costs and may not be available for rural or remote areas. Therefore, it is highly desired that the VSI reactive power information can be globally shared without utilizing any communications. In [77], a small AC harmonic voltage is injected into the VSI voltage, and the frequency of the injected signal is determined by the reactive power value. With this method, reactive power-sharing accuracy is guaranteed at the expense of undesired output current distortions. In [78], the VSI output voltage is controlled via the *Q-V* dot droop control. By linking the reactive power with the derivation of the VSI output voltage magnitude, the reactive power sharing performance can be improved to some extent.

To overcome this issue, this chapter proposes a decentralized reactive power sharing approach through the PWM dead-time effect. The dead-time is an intentionally inserted period, during which both upper and lower switches are turned off. Although the dead-time effect prevents the shoot-through phenomenon, it also brings additional harmonic voltages into the VSI output voltage [79]. For the parallel-VSI system, it is revealed that the dead-time effect may further induce circulating harmonic currents among multiple VSIs [80]. Unlike the previous works that mainly focus on compensating the dead-time effect [81], [82], this chapter utilizes the dead-time effect as feedback to eliminate the fundamental power sharing error. To realize this objective, a supplementary controller is designed and used in conjunction with the conventional voltage droop control. The supplementary controller can automatically equalize the power factors of all VSIs and also eliminate the dead-time induced circulating harmonic currents. It should be noted that the conventional power-sharing schemes that enable accurate reactive power sharing require communications among different VSIs. Although the use of communications facilitates the information exchange, it may not be applicable when VSIs are located far away from each other. Moreover, some other problems also exist, such as stability issues due to communication delays, reliability concerns related to the loss of communications, and vulnerability against cyber attacks. The unique feature of the proposed method is that no communication is required and each VSI can accurately share the reactive power based on local measurements only.

This chapter starts with analyzing the mechanism of inaccurate reactive power sharing. Then, the impact of the dead-time effect and the principle of the proposed controller will be elaborated. Finally, both experimental and simulation results from a typical islanded microgrid prototype will be provided for verification.

2.2. Fundamental Power Sharing

2.2.1. System Configuration

The structure of a typical islanded AC microgrid is illustrated in Fig. 2.1. The system is formed by multiple DESSs, which are coupled to the PCC through grid-interfacing VSIs. To fully utilize the VSI capacities and avoid overloading, the mismatches between power generations (including RESs and diesel generators) and load consumptions should be accurately shared among VSIs based on their respective power ratings. Meanwhile, nonlinear loads also generate additional harmonic currents. To ensure the system power quality, active power filters (APF) have been developed and implemented to compensate for the harmonic currents of nonlinear loads in the literature [83], [84]. Therefore, this chapter only focuses on linear load power sharing.

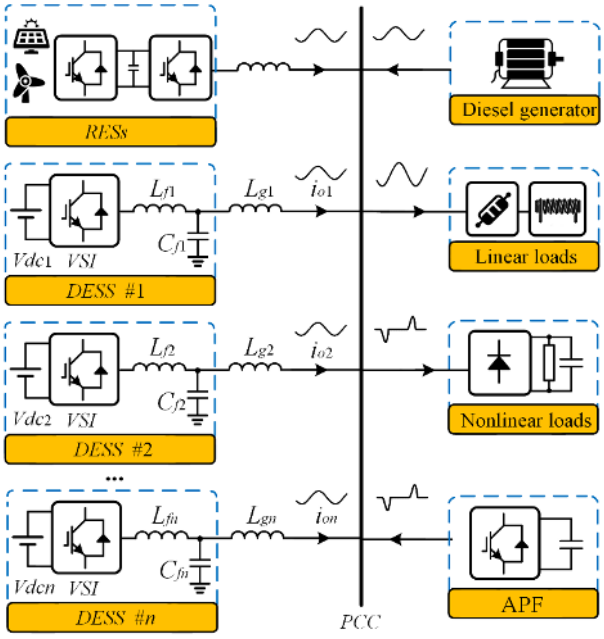


Fig. 2.1. Typical islanded AC microgrid with DESSs.

2.2.2. Droop Control

Conventionally, the power-sharing objective is achieved by the frequency and voltage droop control. The conventional *P-f* and *Q-V* droop controls are given by

$$\omega = \omega_0 - m \cdot P \tag{2.1}$$

$$V = V_0 - n \cdot Q \tag{2.2}$$

where ω_0 and V_0 are the nominal angular speed and voltage magnitude, respectively. P and Q are the measured VSI active and reactive power, respectively. m and n are the droop coefficients. It is worth mentioning that for resistive-impedance cases, Q-f and P-V droop controls will be preferred and the detailed discussions are provided in [20].

The frequency droop control directly links the VSI active power with the frequency. Since all VSIs will reach the same frequency in the steady state, the system active power sharing only depends on the droop coefficient m, i.e.,

$$P_1 \cdot m_1 = P_2 \cdot m_2 = \ldots = P_n \cdot m_n \tag{2.3}$$

However, this principle does not work for reactive power sharing. Fig. 2.2 shows the system equivalent circuit at the fundamental frequency.

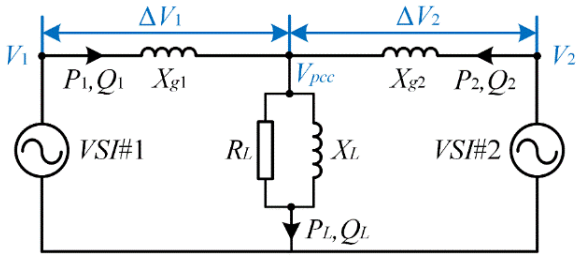


Fig. 2.2. System equivalent circuit at the fundamental frequency.

In Fig. 2.2, VSIs are equivalently modeled as AC voltage sources, and their voltage magnitudes are denoted as V_1 and V_2, respectively. Note that VSI output impedances are not considered in this model since they can be significantly reduced by the well-designed inner-loop voltage controllers. The inner-loop voltage controllers also eliminate voltage tracking errors between the reference voltage and the measured voltage. However, due to voltage sensor scaling errors, the measured VSI output voltages may not reflect the true voltage values. Taking the voltage sensor scaling errors into account, the real VSI voltage magnitudes are expressed as

$$V_1 = \frac{1}{1+\Delta k_1} \cdot (V_0 - n_1 Q_1) \tag{2.4}$$

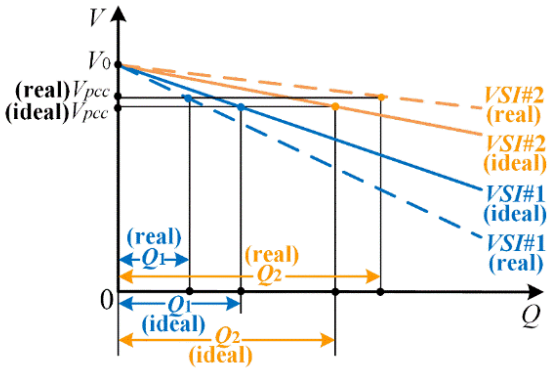
$$V_2 = \frac{1}{1+\Delta k_2} \cdot (V_0 - n_2 Q_2) \tag{2.5}$$

where Δk_1 and Δk_2 are scaling errors of the voltage sensors. The PCC voltage magnitude V_{pcc} can be expressed as

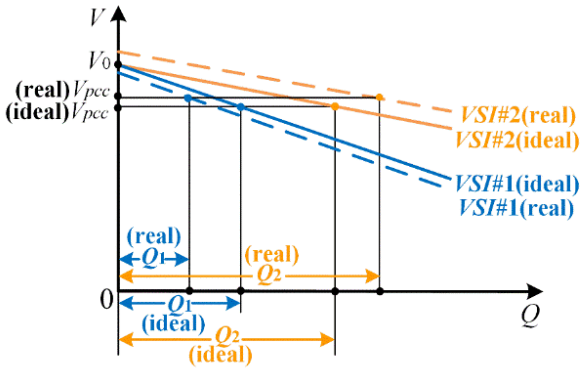
$$V_{pcc} = V_1 - \Delta V_1 = \frac{V_0 - n_1 Q_1}{1 + \Delta k_1} - \frac{2X_{g1}}{V_0} \cdot Q_1 \tag{2.6}$$

$$V_{pcc} = V_2 - \Delta V_2 = \frac{V_0 - n_2 Q_2}{1 + \Delta k_2} - \frac{2X_{g2}}{V_0} \cdot Q_2 \tag{2.7}$$

Fig. 2.3 analyses the reason for inaccurate reactive power sharing. In ideal situations (Δk_1=Δk_2=0, X_{g1}: X_{g2}=n_1:n_2), the reactive power of each VSI is inversely proportional to the droop coefficient n. In Fig. 2.3(a), the impact of mismatched line impedances is considered (X_{g1}: X_{g2}≠n_1:n_2) so that the Q-V curves of the two VSIs have different slopes (denoted by dotted lines). As a consequence, the reactive power sharing result is different from the one under ideal situations. In Fig. 2.3(b), the impact of voltage sensor scaling errors is investigated ($\Delta k_1 \neq \Delta k_2$). Since additional offsets are imposed on the Q-V curves of the two VSIs, the reactive power sharing is also inaccurate. In practical situations, mismatched grid impedances and voltage sensor scaling errors will occur simultaneously, which makes it even more challenging for parallel VSIs to accurately share the reactive power.



(a)



(b)

Fig. 2.3. Analysis of reactive power sharing. (a) Impact of mismatched grid impedances. (b) Impact of sensor scaling errors.

2.3. Analysis of the Dead-time Effect

2.3.1. Dead-time Effect

This section aims to analyze and explore the relationship between the dead-time effect and fundamental power sharing. Fig. 2.4 illustrates the bipolar SPWM, where the modulation wave v_r is compared with the carrier wave u_c to generate the driving signals for switches Q_1-Q_4. In Fig. 2.4, $v_{ac(ideal)}$ represents the ideal AC-side voltage without the dead-time effect. However, the real AC-side voltage v_{ac} is different from $v_{ac(ideal)}$ since the dead-time is introduced between the gate signals to prevent the shoot-through. The waveform of v_{ac} can be plotted by analyzing the current paths during different stages. In specific, during the time interval Δt_1, v_{ac} has a positive voltage polarity since Q_1 and Q_4 conduct. On the contrary, v_{ac} has a negative polarity during the time interval Δt_2 since Q_2 and Q_3 conduct. Within the dead-time interval t_d, none of the four switches conduct, and VSI output current i_{ac} will flow through anti-parallel diodes. Therefore, the AC-side voltage polarity is negative during the time interval Δt_3, and positive during Δt_4.

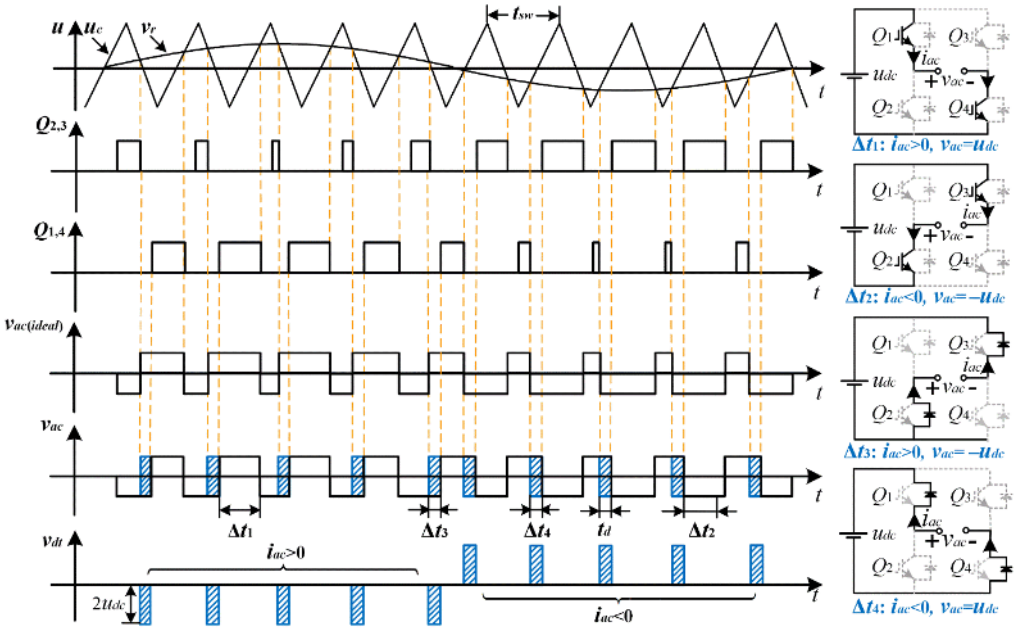
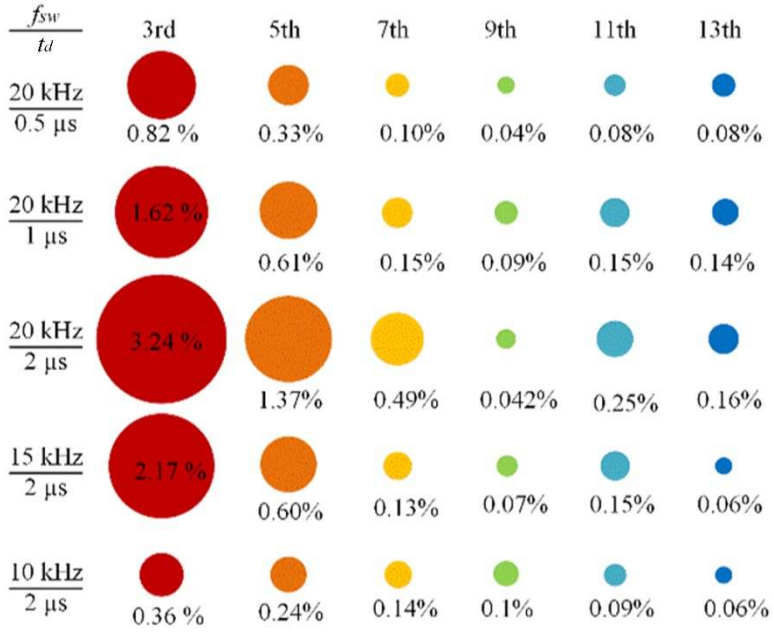


Fig. 2.4. Bipolar SPWM modulation scheme and current paths for an H-bridge VSI.

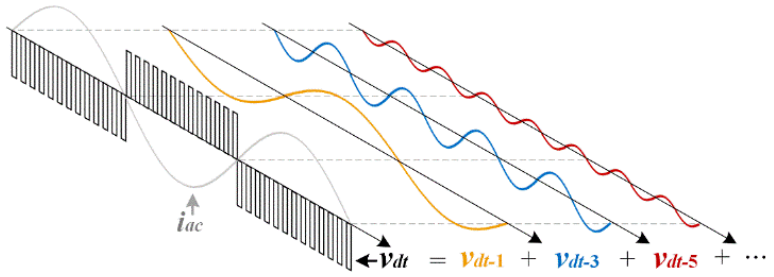
By comparing v_{ac} with $v_{ac(ideal)}$, the dead-time effect equivalently imposes extra voltage pulses v_{dt} on the AC-side voltage, i.e., $v_{dt} = v_{ac} - v_{ac(ideal)}$. According to [76], the hth-order harmonic voltage magnitude of v_{dt} can be calculated and estimated as

$$\left|v_{dt-h}\right| = \frac{8u_{dc}}{h\pi} \cdot \frac{t_d}{t_{sw}} \quad (h = 1,3,5,\ldots) \tag{2.8}$$

where u_{dc} is the DC-input voltage, t_d is the duration of the dead time, and t_{sw} is the switching period. From (2.8), the harmonic voltage magnitude will decrease as the harmonic order goes up. Fig. 2.5(a) and Fig. 2.5(b) respectively provide the magnitude and phase information of the imposed harmonic components. It is observed that the dead-time effect mostly contributes to low-order harmonics. Moreover, the phase of the induced harmonic voltage $v_{dt\text{-}h}$ is determined by the phase of the AC-side output current.



(a)



(b)

Fig. 2.5. Additional harmonics imposed by the dead-time effect. (a). Magnitude information. (b). Phase information.

2.3.2. Control Architecture

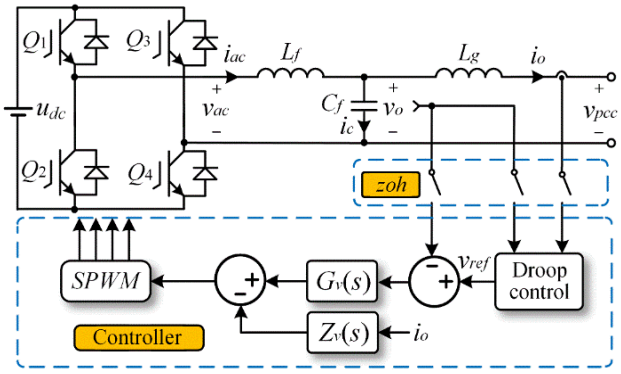
Fig. 2.6 shows a typical circuit and control block diagram of the single-phase VSI. L_f and C_f represent the filter inductor and capacitor, whose impedances are represented by $Z_L(s)$ and $Z_c(s)$. To properly regulate the output voltage, a multi-resonant controller is adopted, and the transfer function $G_v(s)$ is expressed as

$$G_v(s) = k_p + \sum_{h=1,3,5,7...} \frac{k_{ih}\omega_c s}{s^2 + \omega_c s + h^2\omega_0^2} \tag{2.9}$$

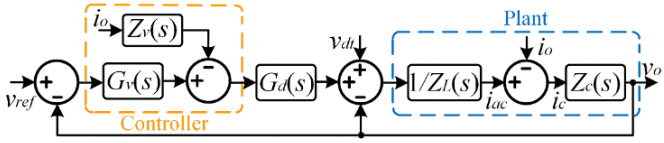
where k_p is the proportional gain and k_{ih} is the resonant gain at the hth-order harmonic frequency, ω_c is the cut-off frequency. The control system delay is represented by $G_d(s)$, which is expressed as

$$G_d(s) = e^{-1.5sT_s} \tag{2.10}$$

where T_s is the sampling period. Moreover, a virtual impedance transfer function $Z_v(s)$ is also implemented to shape the VSI output impedance.



(a)



(b)

Fig. 2.6. Circuit and control block diagram of a single-phase H-bridge VSI. (a) Circuit configuration. (b) Control block diagram.

As shown in Fig. 2.6(b), the dead-time effect is equivalently modeled by an additional disturbance signal v_{dt}, which is directly imposed on the AC-side of the H-bridge inverter. From the control perspective, the model in Fig. 2.6(b) is, in essence, a multi-input single-

output system. By applying Mason's gain formula, the closed-loop voltage transfer function $G_c(s)$ from v_{dt} to v_o can be derived as

$$G_c(s) = \frac{Z_c(s)}{Z_L(s) + Z_c(s) + Z_c(s)G_v(s)G_d(s)} \tag{2.11}$$

where Z_c (s)=1/sC_f is the impedance of filter capacitor, Z_L (s)=sL_f is the impedance of filter inductance. Similarly, the closed-loop transfer function from output current $-i_o$ to output voltage v_o is derived as

$$Z_o(s) = \frac{Z_c(s)Z_L(s) + Z_c(s)G_d(s)Z_v(s)}{Z_L(s) + Z_c(s) + Z_c(s)G_v(s)G_d(s)} \tag{2.12}$$

2.3.3. Impact Analysis

Fig. 2.7 displays the system equivalent circuit at the hth-order harmonic frequency, where the VSIs are modeled in their Thevenin's forms. $i_{o1\text{-}h}$ and $i_{o2\text{-}h}$ are the VSI output harmonic currents; $v_{o1\text{-}h}$ and $v_{o2\text{-}h}$ are VSI output harmonic voltages; $i_{L\text{-}h}$ is the harmonic current of the load impedance Z_L. By properly designing the virtual impedance $Z_v(s)$, the VSI output impedance $Z_o(s)$ can be shaped to be inductive at the harmonic frequency.

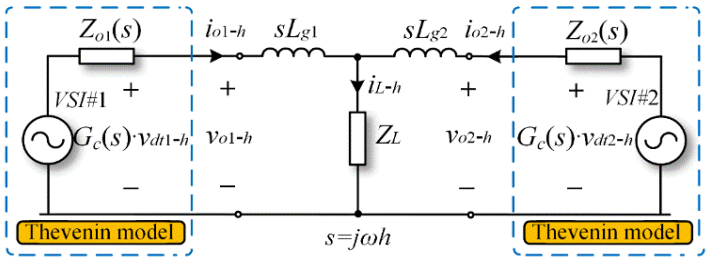


Fig. 2.7. System equivalent model at the hth-order harmonic frequency.

To simplify the analysis, two assumptions have been made:

1.) The harmonic current of Z_L is not considered ($i_{L\text{-}h} \approx 0$). This assumption is valid because Z_L is usually much larger than grid impedances and VSI output impedances.

2.) The influences of grid resistances are neglected, as their harmonic impedance values are much smaller than those of line impedances as well as VSI output impedances, especially at the harmonic frequency.

Based on the above assumptions, Fig. 2.8 shows the phasor diagram of the equivalent model, where $|G_c(j\omega h)|v_{dt1\text{-}h}$ and $|G_c(j\omega h)|v_{dt2\text{-}h}$ denote the dead-time induced harmonic voltages, θ_{12} is the phase angle that $|G_c(j\omega h)|v_{dt1\text{-}h}$ leads $|G_c(j\omega h)|v_{dt2\text{-}h}$.

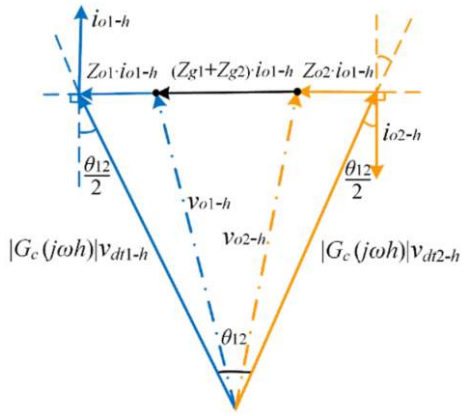


Fig. 2.8. Phasor diagram of the equivalent circuit.

From Fig. 2.7 and Fig. 2.8, the magnitudes of $i_{o1\text{-}h}$ and $i_{o2\text{-}h}$ are calculated as

$$i_{o1-h}=\frac{|G_c(jh\omega)|v_{dt1-h}-|G_c(jh\omega)|v_{dt2-h}}{jh\omega(L_{g1}+L_{g2})+Z_{o1}(jh\omega)+Z_{o2}(jh\omega)} \tag{2.13}$$

$$i_{o2-h}=\frac{|G_c(jh\omega)|v_{dt2-h}-|G_c(jh\omega)|v_{dt1-h}}{jh\omega(L_{g1}+L_{g2})+Z_{o1}(jh\omega)+Z_{o2}(jh\omega)} \tag{2.14}$$

$$|i_{o1-h}|=|i_{o2-h}|=\frac{2|G_c(jh\omega)|\cdot|v_{dt-h}|\cdot\sin\frac{\theta_{12}}{2}}{h\omega\cdot(L_{g1}+L_{g2})+|Z_{o1}(jh\omega)|+|Z_{o2}(jh\omega)|} \tag{2.15}$$

For ease of statement, the nun-fundamental active power, which is the dot product of $v_{oi\text{-}h}$ and $i_{oi\text{-}h}$ is calculated as

$$P_{i-h}=i_{oi-h}\cdot v_{oi-h}=i_{oi-h}\cdot|G_c(jh\omega)|\cdot v_{dti-h} \tag{2.16}$$

From Fig. 2.8, it can be derived that

$$\begin{aligned}P_{1-h}&=|i_{o1-h}|\cdot|v_{dt1-h}|\cdot|G_c(jh\omega)|\cdot\cos\frac{\theta_{12}}{2}\\&=\frac{|G_c(jh\omega)|^2\cdot|v_{dt-h}|^2\cdot\sin\theta_{12}}{h\omega\cdot(L_{g1}+L_{g2})+|Z_{o1}(jh\omega)|+|Z_{o2}(jh\omega)|}\geq 0\end{aligned} \tag{2.17}$$

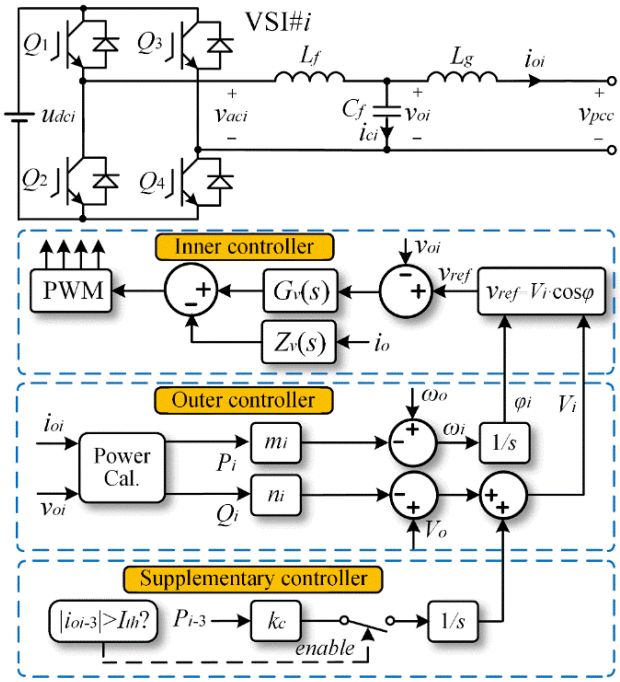
$$\begin{aligned}P_{2-h}&=|i_{o2-h}|\cdot|v_{dt2-h}|\cdot|G_c(jh\omega)|\cdot\cos(\pi-\frac{\theta_{12}}{2})\\&=\frac{-|G_c(jh\omega)|^2\cdot|v_{dt-h}|^2\cdot\sin\theta_{12}}{h\omega\cdot(L_{g1}+L_{g2})+|Z_{o1}(jh\omega)|+|Z_{o2}(jh\omega)|}\leq 0\end{aligned} \tag{2.18}$$

From the above analysis, the VSI with a leading harmonic voltage phasor will yield a positive $P_{i\text{-}h}$ value while the VSI with a lagging harmonic voltage phasor would have a negative $P_{i\text{-}h}$ value. Since the phase of $v_{dt\text{-}h}$ is determined by the phase of VSI output current, the harmonic voltage phase angle difference θ_{12} will be eliminated as long as VSI output currents are exactly in phase with each other, or in other words, VSIs have equalized power factors.

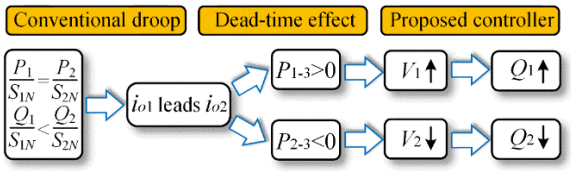
2.4. Proposed Control Strategy

2.4.1. Operating Principle

Fig. 2.9 illustrates the proposed control strategy and its operating principle. In Fig. 2.9(a), a multi-loop architecture is used, including an inner-loop voltage controller, an outer-loop power controller, and the proposed supplementary controller. Among them, the inner-loop controller allows the VSI output voltage to accurately track the reference voltage and the outer-loop controller facilitates decentralized power sharing through the conventional frequency and voltage droop control. To eliminate the reactive power sharing error, a supplementary controller is also implemented to modify the VSI output voltage magnitude V through a simple integral controller, and k_c is the integral gain.



(a)



(b)

Fig. 2.9. Proposed control strategy and its operating principle. (a) Proposed control strategy. (b) Basic operating principle.

The principle of the proposed control strategy is briefly illustrated by the flowchart in Fig. 2.9(b). For simplicity, only two VSIs are considered, and the per-unit active and reactive power are denoted by P_i/S_{iN} and Q_i/S_{iN}, respectively (S_{iN} is the rated power of VSI#i). Originally, the implementation of the conventional droop control can ensure the active power sharing accuracy such that P_1/S_{1N} equals P_2/S_{2N}. However, due to voltage sensor scaling errors and mismatched line impedances, Q_1/S_{1N} is smaller than Q_2/S_{1N}. As a consequence, the output current i_{o1} will lead i_{o2} by some degrees. According to the previous discussions, the dead-time effect will yield positive $P_{i\text{-}h}$ for VSI#1 but negative $P_{i\text{-}h}$ for VSI#2. In this chapter, the 3rd order harmonic component is utilized to calculate $P_{i\text{-}h}$ since it is the most dominant low-order harmonic component. Through the proposed control strategy, the VSI output voltage magnitude V_1 will increase whereas V_2 will decrease. Through this effort, the reactive power sharing error between Q_1/S_{1N} and Q_2/S_{1N} will be gradually reduced, until the two VSIs have the same power factors.

However, even if parallel VSIs have the same power factors, the non-fundamental harmonic power may not be fully eliminated because of the harmonic current $i_{L\text{-}h}$ in Fig. 2.7. Although $i_{L\text{-}h}$ is very small, the internal controller k_c/s will work continuously and lead to large voltage magnitude deviations in the longer term. To avoid this problem, the integral controller in Fig. 2.9(a) is enabled only if the VSI harmonic current magnitude is larger than pre-defined a small threshold value I_{th}, which is determined as

$$I_{th} = |v_{dti-3}| \cdot \frac{2S_i}{V_0^2} \tag{2.19}$$

where $|v_{dti\text{-}3}|$ can be calculated by (2.8), and S_i is the apparent output power of VSI#i. The impact of the threshold value on the reactive power sharing accuracy is negligible, as will be verified by the simulation and experimental results in the later section.

2.4.2. Control Parameter Design

As previously discussed, a multi-resonant controller $G_v(s)$ is adopted to regulate the VSI output voltage. Since only 3rd-order harmonic voltages are utilized for the reactive power sharing, resonant gains k_{i5}, k_{i7}, and k_{i9}… can be tuned large enough to effectively mitigate higher-order harmonic distortions. However, if k_{i3} is too large, the 3rd-order harmonic voltage will be significantly attenuated, which makes the 3rd-order harmonic power difficult to be measured precisely. On the other hand, if k_{i3} is too small, the VSI output voltage may contain considerable 3rd-order harmonic distortions. Therefore, the value of k_{i3} should be properly designed such that the voltage quality and the harmonic

power measurement accuracy are well balanced. The VSI 3rd-order harmonic voltage magnitude can be estimated as

$$|v_{oi-3}| = |v_{dt-3}| \cdot |G_c(j3\omega_0)| \tag{2.20}$$

$$|v_{oi-3}| = \frac{8u_{dc}t_d}{h\pi t_{sw}} \cdot |G_c(j3\omega_0)| \tag{2.21}$$

To comply with the IEEE power quality standard, the 3rd-order harmonic voltage distortion needs to be kept smaller than 3% of the fundamental voltage, i.e.,

$$|v_{oi-3}| < 3\% \cdot V_0 \tag{2.22}$$

where V_0 is the fundamental voltage magnitude. Therefore, the resonant gain k_{i3} should be properly designed to satisfy this condition.

Next, the design of integral control gain k_c will be discussed. For ease of analysis, the inner voltage controller is not considered since its dynamic is much faster than that of the outer power controller. Based on this assumption, the VSI output reactive power is calculated as

$$Q_i = \frac{V_0(V_i - V_{pcc})}{2X_{gi}} \quad (i=1,2) \tag{2.23}$$

where V_i and V_{pcc} are voltage magnitudes for VSI#i and the PCC. The system reactive power balance ensures that

$$\sum_{i=1,2} Q_i = Q_L \tag{2.24}$$

where Q_L is the total reactive power generated by the load. Combining (2.23) and (2.24) yields

$$V_2 - V_1 = \frac{2(X_{g1} + X_{g2})}{V_0} \cdot Q_2 - \frac{2X_{g1}}{V_0} \cdot Q_L \tag{2.25}$$

With the proposed control strategy, the voltage magnitude of VSI is expressed as

$$V_i = V_0 - n_i Q_i + \frac{k_c}{s} \cdot \frac{P_{i-3}}{1+s\tau} \quad (i=1,2) \tag{2.26}$$

Note that a first-order transfer function $1/(1+\tau s)$ is included in (2.26) to equivalently represent the time delay caused by the harmonic power calculation. From (2.26), the VSI voltage magnitude difference is calculated as

$$V_2 - V_1 = n_1 Q_1 - n_2 Q_2 + \frac{k_c}{s} \cdot \frac{P_{2-3} - P_{1-3}}{1+\tau s} \tag{2.27}$$

$$V_2 - V_1 = n_1(Q_L - Q_2) - n_2 Q_2 + \frac{k_c}{s} \cdot \frac{2P_{2-3}}{1+\tau s} \tag{2.28}$$

Substituting (2.28) into (2.25) yields:

$$\dot{Q}_2 + \tau \ddot{Q}_2 = \frac{k_c V_0}{n_1 V_0 + n_2 V_0 + 2X_{g1} + 2X_{g2}} \cdot 2P_{2-3} \tag{2.39}$$

From (2.16), the harmonic power of VSI#2 is calculated as

$$P_{2-3} = \frac{\left|G_c(j3\omega)\right|^2 \cdot \left|v_{dt-3}\right|^2 \cdot \sin\left(3\arctan\frac{Q_L - Q_2}{P_1} - 3\arctan\frac{Q_2}{P_2}\right)}{3\omega \cdot (L_{g1} + L_{g2}) + \left|Z_{o1}(j3\omega)\right| + \left|Z_{o2}(j3\omega)\right|} \tag{2.30}$$

In (2.30), the VSI active power P_1 and P_2 are shared according to the frequency-droop coefficients m_1 and m_2. According to the above differential equation, the reactive power allocation model can be established by regarding Q_2 as the state variable. However, since trigonometric functions are involved in the equations, the system becomes nonlinear and cannot be analyzed by conventional small-signal modeling approaches. As an alternative, the phase portrait analysis is adopted in this chapter following the steps in [85]. Fig. 2.10 displays the phase portraits after implementing the proposed control strategy, where the system initial state is determined by the parameters listed in Table 2.1.

In Fig. 2.10, the reactive power Q_2 will reach the equilibrium point (50%·Q_L=117 var) so that the reactive power sharing error is eliminated. It can be found out that the value of the integral gain k_c will influence the system dynamic performance. When k_c is larger than 0.4, the VSI reactive power will oscillate since the derivation of Q_2 is sometimes positive and sometimes negative. To avoid the undesired reactive power oscillations, the integral gain k_c is selected as 0.2 in this chapter, and the corresponding phase portrait is shown by the red solid line in Fig. 2.10.

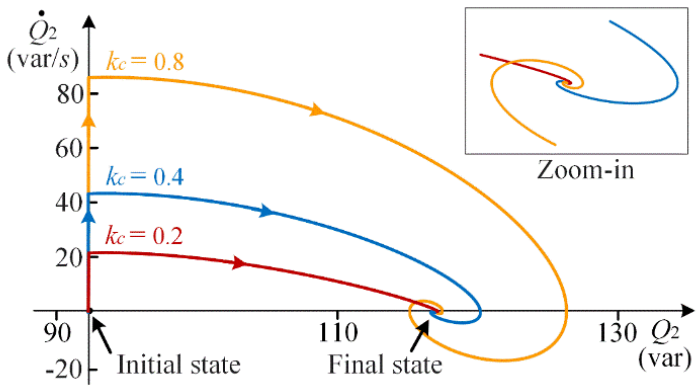


Fig. 2.10. Phase portraits of the reactive power after the implementation of the proposed control strategy.

Table 2.1 Parameters for the system initial state

Parameters	Descriptions	Values
V_0	AC voltage magnitude	100 V
u_{dc}	DC-input voltage	140 V
X_{g1}	line inductance	0.20 Ω
X_{g2}	line inductance	0.31Ω
m_1, m_2	Droop coefficient	5×10^{-4} rad/(s·W)
n_1, n_2	Droop coefficient	5×10^{-4} V/Var
P_L	Resistive load	185 W
Q_L	Reactive load	233 Var
f_{sw}	Switching frequency	20 kHz
t_d	Dead-time	1 μs
τ	Time delay constant	0.3 s

2.5. Verifications

2.5.1. Simulation Results

To prove the theoretical findings discussed above, the simulation studies were carried out under the Piecewise Linear Electrical Circuit Simulation (PLECS) environment with the parameters listed in Table 2.1.

A. Power Sharing among Two Parallel VSIs

In the first scenario, two parallel VSIs with equal power ratings are studied, and the system active and reactive powers are expected to be equally shared among them. In the simulation, line impedances for VSI#1 and VSI#2 are 0.65 mH and 1.05 mH. The active power, reactive power, and values of $P_{i\text{-}3}$ are shown in Fig. 2.11. Note that the proposed control scheme is enabled at t_1.

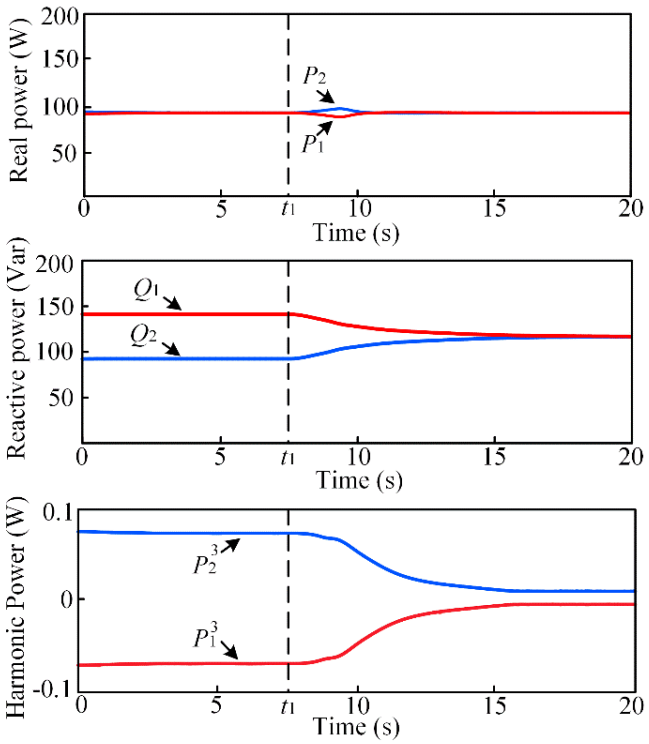


Fig. 2.11. Power-sharing results for two parallel VSIs.

B. Plug-and-play Capability

Next, the plug-and-play capability has been verified. Fig. 2.12 shows the simulation result. In the simulation, a new VSI, i.e., VSI#3, is connected to the islanded microgrid at t_1. To prevent current overshoots, a pre-synchronization procedure is implemented to reduce the phase differences between VSI#3 and the rest VSIs before t_1. As illustrated in Fig. 2.12, the fundamental active and reactive power can be accurately shared among VSIs in the steady state.

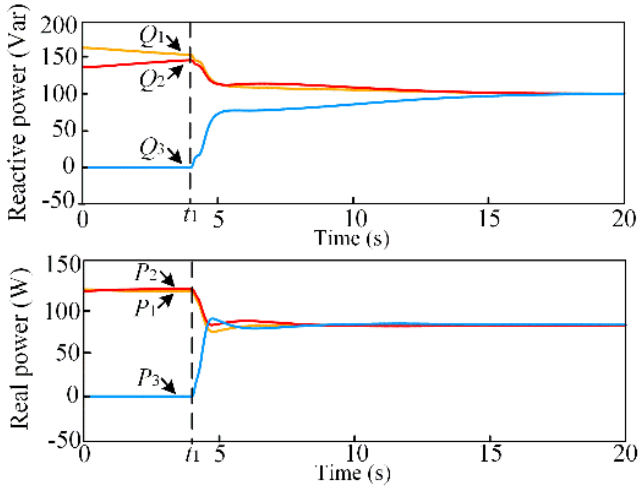


Fig. 2.12. Power-sharing performance when a new VSI is added to the microgrid.

2.5.2. Experimental Results

A prototype was also built in the laboratory to experimentally verify the proposed control strategy. Fig. 2.13 shows the whole system setup, where multiple VSIs were connected in parallel through emulated line impedances. Apart from mismatched grid impedances, voltage sensor scaling errors also exist and degrade the reactive power sharing performance. The overall samplings and controls were processed by a PLECS RT-Box, and the parameters for experiments remain the same as those for simulations. Five different cases were tested, and the corresponding experimental results are provided below.

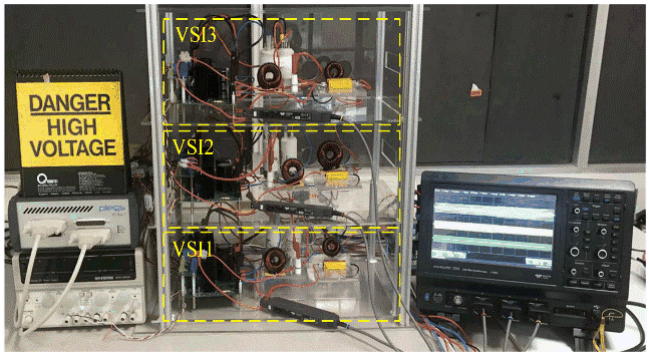


Fig. 2.13. Laboratory setup for experimental verification.

A. Equal Load Power Sharing

In the first case, the two VSIs have the same power ratings, and the load power is expected to be equally shared. Fig. 2.14 shows the VSI output current waveforms without the proposed control scheme. Due to the grid impedance mismatch and voltage sensor errors, i_{o2} leads i_{o1} by some degrees. As a result, the dead-time effect brings extra 3rd-order circulating harmonic currents so that i_{o1} and i_{o2} are distorted.

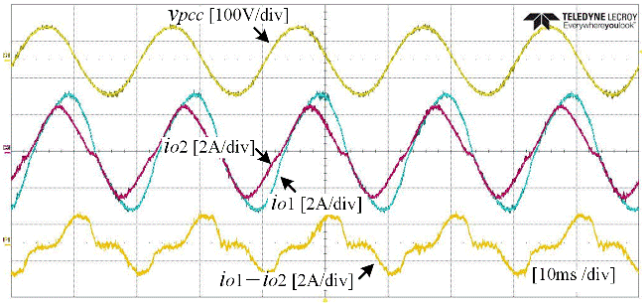


Fig. 2.14. VSI output currents without the proposed control scheme.

Then, the proposed control scheme is enabled at t_1. Fig. 2.15 shows the dynamic response of the VSI fundamental powers, Fig. 2.16 shows the dynamic response of the

$P_{i\text{-}3}$ and Fig. 2.17 shows the steady-state VSI output currents. It is clear that the proposed control scheme not only enhances the reactive power sharing accuracy but also reduces circulating harmonic currents caused by the dead-time effect. Besides, the PCC voltage contains less harmonic distortions (THD=1.6%).

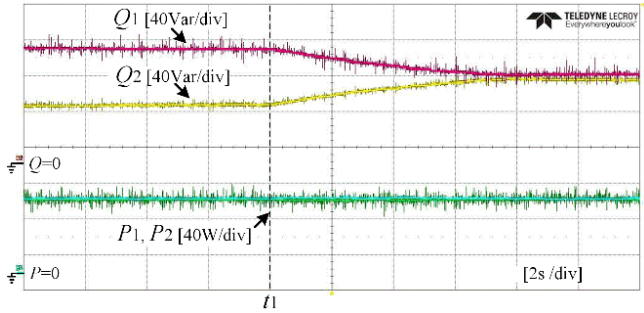


Fig. 2.15. Dynamic response of the VSI output fundamental powers.

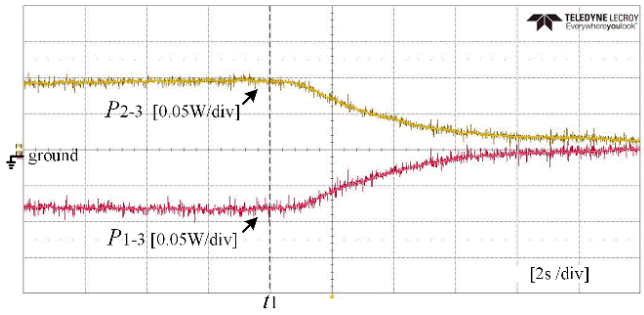


Fig. 2.16. Dynamic responses of $P_{i\text{-}3}$.

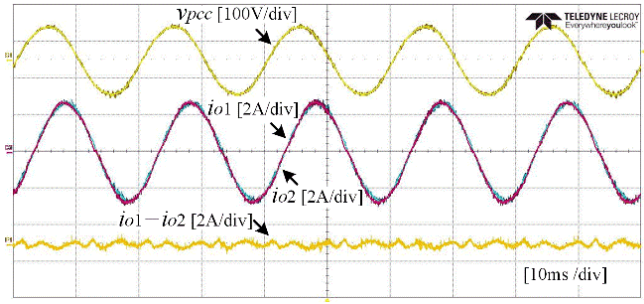


Fig. 2.17. VSI output currents with the proposed control scheme.

B. Proportional Load Power Sharing

In the second case, the power rating of VSI#1 is twice as much as that of VSI#2. Fig. 2.18 and Fig. 2.19 shows the VSI output currents without and with the proposed control strategy, respectively. It is observed that the proposed control scheme can accurately share the reactive power as the desired ratio 2:1.

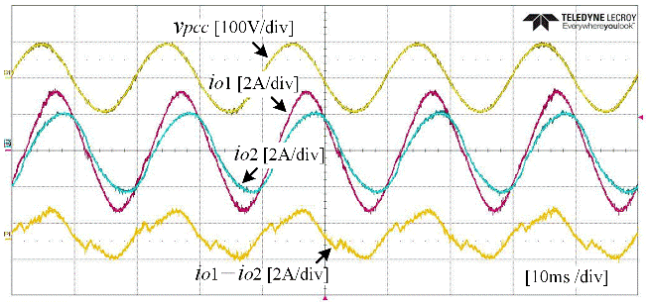


Fig. 2.18. VSI output currents without the proposed control scheme.

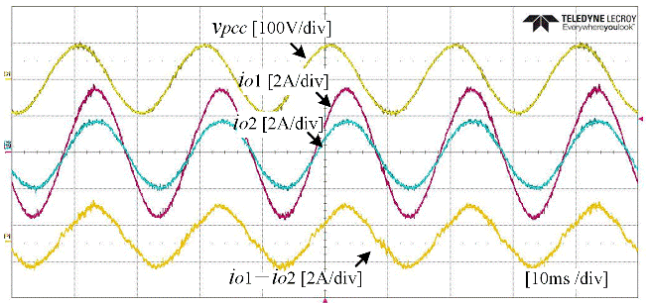


Fig. 2.19. VSI output currents with the proposed control scheme.

C. Power Sharing among Multiple VSIs.

Finally, the experimental verification for multiple parallel VSIs is provided. Fig. 2 20 shows the VSI output currents without the proposed control scheme, while Fig. 2.21 shows the VSI output currents with the proposed control scheme. It can be seen that the proposed control scheme can also be applied to enhance the reactive power sharing for n ($n > 2$) VSI units.

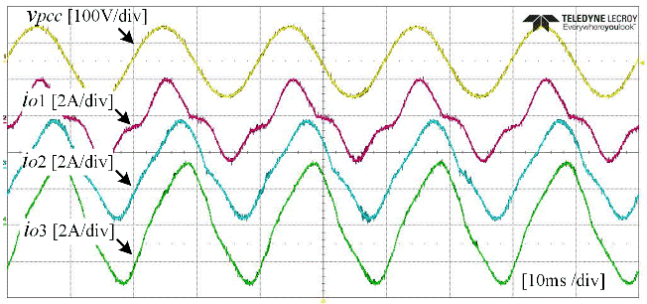


Fig. 2.20. VSI output currents without the proposed control scheme.

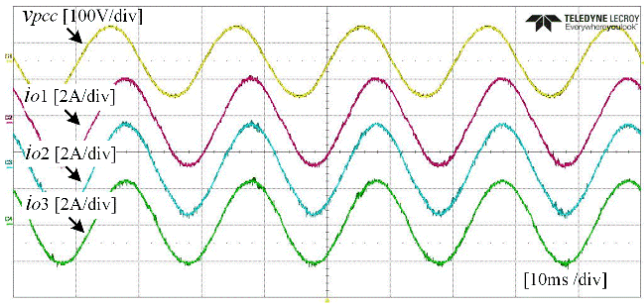


Fig. 2.21. VSI output currents with the proposed control scheme.

2.6. Summary

In this chapter, a decentralized control algorithm is proposed to accurately share the reactive power sharing among multiple VSIs. As the control scheme only requires the local information, communication infrastructure and time-delays can be avoided. A supplementary controller is designed and used in conjunction with the conventional droop control to adjust the reactive power output for better power sharing. By doing so, accurate reactive power sharing among multiple VSIs is achieved wirelessly.

Chapter 3 Robust Power Sharing Control for Parallel Three-phase Inverters Against Voltage Measurement Errors

In the previous chapter, it is revealed that voltage measurement errors will deteriorate the power-sharing performance. The associated consequences will be severer in a three-phase system due to the potential unbalance issue. This chapter further points out that even small voltage measurement errors may inject both positive- and negative-sequence circulating currents among parallel three-phase VSIs. An explicit analysis will be carried out. On this basis, a hybrid feedback and feedforward impedance shaping control is proposed and makes the power-sharing performance robust against voltage measurement errors. The experimental results show that the proposed method can reduce the power-sharing error to be less than 10% in the presence of 2% voltage sensor scaling errors while maintaining the voltage THD less than 3%.

3.1. Introduction

To facilitate the power sharing among VSIs, the well-known droop control and virtual synchronous generator controls are proposed in the literature [86], [87]. These methods achieve decentralized power sharing by linking VSI frequency and voltage magnitude with the active and reactive power, respectively. Despite the accurate active power sharing, it is found that the reactive, unbalanced, and harmonic power sharing accuracy cannot be ensured due to mismatched line impedances [43]. In view of this challenge, a straightforward solution is to compensate for the line impedance mismatch by reshaping VSI impedances at the fundamental and harmonic frequencies. To realize this objective, virtual impedance controls are developed and widely implemented in the literature [62], [88]. By feeding the VSI output current to its reference voltage through an impedance transfer function, the line impedance can be equivalently modified without requiring passive components. The successful implementation of a virtual impedance requires the voltage-feedback control to accurately track the measured voltages with the reference voltages. Accordingly, many high-performance voltage controllers, including repetitive controllers [89], resonant controllers in the stationary $\alpha\beta$ frame [90], and proportional-integral controllers under the synchronous dq frame [91], are employed to eliminate the voltage tracking errors.

However, most of the existing works assume that voltage measurements are accurate. This ideal assumption may not hold in practical scenarios since DC offsets and scaling errors inevitably exist due to thermal drifts and imperfect calibrations. Previously, the measurement error impacts have already been investigated for motor drive systems [92] and grid-connected DC/AC converters [93], [94]. Moreover, some active compensation schemes are also developed to estimate the measurement errors from the DC-link voltage ripple [95], to suppress the DC current injection [96], and also to reduce the unbalanced currents caused by scaling errors [97]. Yet, when it comes to microgrids with multiple parallel VSIs, sensor measurement errors exist for each VSI and are therefore more difficult to be compensated. It is revealed in this chapter that even small voltage sensor scaling errors may lead to large positive- and negative-sequence circulating currents among VSIs. Notice that a similar phenomenon was also observed in [96], whereas the underlying cause was not explicitly analyzed. To clearly explain the mechanism, a quantitative analysis is performed for parallel VSIs. It is found out that voltage scaling errors will be reflected in the real VSI output voltages, given that the voltage-feedback control is well designed with excellent tracking ability. In this case, extra fundamental

positive- and negative-sequence voltages are introduced for individual VSI. Since line impedances have little blocking effect at the fundamental frequency, the introduced voltages, though small in magnitudes, can still generate considerable circulating currents among VSIs. Therefore, reactive and unbalanced power sharing is degraded.

Though this problem may be addressed by the communication-based power-sharing approaches [97], many other issues will arise accordingly, such as the increased cost and infrastructure requirements, degraded reliability due to the communication link failure, compromised system stability caused by delays, and vulnerability against cyber-attacks. Instead, large virtual impedances can be synthesized with the attempt to block such circulating currents, whereas the point of common coupling (PCC) voltage quality will be compromised [98].

Fortunately, the feedforward impedance control, also known as the inner virtual impedance [99], provides another possibility for the impedance reshaping. The unique feature of feedforward control makes it easy to shape the VSI impedance by directly feeding the output current to the PWM modulator. As the voltage-feedback control does not need to have high open-loop gains, the negative influences of voltage measurement errors can be mitigated. However, as also pointed out in [63], the digital system delay will influence the impedance shaping accuracy at higher frequencies. Hence, the harmonic power sharing will be deteriorated. In some worst cases, the VSI impedance may even have a negative real part and threaten the system stability. Though a delay compensation scheme is used in [100], it requires too many current decomposition and phase compensation blocks, which significantly increases the computation burden of a digital controller.

To address the above technical issues, this chapter proposes a hybrid control scheme for power sharing, which simultaneously avoids the respective limitations of feedback and feedforward controls. Specifically, the reactive and unbalanced power sharing are guaranteed by the feedforward-based impedance control and therefore become robust against voltage measurement errors. Meanwhile, harmonic power sharing is ensured by the feedback-based impedance shaping control and immune from the control delay. This hybrid control architecture can effectively mitigate the negative impacts of measurement errors and improve the power sharing in a fully decentralized manner.

This chapter starts with a brief introduction to VSI control scheme and the impact of voltage measurement error. Then, the proposed control strategy and control parameter design guidelines will be elaborated. Finally, both simulation and hardware experimental

results are provided to verify the theoretical findings and the feasibility of the proposed method.

3.2. Problem Formulation

3.2.1. Circuit and Control Block Diagrams

Fig. 3.1 illustrates the typical circuit and control diagram of a droop-controlled VSI, where L_f and C_f are filter inductor and capacitor; L_g and R_g denote the grid impedance; $i_{abc\text{-}m}$ and $v_{abc\text{-}m}$ are the measured VSI output currents and voltages. The entire VSI control scheme contains a power-loop control as well as a voltage-feedback control.

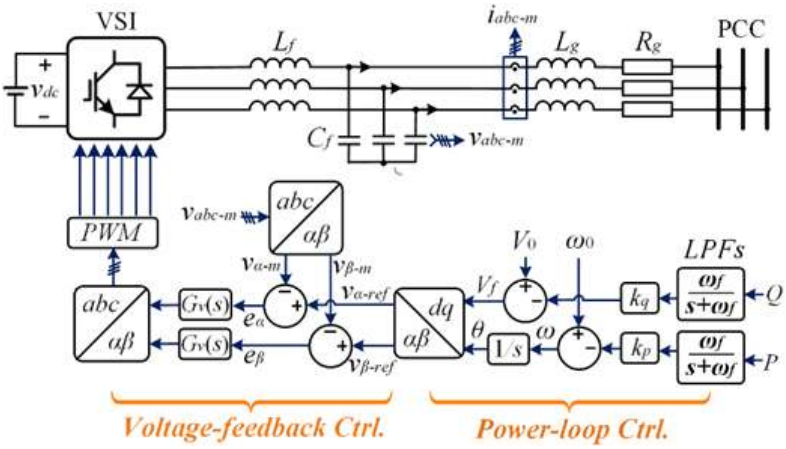


Fig. 3.1. Circuit configuration of the conventional VSI control scheme.

The power-loop control is adopted to facilitate the active and reactive power sharing through the well-known droop equations:

$$\omega = \omega_0 - m \cdot \frac{\omega_f}{s + \omega_f} \cdot P \tag{3.1}$$

$$V = V_0 - n \cdot \frac{\omega_f}{s + \omega_f} \cdot Q \tag{3.2}$$

where V and ω are the VSI voltage magnitude and frequency; V_0 and ω_0 are the nominal voltage magnitude and frequency; m and n are droop coefficients; P and Q are the real and reactive power; ω_f is the cut-off frequency of low-pass filters, which are utilized to attenuate power ripples and provide the equivalent inertia support. As shown in Fig. 3.1, the reference voltages are generated via the $dq/\alpha\beta$ transformation, with the d-axis voltage equaling V and the q-axis voltage being zero. In addition, the transformation phase angle θ is obtained as the integration of ω.

3.2.2. Measurement Errors

To eliminate the $\alpha\beta$-frame voltage tracking errors e_α and e_β, the resonant controller is usually adopted for the voltage controller $G_v(s)$. It should be noted that a similar effect can also be achieved by PI controllers under the synchronous dq frame.

Given that the VSI reference voltages are well-balanced, i.e.:

$$\begin{cases} v_{a-ref}(t) = V\cos(\omega t + \theta_0) \\ v_{b-ref}(t) = V\cos(\omega t + \theta_0 - 2\pi/3) \\ v_{c-ref}(t) = V\cos(\omega t + \theta_0 + 2\pi/3) \end{cases} \tag{3.3}$$

where θ_0 is the initial phase angle. Through the abc-$\alpha\beta$ transformation, the stationary-frame reference voltages are derived as

$$\begin{cases} v_{\alpha-ref}(t) = V\cos(\omega t + \theta_0) \\ v_{\beta-ref}(t) = V\sin(\omega t + \theta_0) \end{cases} \tag{3.4}$$

Taking the voltage sensor errors into account, the measured VSI output voltages are expressed as

$$\begin{cases} v_{a-m}(t) = v_a(t)\cdot(1+\Delta k_a) + X_{a-dc} \\ v_{b-m}(t) = v_b(t)\cdot(1+\Delta k_b) + X_{b-dc} \\ v_{c-m}(t) = v_c(t)\cdot(1+\Delta k_c) + X_{c-dc} \end{cases} \tag{3.5}$$

where Δk_a, Δk_b, and Δk_c are scaling errors; $X_{a\text{-}dc}$, $X_{b\text{-}dc}$, and $X_{c\text{-}dc}$ are DC offsets; $v_a(t)$, $v_b(t)$, and $v_c(t)$ are the real VSI output voltages, whereas $v_{a\text{-}m}(t)$, $v_{b\text{-}m}(t)$, and $v_{c\text{-}m}(t)$ are the measured VSI output voltages. Supposing that $G_v(s)$ can block DC offsets and accurately track the fundamental voltages in the $\alpha\beta$ frame, it is clear that

$$\begin{cases} v_{\alpha-m}(j\omega) = v_{\alpha-ref}(j\omega) \\ v_{\beta-m}(j\omega) = v_{\beta-ref}(j\omega) \end{cases} \tag{3.6}$$

Besides, as there is no zero-sequence voltage in the system, the sum of three-phase voltages equals zero.

$$v_a(t) + v_b(t) + v_c(t) = 0 \tag{3.7}$$

Based on (3.4)–(3.7), the real VSI output voltages are calculated and expressed as

$$v_a(t) = \frac{2+\Delta k_b+\Delta k_c}{\sqrt{3}M}\cdot V\cos(\omega t+\theta_0) + \frac{\Delta k_b-\Delta k_c}{3M}\cdot V\sin(\omega t+\theta_0) \tag{3.8}$$

$$v_b(t) = \frac{1+\Delta k_c}{-\sqrt{3}M}\cdot V\cos(\omega t+\theta_0) + \frac{3+2\Delta k_a+\Delta k_c}{3M}\cdot V\sin(\omega t+\theta_0) \tag{3.9}$$

$$v_c(t) = \frac{1+\Delta k_b}{-\sqrt{3}M}\cdot V\cos(\omega t+\theta_0) - \frac{3+2\Delta k_a+\Delta k_b}{3M}\cdot V\sin(\omega t+\theta_0) \tag{3.10}$$

where,

$$M = \frac{2\sqrt{3}}{3} + \frac{4\sqrt{3}}{9}(\Delta k_a + \Delta k_b + \Delta k_c) + \frac{2\sqrt{3}}{9}(\Delta k_a \Delta k_b + \Delta k_b \Delta k_c + \Delta k_c \Delta k_a) \tag{3.11}$$

Based on the method of symmetrical components, the real VSI output voltages can be expressed as the sum of balanced positive- and negative-sequence three-phase voltages, i.e.,

$$\begin{cases} v_a(t) = V_p \cos(\omega t + \varphi_P) + V_N \cos(\omega t + \varphi_N) \\ v_b(t) = V_p \cos(\omega t + \varphi_P - \frac{2\pi}{3}) + V_N \cos(\omega t + \varphi_N + \frac{2\pi}{3}) \\ v_c(t) = V_p \cos(\omega t + \varphi_P + \frac{2\pi}{3}) + V_N \cos(\omega t + \varphi_N - \frac{2\pi}{3}) \end{cases} \tag{3.12}$$

where V_P and V_N represent the positive- and negative-sequence voltage magnitudes; φ_P and φ_N are the associated phase angles. Their values are calculated as

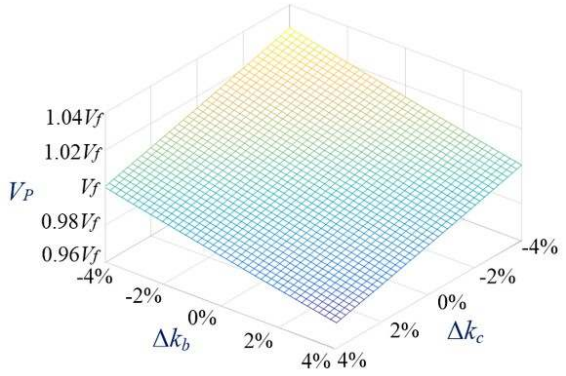
$$V_P = \frac{6 + 2(\Delta k_a + \Delta k_b + \Delta k_c)}{3\sqrt{3}M} \cdot V \tag{3.13}$$

$$V_N = \frac{2V_f \sqrt{\Delta k_a^2 + \Delta k_b^2 + \Delta k_c^2 - \Delta k_a \Delta k_b - \Delta k_c \Delta k_b - \Delta k_a \Delta k_c}}{3\sqrt{3}M} \tag{3.14}$$

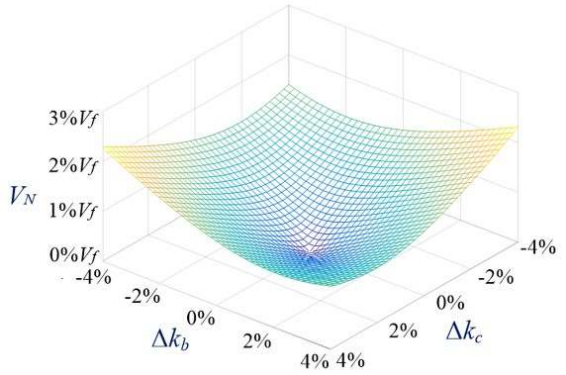
$$\varphi_P = \theta_0 \tag{3.15}$$

$$\varphi_N = \theta_0 - \arctan\frac{\sqrt{3}\Delta k_b - \sqrt{3}\Delta k_c}{\Delta k_b + \Delta k_c - 2\Delta k_a} \tag{3.16}$$

From (3.13) and (3.14), the existence of scaling errors Δk_a, Δk_b, and Δk_c will differ V_p from V_f and make V_N nonzero. To quantify the effect of voltage measurement errors, Fig. 3.2 shows the values of V_p and V_N with varying scaling errors. (for the ease of plotting, Δk_a is set as zero on purpose). As suggested by Fig. 3.2, voltage measurement errors can equivalently impose additional positive- and negative-sequence voltages for the VSI. Notice that the imposed voltages are mainly fundamental components since harmonic voltage magnitudes are small enough (much less than V_f) to be neglected.



(a)

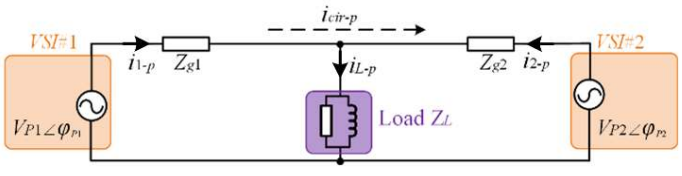


(b)

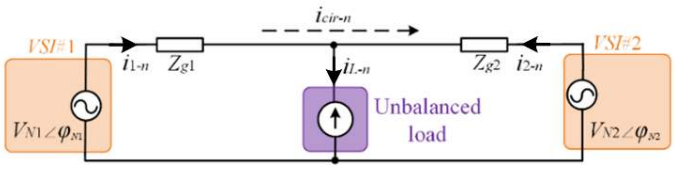
Fig. 3.2. Impacts of scaling errors Δk_b and Δk_c. (a) Value of V_p. (b) Value of V_N.

3.2.3. System Model

Fig. 3.3 shows the system equivalent circuit with voltage measurement errors, where every VSI is modeled in Thevenin's circuit form. Apart from voltage measurement errors, the unevenly distributed single-phase loads will also cause the voltage unbalance. They can be modeled by a lumped negative-sequence current source, as illustrated in Fig. 3.3(b). Note that the locations of unbalanced loads would influence the equivalent impedances Z_{g1} and Z_{g2} and consequently affect the unbalanced power sharing between parallel VSIs.



(a)



(b)

Fig. 3.3. Equivalent circuits of parallel VSIs with voltage measurement errors. (a) positive-sequence domain. (b) negative-sequence domain.

Because of voltage measurement errors, extra positive-sequence circulating current $i_{cir\text{-}p}$ and negative-sequence circulating current $i_{cir\text{-}n}$ will occur and can be expressed as

$$i_{cir-p} = \frac{V_1\angle\varphi_{P1} - V_2\angle\varphi_{P2}}{Z_{g1} + Z_{g2}} \tag{3.17}$$

$$i_{cir-n} = \frac{V_{N1}\angle\varphi_{N1} - V_{N2}\angle\varphi_{N2}}{Z_{g1} + Z_{g2}} \tag{3.18}$$

where Z_{g1} and Z_{g2} are grid impedances. In the steady state, the P-ω droop control will achieve the phase synchronization between VSIs such that φ_{P1} is close to φ_{P2}. The difference between V_{P1} andV_{P2} directly affects the reactive power sharing. Besides, the imposed negative-sequence voltages are mismatched both in phases and magnitudes. Consequently, the unbalanced power-sharing performance will also be deteriorated.

It is known that mismatched line impedances are responsible for inaccurate reactive and unbalance power sharing. To compensate for the line impedance mismatches, VSI output impedances are usually reshaped through the virtual impedance control. However, the above analysis implies that voltage sensor measurement errors may deteriorate the fundamental power-sharing performance. Moreover, such negative impacts can hardly be avoided if $G_v(s)$ is designed to have excellent tracking ability at the fundamental frequency.

3.3. Proposed Control Strategy

To mitigate the impacts of voltage measurement errors and enhance the power-sharing performance, a decentralized control scheme is developed in this chapter.

3.3.1. Control Strategy

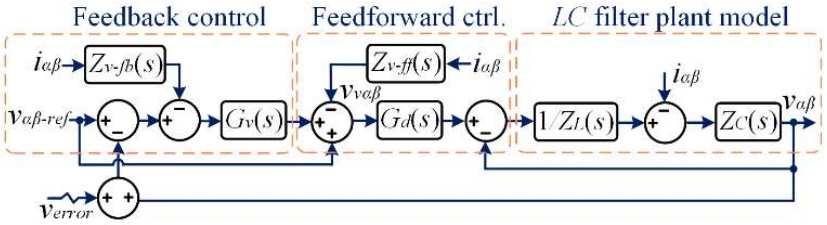
Fig. 3.4(a) illustrates the circuit and control block diagram, where $i_{\alpha\beta}$ and $v_{\alpha\beta}$ are the stationary-frame VSI output currents /voltages. v_{error} represents the voltage measurement

error. $Z_{v\text{-}fb}(s)$ and $Z_{v\text{-}ff}(s)$ are feedback-based and feedforward-based impedance transfer function, respectively. $G_d(s)$ is the control system delay, which equals to

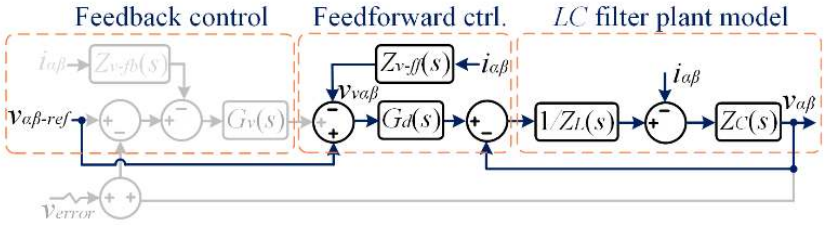
$$G_d(s) = e^{-1.5sT_s} \tag{3.19}$$

where T_s is the sampling frequency. Moreover, LC filter impedances $Z_L(s)$ and $Z_C(s)$ are respectively expressed as

$$Z_L(s) = sL_f + r, \quad Z_C(s) = \frac{1}{sC_f} \tag{3.20}$$



(a)



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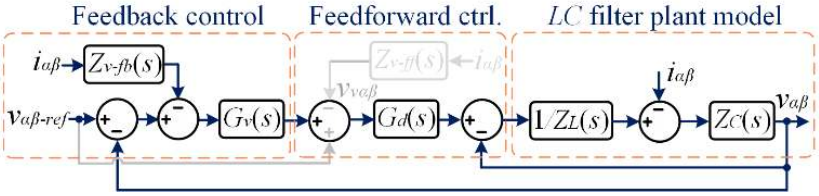


(c)

Fig. 3.4. Block diagram of the proposed control strategy. (a) Overall control architecture. (b). For the fundamental frequency. (c) For harmonic frequencies.

where r is the inductor equivalent series resistance (ESR). The voltage controller $G_v(s)$ is designed as

$$G_v(s) = \sum_{h=5,7,11,13} \frac{k_{ih} \cdot s}{s^2 + h^2 \omega_0^2} \tag{3.21}$$

where k_{ih} is the resonant gain for the hth-order harmonic. It is clear that $G_v(s)$ has very large gains at harmonic frequencies but a very small gain at the fundamental frequency, i.e.,

$$\left|G_v(j\omega_0)\right| = \sum_{h=5,7,11,13} \frac{k_{ih}}{(h^2-1)\cdot\omega_0} << 1 \tag{3.22}$$

Besides, $G_v(s)$ has a zero gain for the DC component, i.e.,

$$\left|G_v(j0)\right| = \sum_{h=5,7,11,13} \frac{k_{ih}\cdot 0}{0^2 + h^2\omega_0^2} = 0 \tag{3.23}$$

Equations (3.22) and (3.23) suggest that $G_v(s)$ will effectively block the fundamental and DC voltage components. Based on Mason's gain formula, the VSI output impedance is derived according to Fig. 3.4(a).

$$Z_o(s) = \frac{v_{\alpha\beta}}{-i_{\alpha\beta}} = \frac{Z_L(s) + Z_{v-ff}(s)G_d(s)}{Z_L(s)Z_C^{-1}(s) + 1 + G_v(s)G_d(s)} + \frac{Z_{v-fb}(s)G_v(s)G_d(s)}{Z_L(s)Z_C^{-1}(s) + 1 + G_v(s)G_d(s)} \tag{3.24}$$

The first term of (3.24) is related to the feedforward control while the second term is related to the feedback control. At the fundamental frequency, the below assumptions are valid.

$$\begin{cases} |G_v(j\omega_0)| << 1. \\ G_d(j\omega_0) = e^{-1.5j\omega_0 T_s} \approx 1\angle 0^\circ \\ |Z_C(j\omega_0)| >> |Z_L(j\omega_0)| \end{cases} \tag{3.25}$$

The second equation of (3.25) holds because the sampling frequency is much larger than the fundamental frequency. For example, a 10 kHz sampling frequency only yields a 2.7-degree phase delay at the fundamental frequency. Besides, the third assumption is reasonable since the LC resonant frequency is far away from the fundamental frequency. With these assumptions, the fundamental VSI output impedance can be approximated as

$$Z_o(j\omega_0) \approx Z_L(j\omega_0) + Z_{v-ff}(j\omega_0) \tag{3.26}$$

Equation (3.26) suggests that the VSI fundamental impedance is mainly determined by the filter inductance and $Z_{v\text{-}ff}(s)$. In this case, the fundamental power sharing can be improved through the proper design of $Z_{v\text{-}ff}(s)$. Besides, voltage measurement errors are effectively blocked by $G_v(s)$, as illustrated by the fundamental frequency signal flow of Fig. 3.4(b). At selective harmonic frequencies, $G_v(s)$ has considerable gains such that (3.24) can be approximated as

$$Z_o(jh\omega_0) \approx 0 + Z_{v-fb}(jh\omega_0). \quad (h = 5,7,11,13...) \tag{3.27}$$

Equation (3.27) indicates that the VSI harmonic impedance is mainly determined by the feedback-based impedance $Z_{v\text{-}fb}(s)$. One attractive feature is that the VSI harmonic impedance will not be affected by the control system delay $G_d(s)$, which is a limitation of the conventional feedforward-based impedance control. This is because the effect of

feedforward control has been overlapped by the feedback control, as illustrated in the harmonic-frequency signal flow of Fig. 3.4(c). Therefore, the VSI harmonic impedance can be precisely reshaped as desired, which helps to reduce the harmonic power-sharing error caused by mismatched grid impedances.

3.3.2. Design of Voltage Controller

This section will provide a detailed control parameter design process for the proposed control scheme, starting from the design of voltage controller $G_v(s)$.

The voltage controller $G_v(s)$ must be designed to fulfill the stability requirement. From Fig. 3.4(a), the open-loop voltage transfer function $T(s)$ is derived as

$$T(s)=\frac{G_v(s)G_d(s)Z_C(s)}{Z_L(s)+Z_C(s)} \tag{3.28}$$

To stabilize the closed-loop, a sufficient gain margin (GM) is required at the phase crossover frequency, which is close to the LC resonant frequency ω_r. The open-loop gain at the cross over frequency equals to

$$\left|T(j\omega_r)\right|=\frac{\left|G_v(j\omega_r)\right|}{\omega_r C_f r}=\frac{1}{C_f r}\sum_{h=5,7,11,13}\frac{k_{ih}}{\omega_r^2-h^2\omega_0^2} \tag{3.29}$$

Restrictions shall be applied to the resonant gains k_{ih} so that

$$\left|T(j\omega_r)\right|<1 \tag{3.30}$$

The values of k_{ih} can be quantitatively selected from (3.29) and (3.30). Fig. 3.5 shows the bode diagrams of $T(s)$ with different k_{ih}. It is observed that large resonant gains lead to a negative gain margin (GM) and hence make the system unstable. However, a 6.7 dB GM can be obtained by tuning k_{i5}, k_{i7}, k_{i11}, and k_{i13} as 20. It should be mentioned that due to the ESR damping effect, the VSI stability can still be obtained even if ω_r is smaller than the critical frequency $\omega_s/6$ [101].

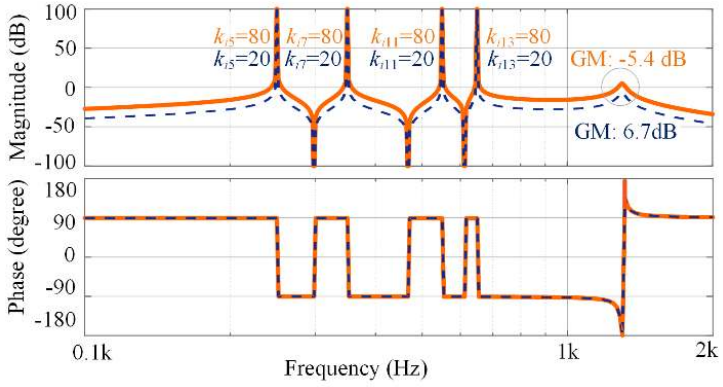


Fig. 3.5. Bode diagrams of $T(s)$, C_f =15 μF, L_f =1 mH, r =0.2 Ω, and T_s =100 μs.

3.3.3. Design of Feedback-based Impedance

In this section, the design of feedback-based virtual impedance will be discussed. The feedback-based impedance $Z_{v\text{-}fb}(s)$ is designed as a resistor, whose value is proportional to the VSI rated power S_N:

$$Z_{v-fb}(s) = \frac{b_f}{S_N} \tag{3.31}$$

where b_f is the proportional gain. Fig. 3.6 illustrates the system equivalent circuit at the hth-order harmonic frequency, where i_{hL} is the total load harmonic current, i_{h1} and i_{h2} are the harmonic currents of the two VSIs.

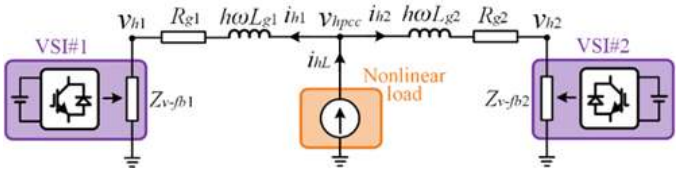


Fig. 3.6. System equivalent circuit at the hth-order harmonic-frequency domain.

Clearly, the harmonic current sharing ratio is determined by

$$\frac{i_{h1}}{i_{h2}} = \frac{Z_{v-fb2} + Z_{g2}}{Z_{v-fb1} + Z_{g1}} \tag{3.32}$$

Suppose that the proportional gain b_f is very small such that $Z_{v\text{-}fb1}$ and $Z_{v\text{-}fb2}$ are much smaller than Z_{g1} and Z_{g2}. (3.32) can then be approximated as

$$\frac{i_{h1}}{i_{h2}} = \frac{Z_{v-fb2} + Z_{g2}}{Z_{v-fb1} + Z_{g1}} \approx \frac{Z_{g2}}{Z_{g1}} \neq \frac{S_{1N}}{S_{2N}} \tag{3.33}$$

In this case, the harmonic current is mainly shared according to the line impedance ratio. However, line impedances are usually mismatched, which means that harmonic power cannot be properly shared according to the VSI power ratings. By contrast, if the gain b_f is large enough such that $Z_{v\text{-}fb1}$ and $Z_{v\text{-}fb2}$ are much larger than Z_{g1} and Z_{g2}., (3.32) is approximated as

$$\frac{i_{h1}}{i_{h2}} = \frac{Z_{v-fb2} + Z_{g2}}{Z_{v-fb1} + Z_{g1}} \approx \frac{Z_{v-fb2}}{Z_{v-vb1}} = \frac{S_{1N}}{S_{2N}} \tag{3.34}$$

which indicates that harmonic power can be shared in proportion with the VSI power ratings. From the above discussions, the increase of the proportional gain b_f improves the harmonic power-sharing accuracy. Nevertheless, since a larger b_f leads to a larger VSI harmonic impedance, more voltage distortions would also occur. To reach a compromise between these two aspects, the value of b_f is designed by the following guideline. According to [37], the harmonic power of a VSI is calculated as

$$H = \frac{3}{2} V_f \cdot (I_{o5}^2 + I_{o7}^2 + I_{o11}^2 + I_{o13}^2 + ...)^{1/2} \tag{3.35}$$

where I_{oh} is the magnitude of the hth-order harmonic current. Based on Fig. 3.6, the VSI output voltage THD is calculated as

$$THD = \frac{(V_5^2 + V_7^2 + V_{11}^2 + V_{13}^2 + ...)^{1/2}}{V_f} = \frac{Z_{v-fb}(I_{o5}^2 + I_{o7}^2 + I_{o11}^2 + I_{o13}^2 + ...)^{1/2}}{V_f} = \frac{2b_f H}{3S_N V_f^2}. \tag{3.36}$$

As required by IEEE Std. 519-2014, the THD of VSI voltage must be maintained within 8%. Hence, the constant b_f shall satisfy the below condition:

$$b_f \le \frac{3S_N V_f^2}{2H_{\max}} \cdot THD_{\max} \tag{3.37}$$

where $THD_{\max}$ = 8% and H_{max} is the maximum harmonic power that can be provided by the VSI. By selecting b_f as the critical value in (3.37), the harmonic power-sharing error can be reduced to a great extent, without violating the power quality standard.

3.3.4. Design of Feedforward-based Impedance

Finally, the design of the feedforward-based virtual impedance will be elaborated. Fig. 3.7 details the control block diagram of feedforward-based impedance shaping, where $i_{\alpha\text{-}p}$ and $i_{\beta\text{-}p}$ are fundamental positive-sequence VSI currents; $i_{\alpha\text{-}n}$ and $i_{\beta\text{-}n}$ are fundamental negative-sequence VSI currents. All of these current components are extracted through the *abc/dq* transformation and filtered by moving average filters (MAFs) with a 0.01s averaging time. $v_{v\alpha}$ and $v_{v\beta}$ are the outputs of the feedforward control, which are directly fed to the PWM unit.

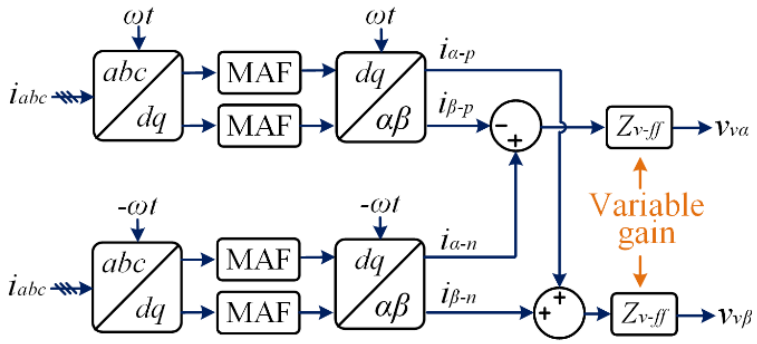


Fig. 3.7. Control block diagram of the feedforward-based impedance shaping.

Fig. 3.8 shows the VSI equivalent circuits as affected by the feedforward control. It is seen that the feedforward control equivalently imposes a positive-sequence inductance $jZ_{v\text{-}ff}$ and a negative-sequence resistance $Z_{v\text{-}ff}$.

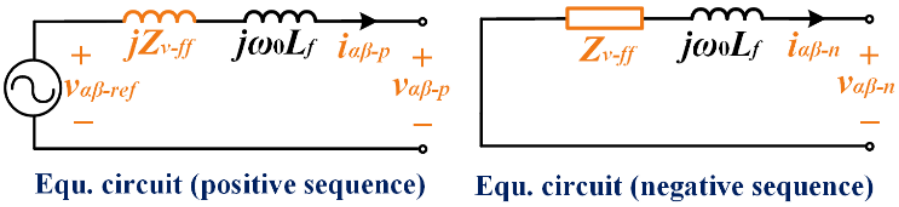


Fig. 3.8. VSI equivalent circuit as affected by the feedforward control.

To further improve the fundamental power sharing, the value of $Z_{v\text{-}ff}$ is designed to be linearly dependent on the fundamental apparent power S.

$$Z_{v-ff} = Z_{\min} \cdot \frac{S_N - S}{S_N} + Z_{\max} \cdot \frac{S}{S_N} \tag{3.38}$$

where Z_{min} and Z_{max} are the minimum and maximum values of $Z_{v\text{-}ff}$, respectively and S_N is the rated apparent power. (3.38) suggests that $Z_{v\text{-}ff}$ will become Z_{min} under the no-load condition and Z_{max} under the full-load condition. The basic principle behind this proposal is that if a VSI shares more apparent power S than others, its impedance will also become larger according to (3.38), which helps to reduce its power output and decrease the power-sharing error. Clearly, a wider range between Z_{min} and Z_{max} implies that the VSI has a stronger ability to mitigate the power-sharing error. Next, the selection of Z_{max} and Z_{min} will be discussed.

The upper limit Z_{max} is restricted to the maximum-allowed VSI voltage magnitude deviation. The VSI voltage magnitude deviation ΔV is calculated as

$$\Delta V = k_q \cdot \Delta Q + \frac{2Q}{3V_0} \cdot (Z_{v-ff} + \omega_0 L_f) \tag{3.39}$$

On the right side of (3.39), the first term represents the voltage drop caused by the Q-V droop control while the second term is the voltage drop across filter inductance and the feedforward impedance. To ensure that the maximum voltage deviation is within the specified range, e.g., 10%, (3.39) is rewritten as

$$\frac{\Delta V}{V_0} = \frac{Q \cdot (3k_q V_0 + 2Z_{\max} + 2\omega_o L_f)}{3V_0^2} \le 10\% \tag{3.40}$$

Notice that the maximum voltage magnitude deviation will occur if the reactive power Q reaches the rated apparent power S_N. Therefore, Z_{max} is determined as

$$Z_{\max} = 10\% \cdot \frac{3V_0^2}{2S_N} - \frac{3k_q V_0}{2} - \omega_0 L_f \tag{3.41}$$

On the other hand, Z_{min} is determined according to the stability requirement of droop control. Based on the positive-sequence VSI equivalent circuit in Fig. 3.8, the active and reactive powers of VSI are derived as

$$P = \frac{3}{2} \cdot \frac{VV_{pcc} X_{\Sigma} \sin\delta + V(V - V_{pcc}\cos\delta) R_g}{R_g^2 + X_{\Sigma}^2} \tag{3.42}$$

$$Q = \frac{3}{2} \cdot \frac{-VV_{pcc} R_g \sin\delta + V(V - V_{pcc}\cos\delta) X_{\Sigma}}{R_g^2 + X_{\Sigma}^2} \tag{3.43}$$

$$X_{\Sigma} = \omega_0 L_g + \omega_0 L_f + Z_{v-ff} \tag{3.44}$$

where δ is the phase angle difference between VSI voltage and the PCC voltage. V_{pcc} is the PCC voltage magnitude. Perturbing (3.42) and (3.43) gives

$$\begin{bmatrix} \Delta P \\ \Delta Q \end{bmatrix} = \begin{bmatrix} G_{\delta P} & G_{VP} \\ G_{\delta Q} & G_{VQ} \end{bmatrix} \cdot \begin{bmatrix} \Delta\delta \\ \Delta V_f - \Delta V_{pcc} \end{bmatrix} \tag{3.45}$$

Given that the steady-state value of δ is usually very small, the coefficients $G_{\delta P}$, G_{VP}, $G_{\delta Q}$, and G_{VQ} can be approximated as

$$\begin{cases} G_{\delta P} = \dfrac{3V_f}{2} \cdot \dfrac{V_{pcc} X_{\Sigma}}{R_g^2 + X_{\Sigma}^2} \\ G_{\delta Q} = \dfrac{3V_f}{2} \cdot \dfrac{-V_{pcc} R_g}{R_g^2 + X_{\Sigma}^2} \\ G_{VP} = \dfrac{3V_f}{2} \cdot \dfrac{R_g}{R_g^2 + X_{\Sigma}^2} \\ G_{VP} = \dfrac{3V_f}{2} \cdot \dfrac{X_{\Sigma}}{R_g^2 + X_{\Sigma}^2} \end{cases} \tag{3.46}$$

Based on (3.42) and (3.46), the overall system model is established in Fig. 3.9 and further simplified in Fig. 3.10. where the equivalent block diagram $G_{eq}(s)$ is derived as

$$G_{eq}(s) = \frac{-k_q \omega_f G_{\delta Q} G_{VP}}{s + \omega_f (1 + k_q G_{VQ})} \tag{3.47}$$

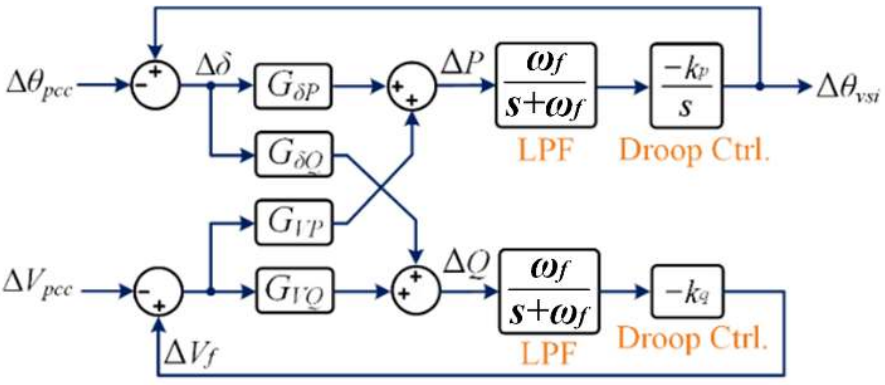


Fig. 3.9. A small-signal model of the droop control.

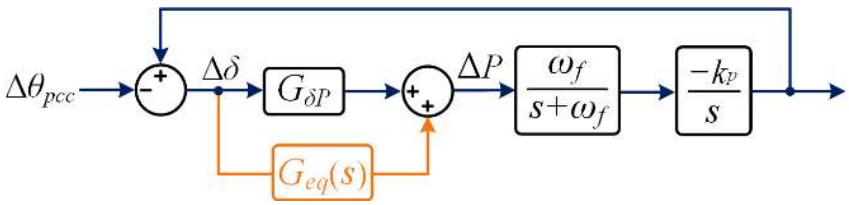


Fig. 3.10. Simplified small-signal model of the droop control.

Accordingly, the system open-loop transfer function (with regard to the disturbance $\Delta\theta_{pcc}$) is derived as

$$T_o(s) = \frac{\omega_f k_p G_{\delta P} + \omega_f k_p G_{eq}(s)}{s^2 + \omega_f \cdot s} \tag{3.48}$$

Fig. 3.11 shows the Bode diagrams of $T_o(s)$ with different X_Σ values, while the rest of the parameters are provided in Table 3.1. It is seen that the decrease of X_Σ increases the power-loop bandwidth but degrades the system phase margin (PM). As a result, the VSI phase angle may be oscillatory and even unstable. Normally, a 60-degree PM is preferred with a guaranteed stability margin.

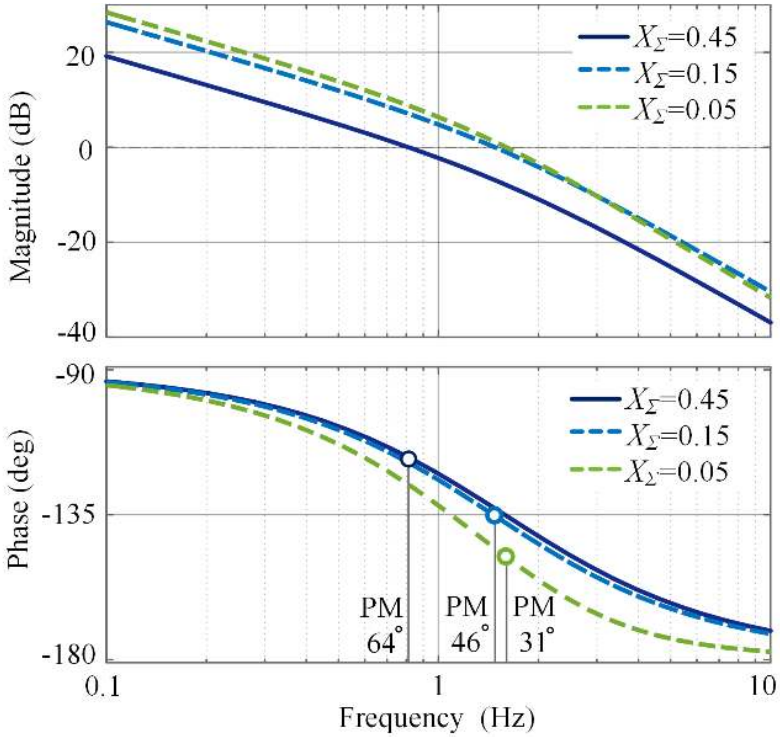


Fig. 3.11. Bode diagrams of $T_o(s)$ with different X_Σ values.

Table 3.1 System and control parameters

Parameters	Descriptions	Values
V_0	AC voltage magnitude	75 V
u_{dc}	DC-input voltage	200 V
L_{g1}, L_{g2}	Grid inductances	0.8 mH, 1mH
R_{g1}, R_{g2}	Grid resistances	0.1 Ω, 0.1 Ω
m_1, m_2	Droop coefficients	1×10^{-4} rad/(s·W)
n_1, n_2	Droop coefficients	1×10^{-4} V/Var
f_{sw}	Switching frequency	10 kHz
L_f	Filter inductance	1 mH
C_f	Filter capacitor	$15\mu F$
S_N	VSI rated power	1000 VA
k_{i5}, k_{i7}, k_{i11}, k_{i13}	Resonant control gains	20
b_f	Proportional gain	3375 Ω/VA
Z_{min}	Lower limit of $Z_{v\text{-}ff}$	0.52 Ω
Z_{max}	Upper limit of $Z_{v\text{-}ff}$	0.05 Ω

To fulfill the stability demand and ensure satisfying dynamic performance, X_Σ should be larger than the critical value X_{cri}, which corresponds to a 60-degree PM in Fig. 3.11. The value of X_{cri} can be acquired from the bode diagram and is around 0.36 Ω. According to the below discussions, it is desired that

$$X_\Sigma = \omega_0 L_f + \omega_0 L_g + Z_{v-ff} \geq X_{cri} \tag{3.49}$$

Notice that line inductance L_g is an unknown nonnegative value while $Z_{v\text{-}ff}$ is between Z_{min} and Z_{max}. Therefore, a sufficient condition for (3.49) is

$$Z_{\min} = X_{cri} - \omega_0 L_f \tag{3.50}$$

Equation (3.50) selects the lower limit $Z_{v\text{-}ff}$ from the small-signal stability perspective. Combined with the upper limit specified by (3.41), the design of feedforward impedance shaping control has been elaborated.

3.4. Simulation Results

To verify the impacts of measurement errors and the feasibility of the proposed control scheme, simulations with two parallel three-phase VSIs were carried out under the PLECS environment. The key control and system parameters are provided in Table 3.1, while the sensor errors are set according to [102] and detailed in Table 3.2. Notice that

the current sensor measurement errors are included. However, little influence do they have since they are only involved in the power calculations.

Table 3.2 Sensor measurement errors

VSI	VSI #1		VSI #2	
Tolerances	Voltages	Currents	Voltages	Currents
Δk_a	0 %	+ 2 %	+ 2 %	+ 1 %
Δk_b	0 %	0 %	0 %	– 1 %
Δk_c	– 2 %	– 1 %	0 %	+ 0 %
$X_{a\text{-}dc}$	+ 1.0 V	+ 0.02 A	– 0.3 V	– 0.05 A
$X_{b\text{-}dc}$	– 2.0 V	+ 0.08 A	+ 0.2 V	– 0.07 A
$X_{c\text{-}dc}$	– 1.5 V	– 0.05 A	– 1.2 V	+ 0.12 A

Fig. 3.12 shows the system configuration, where different types of load are connected at the PCC, including a three-phase balanced load (each phase has a 20 Ω resistance paralleled with a 0.1 H inductance), an unbalanced load (which is a 40 Ω resistance connected between phase A and phase B), and a nonlinear load (a typical three-phase rectifier).

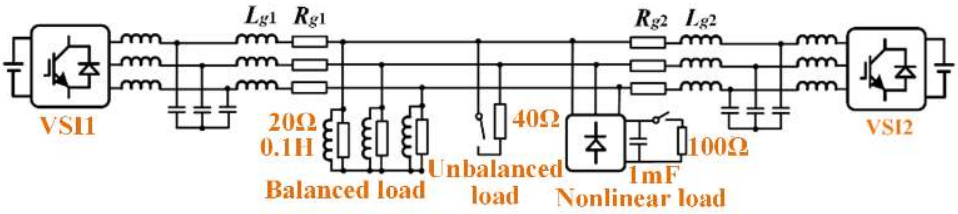


Fig. 3.12. Schematic diagram of the tested system.

3.4.1. Balanced Load Power Sharing

Initially, only the balanced three-phase load is connected at the PCC. Fig. 3.13 shows the dynamic response of VSI active and reactive power. During Stage 1, the conventional voltage feedback control is adopted to eliminate the fundamental voltage tracking error. Since no unbalanced load is in the microgrid, both I_N1 and I_{N2} should be zero. However, due to voltage measurement errors, I_N1 and I_{N2} have the same values, indicating that the negative-sequence current is circulating between the VSIs. This indicates that voltage measurement errors can severely degrade the reactive power sharing and introduce a negative-sequence circulating current. During Stage 2, the proposed control scheme is enabled, which greatly improves the reactive power sharing and reduces negative-sequence circulating currents. For Stage 3 and Stage 4, the load is disconnected and reconnected. It is clear that good power-sharing performance can still be maintained, regardless of load variations.

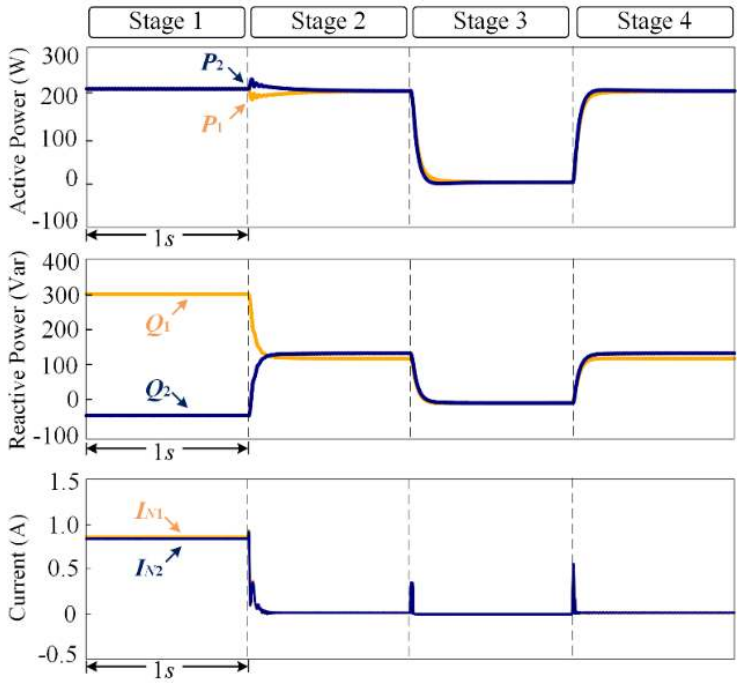


Fig. 3.13. Dynamic responses of the fundamental power sharing.

Fig. 3.14 illustrates the VSI output currents during different stages. The circulating currents, which are defined as the differences between VSI currents, are significant during Stage 1 but much smaller after the proposed control scheme is enabled.

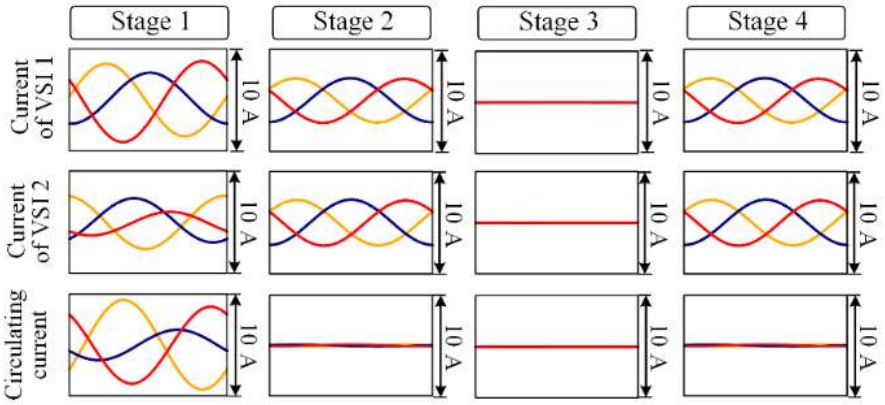
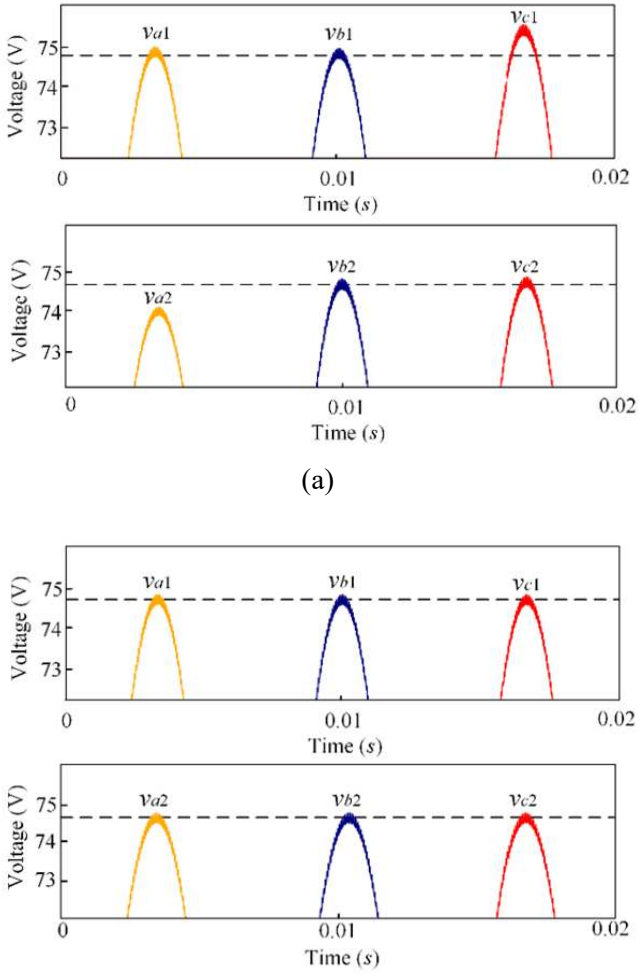


Fig. 3.14. VSI current waveforms during different stages.

Fig. 3.15 displays zoomed-in views of VSI voltages. In Fig. 3.15(a), the conventional voltage-feedback control is utilized. It is seen that v_{c1} has a larger voltage magnitude and v_{a2} has a smaller voltage magnitude. This happens because VSI #1 has a –2% voltage scaling error for phase C and VSI#2 has a +2% voltage scaling error for phase A. In comparison, Fig. 3.15(b) shows the zoom-in VSI voltage waveforms with the proposed

control scheme. It can be observed that the impacts of voltage measurement errors are effectively mitigated.



(a)

(b)

Fig. 3.15. Zoomed-in VSI voltage waveforms. (a) Conventional voltage-feedback control. (b) Proposed control scheme.

3.4.2. Complex Load Power Sharing

For the next case, the balanced load, unbalanced load, as well as nonlinear load are connected at the same time. Fig. 3.16 displays the dynamic responses of unbalanced/ harmonic power sharing while Fig. 3.17 shows the VSI output currents for different stages. During Stage 5, the conventional voltage-feedback control is adopted and the unbalanced power is poorly shared (since I_{N1} is quite different from I_{N2}). During Stage 6, the proposed control scheme is enabled, and the unbalanced power-sharing accuracy is greatly improved. Then, the unbalanced and nonlinear loads are disconnected during

Stage 7 and reconnected again during Stage 8. It can be seen that good power-sharing performance can always be maintained.

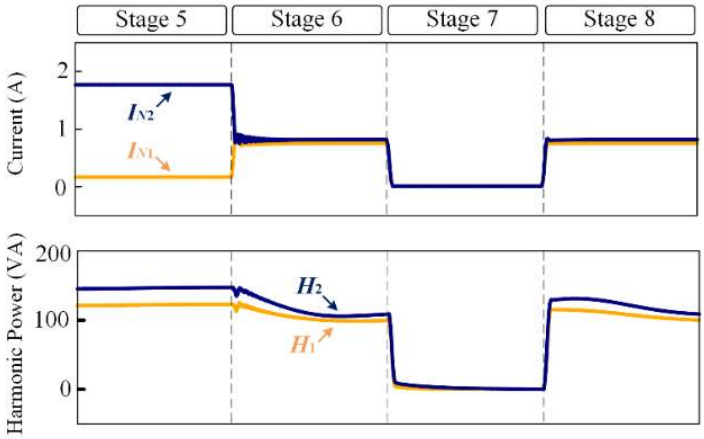


Fig. 3.16. Dynamic responses of unbalanced and harmonic power sharing.

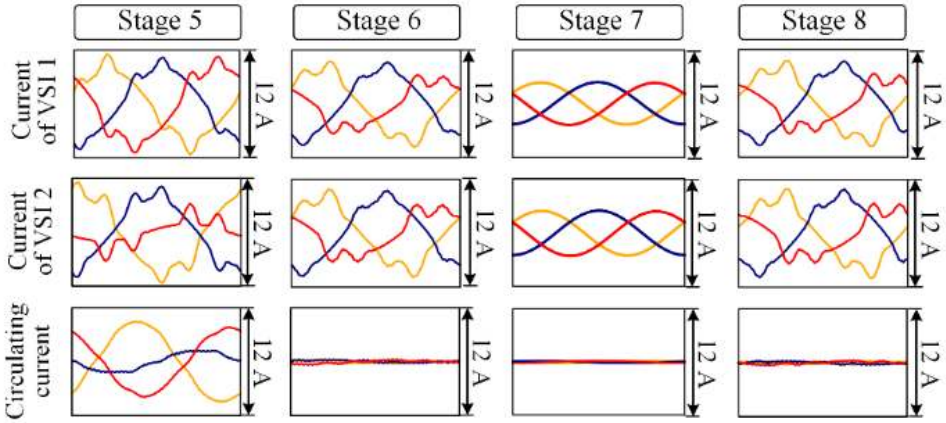


Fig. 3.17. VSI current waveforms during different stages.

3.5. Experimental Results

In addition to simulation results, experimental results from a scaled-down islanding microgrid prototype are also provided for verification. Fig. 3.18 shows the laboratory setup picture, where the digital controls were implemented by a dSPACE MicroLab-Box. Two three-phase VSIs were built with MOSFETs (C3M0120090D) and connected in a parallel configuration. The circuit configuration and control parameters keep the same with those for simulations.

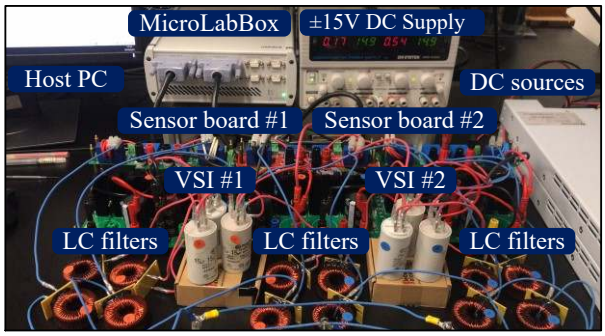


Fig. 3.18. Photo of the laboratory hardware setup.

3.5.1. Balanced Three-phase Load

Initially, only a balanced three-phase load is connected to the PCC. Fig. 3.19 shows the currents of VSI#1 and circulating currents. It is found that voltage measurement errors would result in unbalanced three-phase currents even without the presence of unbalanced loads. Note that the undesired circulating currents will linearly increase with the AC voltage magnitude. Therefore, the problems will be much more serious in real microgrids with a much higher voltage level.

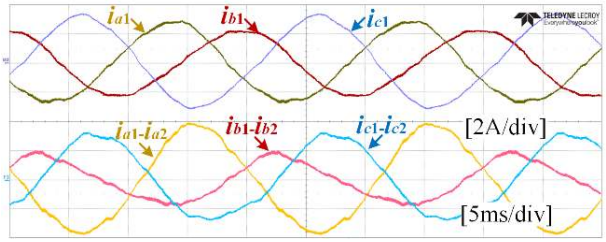


Fig. 3.19. VSI currents with the conventional voltage-feedback control.

In contrast, Fig. 3.20 shows the current waveforms with the proposed control scheme. It is observed that circulating currents are effectively attenuated, which indicates a good fundamental power sharing between the two VSIs.

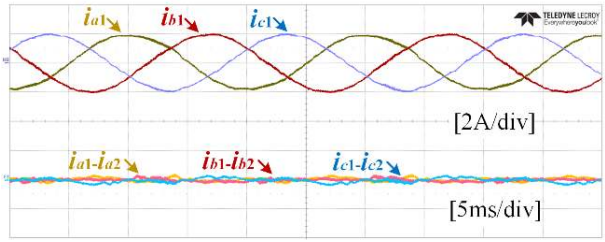


Fig. 3.20. VSI currents with the proposed control scheme.

3.5.2. Complex Load Scenarios

Next, the balanced load, unbalanced load, and nonlinear load are supplied at the same time. Fig. 3.21 and Fig. 3.22 respectively show the current waveforms with the conventional-voltage feedback control and the proposed control scheme. In Fig. 3.22, the small differences between VSI output currents suggest that the negative-sequence and harmonic currents can also be properly shared by the proposed control scheme.

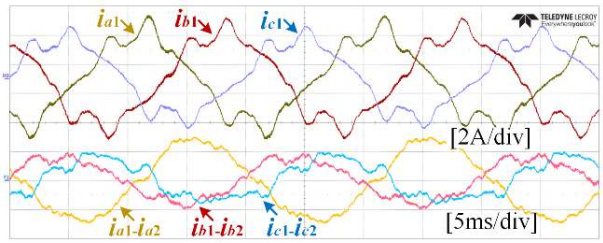


Fig. 3.21. VSI currents with the conventional voltage-feedback control.

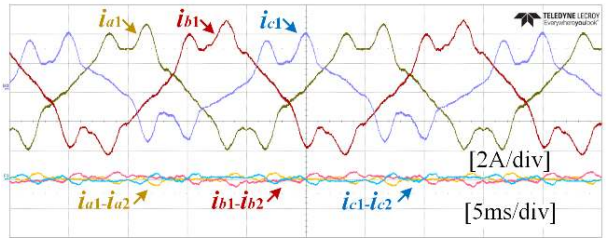


Fig. 3.22. VSI currents with the proposed control scheme.

Moreover, the PCC voltage waveforms are shown in Fig. 3.23 and the corresponding FFT analysis result is provided in Fig. 3.24. Due to the presence of nonlinear load, there exist certain harmonic distortions. Even though, the proposed control strategy ensures that PCC voltage THD is around 2.3%, which satisfies the voltage quality requirement of IEEE Std. 519-2014.

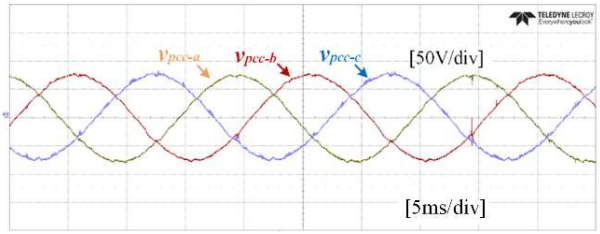


Fig. 3.23. PCC voltage waveforms with the proposed control scheme.

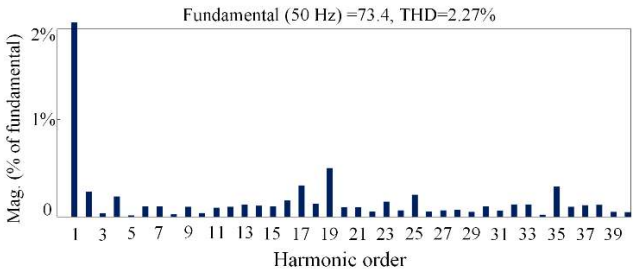


Fig. 3.24. FFT analysis of the PCC voltage.

3.6. Summary

This chapter investigates the impacts of voltage measurement error on power sharing among parallel VSIs. It is found that voltage sensor scaling errors may cause significant circulating currents among parallel VSIs, given that the voltage-feedback control is well designed with excellent tracking ability. To solve this issue, a hybrid impedance shaping control is proposed to mitigate the negative impacts of voltage measurement errors and improve power-sharing accuracy. The proposed control scheme can be implemented in a completely decentralized manner and its feasibility has been verified by both simulation and experimental results.

Chapter 4 Two-dimensional Impedance Shaping Control for Accurate Harmonic Current Sharing

In Chapter 2 and Chapter 3, the reactive power and unbalanced power sharing among parallel VSIs have been analyzed and discussed, respectively. This chapter will focus on the harmonic current sharing among parallel VSIs. Though the virtual impedance control developed in Chapter 3 helps to improve the harmonic current sharing performance, it is revealed in this chapter that the circulating harmonic currents cannot be eliminated if the virtual impedance is adjusted in one dimension only, i.e., just regulate the resistive part or the inductive part. To address this issue, this chapter develops a two-dimensional impedance-shaping control, which can ensure accurate harmonic current sharing under arbitrary line impedances. The experimental test shows that the two-dimensional virtual impedance can reduce the circulating harmonic current by more than 50% in comparison with the conventional droop control.

4.1. Introduction

The proliferation of nonlinear loads can introduce significant harmonic currents. Such harmonic currents may trigger the current protection or lead to overloading of VSIs if they are not properly allocated. As previously discussed, the conventional droop control only takes effect at the fundamental positive-sequence frequency and has little influence on the harmonic current sharing performance.

According to the analysis in [98], the harmonic currents are distributed among parallel VSIs according to the effective harmonic impedances, namely, the sums of VSI output impedances and line impedances. Therefore, the harmonic current sharing issue can be addressed in a similar way by reshaping VSI output impedances at harmonic frequencies. In [103], [104], large VSI harmonic impedances are adopted to attenuate line impedance mismatches. However, the point of common coupling (PCC) voltage is highly distorted due to considerable harmonic voltage drops across VSI impedances. As an alternative, negative virtual impedances are also used to share harmonic power while maintaining a good PCC voltage quality in [100] and [103], whereas prior line impedance knowledge is normally required.

To further enhance the harmonic power-sharing performance, VSI output impedances are adaptively regulated according to the delivered harmonic power in [104]–[107]. In specific, a conductance-harmonic var (*G-H*) droop is developed in [105] to link the VSI impedance with the delivered harmonic power, while similar effects are achieved either by the harmonic impedance controller (HIC) in [106] or by the feedforward control in [100]. Although the above techniques are employed in a fully decentralized manner, the harmonic current sharing error cannot be eliminated. To overcome this limitation, a disturbance term associated with the harmonic power is added to the conventional *P-f* droop in [108] such that VSI output impedances are periodically updated based on the transient active power variation. This online impedance-shaping strategy can ensure the harmonic current accuracy without acquiring prior line impedance knowledge. Besides, harmonic sharing and filtering functionalities are simultaneously achieved by feeding the PCC harmonic voltage to local VSI controllers in [109], [110]. Since the PCC harmonic voltage can be modulated to corresponding DC components through the Park transformation, only low-bandwidth communications are needed for signal transmission. Considering that the phase angles used for the Park transmission may vary for different VSIs, an additional synchronization unit is adopted in [111] to further improve the controller accuracy. Moreover, a centralized harmonic power sharing control algorithm

is reported in [112], where VSI harmonics impedances are dynamically shaped based on the information provided by a microgrid central controller. To avoid the centralized structure and improve the system reliability, a distributed consensus control protocol is also developed in [46] such that the harmonic power-sharing problem has been well addressed.

Nevertheless, problems arise for low-voltage microgrids characterized by complex line impedances. As the previous impedance-shaping techniques solely regulate the resistive or inductive part of VSI output impedances, only one control degree of freedom (DOF) is provided for impedance shaping. Such maneuvers can hardly fulfil the proper harmonic current sharing requirement: the effective harmonic impedances should have unified impedance angle and magnitude. Failure of meeting such a requirement would generate additional circulating harmonic currents among multiple parallel VSIs, even if the harmonic power has been accurately shared.

To fill in this gap, this chapter proposes a two-dimensional impedance-shaping control to enhance the harmonic current sharing performance under complex line impedance situations. In specific, both the resistive and the inductive parts of VSI impedances are adaptively shaped through a distributed consensus control algorithm. As a result, the harmonic power sharing accuracy is ensured, and circulating harmonic currents are also eliminated. Compared with the existing techniques, the proposed control algorithm is widely applicable to any grid impedance scenarios, even for the worst cases that line impedances are mismatched both in the magnitude and in the impedance angle [113].

This chapter starts with a brief introduction of the harmonic current sharing principle. The research issue of improper harmonic current sharing under complex line impedance situations is then formed by analysing the VSI effective impedances in the complex impedance plane. Then, the proposed control strategy will also be elaborated in detail. Finally, the feasibility of the proposed control strategy is validated through experimental results from an islanded microgrid prototype with three parallel VSIs.

4.2. Problem Formulation

4.2.1. Circuit Configuration

Fig. 4.1 shows a typical islanded microgrid with n parallel VSI units cooperatively supplying power to the PCC loads. L_f and C_f are the filter inductor and capacitor, which are normally adopted to attenuate high-frequency switching harmonics. L_g and R_g are the line inductance and resistance, respectively, and their values will vary with the system

voltage level, the transmission line length, and the type of electrical wires. In the steady state, the active, reactive, and harmonic power consumed by the PCC loads are expected to be proportionally shared among multiple VSIs according to their power ratings.

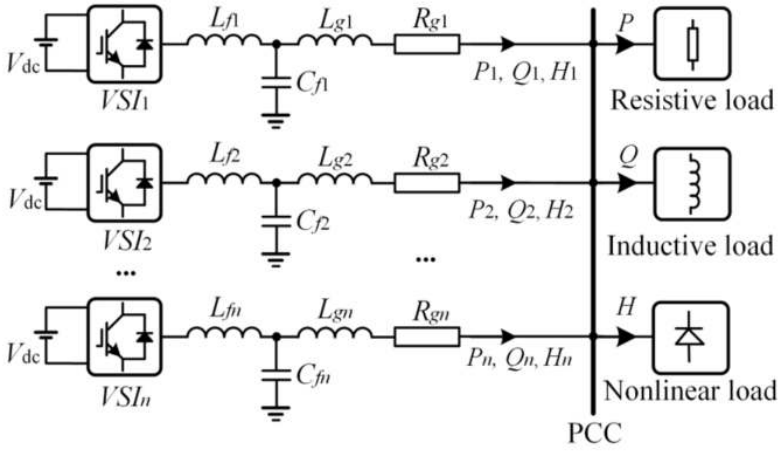


Fig. 4.1. Schematic of an inverter-based islanded microgrid with multiple parallel VSIs.

To analyse the harmonic current sharing principle, the system equivalent model is established at the hth-order harmonic frequency ($\omega=h\omega_0$, where ω_0 is the fundamental frequency). Fig. 4.2 illustrates the system equivalent model, where the nonlinear load is represented by a harmonic current source i^h, while the VSI is modelled as a harmonic impedance $Z_o(h\omega_0)=R_o+jX_o(h\omega_0)$ in its Thevenin's form. The magnitude and impedance angle of $Z_o(h\omega_0)$ is mainly determined by the filter parameters as well as the controller design.

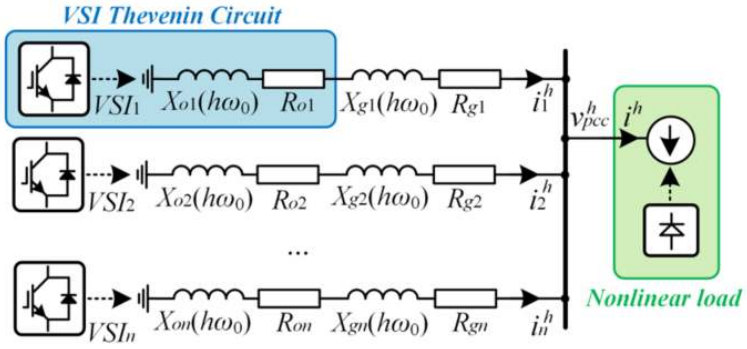


Fig. 4.2. Equivalent model of an islanded microgrid at the hth-order harmonic frequency.

4.2.2. Harmonic Sharing Principle

According to Kirchhoff's voltage law (KVL), harmonic currents of the nonlinear load are distributed among parallel VSIs according to line impedances and VSI harmonic impedances

$$i_i^h = \frac{v_{pcc}^h}{R_{gi} + R_{oi} + jX_{gi}(h\omega_0) + jX_{oi}(h\omega_0)} \tag{4.1}$$

where R_{oi} and $X_{oi}(h\omega_0)$ are respectively the resistance and reactance (when $\omega=h\omega_0$) of VSI#i, i_i^h is the hth-order harmonic current of VSI#i, and v_{pcc}^h is the hth-order PCC harmonic voltage.

The VSI effective impedance is defined as the sum of the line impedance and the VSI output impedance

$$Z_{ei}(h\omega_0) = R_{ei} + jX_{ei},\ R_{ei} = R_{gi} + R_{oi},\ X_{ei} = X_{gi}(h\omega_0) + X_{oi}(h\omega_0) \tag{4.2}$$

Combining (4.1) and (4.2) yields

$$i_i^h = \frac{v_{pcc}^h}{R_{ei} + jX_{ei}(h\omega_0)} \tag{4.3}$$

According to the IEEE Std. 1459-2010, the hth-order apparent harmonic power S^h can be calculated as

$$S^h = \frac{1}{2} \cdot V_0^f \cdot I^h \tag{4.4}$$

where $V_0{}^f$ is the fundamental voltage magnitude, and I^h is the hth-order harmonic current magnitude. From (4.3) and (4.4), the hth-harmonic power of VSI#i is expressed as:

$$S_i^h = \frac{V_0^f \cdot \left| v_{pcc}^h \right|}{2 \cdot \left| R_{ei} + jX_{ei}(h\omega_0) \right|} \tag{4.5}$$

In order to proportionally share the harmonic power according to VSI power ratings, the following condition needs to be met

$$S_{iN} \cdot \left| R_{ei} + jX_{ei}(h\omega_0) \right| = S_{jN} \cdot \left| R_{ej} + jX_{ej}(h\omega_0) \right| \quad \forall i, j \in (1,2,...,n) \tag{4.6}$$

where S_N is the rated power of the VSI.

4.2.3. Analysis of Circulating Harmonic Current

However, even if (4.6) is satisfied, there may still exist circulating harmonic currents among VSIs. The hth-order circulating harmonic current between VSI#i and VSI#j is given by

$$i_{ij}^{h} = \frac{i_i^h}{S_{iN}} - \frac{i_j^h}{S_{jN}} \tag{4.7}$$

$$i_{ij}^{h} = \frac{v_{pcc}^{h}}{S_{iN} \cdot [R_{ei} + jX_{ei}(h\omega_0)]} - \frac{v_{pcc}^{h}}{S_{jN} \cdot [R_{ej} + jX_{ej}(h\omega_0)]} \tag{4.8}$$

From (4.8), the circulating harmonic currents can be eliminated under the condition that

$$S_{iN} \cdot [R_{ei} + jX_{ei}(h\omega_0)] = S_{jN} \cdot [R_{ej} + jX_{ej}(h\omega_0)] \tag{4.9}$$

A comparison indicates that the condition in (4.9) is more stringent than that in (4.6), since it not only ensures the harmonic power-sharing accuracy but also guarantees that VSI harmonic currents are exactly in phase with each other. However, such a condition can hardly be satisfied in practical situations due to line impedance mismatches.

Fig. 4.3 analyses the improper harmonic power-sharing results caused by mismatched effective harmonic impedances. For simplicity, only two parallel VSIs (namely VSI#*i* and VSI#*j*) with equal power ratings are considered. The conclusions, however, can also be extended to multiple parallel VSIs with different power ratings. Initially, effective harmonic impedances Z_{ei} and Z_{ej} have the same impedance angle but different magnitude in the first case ($\theta_i=\theta_j$, $|Z_{ei}|\neq|Z_{ej}|$) and the total harmonic current i^h is unequally distributed between VSI#*i* and VSI#*j*. For the second case, Z_{ei} and Z_{ej} have the same magnitude but different impedance angles. Consequently, harmonic current i^h_i is lagging behind i^h_j since Z_{ei} has a higher X/R ratio as compared to Z_{ej}. In addition, the circulating harmonic current is not eliminated ($i^h_i - i^h_j \neq 0$), although the harmonic power has been equally shared between the two VSIs. Such improper harmonic power sharing can produce additional harmonic power, as the sum of $|i^h_i|$ and $|i^h_j|$ is even larger than $|i^h|$. Finally, a more generalized scenario is considered in the third case, where the effective impedances Z_{ei} and Z_{ej} are mismatched both in the magnitude and in the impedance angle.

The harmonic power-sharing performance is poor not only because the total harmonic current is unevenly distributed, but also additional harmonic power has been produced.

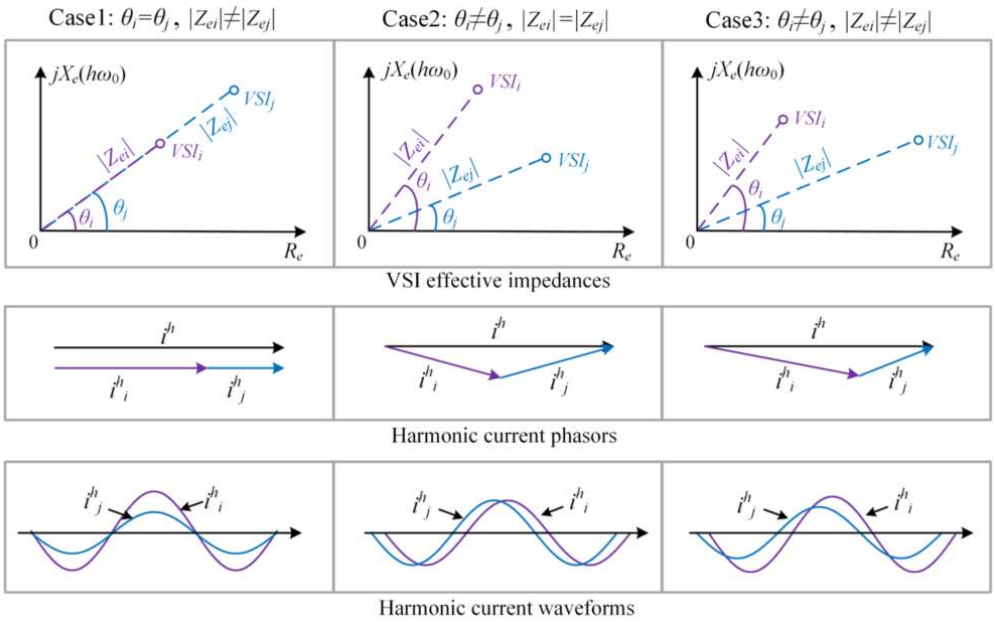
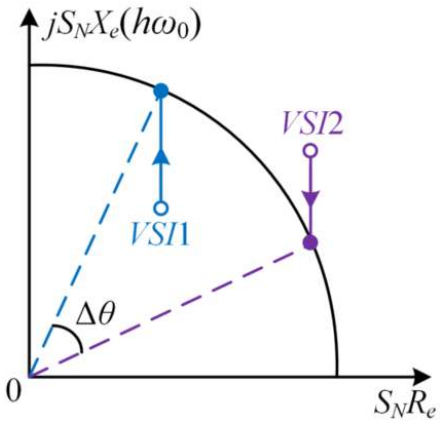


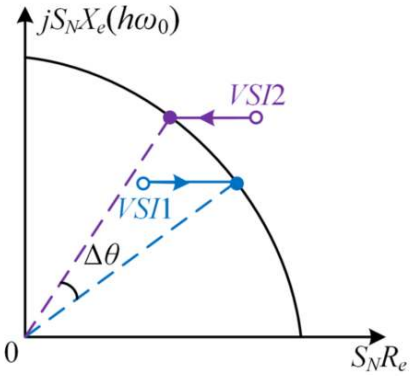
Fig. 4.3. Analysis of the improper harmonic power sharing caused by mismatched effective harmonic impedances.

To enhance the harmonic power-sharing accuracy, impedance-shaping controls can be utilized to modify the VSI effective impedances at selective harmonic frequencies. However, as the conventional techniques only regulate VSI output impedances in one dimension, the requirement for proper harmonic power sharing can hardly be fulfilled if line impedances are complex. Fig. 4.4 illustrates the principles of one-dimensional impedance-shaping controls.

In Fig. 4.4(a), the inductive parts of VSI output impedances are reshaped to enhance the harmonic power-sharing performance. In the steady state, the harmonic power is accurately shared as the rated effective impedances $S_{1N}Z_{e1}$ and $S_{2N}Z_{e2}$ are located on the orbit of a quarter circle. However, the impedance angle difference $\Delta\theta$ still exists, and hence leads to circulating harmonic currents. A similar result can be found in Fig. 4.4(b), where the resistive parts of VSI output impedances are reshaped. The reason for such improper harmonic power sharing is that the effective impedances of VSIs, which are two-dimensional phasors in the complex impedance plane, cannot be equalized if only one control DOF is provided for the impedance shaping.



(a)



(b)

Fig. 4.4. Conventional impedance-shaping controls with only one DOF. (a) Inductance shaping. (b) Resistive shaping.

4.3. Proposed Control Strategy

To solve this issue, a two-dimensional impedance-shaping control is proposed in this subsection.

4.3.1. Overall Control Architecture

Fig. 4.5 depicts the overall controller, which contains an inner-loop voltage controller and outer-loop impedance-shaping controllers. Among them, the outer-loop impedance-shaping controllers are designed to ensure the harmonic current sharing accuracy by adaptively regulating the VSI resistance value R_i and the inductance value L_i, while the inner-loop voltage controller is implemented to eliminate the reference voltage tracking error.

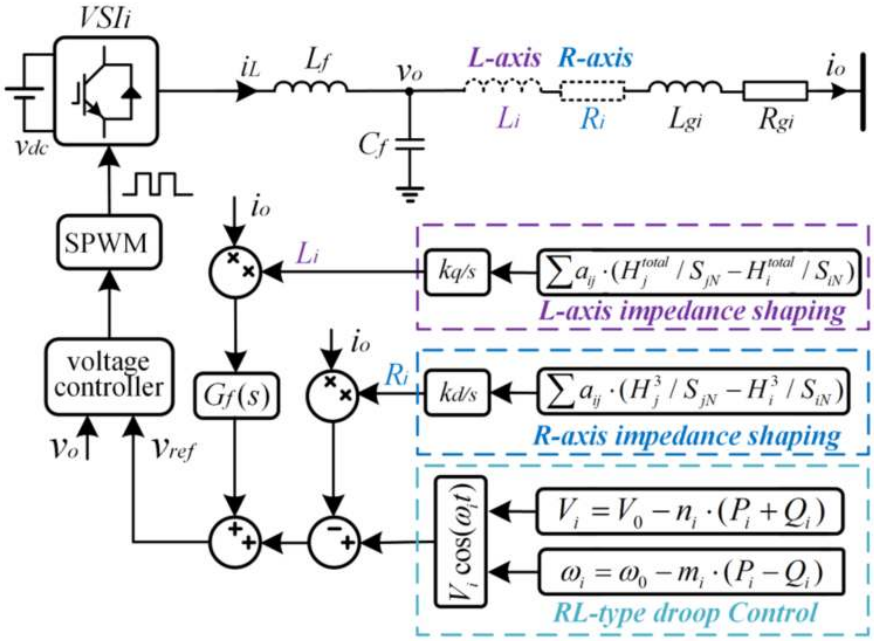


Fig. 4.5. Overall circuit and control block diagram.

In Fig. 4.5, $G_f(s)$ consists of multiple band-pass filters, which can be expressed as

$$G_f(s) = \sum_{h=1,3,5,7\ldots} h\omega_0 \cdot \frac{kh^2\omega_0^2}{s^2 + kh\omega_0 \cdot s + h^2\omega_0^2} \tag{4.10}$$

At selective harmonic frequencies ($s = jh\omega_0$), the reference voltage $v_{ref}(jh\omega_0)$ can be written as

$$v_{ref}(jh\omega_0) = i_o(jh\omega_0) \cdot G_f(jh\omega_0) \cdot L_i - i_o(jh\omega_0) \cdot R_i \tag{4.11}$$

Given that the voltage controller is well designed and can accurately track $v_{ref}(jh\omega_0)$ at selective harmonic frequencies, i.e.,

$$v_o(jh\omega_0) = v_{ref}(jh\omega_0) \tag{4.12}$$

According to (4.11) and (4.12), the VSI output harmonic impedance can be expressed as

$$Z_o(jh\omega_0) = \frac{v_o(jh\omega_0)}{-i_o(jh\omega_0)} = -G_f(jh\omega_0) \cdot L_i + R_i \tag{4.13}$$

$$Z_o(jh\omega_0) = -h\omega_0 \cdot \frac{kh^2\omega_0^2}{kh\omega_0 \cdot jh\omega_0} \cdot L_i + R_i \tag{4.14}$$

$$Z_o(jh\omega_0) = jh\omega_0 \cdot L_i + R_i \tag{4.15}$$

The above analysis indicates that a properly-designed voltage controller can ensure that the VSI inductance and resistance are well regulated as the desired values L_i and R_i, respectively.

4.3.2. Repetitive Controller Design

As mentioned above, the inner-loop voltage controller should be properly designed so that v_{ref} can be accurately tracked at selective harmonic frequencies. To effectively compensate the low-order harmonic voltage distortions, a repetitive-based voltage controller is designed and shown in Fig. 4.6.

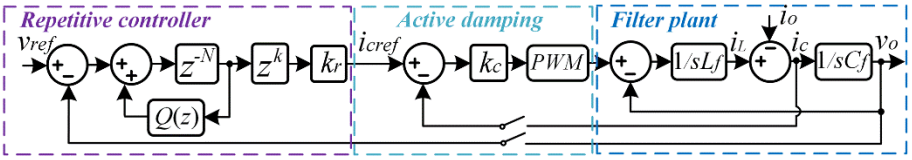


Fig. 4.6. System and control block diagram of the inner-loop repetitive controller.

In Fig. 4.6, z^{-N} refers to the time delay unit, where N is the number of samples in one fundamental period. $Q(z)$ is a low-pass filter, which is normally employed to improve the repetitive control system robustness. z^{k} is the time advance unit. k_r is the repetitive controller gain and k_c is the current controller gain.

The first step is to design the current controller gain k_c. By applying the capacitor current feedback control, the compensated LC filter plant transfer function $G_p(s)$ and the corresponding damping ratio can be approximated as [83]

$$G_p(s) = \frac{k_c}{L_f C_f s^2 + k_c C_f s + 1} \tag{4.16}$$

$$\xi = \frac{k_c}{2} \cdot \sqrt{\frac{C_f}{L_f}} \tag{4.17}$$

From (4.17), gain k_c is tuned so that the damping factor ξ equals 0.707 (a very typical value for second-order systems). Note that the system delay z^{-1} is not considered in (4.16) for simplicity, but cannot be ignored when analysing the closed-loop system stability. Taking the digital delay into account, the discrete closed-loop transfer function from i_{cref} to v_o is derived as

$$G_p(z) = \frac{k_c z^{-1} \cdot Z_{zoh}\left(\frac{1}{L_f C_f s^2 + 1}\right)}{1 + k_c z^{-1} \cdot Z_{zoh}\left(\frac{C_f s}{L_f C_f s^2 + 1}\right)} \tag{4.18}$$

Based on (4.18), the closed-loop transfer function from v_{ref} to v_o can be obtained as

$$G_{cv}(z) = \frac{k_r G_p(z) z^k}{z^N - Q(z) + k_r G_p(z) z^k} \tag{4.19}$$

According to (4.19), the voltage control loop is stable if all roots of the denominator are placed inside the unit circle centered at the origin of z-plane. Usually, a sufficient condition is employed for evaluating the stability [114], which is written as

$$\left|Q(z)-k_r G_p(z)z^k\right|<1,\ \forall z=e^{j\omega T_s},\ 0\le\omega T_s\le\pi \tag{4.20}$$

where T_s is the sampling frequency. It is clear that the inequality in (4.20) is solvable only if the condition

$$1-\left|Q(e^{j\omega T_s})\right|\le k_r\left|G_p(e^{j\omega T_s})\right|\le 1+\left|Q(e^{j\omega T_s})\right|,\ 0\le\omega T_s\le\pi \tag{4.21}$$

holds. In order to satisfy the above condition, the value of k_r should be within a certain range

$$0\le k_r\le\frac{1+\left|Q(e^{j\omega T_s})\right|}{\left|G_p(e^{j\omega T_s})\right|},\ 0\le\omega T_s\le\pi \tag{4.22}$$

In this chapter, the low-pass filter $Q(z)$ is designed as $Q(z) = 0.25z + 0.5 + 0.25/z$ with a cut-off frequency of 3.63 kHz. The detailed inner-loop control parameters are provided in Table 4.1.

Table 4.1 Parameters for the inner-loop voltage controller

Parameters	Symbols	Values
DC-link voltage	u_{dc}	140 V
AC voltage magnitude	V_0	100 V
Nominal frequency	f_0	50 Hz
Filter inductance	L_f	0.5 mH
Filter capacitance	C_f	40 μF
Switching frequency	f_c	20 kHz
Sampling frequency	f_s	20 kHz
Number of delay units	N	400
Current control gain	k_c	5
Repetitive control gain	k_r	0.2
Number of advance units	k	4

Taking both the stability and the dynamic response into account, the repetitive control gain k_r is selected as 0.2 in order to reach a good compromise between the two aspects. The last step is to ensure system stability by properly designing the time advance unit z^k. Fig. 4.7 displays the Nyquist locus of $Q(z) - k_r G_p(z) z^k$ with different k. It can be observed that the stability condition is satisfied when $3 \le k \le 6$, as all roots are always located

inside the unit circle. To obtain the largest stability margin, the time advance integer k is selected as 4 in this chapter.

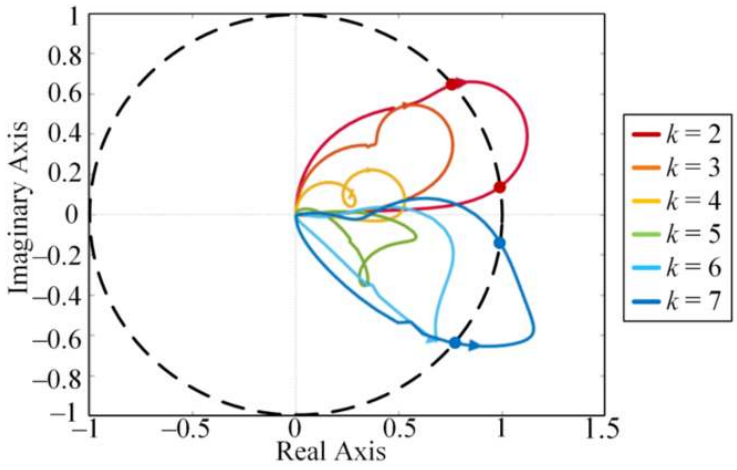


Fig. 4.7. Nyquist plot of $Q(z) - k_r G_p(z) z^k$ with different k.

4.3.3. Two-dimensional Impedance Shaping

To guarantee the harmonic power-sharing accuracy and eliminate the circulating harmonic currents, a two-dimensional impedance-shaping control is implemented to adaptively regulate the VSI resistance and inductance. As shown in Fig. 4.5, the R-axis impedance-shaping control is implemented to ensure the lowest-order harmonic power-sharing accuracy (In this chapter, the 3rd-order harmonic power is considered as the lowest-order harmonic power). Besides, the value of R_i is determined by the distributed consensus control algorithm

$$R_i = \frac{k_d}{s} \cdot \sum_{j=1}^{n} a_{ij} \left(\frac{S_i^3}{S_{iN}} - \frac{S_j^3}{S_{jN}} \right) \tag{4.23}$$

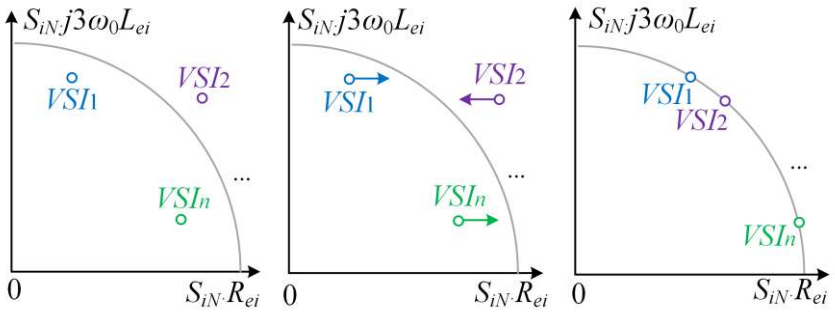
where a_{ij} is the element of communication matrix. $a_{ij} = 1$ means VSI#i is communicating with VSI#j, while $a_{ij} = 0$ indicates that no information is exchanged between VSI#i and VSI#j. H_i^3 and H_j^3 are the 3rd-order harmonic powers of VSI#i and VSI#j, respectively. k_d is the integral gain, and it determines the convergence rate of the harmonic power sharing. In the meanwhile, the L-axis impedance-shaping control is also implemented to provide an additional DOF for the impedance shaping, and the value of L_i is determined as

$$L_i = \frac{k_q}{s} \cdot \sum_{j=1}^{n} a_{ij} \left(\frac{S_i^{total}}{S_{iN}} - \frac{S_j^{total}}{S_{jN}} \right) \tag{4.24}$$

$$S^{total} = \sum_{h=3,5,7,\ldots} S^{h} \tag{4.25}$$

where S_i^{total} and S_j^{total} are the total harmonic powers of VSI#i and VSI#j, respectively. To avoid the control conflict and decouple the R-axis and L-axis impedance-shaping controls, the integral gain k_q should be tuned much smaller than the integral gain k_d so that the dynamic response of the R-axis impedance-shaping control is much faster than that of the L-axis impedance shaping control.

The principle of the proposed control strategy is briefly illustrated by plotting VSI effective impedance trajectories in the complex impedance plane. Fig. 4.8 shows the VSI resistance regulation process, during which the impact of the L-axis impedance-shaping control is not considered due to its slow dynamic response.



(a). (b). (c).

Fig. 4.8. Principle of the R-axis impedance-shaping control. (a) Original case. (b) Transient performance. (c) Steady-state performance.

For the original case in Fig. 4.8(a), the 3rd-order harmonic power is not proportionally shared among VSIs because of the effective harmonic impedance mismatch. When the R-axis impedance-shaping controller is implemented in Fig. 4.8(b), the resistance of a VSI will increase if its rated 3rd-order harmonic power is larger than the neighboring average value, and will decrease in the opposite scenario. A consensus will be finally reached and makes the 3rd-order harmonic power proportionally shared among parallel VSIs according to their power ratings. In the steady state, the VSI effective inductances and resistances shall satisfy the below condition

$$\left|S_{iN}R_{ei} + jS_{iN}3\omega_0L_{ei}\right| = C \quad (\forall i \in 1,2,\ldots,n) \tag{4.26}$$

where C is a constant for all VSIs. The constraint in (4.26) is also illustrated in Fig. 4.8 (c), where all the VSI effective impedances (for the 3rd-order harmonic) are located on the orbit of a quarter circle.

From (4.26), the relationship between effective resistances and effective inductances is expressed as

$$S_{iN}R_{ei} = \sqrt{C^2 - (3S_{iN}\omega_0 L_{ei})^2} \tag{4.27}$$

For higher-order harmonics, the magnitude of the VSI rated effective impedance can be calculated as

$$S_{iN} \cdot \left|Z_{ei}(jh\omega_0)\right| = \sqrt{(S_{iN}R_{ei})^2 + (S_{iN}h\omega_0 L_{ei})^2} \tag{4.28}$$

$$S_{iN} \cdot \left|Z_{ei}(jh\omega_0)\right| = \sqrt{C^2 + (h^2 - 3^2)\cdot(S_{iN}\omega_0 L_{ei})^2} \tag{4.29}$$

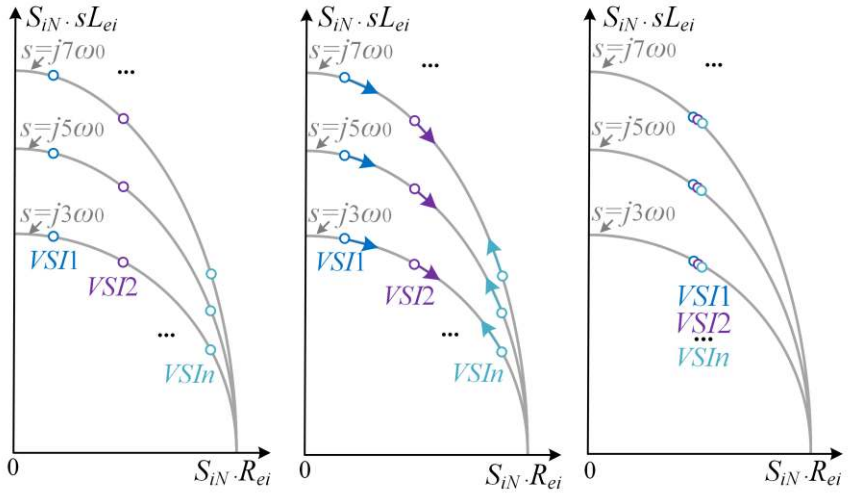
From (4.5) and (4.25), the rated total harmonic power of VSI#*i* is calculated as

$$\frac{H_i^{total}}{S_{iN}} = \sum_{h=3,5,7,9,\ldots} \frac{V_0^f \cdot \left|v_{pcc}^h\right|}{2 \cdot S_{iN}\left|Z_{ei}(jh\omega_0)\right|} \tag{4.30}$$

$$\frac{H_i^{total}}{S_{iN}} = \sum_{h=3,5,7,9,\ldots} \frac{V_0^f \cdot \left|v_{pcc}^h\right|}{2 \cdot \sqrt{C^2 + (h^2 - 3^2)\cdot(S_{iN}\omega_0 L_{ei})^2}} \tag{4.31}$$

(4.31) implies that the rated total harmonic power H_i^{total}/S_{iN} is a monotonic decreasing function of $S_{iN}L_{ei}$. In other words, the rated total harmonic power of a VSI will decrease if its rated effective inductance increases, and vice versa. With this principle, the *L*-axis impedance-shaping control can be used to equalize the rated effective inductances for all VSIs.

Fig. 4.9 illustrates the VSI inductance regulation process, during which the fast *R*-axis impedance-shaping control ensures the 3rd-order harmonic power-sharing accuracy.



(a). (b). (c).

Fig. 4.9. Principle of the *L*-axis impedance-shaping control. (a) original case. (b) transient performance. (c) steady-state performance.

In Fig. 4.9(a), although the 3rd-order harmonic power has been proportionally shared among multiple VSIs according to their power ratings, VSI effective impedances are still not equalized. Based on the previous analysis, the *L*-axis impedance-shaping control will properly regulate VSI inductances according to the rated total harmonic power, and the transient performance is illustrated in Fig. 4.9(b). Finally, the consensus will be reached in Fig. 4.9(c) such that all the VSI effective impedances converge to the unified equilibrium point.

In the steady state, VSI effective resistances and inductances are well regulated to be inversely proportional to their power ratings.

$$S_{1N}R_{e1} = S_{2N}R_{e2} = ... = S_{nN}R_{en} \tag{4.32}$$

$$S_{1N}L_{e1} = S_{2N}L_{e2} = ... = S_{nN}L_{en} \tag{4.33}$$

Fig. 4.10 illustrates the system equivalent circuit at selective harmonic frequencies. Without loss of generality, nonlinear loads can be lumped together and equivalently modeled by multiple parallel harmonic current sources (i^3_L, i^5_L, i^7_L…).

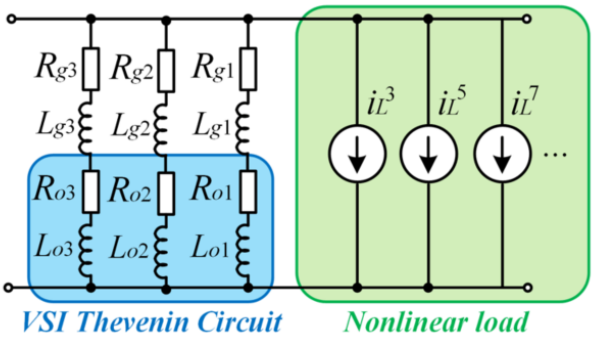


Fig. 4.10. System equivalent circuit at selective harmonic frequencies.

According to the Superposition theorem, the *h*th-order (*h* =3,5,7…) harmonic current of a VSI is derived as

$$i_i^h = i_L^h \cdot \frac{Z_s(jh\omega_0)}{(R_{gi} + R_{oi}) + jh\omega_0(L_{gi} + L_{oi})} \tag{4.34}$$

where $Z_s(jh\omega_0)$ is the total harmonic impedance of parallel VSIs. From (4.32) to (4.34), it can be obtained that

$$\frac{i_1^h}{S_{1N}} = \frac{i_2^h}{S_{2N}} = ... = \frac{i_n^h}{S_{nN}} \tag{4.35}$$

Therefore, the *h*th-order load harmonic power can be accurately shared among parallel VSIs according to their power ratings. From the above analysis, it is clear that the power sharing is accurate at all harmonic frequencies (as long as the inner-loop voltage control

can provide the harmonic compensation ability). In addition, the power-sharing accuracy is also independent of the number or the type of nonlinear loads.

4.3.4. Design of Distributed Averaging Controller

To properly design the distributed averaging controller gains k_d and k_q, the system is linearized at the equilibrium point. It should be mentioned that the dynamic response of the voltage controller is not considered for simplicity. This assumption is reasonable as the response time of the voltage controller is much faster than that of the impedance-shaping controllers. With this assumption, the small-signal model of the impedance-shaping control can be established as

$$\frac{d}{dt}\Delta R_i = k_d \cdot \sum_{j=1}^{n} a_{ij}\left(\frac{\Delta S_i^3}{S_{iN}} - \frac{\Delta S_j^3}{S_{jN}}\right) \tag{4.36}$$

$$\frac{d}{dt}\Delta L_i = k_q \cdot \sum_{j=1}^{n} a_{ij}\left(\frac{\Delta S_i^{total}}{S_{iN}} - \frac{\Delta S_j^{total}}{S_{jN}}\right) \tag{4.37}$$

The plant model can also be derived as

$$\Delta S_i^3 = \sum_{j=1,2,\ldots,n} \frac{\partial S_i^3}{\partial R_j} \cdot \Delta R_j + \sum_{j=1,2,\ldots,n} \frac{\partial S_i^3}{\partial L_j} \cdot \Delta L_j \tag{4.38}$$

$$\Delta S_i^{total} = \sum_{j=1,2,\ldots,n} \frac{\partial S_i^{total}}{\partial R_j} \cdot \Delta R_j + \sum_{j=1,2,\ldots,n} \frac{\partial S_i^{total}}{\partial L_j} \cdot \Delta L_j \tag{4.39}$$

Combing the controller model and the plant model together, the linearized system state-space model can be derived as

$$\frac{d}{dt}\boldsymbol{x}(t) = \boldsymbol{A_{inv}} \cdot \boldsymbol{x}(t) \tag{4.40}$$

where the state variables are represented as $\boldsymbol{x} = [\Delta R_1, \Delta R_2, \ldots, \Delta R_n, \Delta L_1, \Delta L_2, \ldots, \Delta L_n]$. The detailed expression of the matrix $\boldsymbol{A_{inv}}$ is provided hereinafter

$$\boldsymbol{A_{inv}} = \begin{bmatrix} \boldsymbol{A}_1\boldsymbol{B}_1 & \boldsymbol{A}_1\boldsymbol{B}_2 \\ \boldsymbol{A}_2\boldsymbol{B}_3 & \boldsymbol{A}_2\boldsymbol{B}_4 \end{bmatrix} \tag{4.41}$$

where,

$$\boldsymbol{A}_1 = k_d \cdot \begin{bmatrix} \sum_{j=1,2,\ldots,n} \frac{a_{ij}}{S_{1N}} & \cdots & \frac{-a_{1n}}{S_{nN}} \\ \cdots & \cdots & \cdots \\ \frac{-a_{n1}}{S_{nN}} & \cdots & \sum_{j=1,2,\ldots,n} \frac{a_{nj}}{S_{nN}} \end{bmatrix} \tag{4.42}$$

$$\boldsymbol{A}_2 = k_q \cdot \begin{bmatrix} \sum_{j=1,2,\ldots,n} \frac{a_{ij}}{S_{1N}} & \cdots & \frac{-a_{1n}}{S_{nN}} \\ \cdots & \cdots & \cdots \\ \frac{-a_{n1}}{S_{nN}} & \cdots & \sum_{j=1,2,\ldots,n} \frac{a_{nj}}{S_{nN}} \end{bmatrix} \tag{4.43}$$

$$\boldsymbol{B}_1 = \begin{bmatrix} \frac{\partial S_1^3}{\partial R_1} & \cdots & \frac{\partial S_1^3}{\partial R_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial S_n^3}{\partial R_1} & \cdots & \frac{\partial S_n^3}{\partial R_n} \end{bmatrix} \quad \boldsymbol{B}_2 = \begin{bmatrix} \frac{\partial S_1^3}{\partial L_1} & \cdots & \frac{\partial S_1^3}{\partial L_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial S_n^3}{\partial L_1} & \cdots & \frac{\partial S_n^3}{\partial L_n} \end{bmatrix} \tag{4.44}$$

$$\boldsymbol{B}_3 = \begin{bmatrix} \frac{\partial S_1^{total}}{\partial R_1} & \cdots & \frac{\partial S_1^{total}}{\partial R_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial S_n^{total}}{\partial R_1} & \cdots & \frac{\partial S_n^{total}}{\partial R_n} \end{bmatrix} \quad \boldsymbol{B}_4 = \begin{bmatrix} \frac{\partial S_1^{total}}{\partial L_1} & \cdots & \frac{\partial S_1^{total}}{\partial L_n} \\ \cdots & \cdots & \cdots \\ \frac{\partial S_n^{total}}{\partial L_1} & \cdots & \frac{\partial S_n^{total}}{\partial L_n} \end{bmatrix} \tag{4.45}$$

It has been widely accepted that the system dynamic and stability can be reflected by the dominant eigenvalues of the matrix $\boldsymbol{A_{inv}}$. Fig. 4.11 depicts the dominant eigenvalue loci when k_q = 0.01, and k_d increases from 50 to 150.

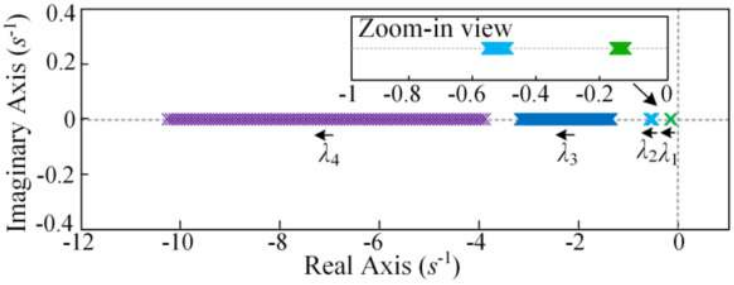


Fig. 4.11. Loci of dominant eigenvalues when k_q = 0.01 and k_d changes from 50 to 150.

In Fig. 4.11, it is observed that the increase of k_d mainly influences the eigenvalues λ_3 and λ_4, which are related to the fast *R*-axis impedance-shaping control. In order to guarantee a satisfactory control performance, the communication sampling rate (20 Hz in this chapter) should be at least 5-10 times higher than the bandwidth of the *R*-axis impedance-shaping control. Therefore, k_d is selected as 100.

Fig. 4.12 shows the loci of dominant eigenvalues when k_d = 100, and k_q increases from 0.005 to 0.015. It is clear that the increase of k_q mainly influences the eigenvalues λ_1 and λ_2, which are related to the slow *L*-axis impedance-shaping control. The value of k_q should be properly designed so that the dynamic response of *R*-axis impedance-shaping

control is well decoupled with that of the L-axis impedance-shaping control. In other words, λ_3 needs to be at least 5-10 times larger than λ_2. With this consideration, the value of k_q is selected as 0.01 in this chapter.

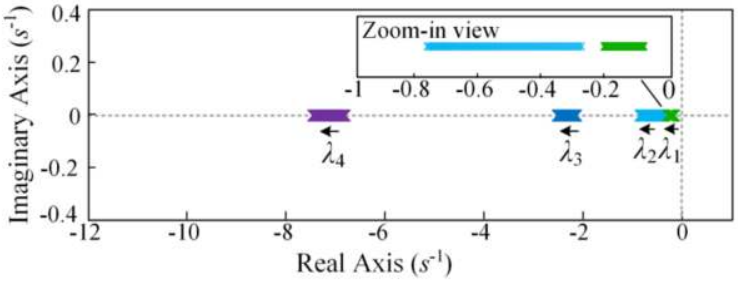


Fig. 4.12. Loci of dominant eigenvalues when k_d = 100 and k_q changes from 0.005 to 0.015.

4.4. Simulation and Experimental Results

To verify the effectiveness of the proposed control strategy, an islanded microgrid was built under the PLECS environment. Fig. 4.13 illustrates the circuit configuration, where three parallel H-bridge single-phase VSIs are connected to the PCC through grid impedances. To guarantee the system reliability, each VSI can communicate with both neighbors through low-bandwidth communication links (20 Hz bandwidth).

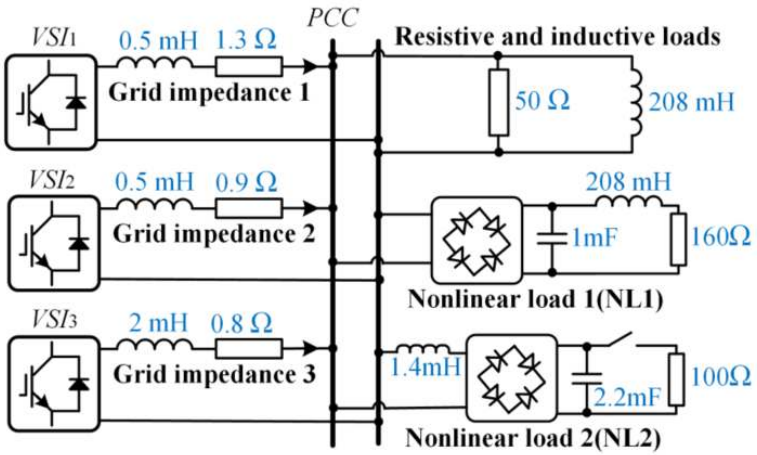


Fig. 4.13. Circuit configuration for the experimental verification.

Fig. 4.14 shows the simulation results when all the VSIs have the same power ratings. It can be observed that VSI currents are different when the proposed impedance shaping control is not implemented. In comparison, VSI output currents become almost identical to the proposed control scheme. Besides, Fig. 4.15 shows the simulation results when the three VSIs have unequal power ratings (S_{1N}: S_{2N}: S_{3N}=1:1:1). Similarly, the proposed

impedance shaping control can still accurately share the load current with respect to the VSI power ratings.

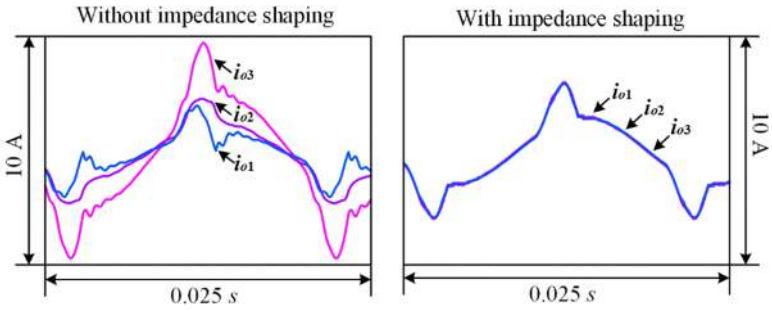


Fig. 4.14. Simulation results when VSIs have equal ratings. (S_{1N}: S_{2N}: S_{3N} =1:1:1)

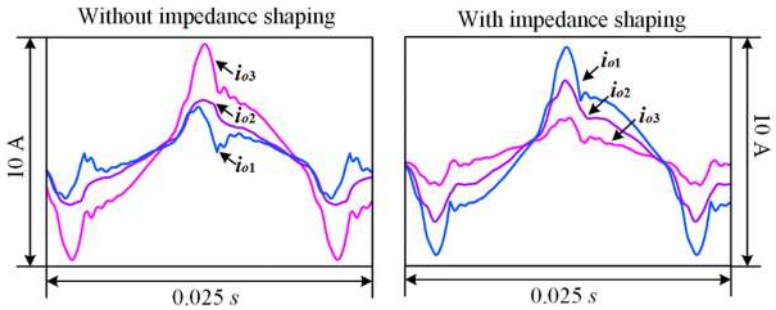


Fig. 4.15. Simulation results when VSIs have unequal ratings. (S_{1N}: S_{2N}: S_{3N} =3:2:1)

Hardware experiments were also conducted for verification. Fig. 4.16 provides the photo of the laboratory setup, and all the digital controls and samplings are processed by a PLECS RT box. In this chapter, five different cases have been studied and tested, i.e., equal power sharing, proportional power sharing, line impedance change, multiple nonlinear loads, and loss of communication links.

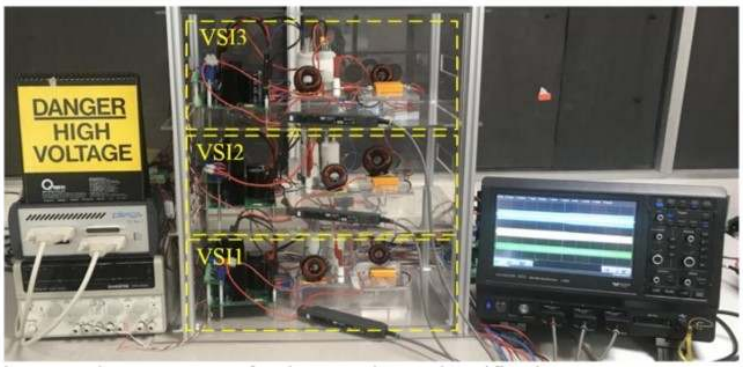


Fig. 4.14. Laboratory setup for the experimental verification.

4.4.1. Equal Power Sharing

In the first case, all three VSIs have the same power ratings (S_{1N} = S_{2N} = S_{3N} =1000 VA), and the experimental result is shown in Fig. 4.17. Initially, the harmonic current sharing is poor when the proposed control strategy is not implemented. As a result, VSI output currents are different from each other. At t_1, the proposed impedance-shaping control is enabled, and VSI output currents are gradually equalized in the steady state.

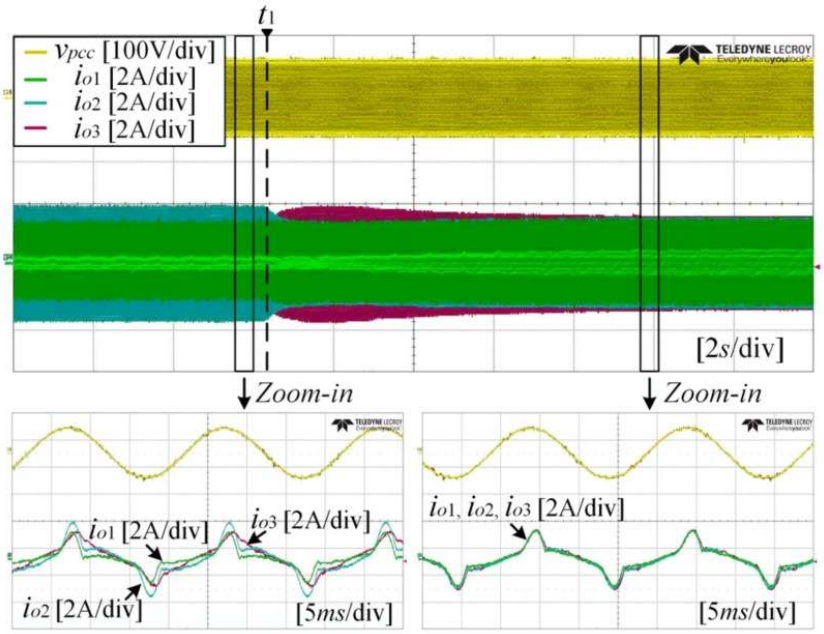


Fig. 4.15. Experimental result when all three VSIs have the same power ratings.

Table 4.2 shows the current Fast Fourier analysis result. When the proposed control strategy is not implemented, the sum of VSI harmonic current magnitudes is even larger than the total load harmonic current magnitude, indicating that additional harmonic power has been produced. As a contrast, the proposed control strategy can effectively enhance the harmonic current sharing. Moreover, as the VSI effective resistances and inductances are reshaped to be inversely proportional to their capacities, the fundamental power sharing performance is also improved.

Table 4.2 Current FFT analysis result

	Without the proposed control (A)					With the proposed control (A)				
Harmonic	1st	3rd	5th	7th	9th	1st	3rd	5th	7th	9th
VSI#1	0.86	0.43	0.31	0.18	0.09	1.14	0.42	0.29	0.15	0.07
VSI#2	1.46	0.60	0.44	0.23	0.06	1.25	0.42	0.28	0.16	0.06
VSI#3	1.38	0.33	0.17	0.08	0.02	1.29	0.42	0.29	0.15	0.05
Total load	3.69	1.27	0.86	0.46	0.17	3.68	1.26	0.86	0.45	0.18

4.4.2. Proportional Power Sharing

In this case, the power ratings of the three VSIs are not the same ($S_{2N} = 2S_{1N} = 2S_{3N} =$ 2000 VA). Therefore, the total load power is expected to be proportionally shared among parallel VSIs. Fig. 4.18 shows the experimental result, and the proposed control strategy is enabled at t_1. In the steady state, all the VSI output currents are exactly in phase with each other, but the magnitude of i_{o2} is twice as much as that of i_{o1} and i_{o3}.

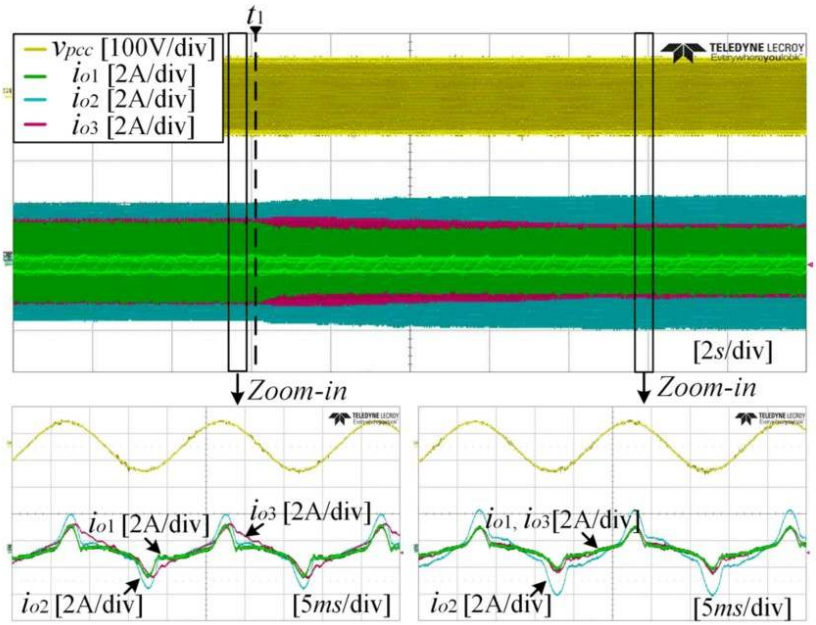


Fig. 4.16. Experimental result when VSIs have different power ratings.

Table 4.3. shows the current Fast Fourier analysis result with and without the proposed control strategy. It is clearly seen that the harmonic power can be proportionally shared according to the power ratings. Notice that a small fundamental power sharing error may still exist because of voltage sensor measurement errors. Nevertheless, the fundamental power sharing error can be eliminated by the control strategy developed in Chapter 3.

Table 4.3 Current FFT analysis result

	Without the proposed control (A)					With the proposed control (A)				
Harmonic	1st	3rd	5th	7th	9th	1st	3rd	5th	7th	9th
VSI#1	0.91	0.43	0.31	0.18	0.09	0.82	0.32	0.23	0.11	0.05
VSI#2	1.36	0.60	0.44	0.23	0.06	1.88	0.64	0.44	0.22	0.08
VSI#3	1.42	0.33	0.17	0.08	0.02	0.98	0.32	0.22	0.11	0.04
Total load	3.69	1.27	0.86	0.46	0.17	3.68	1.27	0.86	0.45	0.16

4.4.3. Line Impedance Change

Next, the feasibility of the proposed control strategy under variable line impedances has been verified in this section, and Fig. 4.19 shows the experimental result. The line resistance of VSI#1 gradually changes from 1.3 Ω to 2.3 Ω right after t_1. As a result, the instantaneous power sharing is not accurate, as i_{o1} is less than i_{o2} and i_{o3}. Nevertheless, the impact of the line impedance change has been gradually ameliorated by the proposed impedance-shaping controller. In the steady state, it is observed that all the VSI output currents are equalized again.

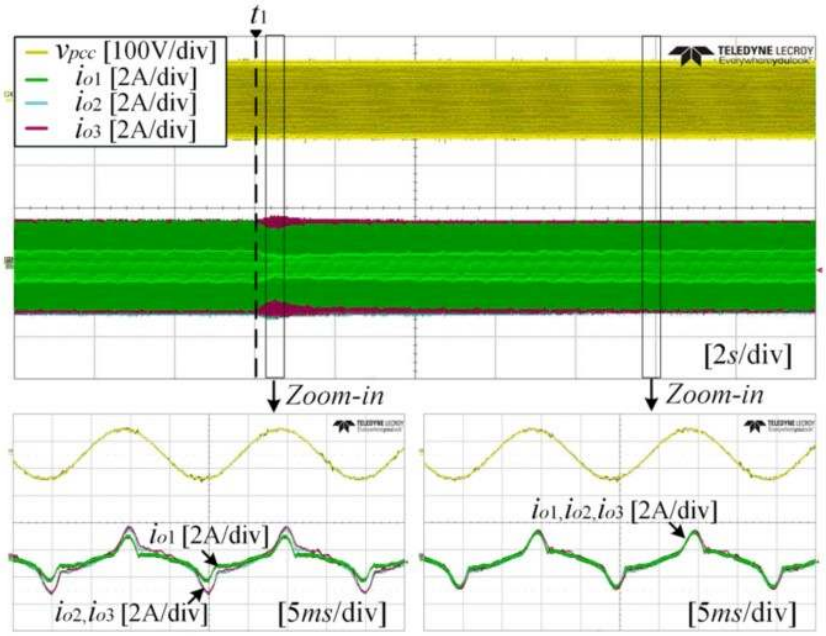


Fig. 4.17. Experimental result under variable line impedances.

4.4.4. Multiple Nonlinear Loads

Next, the experimental result in the presence of multiple nonlinear loads is also provided and shown in Fig. 4.20. Originally, the first nonlinear load is connected at the PCC. At t_1, the second nonlinear load is also added and the total harmonic currents increase. For both scenarios, the proposed impedance-shaping control can ensure the harmonic current sharing accuracy and the VSI output currents are equalized in the steady state.

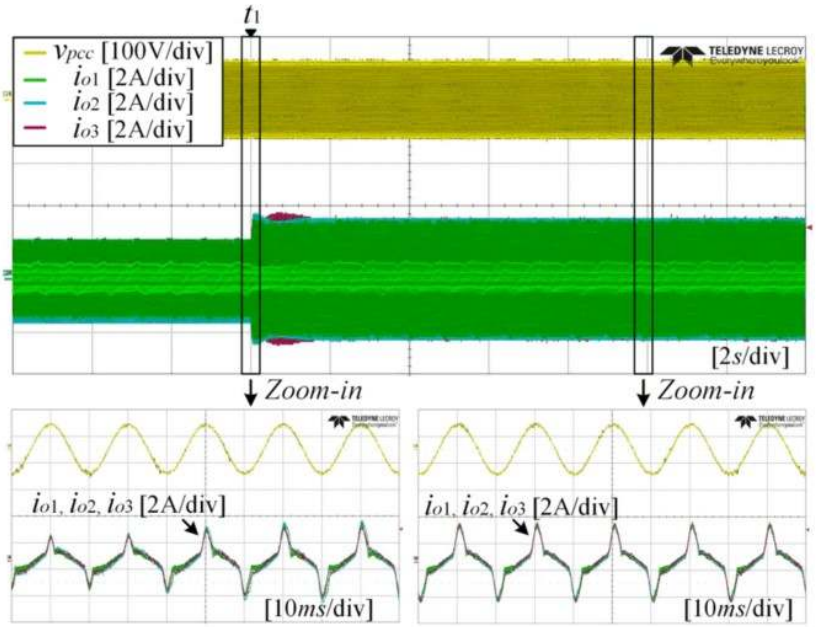


Fig. 4.20. Experimental result for multiple nonlinear loads.

4.4.5. Loss of Communication Links

The reliability of the proposed control strategy has also been verified under the case of communication failures. Firstly, a single communication link failure is considered, and the experimental result is shown in Fig. 4.21. In Fig. 4.21, the communication link between VSI#2 and VSI#3 is lost at t_1. The second nonlinear load is added at t_2 and then removed at t_3. It can be seen that the power-sharing effectiveness is not influenced by the communication link failure between VSI#2 and VSI#3, since the communication topology still maintains a spanning-tree configuration. Therefore, VSI output currents are equalized in the steady state.

Next, the worst case has been considered that multiple communication failures occur simultaneously. Fig. 4.22 shows the experimental result. At t_1, the communication link between VSI#1 and VSI#3 is also lost. The second nonlinear load is added at t_2 and then removed at t_3. It can be found out that the power-sharing effectiveness is still maintained even for the worst case. Although multiple communication failures have isolated VSI#3 in the communication graph, the impedance-shaping process has already been finished before t_1. As a result, the harmonic power-sharing accuracy will not be influenced unless the microgrid configuration is changed.

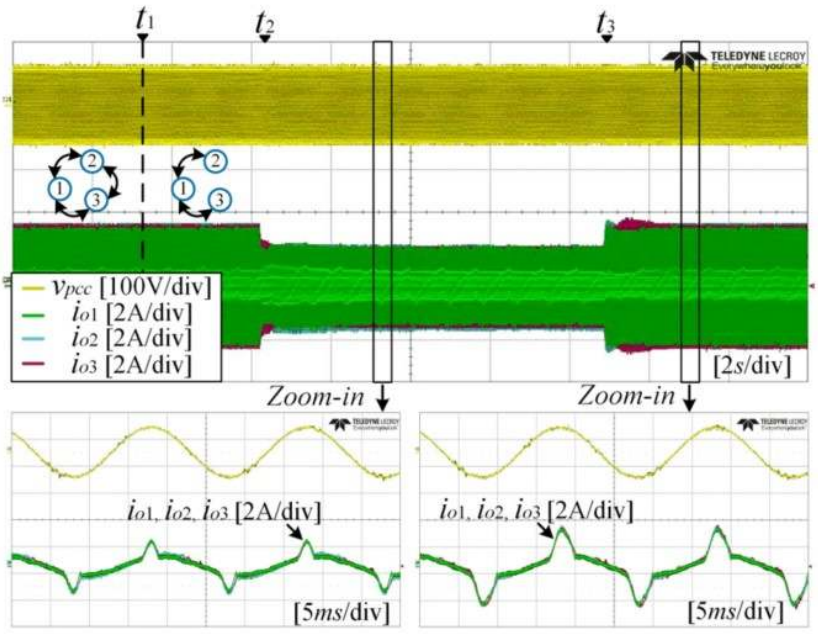


Fig. 4.21. Experimental result under a single communication link failure.

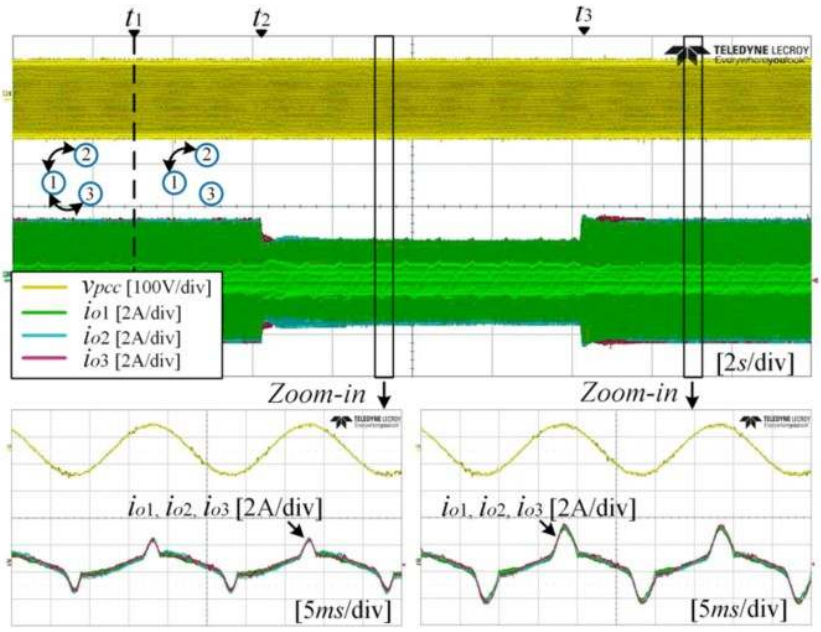


Fig. 4.22. Experimental result under multiple communication link failures.

4.5. Summary

In this chapter, the improper harmonic current sharing issue due to mismatched line impedances is analyzed. To enhance the harmonic power sharing accuracy and eliminate circulating harmonic currents, a two-dimensional impedance-shaping control has been developed. The proposed control strategy is based on the distributed consensus control

algorithm and can provide an additional DOF for the impedance shaping. As a result, the proper harmonic power-sharing result is guaranteed and immunes from complex and mismatched grid impedances. The feasibility of the proposed control strategy has been verified by a typical islanded microgrid with three parallel VSIs and can be further extended for multiple-VSI scenarios. To implement the proposed method on multiple parallel VSIs, at least a spanning tree communication network is required. The spanning tree refers to an undirected graph that connects all the vertices (VSIs) with a minimum possible number of edges (communications). For example, the communication network in the left side covers the spanning tree while the one in the middle is the spanning tree. Both of the two communication networks can work well for harmonic power sharing. However, one of the VSIs is not communicating with others in the right figure. As a consequence, the proposed distributed control strategy cannot be performed well.

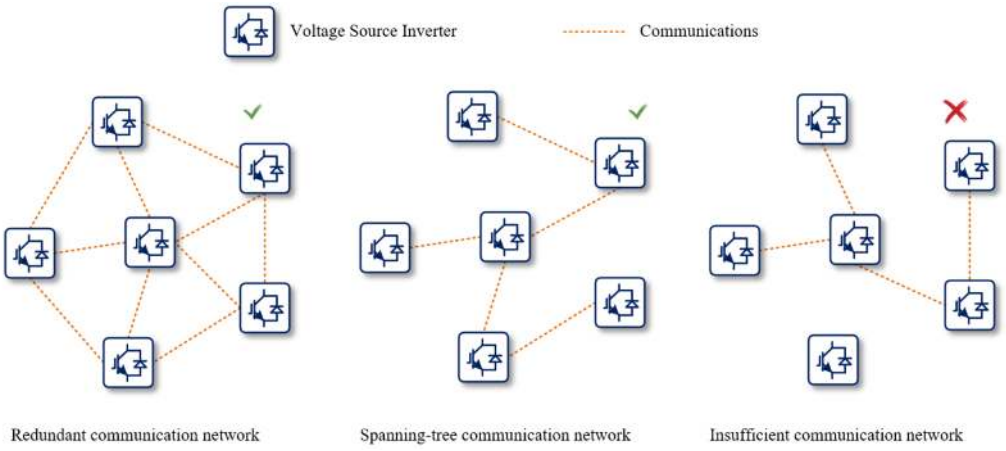


Fig. 4.23. Requirements for the application on multiple VSIs.

Chapter 5 Synchronization Stability for the Grid Integration of DESS

The coordinated control of multiple VSIs has been extensively discussed in previous chapters. Apart from power management schemes, another important aspect with regard to the grid integration of DESSs is synchronization stability, which can be affected by various factors, such as grid structure and feeder impedances. It should be mentioned that DESSs are distributed at different places of a microgrid. From the perspective of a local DESS, the information about the rest of the microgrid, which is crucial to the control parameter design and stability analysis, can hardly be obtained. As a result, unpredicted low-frequency angle oscillations and even the loss of synchronization may occur and pose a significant threat to the power system. In view of these challenges, this chapter is based on the actual view of an individual VSI, to whom the rest DESSs and microgrid is essentially a “black box”. In view of this challenge, a design-oriented synchronization stability analysis for grid integration of DESS. Through this effort, a satisfactory 60-degree stability margin can be ensured even without prior knowledge of the power system.

5.1. Introduction

Driven by the demand of carbon footprint reduction, the power grid is undergoing an evolution with more RESs and DESSs integrated through VSIs. One crucial aspect for VSI operation is the phase synchronization stability, which refers to the ability of a VSI to remain in phase with the power grid after being subjected to a disturbance [115]. In the conventional power grid, the phase synchronization is mainly determined by the swing equation of synchronous machines [116]. Nevertheless, as more and more power-electronic converters are coupled to the grid, their interactions become more complicated, which would probably result in low-frequency angle oscillations and even the loss of synchronization [117]–[118].

As mentioned in Chapter 1, VSIs can be classified into grid-feeding VSIs and grid-forming VSIs. Grid-feeding VSIs are usually controlled as current sources, where the PLL is responsible for the phase synchronization. It is reported that low-frequency angle oscillations will occur because of an improper PLL bandwidth [119], a low short-circuit ratio (SCR) [120], as well as the coupling among different control loops [121]. Besides, grid-forming VSIs are controlled as voltage sources. Instead of relying on PLL, various control schemes, such as droop control, power synchronization control, and the virtual synchronous generator control have been proposed to facilitate the grid synchronization. Similarly, the low-frequency oscillations also occur for grid-forming VSIs. It is revealed that improper VSI outer-loop control parameters would result in a negative damping torque and makes the VSI phase angle sensitive to load variations [29], [122]. In addition, an insufficient feeder impedance may also trigger a resonance as well as undammed oscillations [123]. Though the reasons for angle oscillations are different, the oscillation period is generally ranging from hundreds of milliseconds to dozens of seconds [37].

To simplify the modelling and analysis, many existing works assume the grid to be an ideal voltage source, whose frequency is independent of the active power. However, such an assumption is not reasonable since the practical grid is formed by various power generation units, rather than an infinite AC bus. As a result, the designed VSI controller may fail to fulfill the stability requirements. The common solution towards it is to derive the state-space model of individual units and correlate them together to establish the entire power grid model [124]–[126]. Through eigenvalue analysis, the oscillatory and unstable modes can be identified. Based on that, the angle oscillations can be damped through the power system stabilizer [127] and other damping approaches [128], [129]. Nevertheless, the complexity of modelling increases exponentially as the number of

power generation units goes up. Therefore, the practicability of this approach will be overwhelmed by the tremendous effort spent on modelling. To relieve the computation burden, a component connection method is adopted in [130]. The general idea behind is to partition a complex power grid into several subsystems and algebraically reassemble them in a more efficient way. In addition to this, the power-internal voltage model [131], [132], the DC-link time-scale converter model [133], [134], and the apparent impedance analysis [135] can also be implemented to neglect the dynamics of fast inner-loop control, reduce the modelling effort, and therefore provide clear insights into the synchronization dynamics. Nevertheless, the modelling and analysis process requires detailed power grid information, such as the grid structure, feeder impedances, and parameters of every generation unit. From the perspective of a local VSI, it is difficult to obtain complete information.

An alternative solution from the engineering practice is to regard the power grid as a "black box", whose internal parameters can be obtained through the measuring terminal characteristics, rather than theoretically deriving the overall system model. One typical example is reported as impedance-based stability analysis [136], [137], which evaluates the stability of two interconnected systems based on their impedance ratio. To analyse the low-frequency stability, the *dq*-frame impedances are usually adopted, where the VSI impedance Z_i and the grid impedance Z_g are represented as the 2×2 matrix [138]–[19]. According to the generalized Nyquist criterion (GNC), the system is stable if the characteristic loci of $Z_i \times Z_g^{-1}$ does not encircle the point (–1, j0) [138]. Despite the high prediction accuracy, the GNC-based method requires the mathematical expression of Z_g, which can hardly be acquired as discussed earlier. By contrast, it is more practical to measure the individual element of Z_g through frequency sweeps [140], namely, inject *dq*-frame current perturbations and observe the corresponding *dq*-frame voltage responses. The measured elements of Z_g are respectively compared with those of Z_i through sub-Bode diagrams to predict stability and low-frequency oscillations. However, this approach is only valid if the impedance matrices are diagonal-dominant [139]. Moreover, the impedance matrices contain four elements: Z_{dd}, Z_{dq}, Z_{qd}, and Z_{qq}. As a result, an extra impedance analyser must be required to perform at least two groups of independent measurements at each frequency [140], [141]. Besides, the measurements of dq-frame impedances will be affected by synchronization dynamics and become inaccurate in the low-frequency range [142]. As a result, low-frequency oscillations cannot be well identified and mitigated.

In view of this challenge, this chapter develops a design-oriented approach to analyse the grid synchronization stability of a VSI. Through an analogy with the conventional impedance-based analysis, it is found that the synchronization stability can be evaluated by comparing the frequency power characteristic FPC, i.e., the transfer function from frequency to active power, of a VSI and that of the power grid. Furthermore, a frequency response identification (FRI) technique is also proposed for the simple acquisition of power grid FPC without grid information. In comparison with the existing techniques, the proposed one exhibits the following merits:

1.) There is no need to acquire the grid information and derive a complicated power grid model. Instead, the power grid characteristic can be readily measured by the VSI itself, without requiring any extra devices.

2.) Through the comparison between the FPC of VSI and that of power grid, clear insights are gained into the synchronization dynamics. The time period and severity of low-frequency angle oscillations can be explicitly identified.

3.) The FPC comparison result provides helpful guidance on the VSI controller design. Benefitted from that, undesired low-frequency oscillations can be effectively damped by reshaping the FPC of VSI.

5.2. Problem Formulation

5.2.1. High-entropy Model

Fig. 5.1 illustrates the circuit configuration of a grid-connected VSI, where R_g and L_g are the feeder resistance and inductance; P_i is the active power of VSI; P_g is the active power provided by the power grid; P_L is the active power consumed by a local load; V_i and V_g are the voltage magnitudes of VSI and the grid, respectively; θ_i and θ_g stand for the phase angles of VSI voltage and grid voltage. With an attempt to attenuate high-frequency switching harmonics, either the *LCL* filter ($L_{f2} \neq 0$) or the *LC* filter ($L_{f2} = 0$) can be installed at the AC output of the VSI.

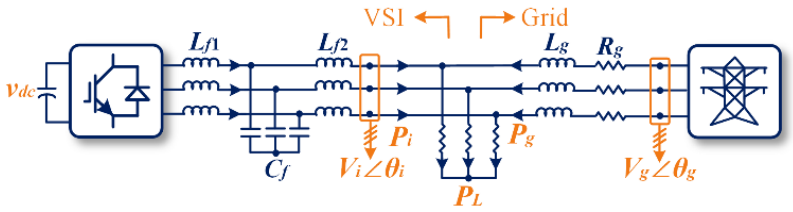


Fig. 5.1. Circuit configuration of a grid-connected VSI.

Under the synchronous reference frame seen from the VSI, the *d*-axis VSI voltage v_{id} equals V_i and the *q*-axis voltage v_{iq} becomes zero. Accordingly, the voltage drops across feeder impedances can be expressed as

$$\begin{cases} V_i - V_g \cos\delta = L_g \dfrac{di_d}{dt} - \omega_0 L_g i_q + R_g i_d \\ 0 - V_g \sin\delta = L_g \dfrac{di_q}{dt} + \omega_0 L_g i_d + R_g i_q \end{cases} \tag{5.1}$$

where $\delta = \theta_g - \theta_i$ is the phase angle difference between VSI and the grid. i_d and i_q are the *dq*-frame currents flowing from the VSI to the power grid. Linearizing (5.1) gives

$$\begin{cases} \Delta V_i + V_g \sin\delta_0 \Delta\delta = L_g \dfrac{d\Delta i_d}{dt} + R_g \Delta i_d - \omega_0 L_g \Delta i_q \\ -V_g \cos\delta_0 \Delta\delta = L_g \dfrac{d\Delta i_q}{dt} + R_g \Delta i_q + \omega_0 L_g \Delta i_d \end{cases} \tag{5.2}$$

where δ_0 is the steady-state phase angle difference between the VSI and grid. Applying the Laplace transforms to (5.2) gives

$$\begin{cases} (sL_g + R_g)\Delta i_d - \omega_0 L_g \Delta i_q = \Delta V_i + V_g \sin\delta_0 \Delta\delta \\ (sL_g + R_g)\Delta i_q + \omega_0 L_g \Delta i_d = -V_g \cos\delta_0 \Delta\delta \end{cases} \tag{5.3}$$

Based on (5.3), the *dq*-frame current perturbations Δi_d and Δi_q are calculated as

$$\begin{aligned} \Delta i_d = & \frac{V_g \sin\delta_0 (sL_g + R_g) - V_g \cos\delta_0 \omega_0 L_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \cdot \Delta\delta \\ & + \frac{sL_g + R_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \cdot \Delta V_i \end{aligned} \tag{5.4}$$

$$\begin{aligned} \Delta i_q = & \frac{-V_g \cos\delta_0 (sL_g + R_g) + V_g \sin\delta_0 \omega_0 L_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \cdot \Delta\delta \\ & - \frac{\omega_0 L_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \cdot \Delta V_i \end{aligned} \tag{5.5}$$

The perturbed VSI active and reactive power are respectively expressed as

$$\begin{cases} \Delta P_i = \dfrac{3}{2}(v_{id0}\Delta i_d + i_{d0}\Delta v_{id} + v_{iq0}\Delta i_q + i_{q0}\Delta v_{iq}) \\ \Delta Q_i = \dfrac{3}{2}(v_{iq0}\Delta i_d + i_{d0}\Delta v_{iq} - v_{id0}\Delta i_q - i_{q0}\Delta v_{id}) \end{cases} \tag{5.6}$$

From (5.1), the values of steady-state *dq*-frame currents i_{d0} and i_{q0} are calculated as

$$\begin{cases} i_{d0} = \dfrac{V_i R_g - V_g (R_g \cos\delta_0 + \omega_0 L_g \sin\delta_0)}{R_g^2 + \omega_0^2 L_g^2} \\ i_{q0} = \dfrac{(V_g \cos\delta_0 - V_i)\omega_0 L_g - V_g R_g \sin\delta_0}{R_g^2 + \omega_0^2 L_g^2} \end{cases} \tag{5.7}$$

According to (5.4)-(5.7), the perturbed VSI active and reactive powers are calculated as

$$\Delta P_i = G_{\delta P}(s) \cdot \Delta\delta + G_{VP}(s) \cdot \Delta V_i \tag{5.8}$$

$$\Delta Q_i = G_{\delta Q}(s) \cdot \Delta\delta + G_{VQ}(s) \cdot \Delta V_i \tag{5.9}$$

where,

$$\begin{cases} G_{\delta P}(s) = \dfrac{3V_g V_i}{2} \cdot \dfrac{\sin\delta_0 (sL_g + R_g) - \cos\delta_0 \omega_0 L_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \\ G_{\delta Q}(s) = \dfrac{3V_g V_i}{2} \cdot \dfrac{\sin\delta_0 \omega_0 L_g - \cos\delta_0 (sL_g + R_g)}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \\ G_{VP}(s) = \dfrac{3V_i}{2} \cdot \dfrac{sL_g + R_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \\ G_{VQ}(s) = -\dfrac{3V_i}{2} \cdot \dfrac{\omega_0 L_g}{(sL_g + R_g)^2 + (\omega_0 L_g)^2} \end{cases} \tag{5.10}$$

Besides, the feeder impedance power loss is expressed as

$$P_{loss} = \frac{3}{2}(V_i - V_g \cos\delta) \cdot i_d - \frac{3}{2} V_g \sin\delta \cdot i_q . \tag{5.11}$$

The perturbed feeder impedance power loss ΔP_{loss} equals

$$\begin{aligned} \Delta P_{loss} = {} & \frac{3}{2} i_{d0} \cdot \Delta V_i + \frac{3V_g}{2}(i_{d0} \sin\delta_0 - i_{q0} \cos\delta_0) \cdot \Delta\delta \\ & + \frac{3}{2}(V_i - V_g \cos\delta_0) \cdot \Delta i_d - \frac{3}{2} V_g \sin\delta_0 \cdot \Delta i_q \end{aligned} \tag{5.12}$$

Notice that ΔP_{loss} is a function of ΔV_i, $\Delta\delta$, Δi_d, and Δi_q. Based on (5.4)–(5.5), Δi_d and Δi_q are also functions of ΔV_i and $\Delta\delta$. Hence, ΔP_{loss} can be generally expressed as

$$\Delta P_{loss} = G_{V_i \to P_{loss}}(s) \cdot \Delta V_i + G_{\delta \to P_{loss}}(s) \cdot \Delta\delta \tag{5.13}$$

where the expressions of $G_{Vi \to Ploss}(s)$ and $G_{\delta \to Ploss}(s)$ can be derived through (5.4)–(5.5) and (5.12).

From the above derivations, the model of a grid-connected VSI is established and shown in Fig. 5.2. To avoid unnecessary complications, the effect of VSI inner-loop control is neglected. Such a simplification is reasonable since the response of inner-loop control (dozens of milliseconds) is much faster than that of outer-loop control (hundreds of milliseconds). With this assumption, the VSI controllers are modeled as $G_{Pi \to \omega i}(s)$ and

$G_{Qi\to Vi}(s)$, which denote the transfer functions from ΔP_i to $\Delta\omega_i$ and from ΔQ_i to ΔV_i, respectively. Meanwhile, the power grid is regarded as a black box. Note that the power grid frequency ω_g will change according to the delivered active power P_g, as it usually happens in practical situations.

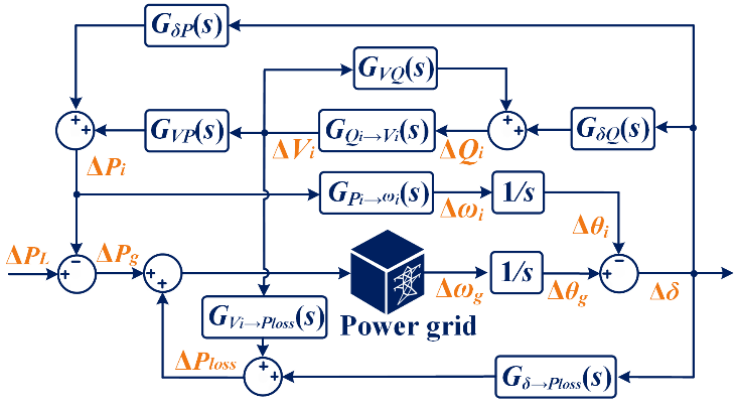


Fig. 5.2. High-entropy model of a grid-connected VSI.

5.2.2. Evaluations and Remarks

Normally, the system stability is analyzed by deriving the characteristic equation and conducting eigenvalue analysis. Nevertheless, this approach can hardly be implemented in the model of Fig. 5.2 due to the following reasons.

1.) The mathematical model of Fig. 5.2 exhibits a high-entropy expression. In other words, the order of characteristic equation is quite high and there exist multi-couplings among different loops. This is especially the case when the power grid contains a lot of power generation units, the interaction among whom greatly increases the grid model complexity.

2.) From a local VSI's perspective, it is impractical to obtain complete knowledge of the power grid, including values of any line impedance and parameters of every power generation unit. In addition, the feeder impedance values R_g and L_g are also not available. As a consequence, the acquired model knowledge is too limited to predict the phase synchronization dynamic.

5.3. Proposed Method

To gain clear insights into the synchronization dynamic, this section aims to present a simple low-entropy model. Prior to analyzing the phase synchronization dynamic, the convention Middebrook Criterion [143], which is widely applied to analyze the stability of interconnected systems through their impedance ratio, will be reviewed.

5.3.1. Middlebrook Criterion

Fig. 5. 3. shows the small-signal representation of the interconnected system, where $Z_s(s)$ is the source output impedance and $Z_l(s)$ is the input impedance of the load system.

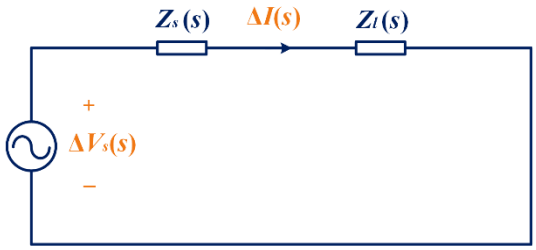


Fig. 5.3. Equivalent circuit of interconnected systems.

The current flowing from the source to the load is expressed as

$$\Delta I(s) = \frac{\Delta V_s(s)}{Z_l(s) + Z_s(s)} \tag{5.14}$$

Rearranging (5.14) yields

$$I(s) = \frac{V_s(s)}{Z_l(s)} \cdot H(s) \tag{5.15}$$

$$H(s) = \frac{1}{1 + Z_s(s) / Z_l(s)} \tag{5.16}$$

It is observed that $H(s)$ resembles the closed-loop transfer function of a negative-feedback control system, which has a unity feedforward gain and a negative feedback gain $Z_s(s)/Z_l(s)$. Due to this reason, the impedance ratio, also known as the minor-loop gain, can be used to evaluate the system stability. Even though, some assumptions must be satisfied before applying this criterion.

1.) The first assumption is that the impedance-based stability criterion is only valid for small-signal stability analysis.

2.) The second assumption is that the source voltage is stable when unloaded and the load current is stable when powered by an ideal source. This is to ensure that $V_s(s)$ and $Z_l(s)$ in (5.15) do not have instability issues.

5.3.2. Frequency Power Characteristic

In the above analysis, voltages are the representations of electrical potentials, the difference between which will generate a current flow. A similar relationship is found in the power flow equation, where phase angles are the symbols of electrical potentials

and the power will flow from the leading phase angle to the lagging one. According to this analogy, Fig. 5.4 shows the power-flow representation of the Middlebrook Criterion.

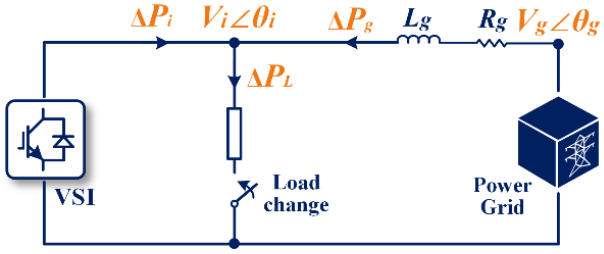


Fig. 5.4. Power-flow representation of Middlebrook Criterion.

The VSI output voltage phase $\Delta\theta_i$ can be expressed as

$$\Delta\theta_i(s) = s^{-1}G_{P_i\to\omega_i}(s)\cdot\Delta P_i(s) = s^{-1}G_{P_g\to\omega_i}(s)\cdot\Delta P_g(s) \tag{5.17}$$

where $G_{Pg\to\omega i}(s)$ is the transfer function from $\Delta P_g(s)$ to $\Delta\omega_i(s)$. Notice that both feeder impedances and power grid have crucial impacts on $G_{Pg\to\omega i}(s)$. In addition, the power balance equation ensures that

$$\Delta P_L(s) = \Delta P_i(s) + \Delta P_g(s) \tag{5.18}$$

From (5.17) and (5.18), the transfer function from the load disturbance $\Delta P_L(s)$ to $\Delta\theta_i(s)$ can be derived as

$$\frac{\Delta\theta_i(s)}{\Delta P_L(s)} = \frac{s^{-1}G_{P_i\to\omega_i}(s)}{1+G_{\omega_i\to P_g}(s)/G_{\omega_i\to P_i}(s)} \tag{5.19}$$

where $G_{\omega i\to Pg}(s)$ and $G_{\omega i\to Pi}(s)$ are the FPC of the grid and the FPC of VSI, respectively. It is clear that high similarities are found by comparing (5.14)–(5.16) with (5.17)–(5.19). Therefore, the synchronization stability can be ensured if $G_{\omega i\to Pg}(s)/G_{\omega i\to Pi}(s)$ does not encircle $(-1, j0)$ for the entire low-frequency range.

The above analysis provides a low-entropy model to analyze the synchronization dynamic. In specific, (5.19) has a simple but well-organized structure with the known (the FPC of VSI) and the unknown (the FPC of the power grid) split up. Though the expression of $G_{\omega i\to Pg}(s)$ still has a high order, it is not necessary to spend tremendous effort on deriving it.

5.3.3. Acquisition of Grid FPC

As discussed above, the grid synchronization stability can be assessed through $G_{\omega i\to Pg}(s)/G_{\omega i\to Pi}(s)$. In this section, an FRI approach is proposed to obtain $G_{\omega i\to Pg}(s)$ without knowing the grid information. Instead of relying on extra measuring devices (such as an

impedance analyzer), the acquisition of $G_{\omega i \to Pg}(s)$ can be achieved by VSI itself. In particular, the VSI is initially operated in the grid-forming mode and its frequency equals to

$$\omega_i = \omega_0 - \frac{P_i}{D} + \omega_{inj} \tag{5.20}$$

where ω_0 is the nominal frequency, ω_{inj} is an injected small AC signal, while D is the equivalent damping coefficient. Fig. 5.5 shows the small-signal model of the proposed FRI technique.

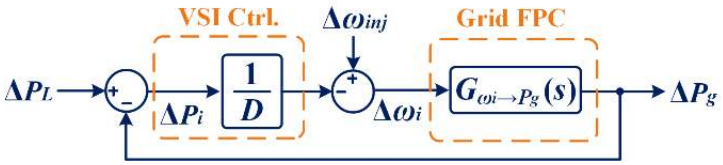


Fig. 5.5. Small-signal model of the proposed FRI technique.

Perturbing (5.20) yields

$$\Delta\omega_i = -\frac{\Delta P_i}{D} + \Delta\omega_{inj} \tag{5.21}$$

The first term on the right of (5.21) facilitates the grid synchronization of VSI and provides a positive damping effect to the grid, while a small disturbance $\Delta\omega_{inj}$ is injected by the second term in order to measure $G_{\omega i \to Pg}(s)$. The transfer function from $\Delta\omega_{inj}$ to ΔP_i is derived as

$$\frac{\Delta P_i(s)}{\Delta\omega_{inj}(s)} = \frac{G_{\omega_i \to P_g}(s)}{D^{-1} \cdot G_{\omega_i \to P_g}(s) - 1} \tag{5.22}$$

By injecting a small sinusoidal signal $\Delta\omega_{inj}$ with frequency ω and observing the response of active power variation ΔP_i at the same frequency. The amplitude gain and phase change can be measured as

$$\frac{|P_i(\omega)|}{|\omega_{inj}(\omega)|} = A_m(\omega) \tag{5.23}$$

$$\angle P_i(\omega) - \angle\omega_{inj}(\omega) = \varphi_m(\omega) \tag{5.24}$$

where $A_m(\omega)$ and $\varphi_m(\omega)$ are the measured amplitude gain and phase addition at the frequency ω. Besides, $A_g(\omega)$ and $\varphi_g(\omega)$ are the desired amplitude gain and phase change of $G_{\omega i \to Pg}(j\omega)$, i.e.,

$$G_{\omega_i \to P_g}(j\omega) = A_g(\omega)\cos\varphi_g(\omega) + jA_g(\omega)\sin\varphi_g(\omega) \tag{5.25}$$

According to (5.22), damping coefficient D is coupled with $G_{\omega i \to Pg}(j\omega)$. Therefore, $A_m(\omega)$ and $\varphi_m(\omega)$ are different from $A_g(\omega)$ and $\varphi_g(\omega)$. To decouple $G_{\omega i \to Pg}(j\omega)$ with D, (5.22) is reorganized in the orthogonal coordinate

$$\begin{aligned} &A_m(\omega)\cdot\cos\varphi_m(\omega) + jA_m(\omega)\cdot\sin\varphi_m(\omega) \\ &\quad = \frac{D\cdot A_g(\omega)\cdot\cos\varphi_g(\omega) + jD\cdot A_g(\omega)\cdot\sin\varphi_g(\omega)}{A_g(\omega)\cdot\cos\varphi_g(\omega) + jA_g(\omega)\cdot\sin\varphi_g(\omega) - D}. \end{aligned} \tag{5.26}$$

By equalizing the real and imaginary parts of (5.26), it can be derived that

$$A_g(\omega) = \frac{A_m(\omega)}{\sqrt{\sin^2\varphi_m(\omega) + (A_m(\omega)D^{-1} - \cos\varphi_m(\omega))^2}} \tag{5.27}$$

$$\tan\varphi_g(\omega) = \frac{D\cdot\sin\varphi_m(\omega)}{D\cdot\cos\varphi_m(\omega) - A_m(\omega)} \tag{5.28}$$

In (5.27) and (5.28), $A_g(\omega)$ and $\varphi_g(\omega)$ can be directly calculated from measured $A_m(\omega)$ and $\varphi_m(\omega)$. It should be mentioned that the definitional domain of a tangent function is within $(-\pi/2, \pi/2)$ such that there will be two $\varphi_g(\omega)$ values within $(-\pi, \pi)$ that satisfies (5.28). As a consequence, the obtained $\varphi_g(\omega)$ (through an arctangent function) should be verified through (5.22) again to determine its real value. Fig. 5.6 shows the flow-chart of the FRI technique. Initially, a small ac variation $\Delta\omega_{inj}$ (with the frequency ω) is imposed on the VSI frequency. Next, the power variation ΔP_i (at the same frequency) is observed and analyzed through the FFT. The values of $A_m(\omega)$ and $\varphi_m(\omega)$ are obtained and subsequently used to calculate $A_g(\omega)$ and $\varphi_g(\omega)$ based on (5.27) and (5.28). By changing the value of ω, the same algorithm will be executed repetitively until the FRI test finishes for the entire low-frequency range.

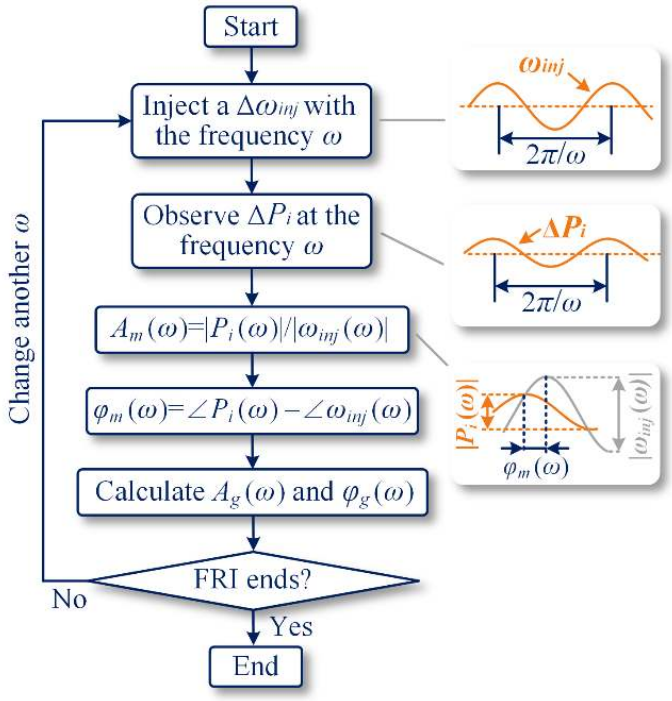


Fig. 5.6. A flow-chart of the FRI technique.

5.4. Case Study

5.4.1. System Configuration

A case study is presented in this section, where a three-phase grid-forming VSI is coupled to the power grid represented by a synchronous machine. Fig. 5.7(a) shows the circuit configuration under study, where P_e is the active power of synchronous machine, which equals the sum of P_g and P_{loss}. In addition, a step load change ΔP_L is applied at the PCC by closing the switch of load 2.

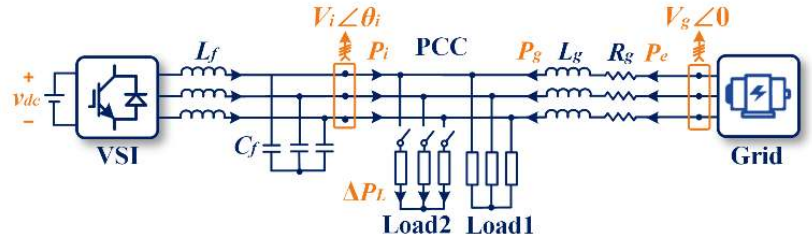
Fig. 5.7(b) shows the frequency regulation framework of the synchronous machine, where R is the frequency droop slope; T_G is the speed governor time constant; F_{HP}, T_{RH}, and T_{CH} are time constants of reheat turbine; H_{SM} is the mechanical inertia of rotor; P_{ref} is the load reference, which remains unchanged; S_N is the rated power of SM.

The transfer function from ΔP_e to $\Delta\omega_g$ is derived as

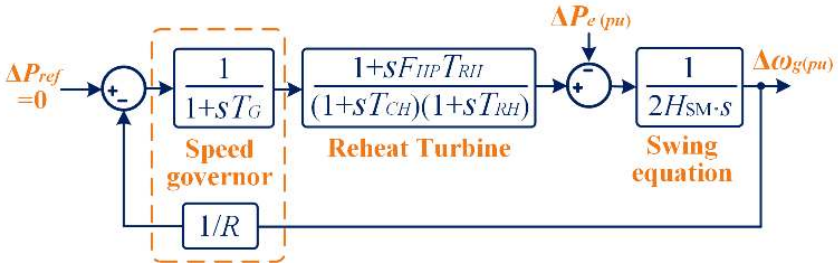
$$G_{P_e\to\omega_g}(s)=\frac{-S_N^{-1}\omega_0 R(1+sT_G)(1+sT_{CH})(1+sT_{RH})}{R(1+sT_G)(1+sT_{CH})(1+sT_{RH})2H_{\mathrm{SM}}s+F_{HP}T_{RH}s+1} \tag{5.29}$$

Besides, Fig. 5.7(c) shows the VSI outer-loop power controls, where k_p and k_q are the frequency-active power droop gain and voltage-reactive power droop gain. Notice that a low-pass filter with a time constant τ is also employed to provide equivalent inertia.

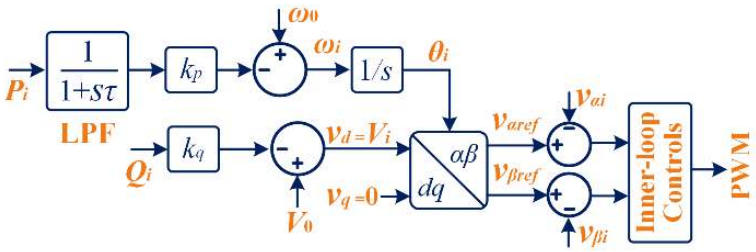
Through the $dq/\alpha\beta$ transformation, the stationary-frame reference voltages $v_{\alpha\beta\text{-}ref}$ are determined and subsequently tracked by fast inner-loop controls.



(a)



(b)



(c)

Fig. 5.7. Circuit and control diagrams of the case study. (a). Overall circuit configuration. (b). Control block diagram of the synchronous machine (power grid). (c). VSI outer-loop control block diagram.

The transfer functions of $G_{Pi\to\theta i}(s)$ and $G_{Qi\to Vi}(s)$ can be derived as

$$\begin{cases} G_{P_i\to\theta_i}(s)=\dfrac{\Delta\theta_i}{\Delta P_i}=\dfrac{-m}{s+s^2\cdot\tau} \\ G_{Q_i\to V_i}(s)=\dfrac{\Delta V_i}{\Delta Q_i}=-n \end{cases} \tag{5.30}$$

According to (5.30), the FPC of VSI is expressed as

$$G_{\omega_i\to P_i}(s)=\frac{1}{s}\cdot G_{P_i\to\theta_i}(s)^{-1}=-\frac{1+s\cdot\tau}{m} \tag{5.31}$$

Table 5.1 provides key control and system parameters unless otherwise mentioned. Notice that the SM and VSI are designed to have equal power ratings.

Table 5.1 System Parameter Values

Parameters	Descriptions	Values
	Synchronous Machine	
R	Frequency droop slope (p.u.)	0.05
T_G	Speed governor constant	0.1 s
F_{HP}	Turbine HP constant	0.3 s
T_{RH}	Reheater time constant	7.0 s
T_{CH}	Inlet volumes time constant	0.2 s
H_{SM}	Inertia constant	5.0 s
V_g	Grid voltage magnitude	75 V
S_N	Power rating of SM	5 kV·A
	Voltage Source Inverter	
m	Frequency droop gain	5×10^{-4} Hz/W
n	Voltage droop gain	1×10^{-4} V/Var
V_0	VSI nominal voltage	75 V
ω_0	VSI nominal frequency	100π (rad/s)
L_f	VSI filter inductance	1 mH
C_f	VSI filter capacitor	15 μF
	Feeder Impedances	
R_g	Feeder resistance	2 Ω
L_g	Feeder inductance	4 mH

For the hardware setup, a voltage-controlled VSI is adopted to perfectly simulate the dynamic behavior of the synchronous machine. All the samplings and digital controls are processed by a PLECS RT Box with a 10 kHz sampling frequency. Two resistive loads are coupled to the PCC, and the power disturbance ΔP_L is applied by manually closing the switch of a load.

5.4.2. Measurement Verification

To verify the measuring accuracy of the FRI approach, the power system FPC is theoretically derived and compared with experimental measurements. The detailed power grid FPC derivation is provided hereinafter. Based on the small-signal model in Fig. 5.2, a signal-flow graph is constructed and shown in Fig. 5.8.

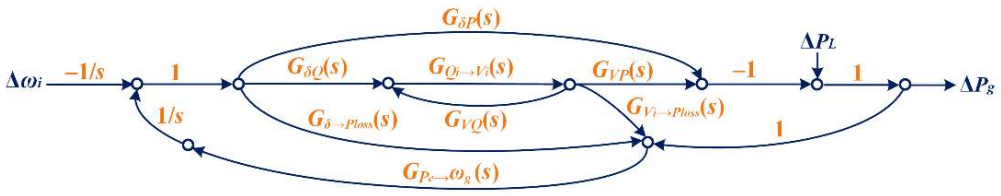


Fig. 5.8. Signal-flow graph of the system model.

In Fig. 5.8, $\Delta\omega_i$ is the input signal, ΔP_g is the output signal, and ΔP_L is considered as a disturbance. The power grid FPC, i.e., the transfer function from $\Delta\omega_i$ to ΔP_g, is derived according to Mason's gain formula

$$G_{\omega_i \to P_g}(s) = \frac{\Delta P_g}{\Delta \omega_i} = \frac{G_1(s)\Delta_1(s) + G_2(s)\Delta_2(s)}{1 - \sum_{i=1}^{5} L_i(s) + L_1(s)L_5(s)} \tag{5.32}$$

where $G_1(s)$ and $G_2(s)$ are the gain of forward paths; $\Delta_1(s)$ and $\Delta_2(s)$ are the associated cofactor values; $L_i(s)$ is the loop gain of each closed loop. The detailed expressions are given as

$$\begin{cases} G_1(s)\Delta_1(s) = s^{-1} G_{\delta Q}(s) G_{Q_i \to V_i}(s) G_{VP}(s) \\ G_2(s)\Delta_2(s) = s^{-1} G_{\delta P}(s)(1 - G_{Q_i \to V_i}(s) G_{VQ}(s)) \\ L_1(s) = s^{-1} G_{P_e \to \omega_g}(s) G_{\delta \to P_{loss}}(s) \\ L_2(s) = s^{-1} G_{P_e \to \omega_g}(s) G_{\delta Q}(s) G_{Q_i \to V_i}(s) G_{V_i \to P_{loss}}(s) \\ L_3(s) = -s^{-1} G_{P_e \to \omega_g}(s) G_{\delta Q}(s) G_{Q_i \to V_i}(s) G_{VP}(s) \\ L_4(s) = -s^{-1} G_{P_e \to \omega_g}(s) G_{\delta P}(s) \\ L_5(s) = G_{Q_i \to V_i}(s) G_{VQ}(s) \end{cases} \tag{5.33}$$

For the experimental measurement, the damping coefficient D is 1000 (W·s)/rad. Fig. 5. 9 shows the VSI current waveforms when the frequency of injected ω_{inj} is 5 Hz. It can be seen that there are small 5 Hz variations on the envelope curve of VSI output currents, which are caused by ω_{inj}. Fig. 5.10 compares the waveform of ω_{inj} and the corresponding active power variation. It can be observed that the peak-to-peak value of ω_{inj} is around 0.57 rad/s (0.09 Hz) while the peak-to-peak value of active power variation is 28 W. Accordingly, the amplitude gain $A_m(\omega=10\pi)$ can be calculated as 49.12. In addition, the phase angle change $\varphi_m(\omega=10\pi)$ can also be read from Fig. 5.10, which is around –91.0 degrees. Based on (5.27) and (5.28), $A_g(\omega=10\pi)$ is calculated as 33.82 dB while φ_g ($\omega=10\pi$) is calculated as 86.2 degrees.

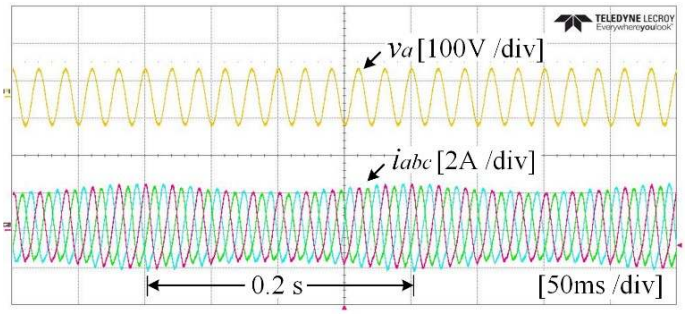


Fig. 5.9. VSI output current waveforms with a 5 Hz ω_{inj}.

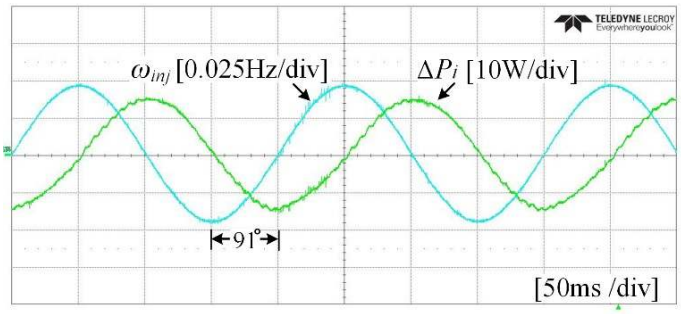


Fig. 5.10. Waveforms of ω_{inj} and the corresponding active power variation ΔP_i.

The above example illustrates how to measure the gain and phase of $G_{\omega i \to Pg}(s)$ at a certain frequency. Through similar efforts, the Bode diagram of $G_{\omega i \to Pg}(s)$ is measured for the entire low-frequency range, i.e., from 0.05 Hz to 20 Hz. Fig. 5.11 illustrates the acquired Bode diagram and the comparison with theoretical analysis.

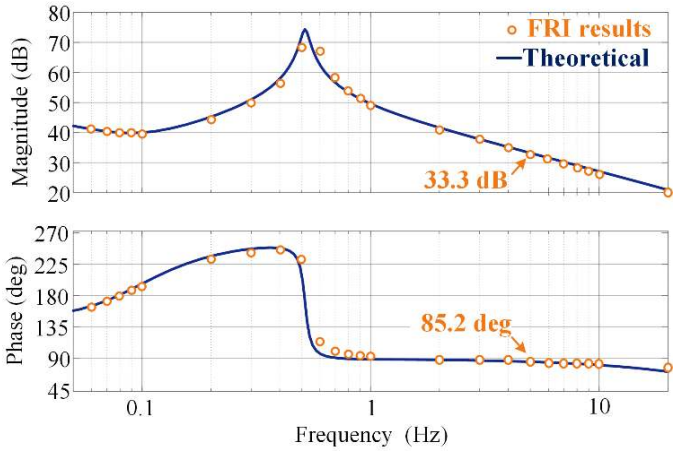


Fig. 5.11. Bode diagrams of $G_{\omega i \to Pg}(s)$ obtained from the FRI technique.

A perfect match is can be observed between the FRI measuring result and the theoretical analysis. Besides, it is worth mentioning that a resonant peak appears at around 0.5 Hz in Fig. 5.11. The resonant frequency is affected by feeder impedances and parameters of the synchronous machine.

5.4.3. Design-oriented Analysis of Grid-forming VSI

Once the power gird frequency-power characteristic is obtained by the FRI method, the potential low-frequency angle oscillations can be easily identified. In particular, this subsection discusses the impact of the VSI inertia constant τ on synchronization stability.

Fig. 5.12 shows the Bodes diagrams of FPC ratio, namely, $G_{\omega i \to Pg}(s)/G_{\omega i \to Pi}(s)$. When the VSI inertia coefficient τ equals 0.4, the system is marginally stable with a 7.71 degree PM. However, when τ equals 1.2, the system becomes unstable due to a negative PM.

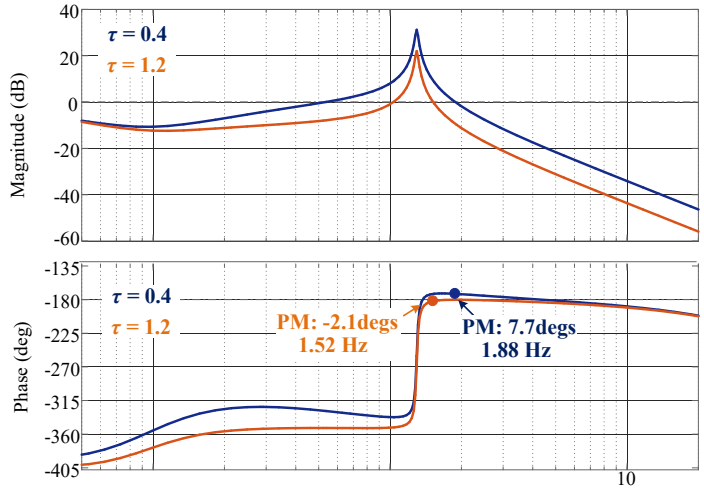


Fig. 5.12. Bodes diagrams of FPC ratio with different τ. (R_g=0.4 and L_g=1 mH)

Fig. 5.13 shows the simulated VSI active power responses when its inertia constant τ has been changed from 0.4 to 1.2. It is observed that active power oscillation occurs and become unbounded as time goes by. This agrees with the Bode diagram analysis that a negative PM is introduced when τ equals 1.2.

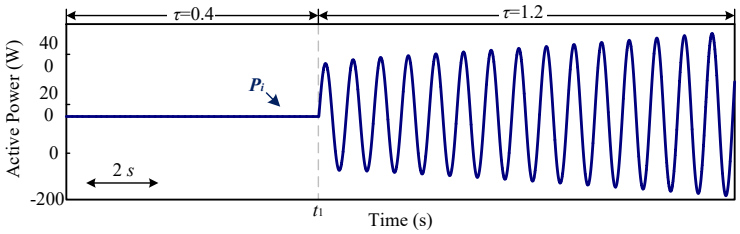


Fig. 5.13. Simulated active power responses with different VSI inertia constants.

Apart from the simulation results, experiments are also conducted for verification. To start with, the VSI inertia constant τ is 0.6, corresponding to a 3.0 s system inertia. Fig. 5.14 shows the Bode diagrams of FPC. In order to guarantee that $G_{\omega i \to Pg}(j\omega)/G_{\omega i \to Pi}(j\omega)$ does not equal $(-1, j0)$ for any frequency, one sufficient condition is to check the phase

difference between $G_{\omega i \to Pg}(j\omega)$ and $G_{\omega i \to Pi}(j\omega)$ at all magnitude intersects. For example, there are two magnitude intersects appearing in Fig. 5.14, which are respectively 0.34 Hz and 0.66 Hz. For the first intersect, the associated phase margin (PM) is 159 degrees (obtained by subtracting 180 degrees with the phase difference at 0.34 Hz). This result indicates good stability.

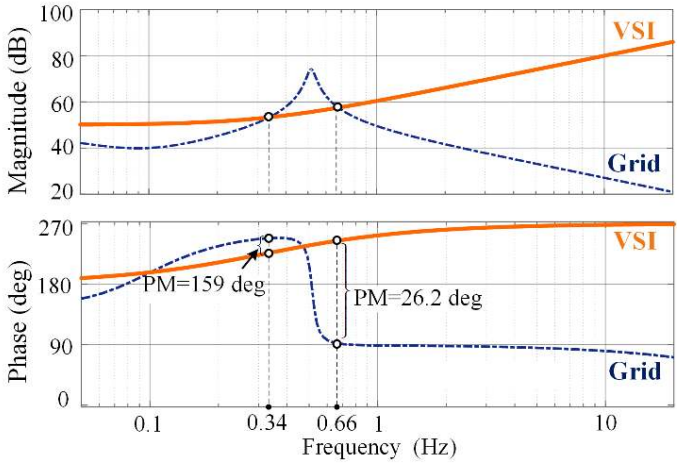


Fig. 5.12. Bode diagrams of frequency-power characteristics (τ=0.6).

However, the second intersect exhibits an inadequate PM (26.2 degrees) such that the system is marginally stable. As a result, considerable low-frequency oscillations have been observed in the VSI output current waveforms (Fig. 5.15) and the phase difference δ (Fig. 5.16) after being subjected to a load disturbance at t. As observed from the experimental results, the time period of low-frequency oscillations is around 1.6 s, i.e., 0.625 Hz, which agrees with the frequency of the second intersect, i.e., 0.66 Hz, as shown in Fig. 5.15.

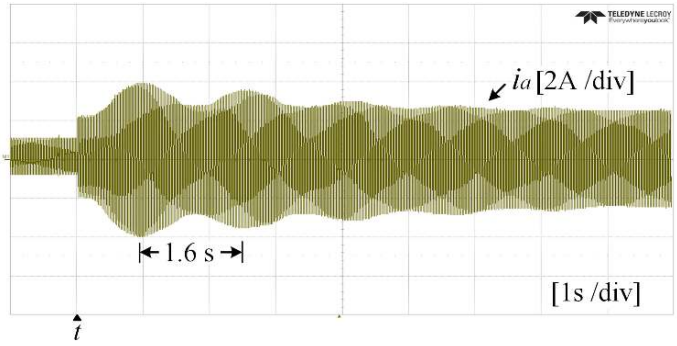


Fig. 5.13. VSI phase A current waveform after a step load change (τ=0.6).

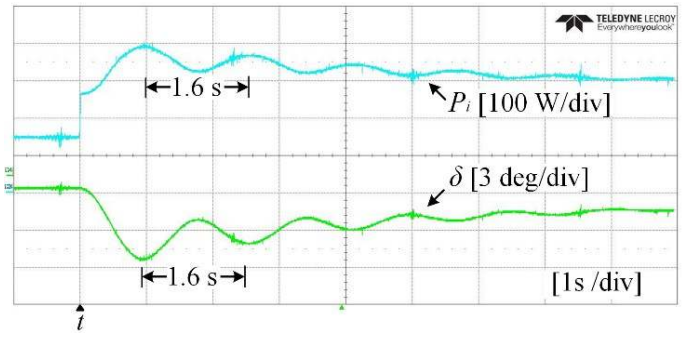


Fig. 5.14. Dynamic responses of power and angle difference (τ=0.6).

According to the above analysis, a large VSI inertia coefficient may not necessarily contribute to better synchronization stability. To avoid low-frequency oscillations, the FPC of VSI can be reshaped to ensure a satisfied PM, e.g., 60 degrees at the critical magnitude intersect. To fulfill this design objective, the inertia constant τ is selected as 0.15 in the Bode diagram of Fig. 5.17 so that the PM has been boosted to 60.5 degrees. Fig. 5.18 and Fig. 5.19 display the dynamic responses when τ equals 0.15. It is observed that low-frequency angle oscillations are effectively damped so that the system smoothly enters a new equilibrium point.

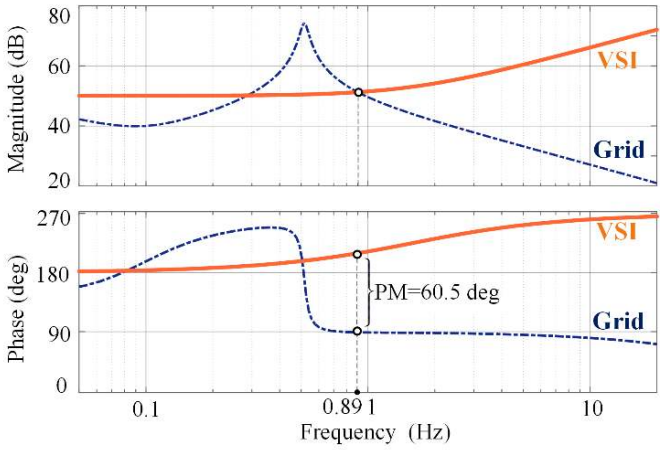


Fig. 5.15. Bode diagrams of frequency-power characteristics (τ=0.15).

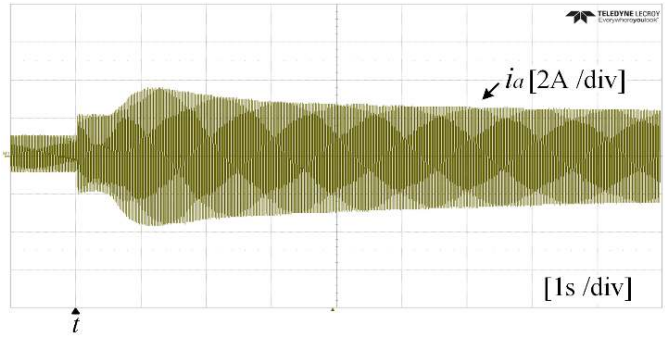


Fig. 5.16. VSI phase A current waveform after a step load change (τ=0.15).

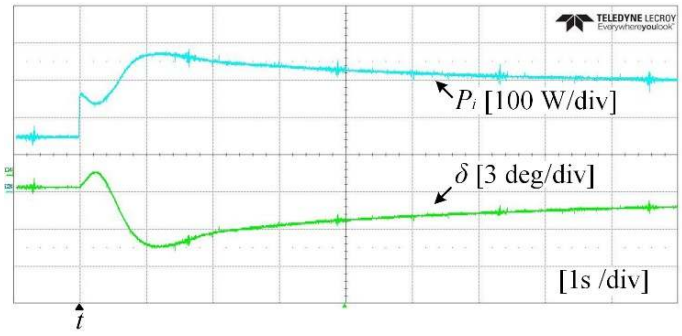


Fig. 5.17. Dynamic responses of power and angle difference (τ=0.15)

5.5. Summary

This chapter presents a design-oriented analysis to evaluate VSI synchronization stability. Particularly, by comparing the FPC of VSI and that of the power grid, potential low-frequency angle oscillations can be identified, which provides helpful guidance on the VSI controller design and the oscillation damping. More importantly, the grid FPC can be easily acquired without grid information or additional measuring devices. This attractive feature offers a promising solution for integrating a new VSI to the existing power grid. Fig. 5.20 illustrates the integration of a new VSI to the existing microgrid with n multiple VSIs.

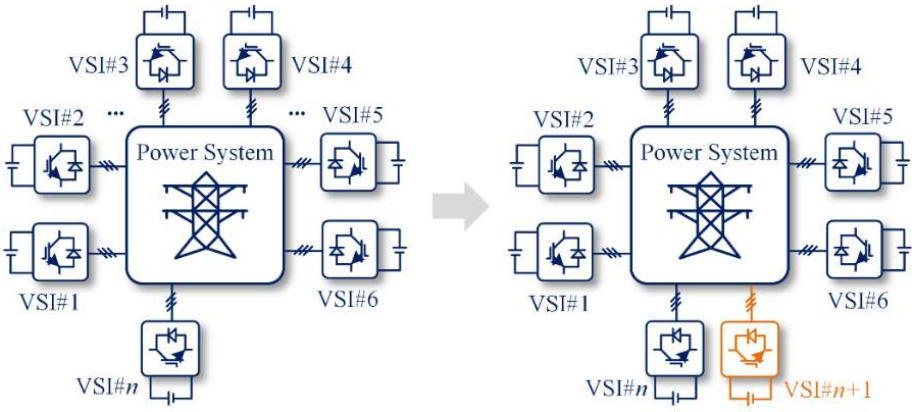


Fig. 5.20. Illustration for the grid integration of a new VSI.

The entire power system expands from n VSI units to n+1 VSI units. The integration contains two steps. Firstly, the new unit, VSI#n+1, serves as a "measuring device" to acquire the power system characteristic. This is achieved by VSI# n +1 itself and does not require additional devices, such as a frequency scanner or an impedance measurement unit. Then, the control architecture of VSI#n+1 can be switched back to the originally-planed one and the measured power system characteristic will be used to

facilitate the control parameter design and ensure synchronization stability. Moreover, when the VSI#n+1 is added to the existing power system, only VSI#n+1 itself needs to measure the grid FPC and reshape its characteristic, while the rest of the VSI units do not need it. The experimental results of a case study are provided for verification, where the power grid is represented by a synchronous machine.

Chapter 6 Conclusions and Future Works

This chapter concludes the whole thesis by summarizing its contents and highlighting its major contributions. Moreover, some future research perspectives with regards to the grid integration of DESS will be discussed.

6.1. Conclusions

This thesis studies the grid integration and coordinated control of VSIs with energy storage systems. Through explicit theoretical analysis and comprehensive experimental verifications, the conclusions are obtained as follows:

The grid integration of DESSs is achieved through the parallel operation of multiple VSIs. To fully utilize VSI capacities and maintain the system normal operation, the total load power is expected to be proportionally shared among multiple VSIs with respect to their power ratings. However, the challenges lie in 1.) the power-sharing accuracy is sensitive to parameter uncertainty, such as line impedances, grid structure, and even sensor errors; 2.) Due to the nature of DESSs, these VSIs are usually located in different places. As a result, they can hardly exchange information with each other through high-bandwidth communications. In some worst cases, they only know their local information. In view of these difficulties, it is challenging to accurately share power among VSIs.

It is well known that active power can always be accurately shared by the conventional droop control, while some reactive power sharing errors exist. In view of this challenge, Chapter 2 first develops a dead-time-related control scheme on the basis of conventional droop control. It is shown that the dead-time effect can introduce circulating harmonic currents among VSIs if they have different power factors. This interesting characteristic can be adopted to equalize the power factors of distributed VSIs, which is successfully achieved by the supplementary controller in Chapter 2. Given that the conventional frequency droop control has already ensured the active power sharing accuracy, the reactive power sharing error is eliminated if all the VSIs have the same power factors. The proposed control strategy does not need any communications and can be applied under various scenarios.

However, the conventional droop control, as well as the dead-time related control, only take effect in the fundamental positive-sequence domain. In other words, the unbalanced power sharing problem cannot be addressed. To fill in this research gap, Chapter 3 has conducted an analysis and came up with solutions for unbalanced power-sharing. It is found that apart from the line impedance mismatch, even small voltage

sensor measurement errors may also lead to significant negative-sequence circulating currents among VSIs. Unfortunately, this negative impact cannot be addressed given that the voltage-feedback control is well designed with excellent tracking ability. To address this issue, a hybrid impedance shaping control is proposed in Chapter 3, which effectively mitigates the negative influences of voltage measurement errors. Similarly, the proposed control strategy can be implemented in a fully decentralized manner and its feasibility is validated by simulation and experimental results.

On the basis of Chapter 3, Chapter 4 further explores the nonlinear load power sharing at selective harmonic frequencies. The improper harmonic power-sharing issue caused by mismatched grid impedances is explicitly analyzed. To enhance the harmonic current sharing performance and eliminate circulating harmonic currents, a two-dimensional impedance shaping control has been developed. The proposed control strategy is based on the distributed consensus control algorithm which only requires low-bandwidth communications and can provide an additional DOF for the impedance shaping. As a consequence, the proper harmonic power-sharing result is guaranteed, and immunes from complex and mismatched grid impedances.

Last but most importantly, one important premise of AC load power sharing is that VSIs can well synchronize with each without stability issues. To ensure synchronization stability, small-signal modelling, analysis and solutions are discussed in Chapter 5. It is revealed that undesired low-frequency angle oscillations and even loss of synchronism may happen when the VSI outer-power control loop is not properly designed. However, it could be difficult to design the VSI outer-power control loop without knowing the power system information. To fill in this research gap, an FRI technique is proposed in Chapter 5 to measure the power-frequency characteristic of the grid without peering into its inner structure. Furthermore, a design-oriented analysis is developed to design the VSI controller and guarantees good synchronization stability. The effectiveness of the above techniques has been verified through a case study, where a grid-forming VSI is connected in parallel with a synchronous machine.

6.2. Future Works

On the basis of the aforementioned research works, this subsection further comes up with some new perspectives on the integration, deployment, and control of DESS. They are briefly summarized as follows:

• System-level stability issues due to the increasing installation of power-electronics converters.

• Reliability against power system faults.

• Cyber-physical security.

More details will be provided in the following subsections.

6.2.1. System-level Stability Issues

It should be noted that Chapter 5 mainly focuses on converter-level stability analysis, namely, the stability issue related to an individual VSI. From a broader perspective, the system-level stability is also of great importance. When heterogeneous power converters are coupled to the microgrid, complicated interactions exist among them and new types of instability issues may occur.

One specific stability issue related to DESSs is the power grid frequency stability. In the conventional power grid, the system inertia is provided by centralized synchronous generators. As a contrast, the invention of the "virtual synchronous generator" concept will make the inertia of the future power grid contributed by distributed power converters with ESSs. Recent studies reveal that if the centralized and large inertia is spilt into distributed but small inertia, resonances will be triggered among power generation units. As a result, considerable overshoots and even instability may occur. The resonance effect is influenced by a number of factors, including the control parameters of virtual synchronous generators, line impedance values, and how are these power generation units coupled. The analysis and mitigation of this issue have not been well studied in the existing works.

From the methodology perspective, conventional methods are to derive the microgrid small-signal model, properly design the controller so that all the poles of characteristic equations are located on the left-hand plane. Nevertheless, this approach can hardly be utilized to address system-level stability issues, since the computation effort will exponentially increase as the number of power converters goes up. One typical example is found in [124], where the state-space matrix of a microgrid already has dozens of orders with only three power converters.

In view of this challenge, some new stability analysis approaches are desired for large microgrids/power systems. It is expected that such approaches can avoid the tremendous effort spent on deriving the entire system model while giving an accurate prediction of the system dynamics.

Moreover, given that system operating points may change from time to time, it would also be important to make sure that the power system is stable for a wide operation range, rather than a specific equilibrium point. Besides, system stability should also be robust

against circuit parameter variations, such as the passive filters and grid impedances. The pursuit of robust stability would be a crucial future research direction.

6.2.2. Power System Reliability

The reliability of power system will be another concern when more and more power-electronic devices are installed. On one hand, research efforts are needed to prolong the lifespans of power converters. This target can be achieved by using redundant modules (in case of a single point failure), avoiding the frequent charging/discharging of DESSs, and replacing the electrolytic capacitor with the film capacitor (which has a much longer lifetime).

On the other hand, it is desired that power converters shall be properly controlled to ride through various types of faults, including unexpected islanding, grid voltage dips, ground faults, and phase-to-phase faults. In this case, the power converters should not only protect themselves from being damaged by overcurrent or overvoltage, but more importantly, make sure that the faults will not affect the crucial loads, expand to a larger area, and even result in the breakdown of the system.

In this regard, some advanced control strategies as well as circuit designs are needed to improve the microgrid reliability and enable power converters to limit the short-circuit current and isolate the fault. While this thesis mainly focuses on the normal operation of microgrids, the reliability strengthening and fault-tolerant operation of power converters will be explored in future works.

6.2.3. Cyber Physical Security

The research works in the thesis mainly focus on primary-layer (low-level) control of voltage source inverters. However, there are some issues that cannot be addressed only by primary-layer control, such as frequency & voltage restoration, system-level energy management, and the economic dispatch. Therefore, communication-based secondary control should be required.

However, it is noted that, despite the numerous advantages brought by the secondary control, the open nature of communication channels also makes the systems vulnerable to potential cyber attacks. Typical attacks in smart grid include integrity attacks, which damage the system operations by injecting false data into original measurements, and Denial-of-Service attacks, where the adversary degrades the system performance by jamming or breaking communications between agents. One typical example is reported in [144], where the distributed load power sharing among DESSs and microgrid stability

have been compromised by a false-data-injection attack. Past works show that such misbehavior can easily interfere with the system operation and degrade performance of the existing control and estimation algorithms without being detected. Given that the applications of the smart grid are usually safety-critical: their failures can lead to large economic losses and even cause irreparable harm to public health, more and more research attention has been paid to the security of the smart grid.

One challenging aspect is the cyber-attack detection, as the manipulation of meter measurements can be achieved without being noticed and the attack scheme can be arbitrary. The other perspective would be the active defense against malicious attacks without interfering with the power system's normal functionality. There is, consequently, an urgent need to develop secure control protocols that enable the microgrid to identify and defense against various malicious attacks. This will form another future research aspect.

Author's Publications

Journal Papers:

[1]. Y. Qi, T. Yang, J. Fang, Y. Tang, K. R. R. Potti, and K. Rajashekara "Grid Inertia Support Enabled by Smart Loads," *IEEE Trans. Power Electron*., vol. 36, no. 1, pp. 947-957, Jan. 2021.

[2]. Y. Qi, Y. Tang, K. R. R. Potti, and K. Rajashekara "Robust Power Sharing Control for Parallel Three-phase Inverters Against Voltage Measurement Errors," *IEEE Trans. Power Electron*., vol. 35, no. 12, pp. 13590-13601, Dec. 2020.

[3]. Y. Qi, P. Lin, Y. Wang, and Y. Tang, "Two-Dimensional Impedance-Shaping Control with Enhanced Harmonic Power Sharing for Inverter-Based Microgrids," *IEEE Trans. Power Electron*., vol. 34, no. 11, pp. 11407-11418, Nov. 2019.

[4]. Y. Qi, J. Fang, and Y. Tang, "Utilizing the Dead-time Effect to Achieve Decentralized Reactive Power Sharing in Islanded AC Microgrids," *IEEE J. Emer. Sel. Topics Power Electron*., vol. 8, no. 3, pp. 2350-2361, Sept. 2020.

[5]. Y. Qi, H. Deng, J. Wang, and Y. Tang "Passivity-based Synchronization Stability Analysis for Power-electronic-interfaced Distributed Generations," *IEEE Trans. Sustain. Energy*., *early access*, 2021.

[6]. Y. Qi, J. Fang, J. Liu, and Y. Tang, "Coordinated control for harmonic mitigation of parallel voltage-source inverters," *CES Trans. on Electric Machine and System*, vol. 2, no. 3, pp. 276-283, Sep. 2018.

Conferences Papers:

[7]. Y. Qi, H. Deng, J. Wang, and Y. Tang, "Tailor-made Power-angle Characteristic: A New Controller Design Perspective for Grid-forming Inverter", IPEMC 2020-ECCE Asia, Nanjing, 2020.

[8]. Y. Qi, J. Liu, Y. Tang, and Kaushik Rajashekara, "Analysis and Mitigation of Voltage Measurement Errors for Three-Phase Parallel Voltage Source Inverters," *IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, 2019.

[9]. Y. Qi, and Y. Tang, "Decentralized Reactive Power Sharing Among Parallel Inverters Through Inherent Dead-time Effect," *IEEE Energy Convers. Congr. Expo.*, Baltimore, MD, 2019.

[10]. Y. Qi, *et al*, "A Transformless Electric Spring with Decoupled Real and Reactive Power Control," 4th *IEEE International Future Energy Electronics Conference*, Singapore, 2019.

[11]. Y. Qi, and Y. Tang, "Enhancing the Harmonic Current Sharing Performance of Low-Switching-Frequency Inverters Though Dynamic Impedance Reshaping," *IEEE Energy Convers. Congr. Expo.*, Portland, OR, 2018, pp. 3150-3155.

[12]. Y. Qi, J. Fang, and Y. Tang, "Frequency-Dependent Droop Control for Distributed Generation in Microgrids," PCIM Asia 2017, Shanghai, China, 2017, pp. 1-7.

[13]. J. Wang, Y. Qi, L. Zhang, J. Yu, and Y. Tang, "A Unified Startup Control Strategy for Modular Multilevel Converters from Either AC Side or DC Side", IPEMC 2020-ECCE Asia, Nanjing, 2020.

[14]. D. Han, J. Fang, Y. Qi, V. Debusschere, and Y. Tang, "A Low Voltage Ride Through Strategy with Load and Grid Support for Grid-Forming Converters", IPEMC 2020-ECCE Asia, Nanjing, 2020.

[15]. J. Liu, Y. Qi, and Y. Tang, "Mitigating the Harmonics of Parallel-Inverter Systems Considering Nonlinear Loads and Deadtime," *IEEE Energy Convers. Congr. Expo.*, Portland, OR, 2018, pp. 5559-5564.

[16]. J. Yan and Y. Qi, "Stability Analysis of a Parallel-Converter System with Master /Slave Configuration," *IEEE CDC Conference*, Dec., 2019.

References

[1]. REN21, Paris, France, "Renewables 2017 global status report", 2017.

[2] Y. Zhong and G. Power, "Some Environmental Impacts of Hydroelectric Projects on Fish in Canada", *Impact Assessment*, vol. 14, no. 3, pp. 285-308, 1996.

[3]. B. Kroposki *et al*., "Achieving a 100% Renewable Grid: Operating Electric Power Systems with Extremely High Levels of Variable Renewable Energy," *IEEE Power and Energy Magazine*, vol. 15, no. 2, pp. 61-73, Mar. 2017.

[4]. J. Traube *et al*., "Mitigation of Solar Irradiance Intermittency in Photovoltaic Power Systems with Integrated Electric-Vehicle Charging Functionality," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 3058-3067, Jun. 2013.

[5]. J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "On the Inertia of Future More-Electronics Power Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 4, pp. 2130-2146, Dec. 2019.

[6]. J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "Distributed Power System Virtual Inertia Implemented by Grid-Connected Power Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8488-8499, Oct. 2018.

[7]. Australian Energy Market Operator, "*Black System South Australia 28 September 2016*."

[8]. Energy Market Authority. "*Singapore Energy Statistics*."

[9]. H. Liu and J. Jiang, "Flywheel energy storage—An upswing technology for energy sustainability", *Energy and Buildings*, vol. 39, no. 5, pp. 599-604, 2007.

[10]. Sabihuddin, S. Kiprakis, A.E. Mueller, and M. A Numerical "Graphical Review of Energy Storage Technologies," *Energies*, no. 8, pp. 172-216, 2015.

[11]. Kretschmer, Katja, "Phosphate-based cathode materials for rechargeable batteries", *Doctoral dissertation*, 2018.

[12]. P. P. Dash and M. Kazerani, "Dynamic Modeling and Performance Analysis of a Grid-Connected Current-Source Inverter-Based Photovoltaic System," *IEEE Transactions on Sustainable Energy*, vol. 2, no. 4, pp. 443-450, Oct. 2011.

[13]. L. M. Tolbert and T. G. Habetler, “Novel multilevel inverter carrier-based PWM method,” *IEEE Transactions on Industry Applications*, vol. 35, no. 5, pp. 1098-1107, Sept. 1999.

[14]. S. Daher, J. Schmid, and F. L. M. Antunes, “Multilevel Inverter Topologies for Stand-Alone PV Systems,” *IEEE Transactions on Industrial Electronics*, vol. 55, no. 7, pp. 2703-2712, July 2008.

[15]. X. Li, J. Fang, P. Lin, and Y. Tang, “Active Magnetic Decoupling for Improving the Performance of Integrated LCL-Filters in Grid-Connected Converters,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1367-1376, Feb. 2018.

[16]. Y. Tang, P. C. Loh, P. Wang, F. H. Choo, F. Gao, and F. Blaabjerg, “Generalized Design of High Performance Shunt Active Power Filter With Output LCL Filter,” *IEEE Transactions on Industrial Electronics*, vol. 59, no. 3, pp. 1443-1452, March 2012.

[17]. Y. Tang, P. C. Loh, P. Wang, F. H. Choo, and F. Gao, “Exploring Inherent Damping Characteristic of LCL-Filters for Three-Phase Grid-Connected Voltage Source Inverters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1433-1443, March 2012.

[18]. A. von Jouanne, P. N. Enjeti, and D. J. Lucas, “DSP control of high-power UPS systems feeding nonlinear loads,” *IEEE Transactions on Industrial Electronics*, vol. 43, no. 1, pp. 121-125, Feb. 1996.

[19]. G. E. Valderrama, A. M. Stankovic, and P. Mattavelli, “Dissipativity-based adaptive and robust control of UPS in unbalanced operation,” *IEEE Transactions on Power Electronics*, vol. 18, no. 4, pp. 1056-1062, July 2003.

[20]. J. Rocabert, A. Luna, F. Blaabjerg, and P. Rodríguez, “Control of Power Converters in AC Microgrids,” *IEEE Transactions on Power Electronics*, vol. 27, no. 11, pp. 4734-4749, Nov. 2012.

[21]. K. De Brabandere, B. Bolsens, J. Van den Keybus, A. Woyte, J. Driesen, and R. Belmans, “A Voltage and Frequency Droop Control Method for Parallel Inverters,” *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1107-1115, July 2007.

[22]. H. Han, Y. Liu, Y. Sun, M. Su, and J. M. Guerrero, “An Improved Droop Control Strategy for Reactive Power Sharing in Islanded Microgrid,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3133-3141, June 2015.

[23]. J. M. Guerrero, J. C. Vásquez, J. Matas, M. Castilla, and L. Garcaí de Vicuna, "Control strategy for flexible microgrid based on parallel lineinteractive UPS systems," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 3, pp. 726–736, Mar. 2009.

[24]. Q. C. Zhong, "Robust droop controller for accurate proportional load sharing among inverters operated in parallel," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1281–1290, Apr, 2013.

[25]. J. M. Guerrero, L. G. de Vicuna, J. Matas, M. Castilla, and J. Miret, "A wireless controller to enhance dynamic performance of parallel inverters in distributed generation systems," *IEEE Transactions on Power Electronics*, vol. 19, no. 5, pp. 1205–1213, Sep. 2004.

[26]. Q. Zhong and G. Weiss, "Synchronverters: Inverters That Mimic Synchronous Generators," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 4, pp. 1259-1267, Apr. 2011.

[27]. J. Liu, Y. Miura, H.Bevrani, and T. Ise, "Enhanced Virtual Synchronous Generator Control for Parallel Inverters in Microgrids," *IEEE Transactions on Smart Grid*,, vol. 8, no. 5, pp. 2268-2277, Sep. 2017.

[28]. W. Du, Q. Fu, and H. Wang, "Power System Small-Signal Angular Stability Affected by Virtual Synchronous Generators," *IEEE Transactions on Power Systems*, vol. 34, no. 4, pp. 3209-3219, Jul. 2019.

[29]. L. Huang, H. Xin, and Z. Wang, "Damping low-frequency oscillations through VSC-HVDC stations operated as virtual synchronous machines," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5803-5818, Jun. 2018.

[30]. Z. Shuai, W. Huang, Z. J. Shen, A. Luo, and Z. Tian, "Active Power Oscillation and Suppression Techniques Between Two Parallel Synchronverters During Load Fluctuations," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4127-4142, April 2020.

[31]. L. Zhang, L. Harnefors, and H. Nee, "Power-Synchronization Control of Grid-Connected Voltage-Source Converters," *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 809-820, May 2010.

[32]. H. Wu and X. Wang, "Design-Oriented Transient Stability Analysis of Grid-Connected Converters with Power Synchronization Control," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 8, pp. 6473-6482, Aug. 2019.

[33]. Y. W. Li, “Control and Resonance Damping of Voltage-Source and Current-Source Converters with LC Filters,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 5, pp. 1511-1521, May 2009.

[34]. X. Li, X. Wu, Y. Geng, X. Yuan, C. Xia, and X. Zhang, “Wide Damping Region For LCL-Type Grid-Connected Inverter With an Improved Capacitor-Current-Feedback Method,” *IEEE Transactions on Power Electronics*, vol. 30, no. 9, pp. 5247-5259, Sept. 2015.

[35]. R. H. Lasseter, Z. Chen, and D. Pattabiraman, “Grid-Forming Inverters: A Critical Asset for the Power Grid,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*. vol. 8, no. 2, pp. 925-935, June 2020.

[36]. P. J. Hart, R. H. Lasseter, and T. M. Jahns, “Coherency Identification and Aggregation in Grid-Forming Droop-Controlled Inverter Networks,” *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2219-2231, May 2019.

[37]. Q. Peng, Q. Jiang, Y. Yang, T. Liu, H. Wang, and F. Blaabjerg, “On the Stability of Power Electronics-Dominated Systems: Challenges and Potential Solutions,” *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 76577670, Nov. 2019.

[38]. IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal, Nonsinusoidal, Balanced, or Unbalanced Conditions, *IEEE Standard* 1459 - 2010, Mar. 2010.

[39]. IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems,” *IEEE Std* 519-1992, pp.1-112, Apr. 1993.

[40] M. Prodanovic and T. C. Green, “Control of power quality in inverter-based distributed generation,” 28th *Annual Conference of the Industrial Electronics Society*, Sevilla, pp. 1185-1189, 2002.

[41]. D. T. Ton and M. A. Smith, “The U.S. department of energy’s microgrid initiative,” *The Electricity Journal*., vol. 25, no. 8, pp. 84–94, Oct. 2012.

[42]. J. C. Vasquez, J. M. Guerrero, A. Luna, P. Rodrgíuez, and R. Teodorescu, “Adaptive droop control applied to voltage-source inverters operating in grid-connected and islanded modes,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 10, pp. 4088–4096, Oct. 2009.

[43]. H. Han, X. Hou, J. Yang, J. Wu, M. Su, and J. M. Guerrero, “Review of Power Sharing Control Strategies for Islanding Operation of AC Microgrids,” *IEEE Transactions on Smart Grid*, vol. 7, no. 1, pp. 200-215, Jan. 2016.

[44]. Z. Liu, J. Liu, X. Hou, Q. Dou, D. Xue, and T. Liu, “Output Impedance Modeling and Stability Prediction of Three-Phase Paralleled Inverters With Master–Slave Sharing Scheme Based on Terminal Characteristics of Individual Inverters,” *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 5306-5320, July 2016.

[45]. Xin Meng, Z. Liu, J. Liu, Teng Wu, Shike Wang, and Baojin Liu, “A seamless transfer strategy based on special master and slave DGs,” 2017 *IEEE 3rd International Future Energy Electronics Conference and ECCE Asia* (IFEEC - ECCE Asia), Kaohsiung, pp. 1553-1558, 2017.

[46]. J. Zhou, S. Kim, H. Zhang, Q. Sun, and R. Han, “Consensus-Based Distributed Control for Accurate Reactive, Harmonic, and Imbalance Power Sharing in Microgrids,” *IEEE Transactions on Smart Grid*, vol. 9, no. 4, pp. 2453-2467, July 2018.

[47]. A. Kahrobaeian and Y. A. Ibrahim Mohamed, “Networked-Based Hybrid Distributed Power Sharing and Control for Islanded Microgrid Systems,” *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 603-617, Feb. 2015.

[48]. Q. Shafiee, J. M. Guerrero, and J. C. Vasquez, “Distributed Secondary Control for Islanded Microgrids—A Novel Approach,” *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 1018-1031, Feb. 2014.

[49]. C. Ahumada, R. Cárdenas, D. Sáez, and J. M. Guerrero, “Secondary Control Strategies for Frequency Restoration in Islanded Microgrids With Consideration of Communication Delays,” *IEEE Transactions on Smart Grid*, vol. 7, no. 3, pp. 1430-1441, May 2016.

[50]. J. Yan, F. Guo, and C. Wen. “False data injection against state estimation in power systems with multiple cooperative attackers.” *ISA transactions*, vol.101, pp. 225-233, 2020.

[51]. Q. Wu, R. Guan, X. Sun, Y. Wang, and X. Li, “SoC Balancing Strategy for Multiple Energy Storage Units with Different Capacities in Islanded Microgrids Based on Droop Control,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 4, pp. 1932-1941, Dec. 2018.

[52]. X. Sun, Y. Hao, Q. Wu, X. Guo, and B. Wang, “A Multifunctional and Wireless Droop Control for Distributed Energy Storage Units in Islanded AC Microgrid Applications,” *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 736-751, Jan. 2017.

[53]. X. Lu, K. Sun, J. M. Guerrero, J. C. Vasquez, and L. Huang, “State-of-Charge Balance Using Adaptive Droop Control for Distributed Energy Storage Systems in DC Microgrid Applications,” *IEEE Transactions on Industrial Electronics*, vol. 61, no. 6, pp. 2804-2815, June 2014.

[54]. C. Li, E. A. A. Coelho, T. Dragicevic, J. M. Guerrero, and J. C. Vasquez, “Multiagent-Based Distributed State of Charge Balancing Control for Distributed Energy Storage Units in AC Microgrids,” *IEEE Transactions on Industry Applications*, vol. 53, no. 3, pp. 2369-2381, May-June 2017.

[55]. Y. Han, H. Li, P. Shen, E. A. A. Coelho, and J. M. Guerrero, “Review of Active and Reactive Power Sharing Strategies in Hierarchical Controlled Microgrids,” *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2427–2451, Mar. 2017.

[56]. Y. Qi, Y. Tang, K. R. R. Potti, and K. Rajashekara “Robust Power Sharing Control for Parallel Three-phase Inverters Against Voltage Measurement Errors,” *IEEE Transactions on Power Electronics*, May 2020.

[57]. Y. Zeng and Q. Zhong, “A droop controller achieving proportional power sharing without output voltage amplitude or frequency deviation,” 2014 *IEEE Energy Conversion Congress and Exposition* (ECCE), Pittsburgh, PA, 2014.

[58]. S. D'Arco and J. A. Suul, “Equivalence of Virtual Synchronous Machines and Frequency-Droops for Converter-Based MicroGrids,” *IEEE Transactions on Smart Grid*, vol. 5, no. 1, pp. 394-395, Jan. 2014.

[59]. Baojin Liu, Zeng Liu, Jinjun Liu, Teng Wu, and Ronghui An, “A novel unbalanced power sharing control method for an islanded microgrid,” 2017 *IEEE 3rd International Future Energy Electronics Conference and ECCE Asia* (IFEEC 2017 - ECCE Asia), Kaohsiung, 2017, pp. 1617-1622.

[60]. X. Wang and F. Blaabjerg, “Harmonic Stability in Power Electronic-Based Power Systems: Concept, Modeling, and Analysis,” *IEEE Transactions on Smart Grid*, vol. 10, no. 3, pp. 2858-2870, May 2019.

[61]. Y. Liao, Z. Liu, H. Zhang, and B. Wen, "Low-Frequency Stability Analysis of Single-Phase System With dq-Frame Impedance Approach—Part I: Impedance Modeling and Verification," *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 4999-5011, Sept. 2018.

[62]. J. He and Y. W. Li, "Analysis, design, and implementation of virtual impedance for power electronics interfaced distributed generation," *IEEE Transactions on Industry Applications*, vol. 47, no. 6, pp. 2525–2538, Sep. 2011.

[63]. X. Wang, Y. W. Li, F. Blaabjerg, and P. C. Loh, "Virtual-Impedance-Based Control for Voltage-Source and Current-Source Converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 7019-7037, Dec. 2015.

[64]. W. Yao, M. Chen, J. Matas, J. M. Guerrero, and Z. M. Qian, "Design and analysis of the droop control method for parallel inverters considering the impact of the complex impedance on the power sharing," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 576–588, Feb. 2011.

[65]. Y. Hu, J. Xiang, Y. Peng, P. Yang, and W. Wei, "Decentralised control for reactive power sharing using adaptive virtual impedance," *IET Generation, Transmission & Distribution*, vol. 12, no. 5, pp. 1198–1205, Mar. 2018.

[66]. J. He, Y. W. Li, J. M. Guerrero, F. Blaabjerg, and J. C. Vasquez, "An Islanding Microgrid Power Sharing Approach Using Enhanced Virtual Impedance Control Scheme," *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5272–5282, Nov. 2013.

[67]. T. Wu, Z. Liu, J. Liu, S. Wang, and Z. You, "A Unified Virtual Power Decoupling Method for Droop-Controlled Parallel Inverters in Microgrids," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5587–5603, Aug. 2016.

[68]. Y. W. Li and C. N. Kao, "An accurate power control strategy for power-electronics-interfaced distributed generation units operating in a low-voltage multibus microgrid," *IEEE Transactions on Power Electronics*, vol. 24, no. 12, pp. 2977–2988, Dec. 2009.

[69]. Y. Zhu, F. Zhuo, F. Wang, B. Liu, and Y. Zhao, "A Wireless Load Sharing Strategy for Islanded Microgrid Based on Feeder Current Sensing," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6706–6719, Dec. 2015.

[70]. A. Micallef, M. Apap, C. Spiteri-Staines, J. M. Guerrero, and J. C. Vasquez, "Reactive power sharing and voltage harmonic distortion compensation of droop controlled single phase islanded microgrids," *IEEE Transactions on Smart Grid*, vol. 5, no. 3, pp. 1149–1158, May. 2014.

[71]. H. Mahmood, D. Michaelson, and J. Jiang, "Reactive Power Sharing in Islanded Microgrids Using Adaptive Voltage Droop Control," *IEEE Transactions on Smart Grid*, vol. 6, no. 6, pp. 3052–3060, Nov. 2015.

[72]. L. Lin, H. Ma, and Z. Bai, "An Improved Proportional Load-Sharing Strategy for Meshed Parallel Inverters System with Complex Impedances," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7338–7351, Sep. 2017.

[73]. T. V. Hoang and H. H. Lee, "An Adaptive Virtual Impedance Control Scheme to Eliminate the Reactive-Power-Sharing Errors in an Islanding Meshed Microgrid," *IEEE Journal of Emerging and Selected. Topics on Power Electron*ics, vol. 6, no. 2, pp. 966–976, Jun. 2018.

[74]. H. Mahmood, D. Michaelson, and J. Jiang, "Accurate Reactive Power Sharing in an Islanded Microgrid Using Adaptive Virtual Impedances," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1605–1617, Mar, 2015.

[75]. J. W. Simpson-Porco, Q. Shafiee, F. Dorfler, J. C. Vasquez, J. M. Guerrero, and F. Bullo, "Secondary Frequency and Voltage Control of Islanded Microgrids via Distributed Averaging," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7025–7038, Nov. 2015.

[76]. Y. Sun, X. Hou, J. Yang, H. Han, M. Su, and J. M. Guerrero, "New Perspectives on Droop Control in AC Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5741–5745, Jul. 2017.

[77]. B. Liu, Z. Liu, J. Liu, T. Wu, S. Wang, and X. Meng, "A small-AC-signal injection based harmonic power sharing method for islanded microgrids," 2016 *IEEE Energy Conversion Congress and Exposition* (ECCE), Milwaukee, WI, pp. 1-6, 2016.

[78]. C. T. Lee, C. C. Chu, and P. T. Cheng, "A new droop control method for the autonomous operation of distributed energy resource interface converters," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1980–1993, Apr. 2013.

[79]. D. H. Lee and J. W. Ahn, “A simple and direct dead-time effect compensation scheme in PWM-VSI,” *IEEE Transactions on Industrial Applications*, vol. 50, no. 5, pp. 3017–3025, Feb. 2014.

[80]. T. Itkonen, J. Luukko, A. Sankala, T. Laakkonen, and R. Pnen, “Modeling and analysis of the dead-time effects in parallel PWM two-level three-phase voltage-source inverters,” *IEEE Transactions on Power Electronics*, vol. 24, no. 11, pp. 2446–2455, Nov. 2009.

[81]. Y. Qi, J. Fang, J. Liu, and Y. Tang, “Coordinated control for harmonic mitigation of parallel voltage-source inverters,” *CES Trans. on Electrical Machines and Systems*, vol. 2, no. 3, pp. 276-283, Sep. 2018.

[82]. X. Chen, X. Ruan, D. Yang, W. Zhao, and L. Jia, “Injected Grid Current Quality Improvement for a Voltage-Controlled Grid-Connected Inverter,” *IEEE Transactions on Power Electronics*, vol. 33, no. 2, pp. 1247–1258, Mar. 2018.

[83]. J. Miret, M. Castilla, J. Matas, J. M. Guerrero, and J. C. Vasquez, “Selective harmonic-compensation control for single-phase active power filter with high harmonic rejection,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 8, pp. 3117–3127, Aug. 2009.

[84]. C. Lascu, L. Asiminoaei, I. Boldea, and F. Blaabjerg, “High Performance Current Controller for Selective Harmonic Compensation in Active Power Filters,” *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1826-1835, Sep. 2007.

[85]. H. Wu and X. Wang, “Transient angle stability analysis of grid-connected converters with the first-order active power loop,” 2018 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 3011-3016, pp. 3011–3016, Mar. 2018.

[86]. J. M. Guerrero, J. C. Vásquez, J. Matas, M. Castilla, and L. García de Vicuna, “Control strategy for flexible microgrid based on parallel line-interactive UPS systems,” *IEEE Transactions on Industrial Electronics*, vol. 56, no. 3, pp. 726–736, Mar. 2009.

[87]. J. Liu, Y. Miura, and T. Ise, “Comparison of Dynamic Characteristics Between Virtual Synchronous Generator and Droop Control in Inverter-Based Distributed Generators,” *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3600-3611, May 2016.

[88]. X. Wang, F. Blaabjerg, and Z. Chen, “Autonomous Control of Inverter-Interfaced Distributed Generation Units for Harmonic Current Filtering and Resonance Damping in an Islanded Microgrid,” *IEEE Transactions on Industrial Applications*, vol. 50, no. 1, pp. 452-461, Feb. 2014.

[89]. S. Jiang, D. Cao, Y. Li, J. Liu, and F. Z. Peng, “Low-THD, Fast-Transient, and Cost-Effective Synchronous-Frame Repetitive Controller for Three-Phase UPS Inverters,” *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2994-3005, Jun. 2012.

[90]. J. C. Vasquez, J. M. Guerrero, M. Savaghebi, J. Eloy-Garcia, and R. Teodorescu, “Modeling, Analysis, and Design of Stationary-Reference-Frame Droop-Controlled Parallel Three-Phase Voltage Source Inverters,” *IEEE Transactions on Industrial Electronics*, vol. 60, no. 4, pp. 1271-1280, Apr. 2013.

[91]. M. Liserre, R. Teodorescu, and F. Blaabjerg, “Multiple harmonics control for three-phase grid converter systems with the use of PI-RES current controller in a rotating frame,” *IEEE Transactions on Power Electronics*, vol. 21, no. 3, pp. 836-841, May. 2006.

[92]. M. Kim, S. Sul, and J. Lee, “Compensation of Current Measurement Error for Current-Controlled PMSM Drives,” *IEEE Transactions on Industrial Applications.*, vol. 50, no. 5, pp. 3365-3373, Oct. 2014.

[93]. Q. N. Trinh, P. Wang, Y. Tang, and F. H. Choo, “Mitigation of DC and Harmonic Currents Generated by Voltage Measurement Errors and Grid Voltage Distortions in Transformerless Grid-Connected Inverters,” *IEEE Transactions on Energy Conversion*, vol. 33, no. 2, pp. 801-813, Jun. 2018.

[94]. Q. N. Trinh, P. Wang, Y. Tang, L. H. Koh, and F. H. Choo, “Compensation of DC Offset and Scaling Errors in Voltage and Current Measurements of Three-Phase AC/DC Converters,” *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5401-5414, Jun. 2018.

[95]. M. Chen, D. Xu, T. Zhang, K. Shi, G. He, and K. Rajashekara, “A Novel DC Current Injection Suppression Method for Three-Phase Grid-Connected Inverter Without the Isolation Transformer,” *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8656-8666, Nov. 2018.

[96]. X. Wang, F. Blaabjerg, and Z. Chen, “An improved design of virtual output impedance loop for droop-controlled parallel three-phase voltage source inverters,”

2012 *IEEE Energy Conversion Congress and Expo*. (ECCE), Raleigh, NC, 2012, pp. 2466-2473.

[97]. L. Meng, X. Zhao, T. Fan, S. Mehdi, D. Tomislav, J. C. Vásquez, and J. M. Guerrero, "Distributed Voltage Unbalance Compensation in Islanded Microgrids by Using a Dynamic Consensus Algorithm," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 827-838, Jan. 2016.

[98]. A. Micallef, M. Apap, C. Spiteri-Staines, and J. M. Guerrero, "Mitigation of Harmonics in Grid-Connected and Islanded Microgrids Via Virtual Admittances and Impedances," *IEEE Transactions on Smart Grid*, vol. 8, no. 2, pp. 651–661, Mar. 2017.

[99]. R. Ni, Y. W. Li, Y. Zhang, N. Zargari, and Z. Cheng, "Virtual impedance based selective harmonic compensation (VI-SHC) PWM for current source rectifiers," *IEEE Transactions on Power Electron*ics, vol. 29, no.7, pp. 3346 3356, Jul. 2014.

[100]. P. Sreekumar and V. Khadkikar, "Direct control of the inverter impedance to achieve controllable harmonic sharing in the Islanded Microgrid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 827–837, Jan. 2017.

[101]. X. Wang, P. C. Loh, and F. Blaabjerg, "Stability Analysis and Controller Synthesis for Single-Loop Voltage-Controlled VSIs," *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 7394-7404, Sep. 2017.

[102]. S. Hwang, L. Liu, H. Li, and J. Kim, "DC Offset Error Compensation for Synchronous Reference Frame PLL in Single-Phase Grid-Connected Converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 8, pp. 3467-3471, Aug. 2012.

[103]. P. Sreekumar and V. Khadkikar, "A New Virtual Harmonic Impedance Scheme for Harmonic Power Sharing in an Islanded Microgrid," *IEEE Transactions on Power Delivery*, vol. 31, no. 3, pp. 936–945, Jun. 2016.

[104]. J. M. Guerrero, L. G. De Vicuña, J. Matas, J. Miret, and M. Castilla, "Output impedance design of parallel-connected UPS inverters," *IEEE Transactions on Industrial Electronics*, vol. 2, no. 4, pp. 1123–1128, 2004.

[105]. T. L. Lee and P. T. Cheng, "Design of a new cooperative harmonic filtering strategy for distributed generation interface converters in an islanding network," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1919–1927, Sep. 2007.

[106]. T. Vandoorn, B. Meersman, J. De Kooning, and L. Vandevelde, "Controllable harmonic current sharing in islanded microgrids: DG units with programmable resistive

behaviour toward harmonics," *IEEE Transactions on Power Delivery*, vol. 27, no. 2, pp. 831–841, Apr. 2012.

[107]. A. H. Yazdavar, M. A. Azzouz, and E. F. El-Saadany, "A Novel Decentralized Control Scheme for Enhanced Nonlinear Load Sharing and Power Quality in Islanded Microgrids," *IEEE Transactions on Smart Grid*, vol. 9, no. 1, pp. 29–39, Jul. 2017.

[108]. J. He, Y. W. Li, and F. Blaabjerg, "An Enhanced Islanding Microgrid Reactive Power, Imbalance Power, and Harmonic Power Sharing Scheme," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3389–3401, Jun. 2015.

[109]. H. Moussa, A. Shahin, J.-P. Martin, B. Nahid-Mobarakeh, S. Pierfederici, and N. Nazih Moubayed, "Harmonic Power Sharing with Voltage Distortion Compensation of Droop controlled Islanded microgrids," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 5335-5347, Sep. 2017.

[110]. X. Zhao, L. Meng, C. Xie, J. M. Guerrero, and X. Wu, "A Unified Voltage Harmonic Control Strategy for Coordinated Compensation with VCM and CCM Converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 8, pp. 7132–7147, Aug. 2018.

[111]. M. S. Golsorkhi, M. Savaghebi, D. D. C. Lu, J. M. Guerrero, and J. C. Vasquez, "A GPS-based control framework for accurate current sharing and power quality improvement in microgrids," *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5675–5687, Jul. 2017.

[112]. T. V. Hoang and H. Lee, "Accurate Power Sharing With Harmonic Power for Islanded Multibus Microgrids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1286-1299, June 2019.

[113]. T. Wu, Z. Liu, J. Liu, S. Wang, and Z. You, "A Unified Virtual Power Decoupling Method for Droop-Controlled Parallel Inverters in Microgrids," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5587–5603, Aug. 2016.

[114]. S. Yang, P. Wang, Y. Tang, and L. Zhang, "Explicit Phase Lead Filter Design in Repetitive Control for Voltage Harmonic Mitigation of VSI-Based Islanded Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 817-826, Jan. 2017.

[115]. P. Kundur *et al*., "Definition and classification of power system stability IEEE/CIGRE joint task force on stability terms and definitions," *IEEE Transactions on Power Systems*, vol. 19, no. 3, pp. 1387-1401, Aug. 2004.

[116]. P. Kundur, *Power System Stability and Control*. New York, NY, USA: McGraw-Hill, 1994.

[117]. R. Rosso, M. Andresen, S. Engelken, and M. Liserre, "Analysis of the Interaction Among Power Converters Through Their Synchronization Mechanism," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12321-12332, Dec. 2019.

[118]. A. Tayyebi, D. Groß, A. Anta, F. Kupzog, and F. Dörfler, "Frequency Stability of Synchronous Machines and Grid-Forming Power Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1004-1018, Jun. 2020.

[119]. J. Fang, X. Li, H. Li, and Y. Tang, "Stability Improvement for Three-Phase Grid-Connected Converters Through Impedance Reshaping in Quadrature-Axis," *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8365-8375, Oct. 2018.

[120]. Y. Huang, X. Zhai, J. Hu, D. Liu, and C. Lin, "Modeling and Stability Analysis of VSC Internal Voltage in DC-Link Voltage Control timescale," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 1, pp. 16-28, March 2018.

[121]. H. Yuan, X. Yuan, and J. Hu, "Modeling of Grid-Connected VSCs for Power System Small-Signal Stability Analysis in DC Link Voltage Control Timescale," *IEEE Transactions on Power Systems*, vol. 32, no. 5, pp. 3981-3991, Sep. 2017.

[122]. Z. Shuai, W. Huang, Z. J. Shen, A. Luo, and Z. Tian, "Active Power Oscillation and Suppression Techniques between Two Parallel Synchronverters during Load Fluctuations," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 4127-4142, April, 2020.

[123]. Y. Hirase, K. Sugimoto, K. Sakimoto, and T. Ise, "Analysis of Resonance in Microgrids and Effects of System Frequency Stabilization Using a Virtual Synchronous Generator," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 4, pp. 1287-1298, Dec. 2016.

[124]. N. Pogaku, M. Prodanovic, and T. C. Green, "Modeling, Analysis and Testing of Autonomous Operation of an Inverter-Based Microgrid," *IEEE Transactions on Power Electronics*, vol. 22, no. 2, pp. 613-625, Mar. 2007.

[125]. S. Leitner, M. Yazdanian, A. Mehrizi-Sani, and A. Muetze, "Small-Signal Stability Analysis of an Inverter-Based Microgrid With Internal Model-Based Controllers," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 5393-5402, Sep. 2018.

[126]. Z. Li and M. Shahidehpour, "Small-Signal Modeling and Stability Analysis of Hybrid AC/DC Microgrids," *IEEE Transactions on Smart Grid*, vol. 10, no. 2, pp. 2080-2095, Mar. 2019.

[127]. R. Majumder, B. Chaudhuri, A. Ghosh, R. Majumder, G. Ledwich, and F. Zare, "Improvement of Stability and Load Sharing in an Autonomous Microgrid Using Supplementary Droop Control Loop," *IEEE Transactions on Power Systems*, vol. 25, no. 2, pp. 796-808, May 2010.

[128]. D. Chen, Y. Xu, and A. Q. Huang, "Integration of DC Microgrids as Virtual Synchronous Machines Into the AC Grid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7455-7466, Sep. 2017.

[129]. X. Wang, F. Blaabjerg, M. Liserre, Z. Chen, J. He, and Y. Li, "An Active Damper for Stabilizing Power-Electronics-Based AC Systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3318-3329, Jul. 2014.

[130]. Y. Wang, X. Wang, Z. Chen, and F. Blaabjerg, "Small-Signal Stability Analysis of Inverter-Fed Power Systems Using Component Connection Method," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 5301-5310, Sep. 2018.

[131]. Q. Peng, J. Fang, Y. Yang, and F. Blaabjerg, "A universal model for grid-connected converters reflecting power-internal voltage characteristics," *IEEE* 4*th Southern Power Electronics Conference* (SPEC), pp. 1-7, 2018.

[132]. Q. Peng, Y. Yang, and F. Blaabjerg, "State-space modelling of grid-connected power converters considering power-internal voltage characteristics," 10*th International Conference on Power Electronics and ECCE Asia* (ICPE 2019-ECCE Asia) pp. 3047-3053, 2019.

[133]. Y. Huang, X. Yuan, J. Hu and P. Zhou, "Modeling of VSC Connected to Weak Grid for Stability Analysis of DC-Link Voltage Control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 1193-1204, Dec. 2015.

[134]. Y. Huang, X. Yuan, J. Hu, P. Zhou, and D. Wang, "DC-Bus Voltage Control Stability Affected by AC-Bus Voltage Control in VSCs Connected to Weak AC Grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 445-458, June 2016.

[135]. A. Rygg and M. Molinas, "Apparent Impedance Analysis: A Small-Signal Method for Stability Analysis of Power Electronic-Based Systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1474-1486, Dec.

2017.

[136]. J. Sun, “Impedance-Based Stability Criterion for Grid-Connected Inverters,” *IEEE Transactions on Power Electronics*, vol. 26, no. 11, pp. 3075-3078, Nov. 2011.

[137]. X. Wang, F. Blaabjerg, and W. Wu, “Modeling and Analysis of Harmonic Stability in an AC Power-Electronics-Based Power System,” *IEEE Transactions on Power Electronisc*, vol. 29, no. 12, pp. 6421-6432, Dec. 2014.

[138]. B. Wen, D. Dong, D. Boroyevich, R. Burgos, P. Mattavelli, and Z. Shen, “Impedance-Based Analysis of Grid-Synchronization Stability for Three-Phase Paralleled Converters,” *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 26-38, Jan. 2016.

[139]. Y. Liao, Z. Liu, H. Zhang, and B. Wen, “Low-Frequency Stability Analysis of Single-Phase System With *dq*-Frame Impedance Approach—Part II: Stability and Frequency Analysis,” *IEEE Transactions on Industry Applications*, vol. 54, no. 5, pp. 5012-5024, Sept. 2018.

[140]. S. Wang, Z. Liu, J. Liu, D. Boroyevich, and R. Burgos, “Small-Signal Modeling and Stability Prediction of Parallel Droop Controlled Inverters Based on Terminal Characteristics of Individual Inverters,” *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 1045-1063, Jan. 2020.

[141]. J. Huang, K. A. Corzine, and M. Belkhayat, “Small-signal impedance measurement of power-electronics-based AC power systems using Line-to-Line current injection,” *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 445–455, Feb. 2009.

[142]. H. Gong, D. Yang, and X. Wang, “Impact Analysis and Mitigation of Synchronization Dynamics for DQ Impedance Measurement,” *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8797-8807, Sep. 2019.

[143]. R. D. Middlebrook, “Input filter considerations in design and application of switching regulators,” in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, 1976.

[144]. H. Zhang, W. Meng, J. Qi, X. Wang, and W. X. Zheng, “Distributed Load Sharing Under False Data Injection Attack in an Inverter-Based Microgrid,” *IEEE Transactions on Industrial Electronics*, vol. 66, no. 2, pp. 1543-1551, Feb. 2019.