# Guest Editorial: IEEE/ACM Symposium on Nanoscale Architectures (NANOARCH07)

As silicon technology is reaching the lower end of nanometer ranges of feature size (45nm CMOS technology is already in use), the continuation of Moore's law-based scaling of silicon technology is now facing several challenges. The reduced feature size implies a larger number of the transistors on the unit area of silicon chips which provides both scopes for newer features in our computation capabilities, coupled with the problem of increased defect rates and susceptibility to transient faults. Since defect rates can go up 10% or more, traditional discarding of silicon chips based on defects would reduce yields to such low levels that alternative measures of yield enhancements are imperative. One possible way is to enhance the computing logic and micro-architectures with defect- and fault-tolerance features that would make computation robust against such high level of defects and faults, hence increasing yields.

On the other hand, engineers and scientists are now engaged in finding alternatives to silicon-based computing such that nanoscale computation can be realized with molecular dynamics, quantum effects, and other nontraditional material and computation paradigms. Molecular transistors, DNA-scaffolding-based computation fabrics, carbon nanotube-based field effect transistors, carbon nanotube-based PLA type fabrics, and many other technological advances are happening in various academic and industrial labs. However, many of these technologies cannot depend on traditional lithographic techniques for manufacturing because of the small range of the dimensions. As a result, self-assembly techniques and various fortifications of techniques to make nature engineer such systems instead of us having to devise the engineering methods to circumvent nature are being worked out. Self-assembly when not tempered with such techniques would also lead to yield problems, hence these techniques and innovations are necessary for nanoscale computing with such technologies to be usable.

While both the low-dimension nanometer-scale silicon technology and nontraditional technologies grapple with these issues of defect and fault, reliability engineering is playing an important part both at the lowest level of manufacturing techniques to the architecture, micro-architecture, and logic level stages of the electronic design flow.

While these have renewed interest in the early work on fault tolerance and defect tolerance as far back as Von Neumann's original work in the early 1950s, some of the techniques imply so much area and latency overhead that one has

Author's address: Electrical and Computer Engineering Department, Virginia Polytechnic and State University, Blacksburg, VA 24061; email: shukla@vt.edu.
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to think in terms of various kinds of trade-offs. So the nanoscale architecture exploration and design has to now include reliability as one major parameter along with area, latency, power, etc.

The other issue one has to be concerned with is that even when reliability challenges can be circumvented, with billions of transistors closely packed on a single chip, various quantum physical phenomena might come into play, and their effect on the computation has to be factored in. This requires very elaborate simulation and analysis mechanisms which demands that scientists and engineers work hand-in-hand on such simulation methodologies. Such methodologies must be able to take into account physics, materials, quantum phenomena, and many other issues for billions of elements interacting together. This gives rise to other computational challenges beyond the technology, fault/defect-tolerant design, or architectural or mapping of computations on reprogrammable nanoscale computational fabrics.

The yearly symposium which started as a one-day workshop in 2005, and later grew into a multiple-day symposium backed by ACM and IEEE, aims at bringing together scientists and engineers to present their latest work related to these challenges and discuss other oncoming issues and directions.

In 2007, this symposium was held in San Jose Oct. 21–22, 2007. The main interest by the organizing committee included the following topics.

—Architectures for nanoelectronic digital and mixed-signal circuits and systems

—Computational paradigms and programming models for nanoscale architectures

—Modeling and simulation of nanoelectronic devices, circuits, and system architecture

—Simulation of complex systems with nanoscale computing architectures

—Implementing microarchitecture concepts using nanoarchitecture building blocks

—Defect and fault tolerant nanoelectronic device, circuit, and system level architectures

—Post manufacture testing of nanoelectronic architectures

—Computer aided design tools and methodologies for nanoelectronic architectures

This list is not all inclusive, but it provided guidance to potential authors and attendees on what issues the meeting will address and discuss. In order to facilitate the publication of some of the most interesting papers presented in the conference in archival journals, two special issues were planned in two different international journals. Papers that were more focused on technology were invited for consideration to be published in the *IEEE Transactions on Nanotechnology*, and papers more focused on design automation, architecture, computational issues for large scale simulation etc. were invited for submission to the ACM *Journal of Emerging Technologies for Computing Systems*.

This editorial pertains to the papers in the latter category. In response to our selective invitations (selected based on 3-4 reviews collected during the

paper selection process of the NANOARCH'07 symposium itself), we received 9 submissions. As per ACM journal standards, these papers were sent to 4 or 5 external reviewers, and after two rounds of reviews, we have selected four papers for this special issue.

The first article in the special issue entitled "Towards Achieving Reliable and High-Performance Nanocomputing via Dynamic Redundancy Allocation", by Shuo Wang, Lei Wang and Faquir Jain, directly addresses the fault- and defect-tolerant mapping of computation onto a specifically designed nanofabric by exploiting the redundancy afforded by the large number of devices made available by reduced feature size. The parallelism avoids temporal redundancy and the extra logic allows for spatial redundancy overlapped in time with the original computation.

The second article by Zhengfei Wang, Huaixiu Zheng, Qinwei Shi and Jie Chan, titled " Emerging Nanodevice paradigm: Graphene-based Electronics for Nanoscale Computing", is about an alternative technology based on Graphene which is a monolayer of carbon atoms packed into a two-dimensional lattice. They present designs of a switch, a negative differential resistance device, and a random access memory out of this material. They show results which might be early indication of the usability of this material for future nanoelectronics.

The third article also looks into another alternative technology, namely Quantum Cellular Automata (QCA), and design of memory architecture using QCA. This paper is authored by Baris Taskin, Andy Chiu, Daniel Venutolo and Jonathan Salkind and titled "A Shift-Register Based QCA Memory Architecture" .

The final article of this special issue is related to simulation and the computational issues related to it. This article by Dennis Huo, Qiaoyan Yu, David Wolpert and Paul Ampadu, titled "A Simulator for Ballastic Nanostructures in 2D Electron Gas", describes a simulator based on classical mechanics of electrons which corroborates important experimental results, and hence shows that certain experimental phenomena can be explained with simpler simulation models. The conclusion of this work is that certain devices that operate on ballistic transport principles can be simulated using this implementation, and logics built on such devices can be experimented with.

Even though we have a sample selection of papers from the 2007 NANOARCH symposium, it is not necessarily representative of all the areas and issues discussed in this series of symposium, and for further information on the whole spectrum of research articles that are discussed, one should refer to the proceedings of this symposium.

Finally, I must thank all the authors who submitted their work to this special issue, all the reviewers who kindly spent their time going through the manuscripts several times, relentlessly criticizing, commenting and suggesting improvements. I also extend my thanks to Professor Vijaykrishnan Narayanan, the Editor-in-Chief for this journal for his willingness to sponsor this special issue, as well as his help in various stages of the year-long process. I also thank Professor Ramesh Karri for working out the details of the special issue related to NANOARCH and entrusting me to handle the special issue.

I sincerely hope that the readers of this special issue will find the articles interesting, enlightening, and will possibly build upon the work presented here for future research in this exciting field.

SANDEEP SHUKLA
*Guest Editor*