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GUIDELINES FOR REDUCED ORDER THERMAL MODELING OF MULTI-FINGER GAN HEMTS

A Thesis in

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by

Robert R. Pearson

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The thesis of Robert R. Pearson was reviewed and approved* by the following:

Sukwon Choi
Assistant Professor of Mechanical Engineering
Thesis Co-Adviser

Alexander Rattner
Assistant Professor of Mechanical Engineering
Thesis Co-Adviser

Bladimir Ramos-Alvarado
Assistant Professor of Mechanical Engineering

Daniel Haworth
Professor of Mechanical Engineering
Associate Head for Graduate Programs, Department of Mechanical Engineering

*Signatures are on file in the Graduate School.

ABSTRACT

The increasing demand for tightly integrated gallium nitride (GaN) high electron mobility transistors (HEMT) into electronics systems requires accurate thermal evaluation. While these devices exhibit favorable electrical characteristics, the performance and reliability suffer when operating at elevated operating temperatures. Localized device self-heating, with peak channel and die level heat fluxes on the order of 1 MW cm^{-2} and 1 kW cm^{-2} respectively, presents a need for thermal management that is reliant on accurate channel temperature predictions. In this thesis, a high-fidelity multiphysics modeling approach employing one-way electrothermal coupling is validated against experimental Raman thermometry of a multi-finger GaN HEMT power amplifier under a set of specified DC-bias conditions. A survey of commonly assumed reduced order approximations, in the form of numerical and analytical models, are systematically evaluated with comparisons to the peak channel temperature rise of the coupled multiphysics model. Deviations from electrothermal and constant heat flux assumptions are provided as an alternative basis. Recommendations of modeling assumptions are made relating to self-heating, material properties, and composite layer discretization for numerical and analytical modeling approaches. The importance of electrothermal coupling is emphasized given the structural and bias condition effect on the self-heating profile. Discretization of the composite layers, with temperature dependent material properties that are physically representative, are also recommended.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

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1. INTRODUCTION

Wide-bandgap gallium nitride (GaN) based high electron mobility transistors (HEMTs) provide high performance amplification and switching of direct current (DC) and radio frequency (RF) electrical signals. GaN HEMT devices are increasingly used alongside other III-V compound field effect transistors (FETs) in commercial and defense communications, sensors, and power regulation systems. Forming a heterostructure between GaN and AlGaN, results in a two-dimensional electron gas (2-DEG) channel with substantially enhanced electron drift velocity and concentration [1]; enabling efficient, high frequency and power operation at elevated operating temperatures.

As devices with increasingly higher output powers are developed, the internal heat generation resulting from Joule-heating within the 2-DEG has proportionally increased to 40 kW cm^{-2} across the transistor fingers [2] with die level fluxes of 1 kW cm^{-2} [3]. During typical high voltage operation, an electric field spike forms under the drain side of the transistor gate [4]. The resulting non-uniform thermal energy distribution is localized to a nanoscale region with an order of magnitude greater local heat flux than across the discrete transistor fingers. This self-heating condition demands high efficacy thermal management; the design of which is reliant upon accurate channel temperature predictions to ultimately predict coupled performance and reliability.

Optimal integration of AlGaN/GaN HEMTs into a system, either as an unmatched transistor or a monolithic integrated circuit (MMIC), requires accurate modeling of not only the electrical performance but also the coupled effects of heat generation and thermal transport. Device performance is affected by elevated channel temperatures during operation, because output power typically degrades by 0.01 dB $°C^{-1}$, and similar performance trends are found for gain and power added efficiency (PAE) depending on the number of device stages [2]. Reliability is also impacted

by elevated peak channel temperatures, as a 10°C temperature rise reduces the mean time to failure (MTTF) by an order of magnitude [5]. The temperature sensitive nature of GaN HEMTs prompts the need for foundational verification of thermal modeling assumptions to ensure accurate channel temperature predictions for a variety of academic and industrial purposes.

GaN HEMTs structurally consist of the AlGaN/GaN heterostructure epitaxially grown on a semi-insulating substrate, most commonly silicon carbide (SiC), separated by a thin nucleation layer (NL) such as aluminum nitride (AlN) as illustrated in Figure 1.

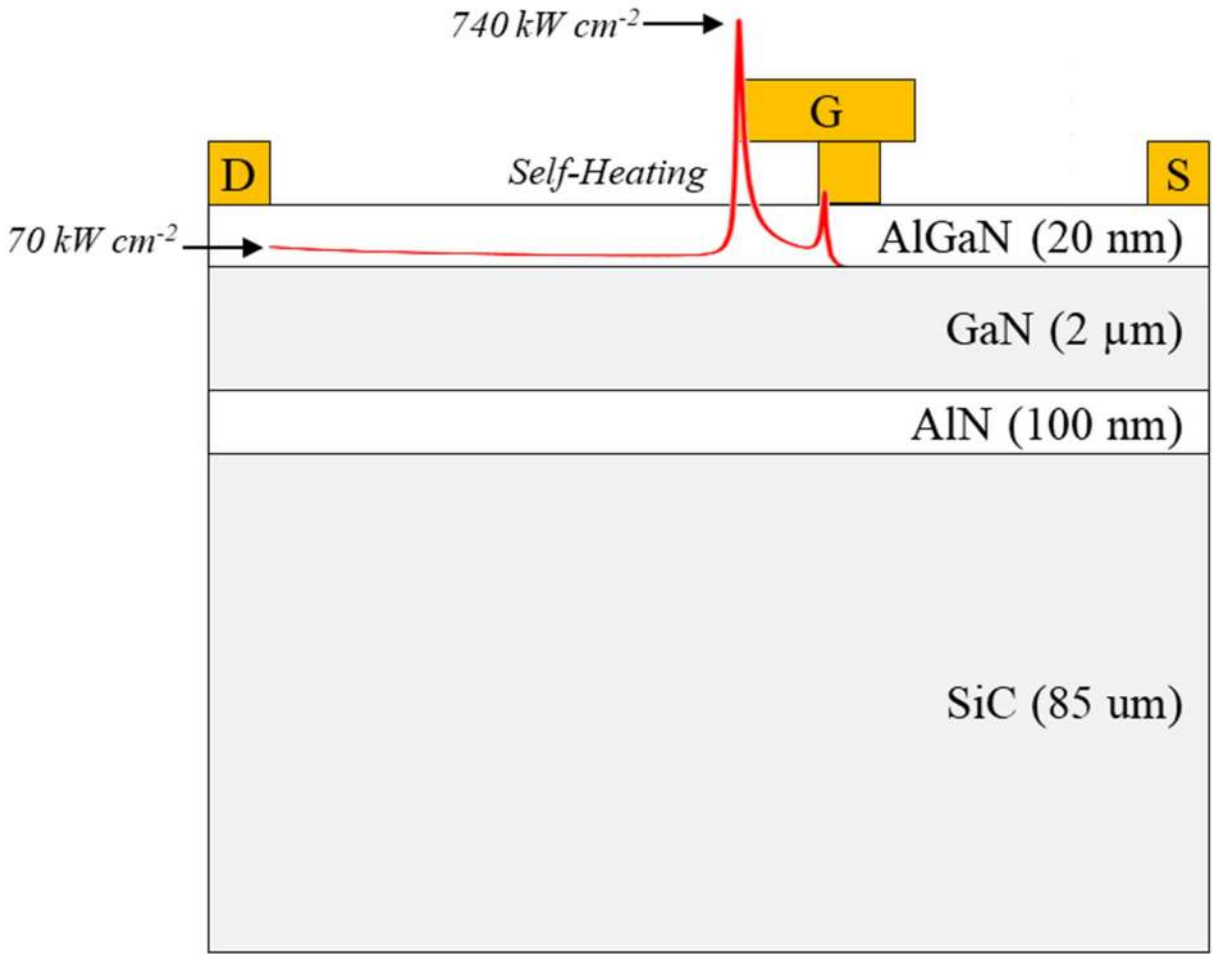

Figure 1 *– GaN HEMT structure, self-heating distribution and magnitudes.*

Typically signal, power, and control are supplied to the die through bond wire connections, with ground provided by an electrically conductive mechanical die attach material at the die base (e.g. conductive adhesive or solder). This arrangement provides a conduction path for the heat to diffuse

from the channel at the drain side of the gate through the GaN, AlN, and SiC substrate at which point it reaches the die attach material and the package and heat-sink assembly. A reliable thermal model of a packaged GaN HEMT must incorporate valid sub-model approximations inherent to this physical problem, including volumetric heat flux distribution, thermal contact resistances between layers, temperature-dependent material and thermal conductivities, and representative boundary conditions. As an illustration of this "best practices" requirement, we found that applying different widely cited modeling approaches and assumptions can lead to up to a 24% deviation for peak device temperature rise over typical device operating conditions.

The goal of this study is to provide modeling guidelines and best practices for accurate channel temperature predictions of AlGaN/GaN HEMTs. This study is intended to aid industrial and academic investigations into device design, packaging, and thermal management. To support this goal, an experiment was performed on a commercially available device to collect temperature data as an exact basis for assessing thermal simulation models. Micro-Raman thermography was used to determine the peak channel temperatures of the device under DC-bias conditions. A high-fidelity numerical model of the packaged device, with one-way coupling to a small-scale device physics electrothermal model, was then validated by comparing the simulation results to experiment. The numerical modeling approach, readily implementable in commercial finite element and volume software packages, is then systematically exercised to evaluate the sensitivity of common modeling assumptions used in a variety of previous investigations to peak channel temperature rise. This includes material properties, self-heating representation, and the presence of composite layers. Numerical modeling with these assumptions is then compared with proposed analytical models as to determine their accuracy. Modeling best practices and use cases for a range of assumptions is then provided.

2. PRIOR THERMAL MODELING METHODS AND ASSUMPTIONS

Analytical methods have been developed and proposed as a computationally efficient means to estimate the peak HEMT channel temperatures. Darwish *et al.* [6] proposed a closed-form solution for steady and uniform surface heating of a homogenous die, which they later augmented with an approximation to account for the epitaxial layer [7]. This method assumes that the heat is applied over the projected gate area and that the number of fingers is sufficiently large for adiabatic symmetry. Ditri [8] employed an exact, Fourier series solution to arbitrary surface heating of a homogenous substrate with orthotropic properties, with one application to thermally asses self-heating integrated circuits. Ditri extended this model to multiple-gate MMIC channel temperature predictions, albeit without provisions for discretizing the epitaxial heterostructure. These select analytical solutions account for temperature dependent thermal conductivity through use of the Kirchhoff transformation. However, this analytic approach cannot resolve the composite mediums and typical convective boundary conditions of packaged GaN HEMTS [9] [10].

Numerical methods have also been employed by performing thermal conduction modeling using continuum-scale heat diffusion (i.e., Fourier's Law). These methods offer expansive modeling flexibility however involve greater computational cost than the analytical methods. Pioneering micro-Raman spectroscopy measurements and method thermal simulations of multiple-finger GaN HEMTs performed by Kuball *et al.* [11] baseline common assumptions. In their finite difference simulations, they assumed that the heat was dissipated within a 1 μm long region at the end of the gate; equivalent to that of the 1 μm spatial resolution of the thermometry technique. They also assumed the thermal conductivity of the GaN and SiC material be to be inversely proportionally to temperature with concerns expressed over the room temperature values and temperature dependence. The thermal boundary resistance (TBR) of the aluminum nitride

(AlN) nucleation layer, located between the AlGaN/GaN heterostructure and substrate, were neglected entirely.

The spatially dependent self-heating profile can be predicted by coupled electrothermal modeling techniques available in commercial software packages. Heller and Crespo [12], [13] used this approach to predict the self-heating distribution under different gate bias conditions for an AlGaN/GaN HEMT. The heterostructure was modeled electrothermally in two dimensions (2D) with coupling to a three dimensional (3D) finite element method (FEM). Their electrothermal simulations indicated that the Joule-heating within the 2-DEG, occurring at the drain edge of the gate, does not scale with the physical gate length as commonly assumed. Multiple-finger HEMT simulations indicated that the temperature distribution across the width of the gates can often be neglected; supporting the 2D modeling assumption. Different bias conditions were shown to affect the power dissipation distribution in the channel, which may impact activation energy predictions critical to predicting device reliability. Subsequent studies by Choi *et al*. [14] and Heller *et al.* [15] confirmed that less negative gate bias conditions, for a given level of total power dissipation, decreased the channel temperature and subsequently the thermal gradient as the channel resistance becomes more uniform. The opposite was observed for increased drain bias voltages. The one-way coupled electro-thermal simulation methodology was recently extended to a fully-coupled modeling scheme by Chatterjee *et al*. [16] to further improve the accuracy of the calculated channel temperatures. While established techniques of electrothermal coupling provide the most accurate prediction of self-heating within the device, the economics of performing the specialized analysis may be prohibitive.

Many different modeling practices and approximations have been previously employed by these methods but have not been systematically assessed to determine their impact on temperature rise predictions and computational cost. Table 1 represents a brief survey of common thermal modeling assumptions used in publications relating to the structural discretization, material properties, and input boundary conditions for numerical studies.

Table 1– *Survey of assumed thermal conductivities, boundary resistances, and self-heating representations.*

Ref.	GaN k(T) ($W\ m^{-1}\ K^{-1}$)	SiC k(T) ($W\ m^{-1}\ K^{-1}$)	TBR R'' ($cm^2\ K\ kW^{-1}$)	Heat Flux Application Method
[11]	$160\times(T/300)^{-1.00}$	$330\times(T/300)^{-1.00}$	0	1 µm x Wg (drain side)
[9]	$160\times (T/300)^{-1.40}$	$340\times(T/300)^{-1.50}$	0	Lg x Wg (gate projection)
[17]	130	400	0	Active area (Ng x Pg) x Wg
[12]	$267-4.25\times10^{-1}\times T+3\times10^{-4}\times T^2$	6H, $387\times(T/293)^{-1.49}$	0.01	Electrothermal coupling
[18]	$130\times(T/300)^{-1.40}$	6H-, $370\times(T/300)^{-1.49}$	0.01	Lg x Wg (gate projection)
[4]	$150\times(T/300)^{-1.40}$	6H-, $387\times(T/293)^{-1.49}$	0.60	Electrothermal coupling
[19]	$150\times(T/300)^{-1.40}$	6H-, $387\times(T/293)^{-1.49}$	0.33	Lg x Wg (gate projection)
[20]	$-0.1623\times T+214.17$	$0.0038\times T^2-4.1734\times T+1259$	0.20	Lg x Wg (gate projection)
[21]	$161\times(T/293)^{-1.45}$	$416\times(T/293)^{-1.50}$	0.33	0.75 µm x Wg (drain side)
[2]	∞	$360\times(T/300)^{-1.90}$	0	NP

Structurally, the most basic models consider only the substrate, compensated with lower room temperature thermal conductivity (k_{ref}) and increased temperature sensitivity (α), while more comprehensive models include the epitaxial layer and the thermal boundary resistance (TBR) of the nucleation layer. Temperature dependent thermal conductivities were assumed for each layer depending on the manufacturing process, and resultant dopants, impurities, and dislocations. For instance, k_{ref} of high-quality bulk GaN is reported as high as 260 $W\ m^{-1}\ K^{-1}$ [22] however can be reduced by half when epitaxially grown [23].

Joule-heating is typically represented by a spatially dependent heat flux distributed over a finite area on the top most composite layer (i.e., the SiC if the GaN epitaxial layer is ignored, otherwise the GaN epitaxial layer). A common heat flux application method is to assume that the

heat is uniformly distributed over the projected length and width of the gate. Uncoupled heat transfer studies that employ this assumption often neglect the effect of device bias conditions. To account for these effects, the most advanced techniques consider full one- [12], [14], [15], [24] or two-way [16] electrothermal coupling to comprehensively include DC-bias dependent effect on self-heating.

3. EXPERIMENTAL APPROACH

To baseline a set of thermal modeling best practices, the channel temperature of a commercially available, multiple-finger GaN HEMT device was determined by experiment. The packaged device was DC-biased at steady-state to manufacturer published typical operating conditions. Midpoint channel temperatures, extracted using linear two-peak fit Raman thermometry, were locally sampled with a spatial resolution of approximately 1 μm along the visible drain side of the device following the procedure outlined in [25]. The two-peak method was utilized as to avoid temperature underprediction from the single peak position method [26], caused by thermoelastic stress, and reduced experimental uncertainty as compared with the linewidth method [27]. The maximum temperature was determined by local sampling to occur away at the 9th finger from the center of the device (22nd inward from the furthest extents of the middle); as the package contains multiple dies to achieve a total of 60 fingers. Two-peak fit method measurements were therefore extracted at this location for direct comparison with simulation results. The uncertainty of these measurements was estimated to be 14% after propagating the errors from bias conditions and thermography techniques [25].

Gate and drain DC-bias conditions, provided in Table 2 alongside the temperature data, were supplied by KEITHLEY 2400 and 2651 source meter units (SMUs) to achieve a transistor power density, over unit gate length, of up to 4 W mm^{-1}.

Table 2 *– Summary of DUT DC-bias conditions and resulting two-peak Raman thermography temperature rise.*

Power Density (W mm^{-1})	Power (W)	V_{gs} (V)	I_{ds} (A)	V_{ds} (V)	Two-Peak ΔT (K)
1	22.2	-2.88	0.56	40.00	33.165
2	44.4	-2.67	1.11	40.00	96.781
3	66.6	-2.42	1.67	40.00	155.324
4	88.8	-2.25	2.22	40.00	215.984

For reference to HEMT heat flux metrics, such as the 40 kW cm^{-2} referenced in [2], the equivalent heat flux for the 4 W mm^{-1} DC-bias condition is 52 kW cm^{-2} when considering the active region of the device (i.e., between the drain and source). The lid of the flanged ceramic package was removed to expose the epitaxial layers of the device to the line of sight of a HORIBA LabRAM confocal Raman microscope.

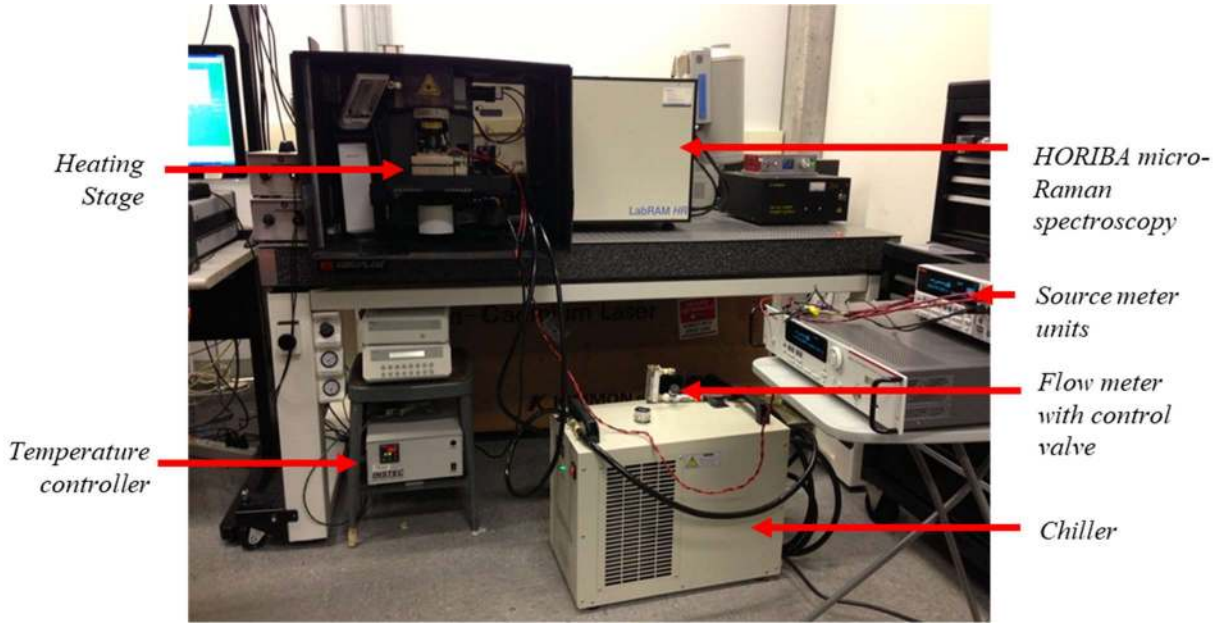

Figure 2 *– Experimental setup used to collect Raman thermometry and stage temperature data for a DC-biased GaN HEMT.*

An annotated photograph of the experimental setup is provided in Figure 2. The 60-finger device under test (DUT) inside the package, with gate width of 370 µm, gate length of 0.8 µm, and gate pitch of 50 µm, is comprised of approximately 2 µm of GaN grown epitaxially using metal-organic chemical vapor deposition (MOCVD) on an 85 µm thick semi-insulating 6H-SiC substrate. A eutectic solder composition of 80% gold and 20% tin (80Au20Sn) attached the substrate to a 15% copper and 85% tungsten (15Cu85W) shim. The base of the 15Cu85W shim was fastened to the oxygen-free copper (C101) equipment chassis of a manufacturer supplied evaluation board. A thin bond-line of Arctic Silver 5, resulting from high pressure (i.e., 7 MPa) mechanical fastening, was

used as a thermal interface material between the shim and the chassis, and between the chassis and INSTEC HCC314S heating stage. Heat diffused through the chassis to the heating stage, while stage temperature was maintained at 24 to 26.2°C for the range of bias conditions by controlling the water temperature with an INSTEC C300W industrial chiller, and the flow rate using a control valve and flow meter.

4. VALIDATED HIGH-FIDELITY MULTIPHYSICS MODELING APPROACH

A three-dimensional (3D), steady-state finite element model was implemented using COMSOL Multiphysics 5.3 [28] to solve the governing equation of steady-state heat conduction with temperature dependent thermal conductivity of the constituent materials.

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)=0 \quad (1)$$

The numerical model consisted of volumes representing the packaged device and the experimental setup including: the device die (a 60 finger GaN HEMT grown on a 6H-SiC substrates), 80Au20Sn solder, 15Cu85W shim, and C101 equipment chassis. Physically valid quarter symmetry (i.e. adiabatic conditions about the Y-Z and Z-X planes) was imposed on the device and package as to assist with computational efficiency, as seen by the annotated isometric view in Figure 3.

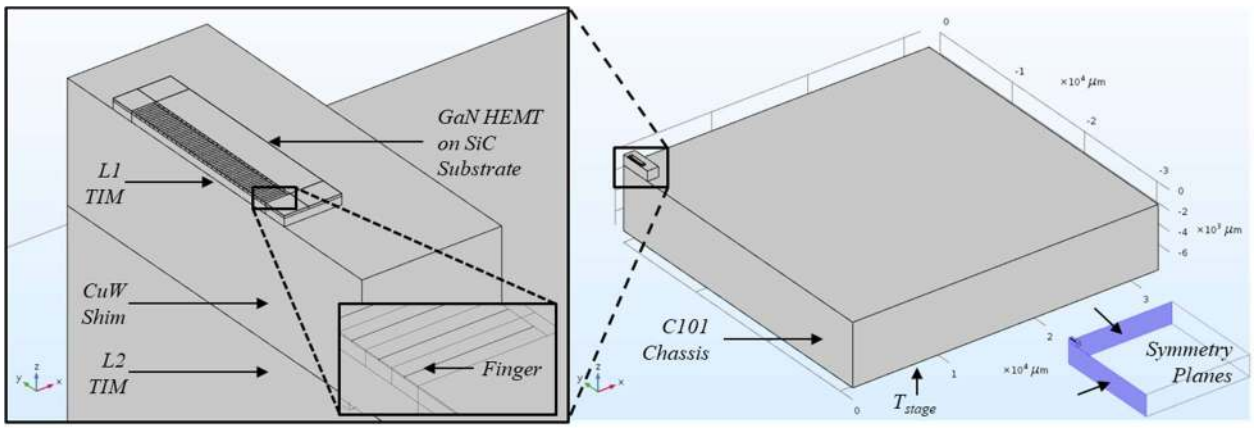

Figure 3 *– Isometric view of quarter symmetric computational domain.*

Several approximations were made to the thin layers deposited on top of the GaN epitaxial layer that are appropriate for heat transport through the substrate base to reduce modeling complexity. The silicon nitride (SiN) passivation, and surface metallization of the source, drain, and gate ohmic contacts were neglected based on their small impact on spreading heat flux in-plane [7]. Similarly,

the presence of the thin AlGaN layer was omitted, as the typically thickness is of two orders of magnitude thinner than the GaN layer with low thermal conductivity (<30 W m^{-1} K^{-1}) [4].

One-way coupled electrothermal modeling was employed by mapping an electrothermal heat flux (ETHF) profile, generated from a two-dimensional (2D) small-scale physics submodel, to the full 3D finite element model. The 2D technology computer aided design (TCAD) model utilizes Synopsys Sentaurus to solve for the heat generation and thermal transport in one finger of the HEMT device [29]. The transport of charge carriers was calculated using Poisson's equation by solving for the electrostatic potential. The thermodynamic model of energy transport, an extension to the drift flux model, was coupled with the heat diffusion equation and solved under the various operating bias conditions. Temperature dependent electronic and thermal properties were used, including: bandgap energy, electron mobility, dielectric constant, and thermal conductivity. These properties were adopted from the values reported in literature [30] [31] [32]. The heat generation profile obtained from the TCAD model was imported into the 3D finite element model to achieve one-way electrothermal coupling. This method captures the effect of different bias conditions on the device self-heating and temperature distribution of the 2-DEG channel [12] [16] which simplistic models fail to capture [33].

The resulting heat flux profile, provided in Figure 4 for each bias condition, predicts a peak flux of up to 740 kW cm^{-2} at the 4 W mm^{-1} condition under the edge of the T-gate flange.

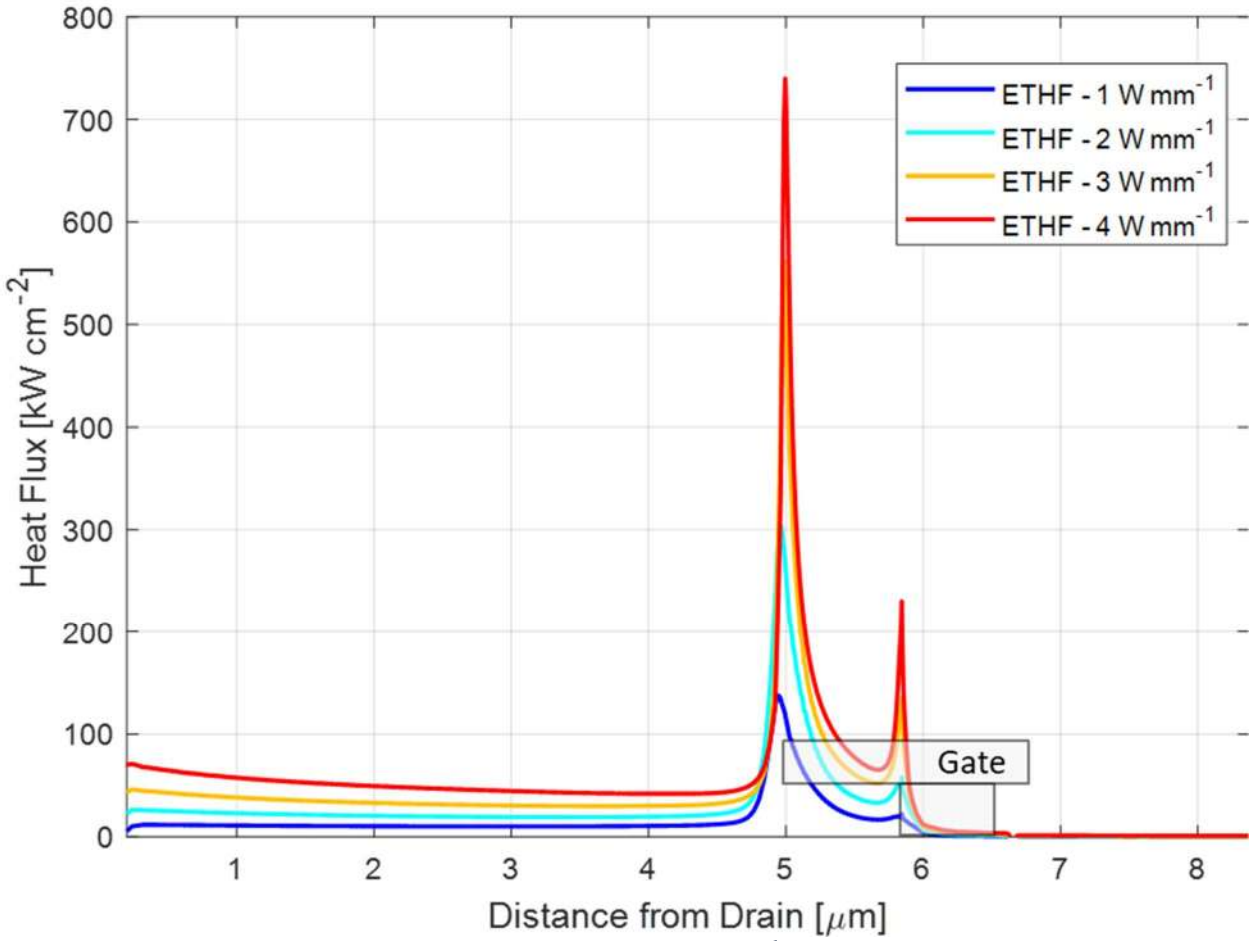

Figure 4 *– ETHF profiles for the 1-4 W mm^{-1} bias conditions.*

Without the AlGaN layer, the areal heat flux was applied to the topside of the GaN contact layer at the physical interface of the AlGaN/GaN heterostructure to represent device self-heating occurring in the 2-DEG channel.

$$q_z'' = -k\frac{dT}{dz} = f(x,y) \tag{2}$$

The base of the equipment chassis was assumed to be isothermal and equal to the instrumented device bias condition dependent heater stage temperature.

$$T(z=0) = T_{stage} \tag{3}$$

Additional heat transfer through free convention and radiation was neglected through specifying adiabatic boundary conditions normal to all other exterior faces [16].

$$0 = -k\frac{\mathrm{dT}}{\mathrm{dn}} \tag{4}$$

The assumed isotropic material properties provided in Table 3 considers the temperature dependent thermal conductivity of the GaN, SiC, and CuW materials.

Table 3 *– Assumed thermal conductivity of solid volumes in the discretized device and package (temperatures in K).*

Material	Thermal Conductivity (W m^{-1} K^{-1})	Reference
GaN	$146x(T/300)^{-1.40}$	[23]
6H-SiC	$387x(T/293)^{-1.49}$	[34]
80Au20Sn	57	[35]
15Cu85Mo	$-7.62E-5xT^2-2.51E-2xT+204$	[36]
C101	385	[37]

The temperature dependence of the thermal conductivity was captured through the typical power-law distribution for the GaN and SiC materials.

$$k = k_{ref}\left(\frac{T}{T_{ref}}\right)^{\alpha} \tag{5}$$

A quadratic regression was chosen for 15Cu85W. Table 4 contains the selected representative thermal impedances of the TBR and L2 TIM.

Table 4 *- Assumed thermal impedance of interfaces within the device and package.*

Material	Thermal Impedance (cm^2 K kW^{-1})	Reference
TBR	0.06	[38]
L2 TIM	30	[39] [40] [41]

These thermal impedances were represented by a thermally thick layer that conserves heat flux out-of-plane but neglects in-plane diffusion due to the small thickness of the layers.

$$q_z'' = -\frac{\Delta T}{R''} \tag{6}$$

Mesh convergence studies were performed to ensure a grid insensitive result, with the assistance of the analytical method proposed by Ditri in [42]. A homogenous SiC substrate was modeled with k_{ref} =387 W/m-K, T_{ref} = 293 K, and α of 1.49 matching the full numerical model. An infinite-number of transistor fingers was represented by modeling a single finger with adjacent symmetry boundary conditions between fingers and half symmetry about the die midplane (i.e. Y-Z plane). The width-wise dimension in line with the X direction was made sufficiently large as to avoid the influence of the die edge. A physically smaller transistor than the DUT, with gate length of 0.25 μm, width of 250 μm, and pitch of 25 μm, was assumed in line with other verification studies [7]. Self-heating was represented by applying a uniform heat flux across the gate projected area with power densities ranging from 5 to 10 W mm^{-1}. The base of the die was set to a constant temperature of 300 K with adiabatic conditions enforced on all other faces to match the boundary conditions of the analytical method used as a basis [42].

The first case (Case 1) placed three elements across the gate length, with the element size along the gate width equal to the gate length, and ten elements biased from the gate to the edge of the infinite finger symmetry plane boundary condition and within the top 20 μm of the substrate. The resolution of this fine mesh case was then sequentially halved twice to form Case 2 and 3 respectively as plotted in Figure 5.

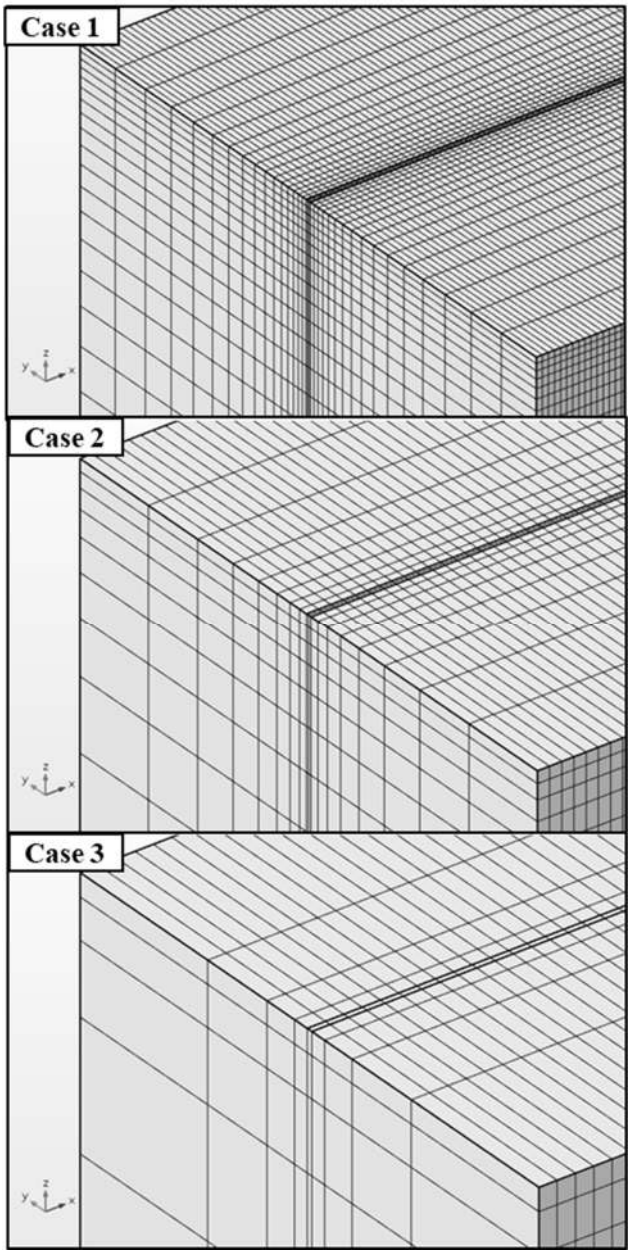

Figure 5 *– Comparison of finest mesh case (Case 1) to Case 2 and 3 with sequentially halved resolution.*

The required mesh resolution using linear and quadratic finite elements was explored by reviewing the results presented in Table 5 and Table 6. The peak temperature rise above the isothermal boundary condition (ΔT_{cb}) predicted by numerical simulation was compared with the exact analytical solution. A monotonic decrease in error between the exact and analytical solution is observed for all but the finest mesh case with quadratic elements. This finest quadratic finite element mesh case still presents agreement with the analytical model for peak temperature rise

within 1%. The change in convergence trends for this case may be due to truncation of the analytical Fourier series solution or round-off of the numerical solution. Discretization errors for these results were calculated per the recommended procedure outlined by the Journal of Fluids Engineering [43].

Table 5 *- Analytical vs. linear finite element mesh sensitivity study results.*

P_{mm}	Analytical	Case 1		Case 2		Case 3	
	ΔT_{cb}	ΔT_{cb}	Error	ΔT_{cb}	Error	ΔT_{cb}	Error
(W mm^{-1})	(K)	(K)	(%)	(K)	(%)	(K)	(%)
5	78.05	77.60	-0.58%	76.00	-2.62%	71.44	-8.46%
7.5	128.95	128.07	-0.68%	125.17	-2.93%	116.99	-9.27%
10	190.85	189.26	-0.83%	184.50	-3.33%	171.33	-10.23%

Table 6 *- Analytical vs. quadratic finite element mesh sensitivity study results.*

P_{mm}	Analytical	Case 1		Case 2		Case 3	
	ΔT_{cb}	ΔT_{cb}	Error	ΔT_{cb}	Error	ΔT_{cb}	Error
(W mm^{-1})	(K)	(K)	(%)	(K)	(%)	(K)	(%)
5	78.05	78.71	0.84%	78.61	0.72%	74.33	-4.77%
7.5	128.95	130.11	0.90%	129.91	0.75%	122.20	-5.24%
10	190.85	192.64	0.94%	192.29	0.75%	179.77	-5.80%

For power densities of 10 W mm^{-1}, the quadratic discretization yielded an empirical convergence rate of 5.16 and an estimated discretization error of 0.07% for the finest mesh. With linear elements, the convergence rate was 1.47 and the discretization error was 0.97% for the finest mesh. The case 2 mesh with quadratic elements was utilized for this investigation as the discretization error is less than 0.1% as compared with the finest mesh case with sample temperature rise results provided in Figure 6. Additional refinement beyond case 1 was applied to the channel probed by micro-Raman thermometry to further minimize discretization error and facilitate mapping of coupled heat fluxes.

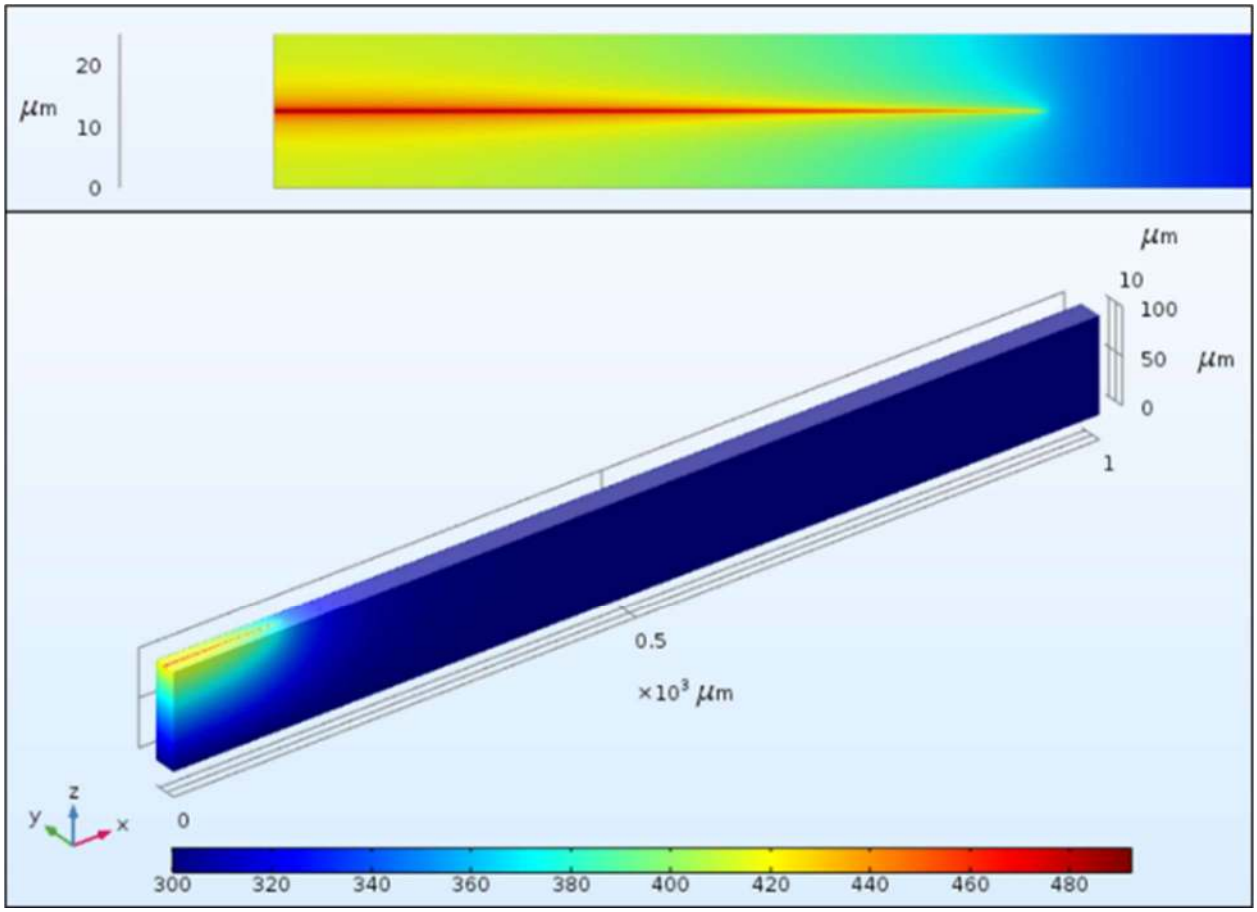

Figure 6 *– Top and isometric views of the temperature distribution through the SiC substrate used for the grid independence study with a peak of 492.3 K for a linear power density of 10 W mm^{-1}.*

The results from the Raman thermometry experiment were used to validate a high-fidelity numerical modeling method with one-way coupling to an electrothermal device simulation. Simulation results were compared with experimental values by volume averaging the temperature at the midpoint of the visible drain edge of the gate as to emulate the thermometry technique. The volume consisted of an extruded unit micron area through the GaN thickness. This closely matches the probing volume of the Raman laser source and allows for direct comparison with experimental results. The maximum temperature at the location of interest was also extracted from the numerical approaches to compare with volume averages. These data are reported as temperature rises relative to the heating stage ($T - T_{\text{stage}}$).

The volume averaged electrothermal simulation correlates well within the uncertainty of the micro-Raman thermometry measurements as seen in Figure 7. An absolute temperature rise percent difference (i.e., $2\times|\Delta T_{mod}-\Delta T_{meas}|/(\Delta T_{mod}+\Delta T_{meas})$) not exceeding 0.9% between volume averaged channel and stage temperature was calculated from 2 to 4 W mm^{-1}. It should be noted that the peak temperature of the local channel was 7.1% to 10.5% greater than the volume averaged results, illustrating the underestimation of the applied thermometry technique from the peak temperature at this location on the device caused by spatial averaging of the temperature field.

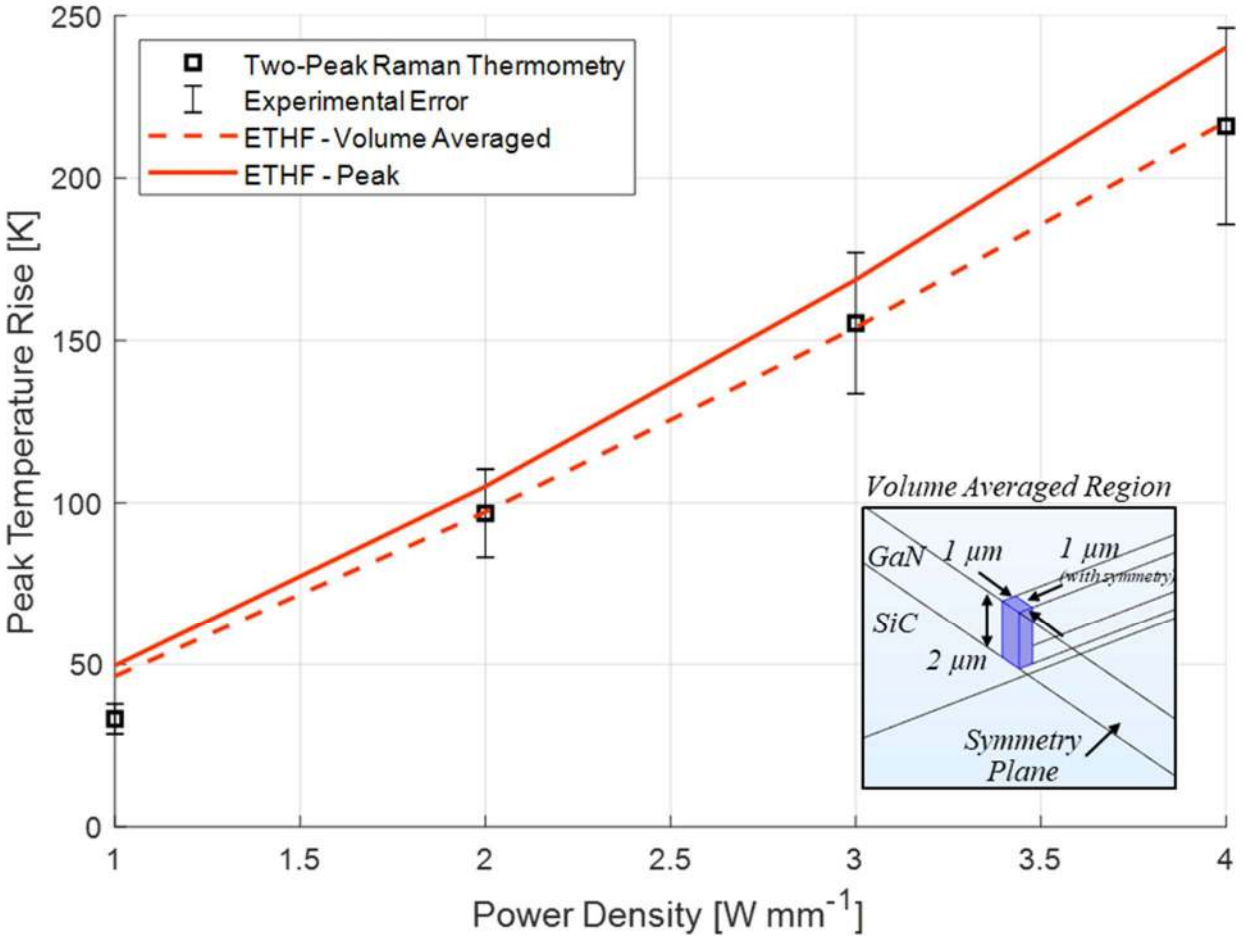

***Figure** 7 – Comparison of experimental and multiphysics model volume and peak channel temperature rises over power density.*

5. ASSESSING ACCURACY AND COMPUTIONAL COST OF ORDER REDUCTION

In Section 4, a high fidelity multiphysics modeling approach was applied to yield close agreement with experimental thermometry of peak device temperature rise. However, this modeling approach incurs significant setup and computational cost. Prior numerical modeling approaches have been proposed that use simplifications relating to the material properties, the self-heating boundary condition, and physical discretization (c.f. Table 1). Additionally, analytical models [6], [7], [8], [42] have been proposed that offer minimal computational costs but adopt even more simplified device descriptions. In this section, such model simplifications will be compared with the validated high-fidelity modeling approach to form practical guidelines and quantify tradeoffs for HEMT simulation results, as well as the peak temperatures predicted by electrothermal thermal modeling. Experimental measurements, reflecting the volume averaged coupling were used as comparison metrics for these reduced order models. A comprehensive set of bias condition dependent data comparing these models to the experimental results, and the results of a common heat flux assumption, can be found in the APPENDIX. These comparisons will assist in future validation exercises and guideline applications.

5.1. CONSTANT HEAT FLUX SELF-HEATING

A common simplification to the bias dependent self-heating profile is to represent the self-heating as a constant heat flux (CHF) zone. Many studies assume the area of this zone to be bounded by a structural dimension such as the area underneath the gate or between the gate and drain electrodes [11], [9], [11], [44], [18], [19] , [20], [21]. Few studies leverage the insights provided by the bias condition dependent electric field provided by electrothermal device simulation [21]. This electric field varies depending on the drain and gate voltage, with less of a

concentration near the drain for fully opened gate bias conditions [14]. This suggests the need for electrothermal modeling to verify the resulting heat flux profile for devices with different transistor structures and use-case dependent bias conditions.

To compare with the accuracy of this device operating with set DC-bias conditions, the heat flux profiles plotted in Figure 4 were studied to determine the length of a CHF zone. For a 4 W mm^{-1} power density, the peak heat flux occurs approximately 0.85 µm away from the drain edge of the gate; coinciding with the overhang length of the T-gate horizontal flange (i.e., the distance between the drain side edge of the vertical position of the gate and the end of the horizontal edge). In comparison with the one-way electrothermal modeling, applying a CHF over this length imposes a uniform heat flux of 470 kW cm^{-2} extending off the drain edge of the T-gate vertical "web" as seen in Figure 8.

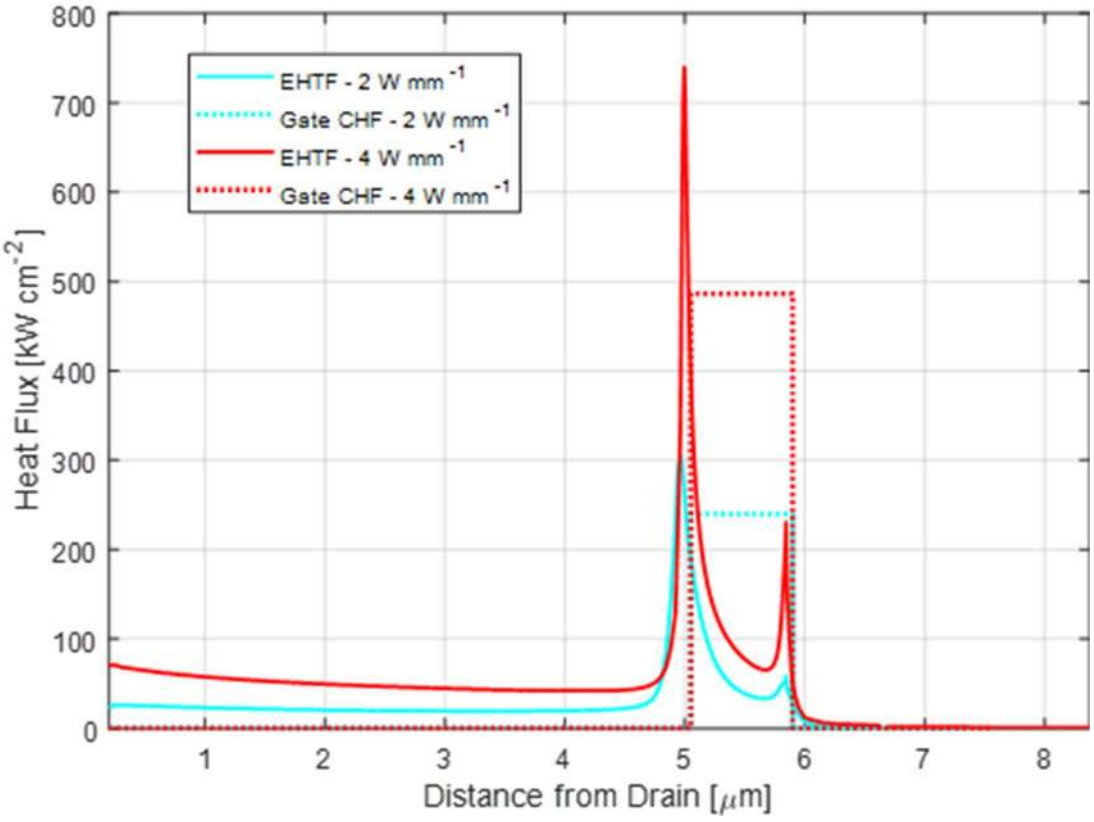

Figure 8 *– ETHF profiles compared with an assumed constant heat flux over an arbitrary length for the 2 and 4 W mm^{-1} bias conditions.*

Simulation shows that applying this CHF simplification increases the difference between volume averaged simulation and the micro-Raman thermometry experiment to 5.2% for a power density of 4 W mm^{-1}. This difference is still within experimental uncertainty of 14%. In comparison with the peak temperature predicted by the multiphysics model with electrothermal heat flux mapping at this gate, this CHF assumption overpredicts the peak temperature rises by 5.8 to 8.9% however. Assuming a heated length of 1 μm [11] instead reduces the peak temperature rise error to 6.3% and 7.7%. This error may be further minimized by continuing to increase the length (e.g., increasing the heated length to 1.5 μm decreases the error to 3.7% at 2 W mm^{-1} and 4.2% at 4 W mm^{-1}). Alternatively the channel may be discretized into two or more heated zones from the gate to drain as to resolve the elevated heat flux near the drain side of the gate and the background flux leading to the drain. Care should be taken however to verify that this assumption is extensible to the range of device operating conditions following calibration.

Another common assumption is to assume that the heat flux is distributed over the multiple-finger HEMT active area [44] , [17] (i.e., up to encompassing all drains, gates, and source contacts and the area in between). Electrothermal modeling insights suggest that this assumption is physically incorrect for the DC-bias conditions applied to the DUT, however certain bias conditions could exist to open the channel for other devices and applications (i.e., gate voltage further from pinch-off and lower drain voltage [14]). If the heat flux was uniformly assumed from the drain edge of the gate to drain ohmic contact, then the equivalent uniform heat flux reduces to 68 kW cm^{-2} from 470 kW cm^{-2} for the 4 W mm^{-1} power density. Furthermore, the heat flux would be further reduced to 52 kW cm^{-2} if the channel was fully opened between the source and drain. The peak temperature rise implications of assuming CHF in these locally active regions are displayed in Figure 9, as compared with the electrothermal and baseline CHF profile. Applying a

CHF zone from the drain to gate underpredicts the peak temperature rise by -5.4% to -7.5% while the fully open gate underpredicts by -7.1% to -9.6% from 2-4 W mm^{-1} power densities. These bounding results further reinforce the need to perform electrothermal modeling as a basis for applied heat-flux order reduction where peak channel temperature accuracy within +/- 5% is required.

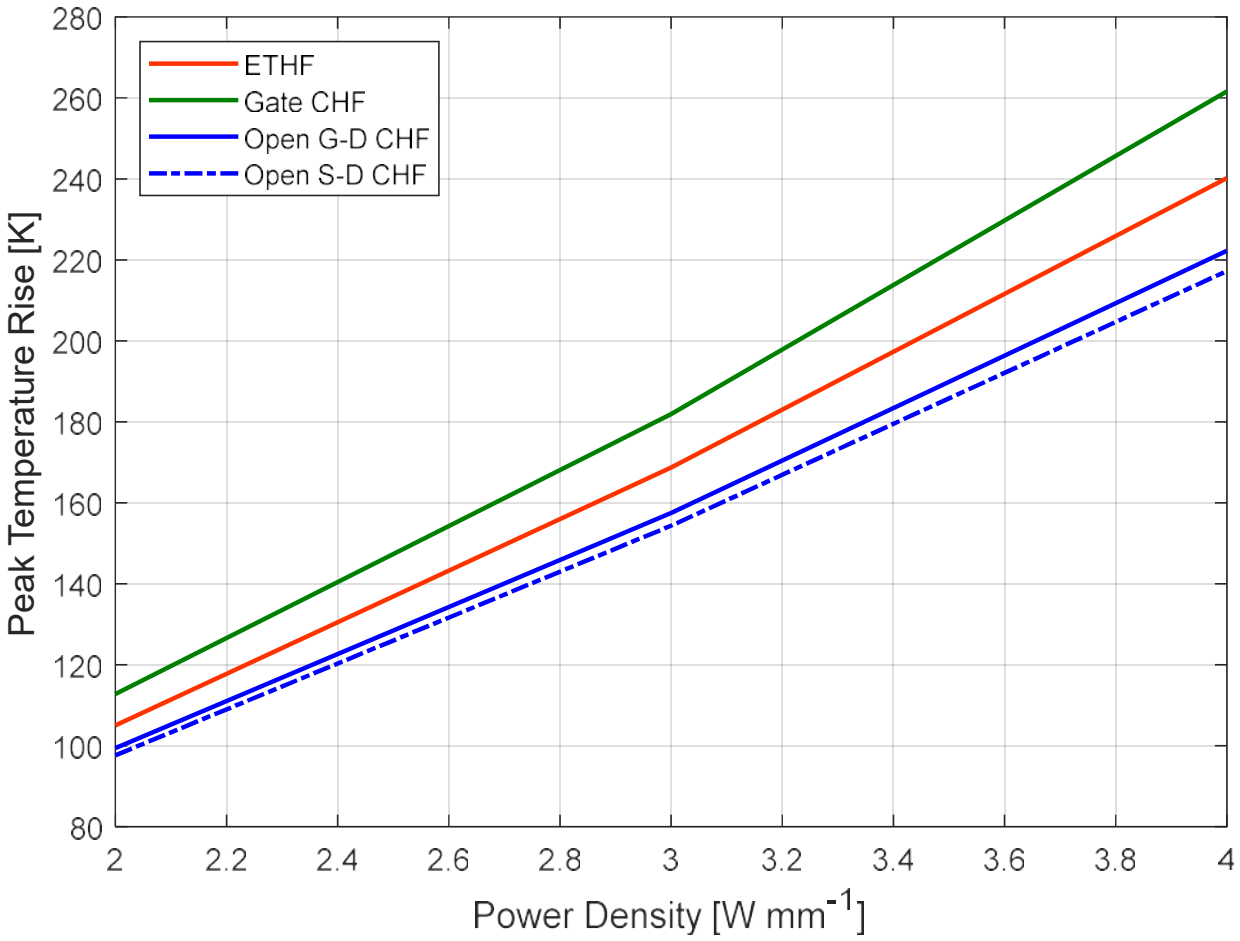

Figure 9 *– Peak temperature rise over power density for the multiphysics model with electrothermal heat flux, constant heat flux referencing the gate geometry, and constant heat flux assuming a locally active regions between the gate and drain, and source and drain.*

5.2. MATERIAL PROPERTIES

Although the multiphysics approach in Section 4 shows close agreement between measured and simulation volume averaged temperature rises, there is some uncertainty in the material properties of the GaN channel, 6H-SiC substrate, and TBR. The surveyed publications (c.f. Table 1) report a GaN epitaxial layer k_{ref} ranging from 130 to 160 W m^{-1} K^{-1}, for α of -1.4 to -1.45, and up to 165 W m^{-1} K^{-1} with α of -0.46 [7] [12]. The GaN epitaxial layer is typically grown on the substrate with MOCVD, as was the case for the DUT, or molecular beam epitaxy (MBE) [45] [46]. Studies that assumed properties with α of -0.46 reflect the early simulations of Zou *et al.* [47] into the effect of quality and doping on k_{ref} for GaN films much thicker than the phonon mean free path with dislocation densities of 10^{10} cm^{-2}. Their findings agree well with experiments on thick GaN samples grown with hydride vapor phase epitaxy (HVPE) [48] [49]. Subsequently Beechem *et al.* [23] performed time domain thermoreflectance measurements and phonon scattering analysis to also include the size effect of thin GaN layers representative of GaN HEMTs. As before, they found that the thermal conductivity is affected in part by the dislocation density and impurity concentration resulting from the epitaxial growth method. Extrinsic p-type doping with Si causes a reduction in k_{ref} at lower impurity concentrations than n-type doping with Mg [23] [50]. Increased phonon scattering as the film reaches the mean free path length scale was also found to reduce bulk GaN k_{ref} by 50% as phonon scattering increases for 1 µm thick films [23]. This agrees well with the frequency domain thermoreflectance measurements performed by Ziade *et al.* [51] of 1 µm thick GaN grown with MBE, with a dislocation density of 5.2 x 10^{9} cm^{-2}, in addition to the time domain thermoreflectance measurements of Bougher *et al.* [52] for 0.31 to 1.27 µm thick GaN grown with MOCVD.

In this study, k_{ref} of the 2 μm thick GaN epitaxial layer grown by MOCVD, with an assumed dislocation density of 5.0 x 10^9 cm^{-2}, was estimated from the phonon scattering analysis of Beechem *et al.* [23] to be approximately 150 W m^{-1} K^{-1}. The commonly assumed value for α of 1.4 was chosen, referencing best fit simulations performed by Sarua *et al.* [53] that matched Raman thermometry of a DC-biased ungated AlGaN/GaN HEMT. With this α, every 10 W/m-K decrease in k_{ref} linearly increases the temperature rise by approximately 4.9 K within the range of 130 to 160 W/m-K. The use of the properties reported by Zou *et al.* [47] with the baseline gate CHF model decreases the peak temperature rise error to 0.15% at 2 W mm^{-1} and -4.4% at 4 W mm^{-1} when compared with the multiphysics peak temperature rise. The agreement between the apparent peak temperature rise predicted by the multiphysics model with this dataset is by coincidence of the assumed CHF length however. As an illustration, these peak temperature rises are 6.7% to 12.2% lower than the baseline CHF model.

Presumably the purity of 6H-SiC substrates has since improved since Burgemeister *et al*. [34] reported a k_{ref} of 387 W m^{-1} K^{-1} at 293 K (374 W m^{-1} K^{-1} at 300 K) with α of -1.49 in 1979. Killat *et al.* in 2014 [54] performed micro-Raman thermography on an ungated HEMT formed by MOCVD of 1.8 μm GaN on 100 μm 4H- and 6H- SiC substrates. They reported a k_{ref} of 410 and 450 W m^{-1} K^{-1} for each respective SiC polytype. They assumed an effective TBR of 0.18 cm^2 K kW^{-1} between the GaN and SiC layer, equivalent to the value reported by Manoi *et al.* [38] for a university research sample with interface temperature between 150 to 175°C. Other commercial samples that they studied with a 70 nm NL exhibit an effective TBR of 0.3 to 0.6 cm^2 K kW^{-1}. Independent evaluation of these increasing the substrate thermal conductivity and halving the effective TBR, with the gate CHF model, reduces the 4 W mm^{-1} peak temperature rise error from 8.9% to 6.4% and 4.8% respectively. A 50% decrease in the effective TBR is shown to reduce

peak temperature rise predictions by -1.5% at the 4 W mm^{-1} power density. The decrease in error suggests that using this set of properties is conservative for engineering applications where a similar CHF assumption may be adopted, as the true peak channel temperature rise will not be under predicted.

Another model reduction technique, especially for thermal management investigations, may be to consider the use of temperature independent material properties [17]. This approximation was explored using the gate defined CHF model as before. The properties defined in Table 3 and Table 4 were used with α set to zero. Without temperature dependent thermal conductivity, but including the TBR, the model underpredicts the peak temperature rise by -6.1% to -17.3% from 2-4 W mm^{-1}. Despite resolving the GaN epitaxial layer and TBR, the use of constant properties produces a temperature rise less than that of the open channel from the gate to drain (c.f. Figure 10). When compared to the baseline CHF model, the use of constant properties underpredicts the peak temperature rise by up to -24%. It is therefore not recommended to use constant material properties at these power densities given the thermal resistance contribution.

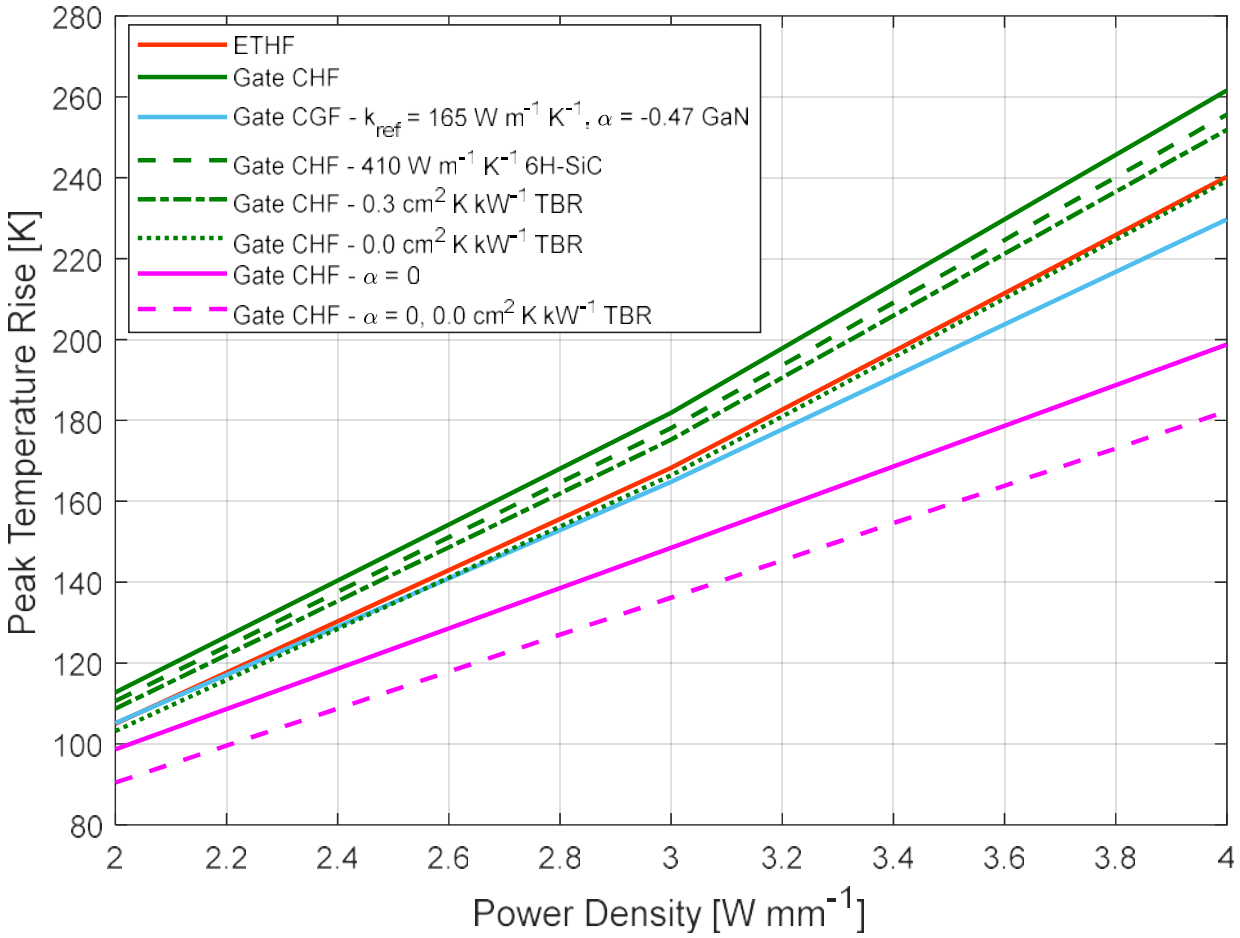

Figure 10 *– Peak temperature rise over power density comparing the multiphysics model to the gate heat flux model with modifications to the constitutive material properties.*

5.3. COMPOSITE LAYERS

Beyond the reductions already investigated, the reduction in accuracy of neglecting the thermal boundary resistance [9], and GaN epitaxial layer entirely [42] were also compared with the peak channel temperature rise predicted by the electrothermal coupled numerical model. To evaluate the effects, the baseline CHF model with temperature dependent properties was modified to first eliminate the thermal impedance of the TBR, with the 2 μm thick GaN layer intact. The GaN layer was then set to the properties of 6H-SiC to represent a homogenous crystal. Omitting the TBR, with constant thermal conductivity assumed in Section 5.2, underpredicts the multiphysics temperature rise by -13.9% to -24.1%. With the temperature dependent properties, removing the TBR results in an apparent peak channel rise error of -1.8% to -0.4% for 2 to 4 W mm^{-1} as seen in Figure 10. The slight underestimation is only by coincidence as stated before, given the assumed heated length of the gate CHF model, as this approximation underpredicts the CHF model temperature rise by 8.5%. This simplification should be avoided without first verifying the accuracy of a CHF assumption for the specific set of bias conditions through electrothermal verification or experimental validation. Additionally, entirely neglecting the TBR and GaN epitaxial layer by considering the die to be an 87 μm homogenous 6H-SiC crystal results in an under prediction of multiphysics peak channel temperature rise by -12.8% to -14.3%, and up to -21.3% when compared to the CHF model, for these bias conditions as illustrated in Figure 11.

5.4. ANALYTICAL MODELING

An analytical open-form solution has been proposed [8], but does not capture the heterostructure epitaxy of the GaN HEMT, and only resolves heating on a homogenous substrate. A product of this homogenous limitation is that the GaN epitaxial layer cannot be included, nor can the TBR. This analytical model allows for the prescription of discrete heat loads on a substrate with the practical application of resolving substrate heat spreading and thermal gradients across these heated regions. The alternative, closed-form analytical solution [7] includes the thermal resistance of the epitaxial layer, however this violates the Kirchhoff transformation and does not account for the TBR. Unlike [8] , this closed-form approach is strictly limited to estimating the peak channel temperature of a HEMT with many fingers due to the symmetry boundary conditions assumed during derivation. These methods propose that for the application of GaN HEMT that the self-heating that the head be applied uniformly over the gate width and length, however this may not be physically valid and requires a form of verification at the process node corresponding to the DUT or device under study. While [7] is limited to CHF heating, the method proposed in [8] is amenable to physically valid analytical expressions that could be efficiently used to represent self-heating profiles predicted by electrothermal models.

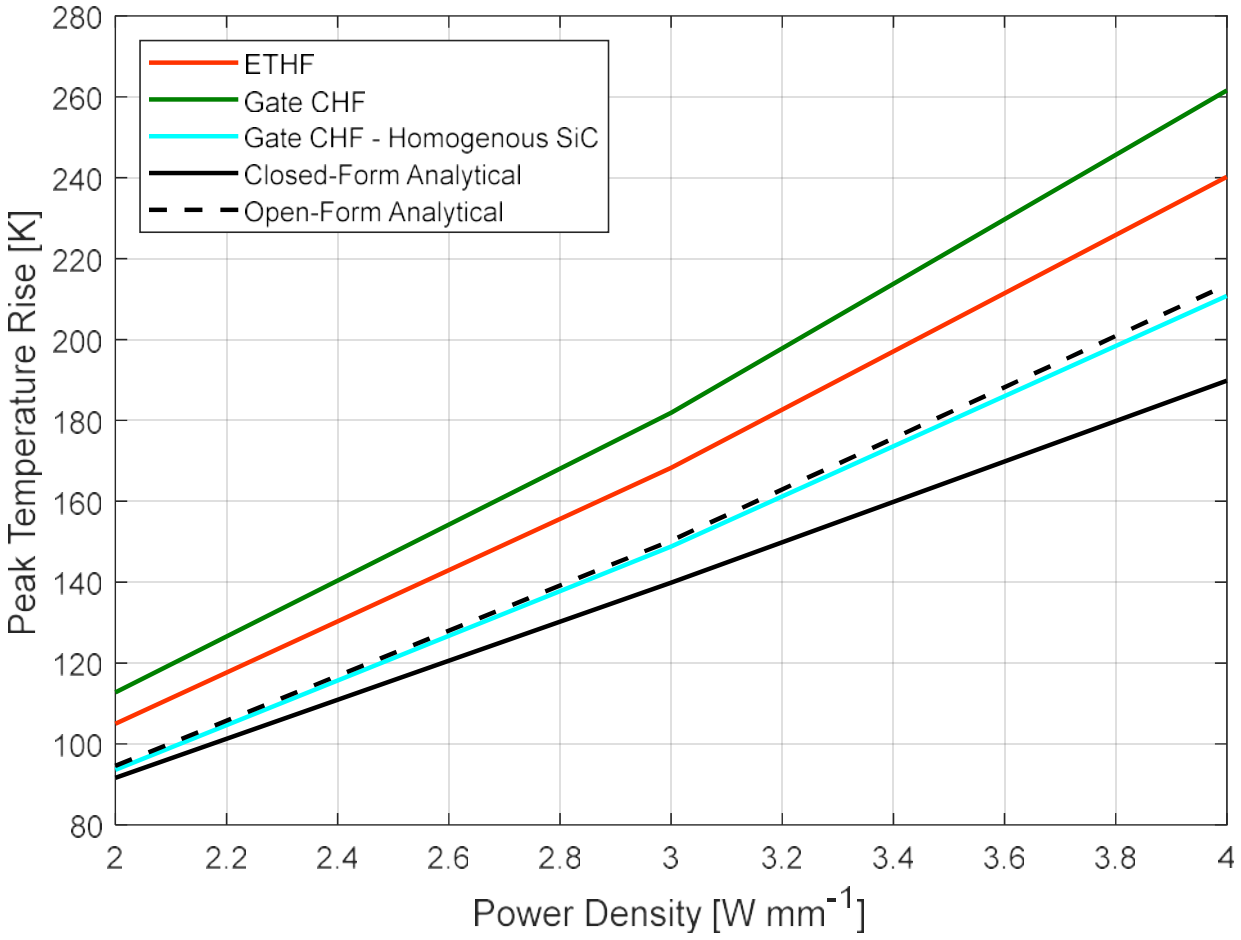

Figure 11 *– Peak temperature rise over power density for the nominal multiphysics, constant heat flux, substrate only, and closed and open form analytical models.*

These analytical models rely upon Dirichlet boundary conditions that represent a constant temperature at the substrate base. In conventional microelectronics packaging, a convective, or Robin boundary condition, may be more appropriate as witnessed by the thermal gradient across the substrate base in Figure 12.

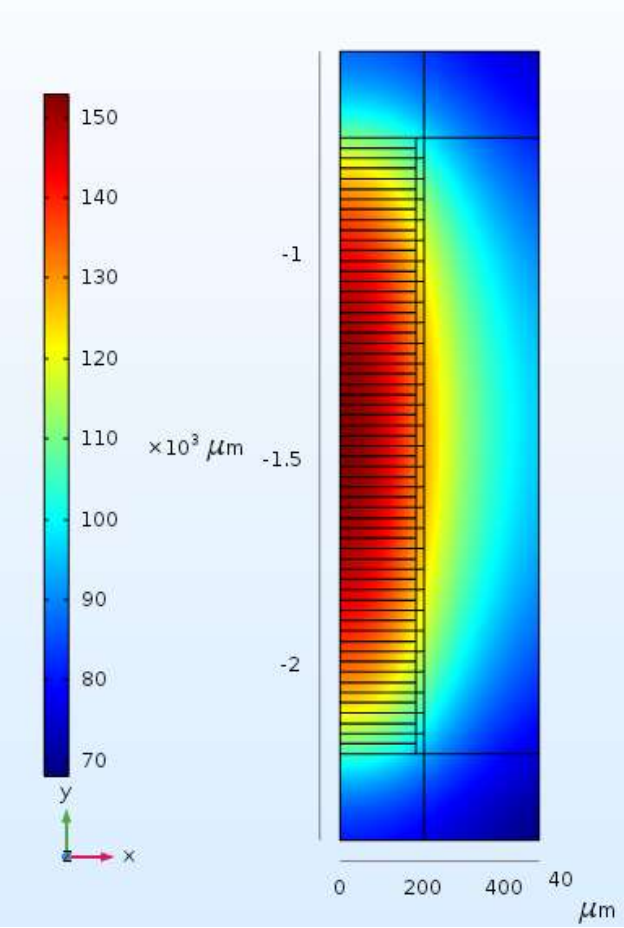

Figure 12 *– Substrate base temperature rise above stage temperature for the 4 W mm^{-1} condition illustrating a packaged die temperature gradient that is inconsistent with analytical modeling boundary conditions.*

To correlate with the results of this study, the maximum base temperature of the die was extracted and set as a constant temperature boundary condition. For the case of the 4 W/mm power density, a 176.8°C isothermal boundary condition was assumed (c.f., Figure 12). The gate length parameter in each model was set to the overhang distance of the T-gate flange as assumed in the baseline CHF numerical model. The material properties defined in Table 3 were applied for the GaN epitaxial layer and SiC substrate in the case of the closed-form model, and only the SiC substrate for the open-form model. Peak channel temperature rises of the electrothermal and gate defined CHF model were compared to the predictions of each analytical method in Figure 11. This CHF model was chosen in addition to the electrothermal model as to more closely match the inherent self-heating assumptions of the analytical solutions. Analysis shows that the open-form solution

slightly under predicts the electrothermal and gate defined CHF channel temperature rise with an error of -11.1% and -18.4% respectively for the 4 W mm^{-1} power density. The closed-form solution further under predicts the peak temperature of the device with an error of -21% and -27.4% respectively when compared to these respective numerical methods. Visual inspection of Figure 11 shows that the open-form analytical model predicts the temperature rise as if the device was a homogenous substrate without epitaxial and thermal boundary layers.

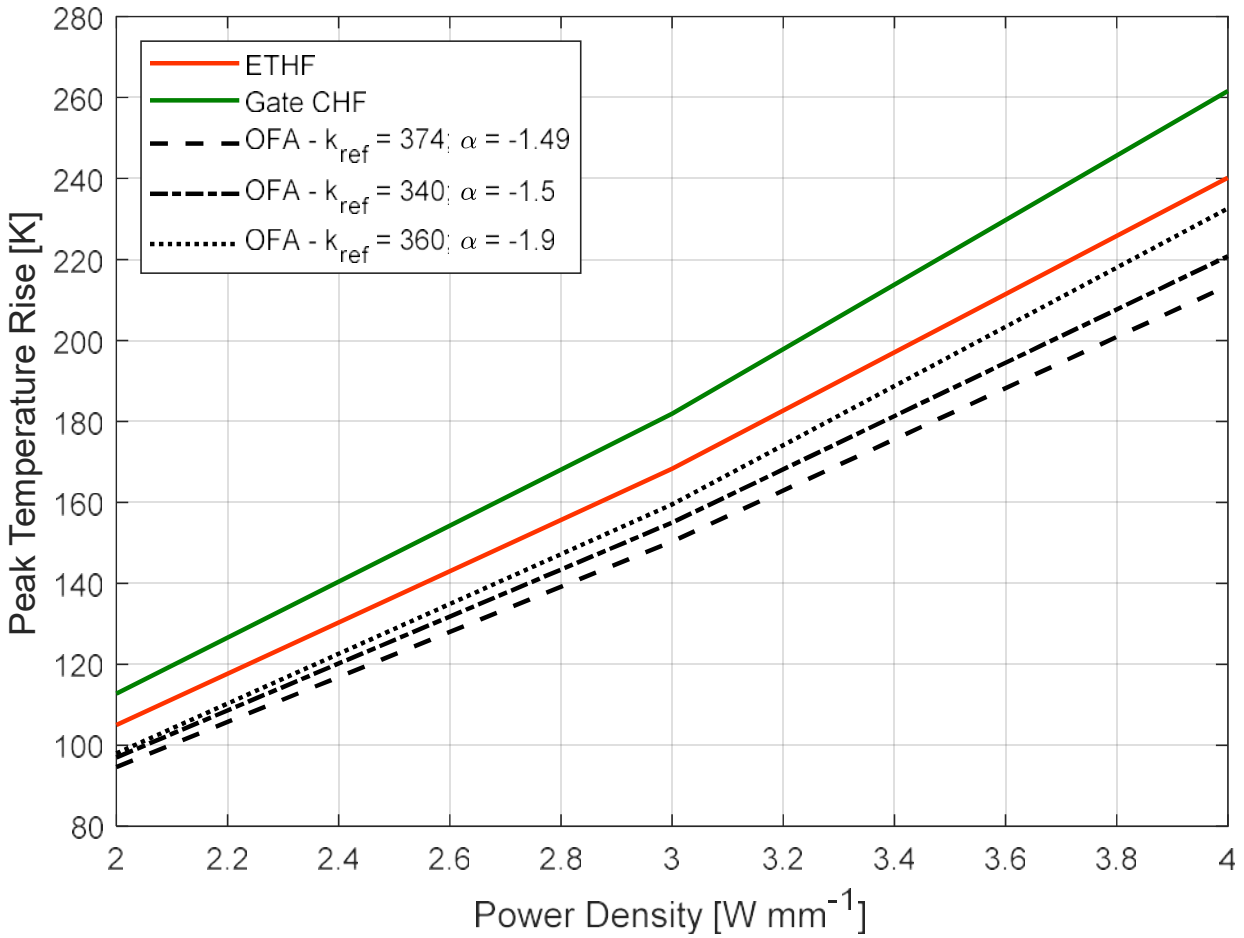

Figure 13 *– Peak temperature rise over power density for the nominal multiphysics, constant heat flux, and open form analytical models with alternate material properties from other publications.*

The considered analytical models tend to underpredict the peak channel temperature rise when applied to a packaged multiple-finger GaN HEMT. The error may be acceptable however for lower power densities or when performing conceptual trade studies on device structures. A mitigating method may be to artificially reduce k_{ref} and increase α of the substrate material as to

lump the composite layer effects. Solving the open-form analytical solution for k_{ref} of 340 W m^{-1} K^{-1} at 300 K with a α of -1.49 [9] [8], and 360 W m^{-1} K^{-1} at T_{ref} of 300 K with α of -1.9 [2] reduces the error to the multiphysics peak temperature rise to -8.4% and -3.2% at 4 W mm^{-1} respectively. Figure 13 compares the temperature rises of the open-form analytical model with the baseline and reduced properties to the nominal electrothermal heat flux and CHF numerical models. Despite physically representing a homogenous substrate, the open-form solution with k_{ref} of 360 W m^{-1} K^{-1} at 300 K with a α of -1.9 may be acceptable for some engineering applications. As before, care should be taken to first verify or validate the CHF assumption for device specific HEMT structure and bias conditions as this property is applied to the entire substrate rather than only near the heat source.

6. CONCLUSIONS

In this thesis, the accuracy of surveyed common thermal analysis assumptions made by academia and industry for use in predicting GaN HEMT channel temperatures was explored. Thermography data from micro-Raman spectroscopy of a DC-based GaN HEMT was compared with a one-way coupled electrothermal simulation and a 3D FEM model to show excellent correlation. For the specific set of bias conditions, a peak channel temperature was extracted from the multiphysics simulation for comparison to various modeling order reductions. These encompassing reduced order modeling approaches were shown to deviate from the apparent peak channel temperature. Comparison of these order reduction for this set of bias conditions suggests the following guidelines:

- Instead of assuming an arbitrary length, a reduced order heat flux distribution should instead be determined by electrical modeling insights dependent upon the transistor structure and bias conditions. A calibrated CHF over an area, set of heat flux over multiple areas, or mathematical expression may then be applied to approximate the self-heating profile for accurate channel temperature predictions to reduce the simulation cost. In this study, the gate length and width defined CHF model was shown to overpredict the peak multiphysics temperature rise above stage temperature by 8.9%
- Representative material properties for each composite layer of the device should be considered. This includes considering for the defect density, impurity concentration, and size effects. The values assumed in this publication matched well with experimental data, however verification is recommended depending on the device. When comparing the models with identical CHF assumptions, peak channel temperature rise underprediction can result from assuming unrepresentative GaN

epitaxial layer properties of up to -12.2%. The temperature dependence of the thermal conductivity should be included as to avoid underpredicting the channel temperature by up to -24% or greater if the TBR is also excluded.

- Neglecting the TBR with temperature dependent properties reduces the peak channel temperature by -8.5% while omitting the GaN layer entirely results in a -21.3% underprediction. This should be avoided as adding a TBR between the epitaxial layer and substrate does not increase computational cost. It may be possible to lump the composite layer effects into a modified material parameter set for the SiC substrate, however extreme care should be taken to establish the range of validity of this assumption against device geometry and bias conditions.
- Analytical models were shown to underpredict the peak channel temperature of a packaged device using physically representative material properties due to discretization limitations. This error can be also reduced through model calibration of either the material parameters or the self-heating assumptions.

To convey the impact of this study, consider a device thermal management study where the objective is to meet reliability and output power requirements. A 4 W mm^{-1} power density is applied as a CHF over the gate length and width. If the device bias conditions matched this study, then the peak temperature of the device would be overpredicted by 21.4°C if the baseline CHF model assumptions were employed. Device power output would be estimated to be 0.21 dB lower than the DUT with two orders of magnitude less reliability. These results may determine that the device or thermal management system is unsuitable for the application. Conversely if the die was assumed to be a homogenous SiC crystal then the study would underpredict the peak

temperature by -34.4°C. In this overly optimistic case, the DUT would experience 0.34 dB lower output power and up to 3 orders of magnitude lower reliability than expected.

The analysis presented in this thesis pertains to a GaN HEMT with gate length of 0.8 μm under specific DC-bias conditions. Commercially available gate lengths available at the time of this publication have reached 0.15 μm [55] [56]. It is recommended that this analysis approach is performed at these process nodes for additional validation. This investigation could be expanded to include the effects of bias conditions, shown to impact self-heating [14], that were not investigated outside of the typical DC-bias recommended by the manufacturer of this RF device.

NOMENCLATURE

α	Exponential temperature dependence coefficient
Δ	Change in quantity
ΔT_{cb}	Channel temperature rise above isothermal die base condition
I_{gs}	Saturated drain current
k	Thermal conductivity
k_{ref}	Thermal conductivity at reference T_{ref}
n	Surface normal
q''	Heat flux
R''	Thermal impedance
T	Temperature
T_{meas}	Temperature measurement
T_{mod}	Modeled temperature
T_{ref}	Reference temperature
T_{stage}	Stage temperature
V_{ds}	Saturated drain voltage
V_{gs}	Saturated gate voltage
X,Y,Z	Cartesian vectors

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APPENDIX

NUMERICAL MODEL TEMPERATURE RISE PREDICTIONS

Maximum temperature rise (T-Ts) at Gate #22

Model/ W/mm	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	49.63	52.51	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	105.03	112.75	111.65	108.92	99.39	97.63	105.19	110.61	108.71	103.19	91.56	98.67	90.45	91.59	94.60	97.00	98.00
3	168.30	181.89	179.93	174.85	157.49	154.33	164.81	178.11	175.24	166.40	145.43	148.51	136.17	139.90	150.30	155.00	159.50
4	240.21	261.56	258.62	250.26	222.25	217.24	229.70	255.64	251.86	239.29	205.79	198.73	182.28	189.80	213.50	220.00	232.60

Percent error between max temperature rise (T-Ts) predicted by the ETHF model at Gate #22

Model/ W/mm	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
1	0.0%	5.8%	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
2	0.0%	7.4%	6.3%	3.7%	-5.4%	-7.1%	0.2%	5.3%	3.5%	-1.8%	-12.8%	-6.1%	-13.9%	-12.8%	-9.9%	-7.6%	-6.7%
3	0.0%	8.1%	6.9%	3.9%	-6.4%	-8.3%	-2.1%	5.8%	4.1%	-1.1%	-13.6%	-11.8%	-19.1%	-16.9%	-10.7%	-7.9%	-5.2%
4	0.0%	8.9%	7.7%	4.2%	-7.5%	-9.6%	-4.4%	6.4%	4.8%	-0.4%	-14.3%	-17.3%	-24.1%	-21.0%	-11.1%	-8.4%	-3.2%
Avg.	0.0%	7.5%	7.0%	3.9%	-6.4%	-8.3%	-2.1%	5.9%	4.2%	-1.1%	-13.6%	-11.7%	-19.0%	-16.9%	-10.6%	-8.0%	-5.0%

Relative change between max temperature rise (T-Ts) predicted by the gate CHF model at Gate #22

Model/ W/mm	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
2	-6.8%	0.0%	-1.0%	-3.4%	-11.8%	-13.4%	-6.7%	-1.9%	-3.6%	-8.5%	-18.8%	-12.5%	-19.8%	-18.8%	-16.1%	-14.0%	-13.1%
3	-7.5%	0.0%	-1.1%	-3.9%	-13.4%	-15.2%	-9.4%	-2.1%	-3.7%	-8.5%	-20.0%	-18.4%	-25.1%	-23.1%	-17.4%	-14.8%	-12.3%
4	-8.2%	0.0%	-1.1%	-4.3%	-15.0%	-16.9%	-12.2%	-2.3%	-3.7%	-8.5%	-21.3%	-24.0%	-30.3%	-27.4%	-18.4%	-15.9%	-11.1%
Avg.	-7.5%	0.0%	-1.1%	-3.9%	-13.4%	-15.2%	-9.4%	-2.1%	-3.6%	-8.5%	-20.1%	-18.3%	-25.1%	-23.1%	-17.3%	-14.9%	-12.2%

- **Method 1:** Electrothermal heat flux (ETHF)
- **Method 2:** CHF over gate projected area (~Lg x Wg)
- **Method 3:** CHF over 1.0 µm length x Wg
- **Method 4:** CHF over 1.5 µm length x Wg
- **Method 5:** CHF from gate to drain (G-D x Wg)
- **Method 6:** CHF from source to drain (S-D x Wg)
- **Method 7:** Method 2 with bulk GaN properties from Zou *et al.* used in early publications more relevant for HVPE of bulk GaN.
- **Method 8:** Method 2 with 6H-SiC properties from a recent Killat *et al.* Raman thermography experiment.
- **Method 9:** Method 8 with a 50% reduction in TBR.
- **Method 10:** Method 2 with 0% reduction in TBR.
- **Method 11:** Method 2 with homogenous 6H-SiC substrate.
- **Method 12:** Method 2 with constant properties.
- **Method 13:** Method 12 without a TBR.
- **Method 14:** Darwish closed-form analytical (CFA)
- **Method 15:** Ditri open-form analytical (OFA)
- **Method 16:** Method 15 with properties from Freeman *et al.*
- **Method 17:** Method 15 with properties from Ditri *et al.*