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H8 Inverter for Common-Mode Voltage reduction in Electric Drives

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***Abstract*—This paper presents a modified two-level three-phase inverter for the reduction of the leakage current. With respect to a traditional two-level inverter, the proposed solution reduces the common-mode voltage, both in amplitude and frequency. Between the DC source and the traditional three-phase bridge, two active DC-decoupling devices and a voltage-clamping network have been added. A dedicated control strategy was developed adopting a modified Space Vector PWM modulation, oriented to the reduction of the common-mode voltage. Simulations showing the good performance of the solution are presented. A preliminary prototype was developed and experimental results are presented.**

***Index Terms*—Three-phase, inverter, drive, H8, PWM, space vector, common-mode voltage, leakage current.**

I. Introduction

Despite the fact that the two-level three-phase inverters are widely used in electronics, it is well known that they exhibit poor common-mode voltage (CMV) characteristics. The existence of several common mode impedance paths between the converter and the motor/drive frame allows leakage currents to flow at every CMV variation, so that high pulse-width modulation frequencies produce high common-mode leakage currents [1]. In motor drive applications, this may lead to motor bearing failures, EMI noise that causes inverter drive trip, or interference with other electronic equipment in the vicinity [2].

The leakage current problem can be faced by reducing as much as possible the CMV, both in amplitude and frequency; ultimately, a constant CMV would not produce such leakage currents. Passive solutions, adopting passive filters at the inverter output or input, end up with increased system cost and size [3]. Depending on the application field, one aspect or the other may represent a more significant drawback. For example, size and weight are particularly relevant in aircraft applications [4], while cost still is significant in more traditional, industrial-based applications. Furthermore, since these currents flow through the system enclosure, they are even more relevant in case of carbon fiber structure used in modern aircraft applications.

This paper proposes a modified two-level inverter to solve the problem. It is an upgraded version of [5], where the same solution was originally presented. Section II presents a brief state of the art review of converter architectures and modulation strategies with reduced CMV. In section III a novel solution is proposed, which takes advantage both from a new topology and from a dedicated control strategy to reduce the CMV.

II. State of the art

In the past, several authors dealt with the CMV problem adopting specific control strategies. In [6] and [7] several PWM strategies are investigated, but they suffer from drawbacks like not allowing to completely eliminate the CMV, leading to high current ripple or distortion or even being not practically feasible. In [8] a combined algorithm with satisfactory CMV reduction performance is proposed, but it still exhibits CMV over the PWM period, although reduced in amplitude and frequency compared to a traditional PWM modulation. For systems including a rectifier and an inverter, the CMV excursion can be reduced taking into account the supply AC voltage waveform for the definition of the SV pattern [9]. In presence of a fully controllable back-to-back rectifier/inverter configuration, synchronizing the rectifier and inverter PWM sequence allows to reduce the number of CMV pulses within a PWM period [10].

In addition to the traditional three-phase bridge (H6), different architectures have been proposed during the past years. Here a list of the most relevant ones is presented.

- The Neutral Point Clamped (NPC) inverter, shown in Fig. 1, was proposed for the first time in [11]; since then, several publications have focused on this topology, which offers benefits such as reduced switching losses, small output current ripple, and split supply voltage. Its main drawback consist in the complexity: more devices and more driver circuitry are necessary compared to other architectures and the control turns out to be more complex as well.
- Another approach to the CMV-related problems consist in a four-legs inverter like that one in Fig. 2, where a fourth leg is added to the H6 for controlling the CMV. Adopting a specific modulation, it can reduce the average output voltage and the differential mode distortion [12].

Other than in motor drive applications, CMV and common mode current are relevant in PV generation adopting transformerless conversion. As a matter of fact, there is a common mode path which includes the panels, the inverter, the grid, the ground and the stray capacitance between the panels and their supporting structure. In this context several modulation techniques have been studied [18] and alternative topologies proposed with the same aim of reducing the CMV and the leakage current.

- The topology proposed in [13] and represented in Fig. 3 reduces the CMV and the leakage current, but it has a great number of components (diodes and switches) which

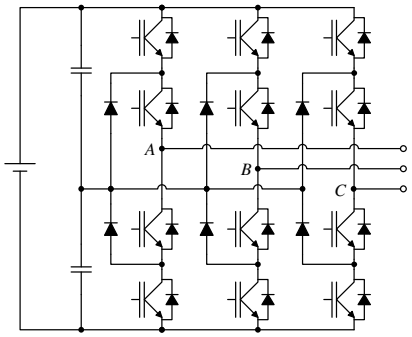


Figure 1. The Neutral Point Clamped inverter [11].

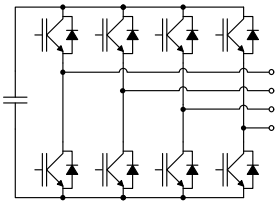


Figure 2. The four-legs inverter [12].

introduce additional switching and conduction losses, as a consequence the efficiency is lower than in the conventional three-phase inverter.

- In [14], the authors propose a solution where seven switches are present (shown in Fig. 4), allowing to break the leakage current conduction path during the freewheeling period. It utilizes RCMV-PWM for reducing the CMV through the elimination of the zero voltage states. However, it only focuses on leakage current elimination compromising issues such as voltage linearity, output current ripple, dc-link current ripple and harmonic distortion.
- The impedance-source converter, depicted in Fig. 5, adds to the H6 structure an impedance network on the source side, resulting in a buck-boost inverter. It can be applied

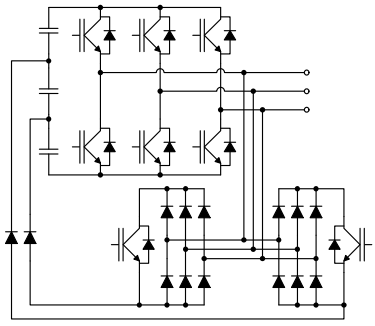


Figure 3. The Two-level Three-phase PV inverter topology [13].

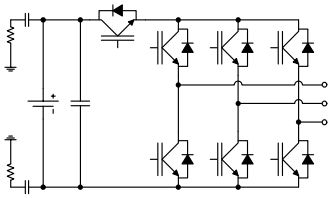


Figure 4. The H7 architecture [14].

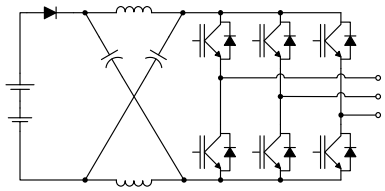


Figure 5. The Z-source inverter [15].

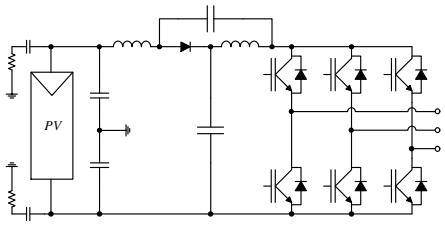


Figure 6. The Quasi-Z-source architecture [16].

to every power conversions and to adjustable speed drive, especially in applications where the input voltage changes widely. It exhibits good efficiency, can minimize stresses and size of the motor and performs a higher output power than a conventional PWM inverter. However, it is suitable for boost ratio range up to 2, while for higher ratios the DC/DC boosted PWM inverter is the best configuration. Furthermore, the presence of a right-hand-plane zero limits the dynamic response and it cannot be eliminated by adjusting the Z-source parameters [15], [19].

- The Quasi-Z-source inverter, depicted in Fig. 6, represent a modified topology with respect to the impedence-source inverter, with all the advantages of the ZSI and additional benefits such as a constant input current and less stress on components, moreover it is suitable for SVPWM modulations for minimizing the CMV [16].
- A topology called DCM-232 is depicted in Fig. 7. It makes use of ten switches, six for the H6 and four (unidirectional, with reverse blocking capability) for a DC multiplexer with two DC sources (PV panels). Both of them are disconnected from the DC bus when the zero vectors are generated, so that the stray capacitance of the panels remains at a constant value and no leakage current arises. The solution performs well in terms CMV and leakage current reduction, however it needs separate DC sources and it increases the complexity both of the hardware and of the control because of the presence of ten switches [17].

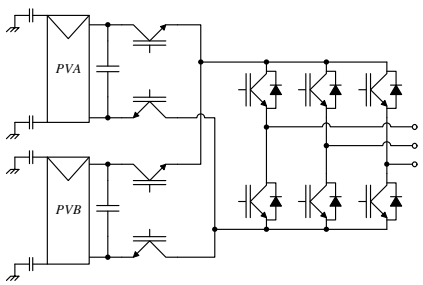


Figure 7. The DCM-232 inverter [17].

III. Proposed inverter architecture and modulation

The proposed inverter architecture (shown in Fig. 8) differs from a traditional H6 for the addition of two active devices at the DC source side, a capacitor divider and two clamping diodes. Deriving from a H6 and having a total of eight active devices, the proposed inverter architecture has been named *"H8"*. The two additional active devices, referred to as $T7$ and $T8$, are placed between the DC source and the three legs block, and they act as DC-decoupling devices during the current freewheeling phases. A capacitive divider is placed on the DC side of the inverter, allowing to obtain voltages equal to $\frac{1}{3}V_{DC}$ and $\frac{2}{3}V_{DC}$, i.e. the CMV values respectively during the active odd and even states. In order to ensure an equal partition of the voltage across the capacitors, an high impedance (to reduce the power losses) resistive divider was added in parallel. Two diodes, named D_H and D_L, are placed between the two intermediate points of the divider and the H6 bridge in order to clamp the voltage at the high side or at the low side of the bridge itself, during the upper or bottom current freewheeling phases, depending on the case.

The CMV is defined as the average of the voltages between the inverter outputs and the negative DC source (addressed as N):

$$V_{CM} = \frac{V_{uN} + V_{vN} + V_{wN}}{3} \tag{1}$$

Table I summarizes the common mode voltage values at the inverter output, both for a traditional three-phase inverter and for the proposed H8 topology. In the case of a traditional H6, the CMV varies from 0 to V_{DC}, with a $\frac{1}{3}V_{DC}$ step at every state commutation. The H8 topology only presents two values for the CMV: $\frac{1}{3}V_{DC}$ for all the odd states and $\frac{2}{3}V_{DC}$ for all the even ones. In fact, differently from the H6, the proposed solution exhibits the same CMV values both during the active state and the inactive ones. This is possible for the presence of the DC-decoupling devices (T_7 and T_8) and of the voltage-clamping diodes (D_H and D_L). Before the high side current freewheeling phase (state 8, or vector V_8), when all the three high side devices in the bridge are on, the upper DC-decoupling device (T_7) is switched off and this causes the diode D_H to turn on clamping the voltage on the upper rail of the bridge to $\frac{2}{3}V_{DC}$. Similarly, before the low side current freewheeling phase (state 7, or vector V_7), when all the three low side devices in the bridge are on, the bottom DC-decoupling device (T_8) is switched off and this causes the diode D_L to turn on and therefore the voltage on the bottom part of the bridge to be $\frac{1}{3}V_{DC}$. Then, for both cases, for the remaining duration of the inactive states the voltage on the interested side of the bridge maintains those values. Figure 9 shows the eight configurations of the inverter for the eight SV states.

Table I
Common-mode voltage (V_{CM}) values

	Vectors	Bridge states	$\frac{V_u}{V_{DC}}$	$\frac{V_v}{V_{DC}}$	$\frac{V_w}{V_{DC}}$	V_{CM}/V_{DC} H6	V_{CM}/V_{DC} H8 inverter
	V_1	100	1	0	0	1/3	1/3
	V_2	110	1	1	0	2/3	2/3
	V_3	010	0	1	0	1/3	1/3
	V_4	011	0	1	1	2/3	2/3
	V_5	001	0	0	1	1/3	1/3
	V_6	101	1	0	1	2/3	2/3
H6	V_7	000	0	0	0	0	
	V_8	111	1	1	1	1	
H8	V_7	000	1/3	1/3	1/3		1/3
	V_8	111	2/3	2/3	2/3		2/3

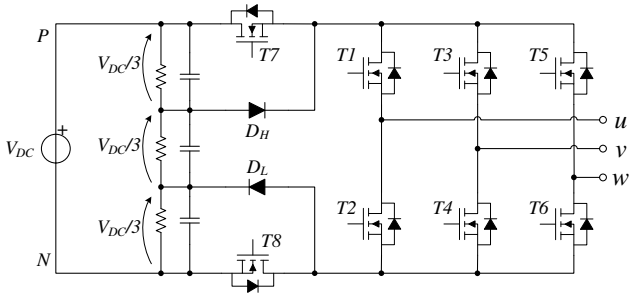


Figure 8. The proposed H8 inverter topology.

Since the two clamping diodes ensure the voltage across T_7 and T_8 to be only one third of the total DC bus, devices with a reduced breakdown voltage can be adopted, reducing than the additional losses those devices introduce.

In order to force D_H or D_L to turn on when the inverter enters into the zero states, the decoupling devices turn off is anticipated with respect to the commutation of the bridge devices. For example, in the transition from state 1 to state 7, first T_8 is switched off, leading to D_L to turn on (Fig. 10(a)); then T_1 is switched off and after a dead time T_2 is switched on, completing the state commutation. Fig. 10 shows the configurations of the inverter which are put in place at every transitions from one active states to the following inactive one. As a matter of fact, during these temporary phases V_{CM} assumes one of the following two values:

$$V'_{CM} = \frac{1}{3}\left(1 + \frac{1}{3} + \frac{1}{3}\right)V_{DC} = \frac{5}{9}V_{DC} = 0.55V_{DC} \tag{2}$$

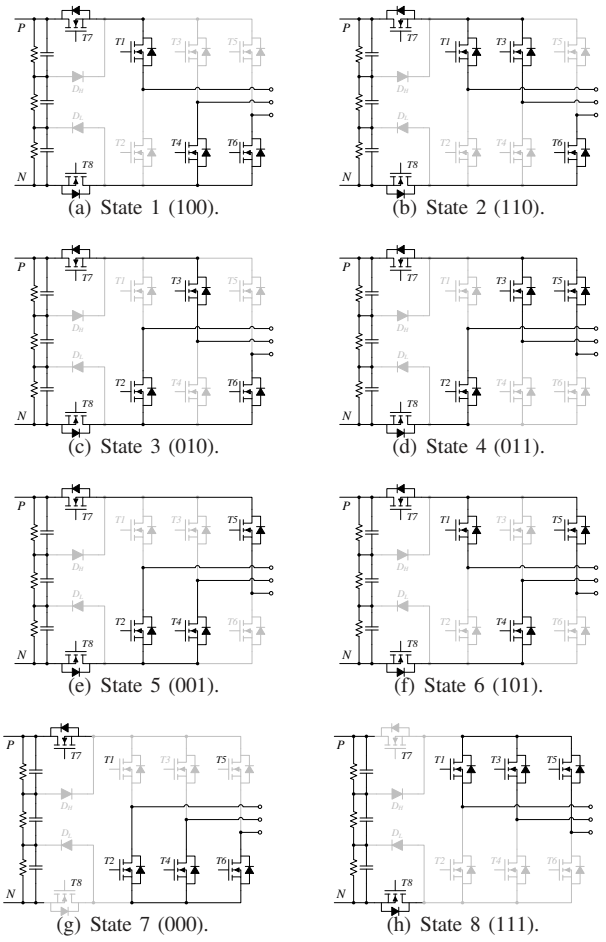
$$V''_{CM} = \frac{1}{3}\left(0 + \frac{2}{3} + \frac{2}{3}\right)V_{DC} = \frac{4}{9}V_{DC} = 0.44V_{DC} \tag{3}$$

In particular, $V_{CM} = V'_{CM}$ in the cases involving odd vectors, depicted in Fig. 10(a), 10(c) and 10(e), whereas $V_{CM} = V''_{CM}$ in the cases involving even vectors, showed in Fig. 10(b), 10(d) and 10(f). This implies that CMV is not constant throughout a PWM period, but it varies from $\frac{1}{3}V_{DC}$ to $\frac{5}{9}V_{DC}$ (odd cases) and from $\frac{2}{3}V_{DC}$ to $\frac{4}{9}V_{DC}$ (even cases) at every transition from an active to an inactive vector. Nevertheless, these variations are smaller than those typical of traditional solutions. In particular, for the two cases they result to be:

$$\Delta V'_{CM} = \frac{5}{9}V_{DC} - \frac{1}{3}V_{DC} = +\frac{2}{9}V_{DC} = +0.22V_{DC} \tag{4}$$

$$\Delta V''_{CM} = \frac{4}{9}V_{DC} - \frac{2}{3}V_{DC} = -\frac{2}{9}V_{DC} = -0.22V_{DC} \tag{5}$$

It is worth to be noted that D_H or D_L turn on only for few nanoseconds, charging or discharging the stray capacitance of

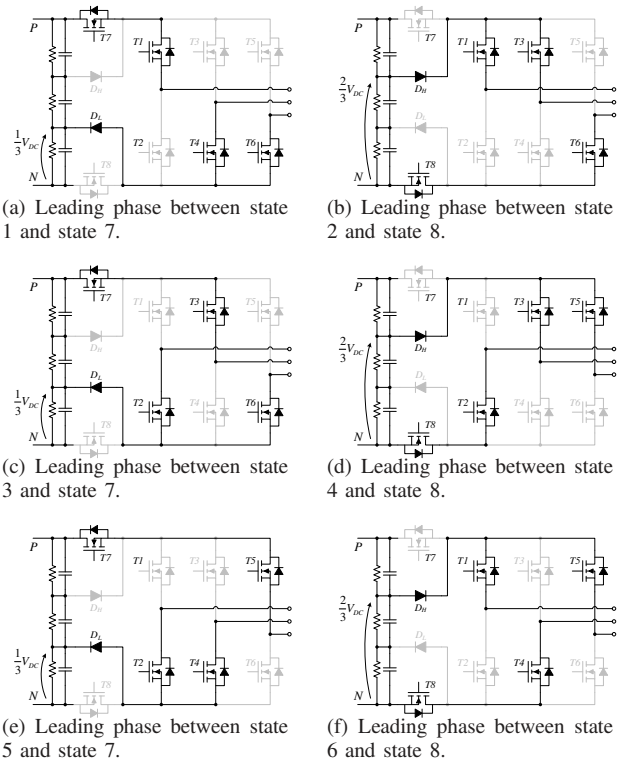


(a) State 1 (100). (b) State 2 (110). (c) State 3 (010). (d) State 4 (011). (e) State 5 (001). (f) State 6 (101). (g) State 7 (000). (h) State 8 (111).

Figure 9. Configurations of the H8 inverter for the eight Space Vector states. Devices are depicted in black if they are on, in gray if they are off. Current conduction through anti-parallel diodes are neglected for simplicity.

the devices, therefore not causing a significant unbalance in the voltage divider. However, they are passive devices, so they need a current flowing from the DC side to the AC side in order to turn on. In case of zero current, this does not occur, hence the CMV deteriorates.

The modulation adopted for the control of the inverter is a novel Space Vector (SV) strategy, specifically developed in conjunction with the H8 architecture, with the aim to achieve an almost constant CMV (as previously discussed, $\pm\frac{2}{9}V_{DC}$ variations are unavoidable) and performing single leg commutations. In the following, this strategy will be addressed as Constant Common-Mode Voltage Space Vector (CCMV-SV), however it can only be applied for modulation indexes lower than 0.5 (Fig. 13(b) and 13(c)). In order to overcome to the linearity range limitation, the system can switch to a different control strategy when a higher modulation index is needed. In such a case, a Near State Space Vector (NS-SV) is adopted, since this extends the modulation index range up to $\sqrt{3}/2$ (see Fig. 13(d)). Compared to CCMV-SV, NS-SV performs worse in terms of CMV, but in conjunction with the proposed topology it ensures advantages over conventional three-phase inverters. The following two subsections discuss in further detail the two developed modulation strategies.



(a) Leading phase between state 1 and state 7. (b) Leading phase between state 2 and state 8. (c) Leading phase between state 3 and state 7. (d) Leading phase between state 4 and state 8. (e) Leading phase between state 5 and state 7. (f) Leading phase between state 6 and state 8.

Figure 10. Configurations of the H8 inverter during transitions from active to inactive states. Devices are depicted in black if they are on, in gray if they are off. Current conduction through anti-parallel diodes are neglected for simplicity.

A. Modulation index smaller than 0.5: CCMV-SV modulation

In order to maintain a constant CMV at the inverter output, this SV strategy only makes use of those vectors exhibiting the same V_{CM}. Table I shows the ratios between V_{CM} and V_{DC} for all the eight SV states. As a matter of fact, odd active vectors (V_1, V_3 and V_5) exhibit $V_{CM} = \frac{1}{3}V_{DC}$, while even active vectors (V_2, V_4 and V_6) have $V_{CM} = \frac{2}{3}V_{DC}$. This is also true considering the H6 and, indeed, several modulations were proposed in literature attempting to keep common-mode voltage constant by using only a set of vectors that exhibit the same V_{CM} [6]. Nevertheless, those modulations do not make use of inactive vectors (V_7, V_8), and this results in simultaneous commutations of more than one bridge leg. On the contrary, adopting the H8 architecture, V_{CM} values of the inactive vectors, thanks to the DC decoupling, can match them of the active states. In this context, it is possible to obtain the same CMV values with all the odd vectors (V_1, V_3, V_5 and V_7), or with all the even ones (V_2, V_4, V_6 and V_8). As already mentioned in Sec. III, at every transition from an active state to an inactive one, CMV becomes equal to $\frac{4}{9}V_{DC}$ or to $\frac{5}{9}V_{DC}$ (see Eq. 2 and 3), leading to a $\pm\frac{2}{9}V_{DC}$ variation of CMV.

The reference vector in the $\alpha - \beta$ plane is synthesized by the use of the two nearest odd or even vectors with the proper modulated duration, plus the proper inactive state fulfilling the remaining time in the PWM period. Applying this scheme, the points which can be synthesized are included in two equilateral triangles having vertexes on the applied active vectors (see Fig. 13(b) and 13(c)). The maximum modulation index which

Table II
VECTORS USAGE IN CCMV-SV MODULATION STRATEGY

Angles	Odd vectors	Even vectors
$0° - 60°$	V_1, V_3, V_7	V_2, V_6, V_8
$60° - 120°$		V_2, V_4, V_8
$120° - 180°$	V_3, V_5, V_7	
$180° - 240°$		V_4, V_6, V_8
$240° - 300°$	V_5, V_1, V_7	
$300° - 360°$		V_2, V_6, V_8

is possible to maintain throughout the entire rotational period is 0.5. This is a rather limiting feature for an electric drive, therefore a different modulation strategy has been adopted for modulation indexes greater than 0.5 (NS-SV), which is exposed in subsection III-B.

In order to perform a single leg commutation for each state transition, the $\alpha - \beta$ plane has been divided into different zones, each one featuring different state sequences. Considering the odd vectors case, shown in Fig. 13(b), there are six 60°-wide zones (nr. 1, 3, 4, 6, 7 and 9), plus 3 zones without a specific angular width, represented as very narrow slices (nr. 2, 5 and 8). Such narrow zones are intended to represent SV sequences just applied for a single PWM period, because they are necessary for matching the state sequences performed in their two adjacent zones. A similar subdivision exists for the dual case adopting even vectors, as shown in Fig. 13(c). Table II summarizes the vectors usage for all the zones throughout the entire rotation period, for odd and even CCMV-SV strategy. In order to achieve symmetry during the switching period, in the 60°-wide zones one of the two active states is split into two separated slots of time at the margin of the sequences. The pulse pattern during a switching period is shown in Fig. 11 for all the zones in the $\alpha - \beta$ plane, both in case of even and odd vectors. In case of no 60°-wide zones (2, 5, 8, 11, 14 and 17) the symmetry is not maintained because, for their native purpose, in those cases sequences must begin and finish with different active states. Moreover, the location of these zones in the $\alpha-\beta$ plane implies that the two modulation values for the active states will be approximately equal. Featuring only three states instead of five (see the central portions of Fig. 11), these intermediate slots must last half the time than the others, otherwise the output would produce a bigger current ripple.

B. Modulation index greater than 0.5: NS-SV modulation

Whenever the control loop requires for the inverter a modulation index higher than 0.5, the control function automatically changes the NS-SV, allowing the inverter to work up to a modulation index equal to $\sqrt{3}/2$. This strategy makes use of the two adjacent active vectors on the $\alpha - \beta$ plane (hence the name Near State modulation), and both the two inactive vectors. States sequences have been designed in order to ensure single leg commutations throughout all the 360°; the resulting pulse pattern is shown in Fig. 12. During each PWM period the time dedicated to inactive vectors is equally distributed between both V_7 and V_8; sequences exhibit a central symmetry

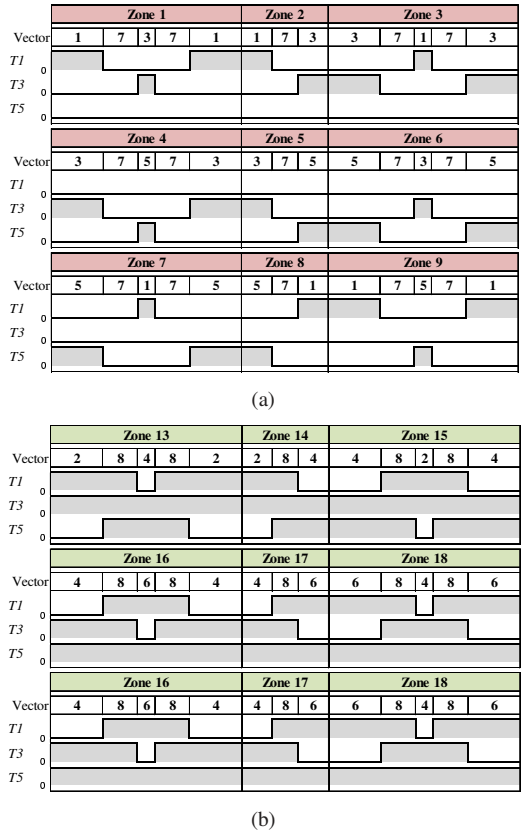


Figure 11. Vectors usage and switch pulse pattern throughout the rotational period for odd vectors CCMV-SV (a) and even vectors CCMV-SV (b). For each zone only one PWM period is represented. Widths of the time slots are chosen as case of example.

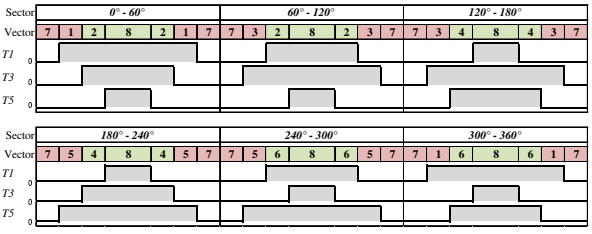
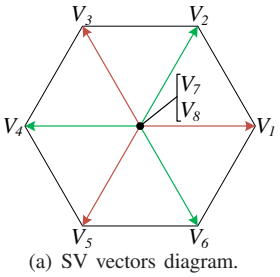


Figure 12. Vectors usage and switch pulse pattern throughout the rotational period for the NS-SV modulation strategy. For each angular sector only one PWM period is represented. Odd vectors are highlighted in red, even vectors in green. Widths of the time slots are chosen as case of example.

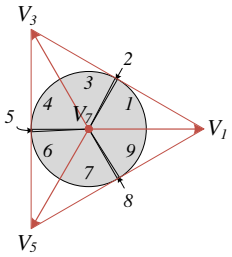
and active states are put in place according to the minimum difference (in terms of switching configuration) they have with respect to the previous or subsequent inactive state. Similarly to the CCMV-SV, V_{CM} becomes equal to $\frac{1}{3}V_{DC}$ when odd vectors are performed and $\frac{2}{3}V_{DC}$ when even vectors are. In each PWM period both odd and even vectors are exploited, so NS-SV exhibits a CMV varying between those two values at the PWM carrier frequency. Hence, compared to CCMV-SV more common-mode voltage is present.

IV. SIMULATION RESULTS

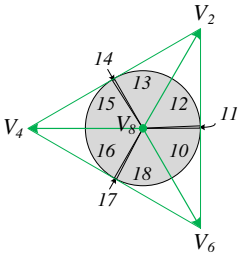
A Matlab/Simulink model of the inverter has been designed, allowing to develop and test the system features. As the purpose of this work is to present the novel inverter architecture along with the proposed modulation strategies, it was



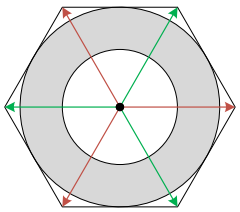
(a) SV vectors diagram.



(b) Linearity region ($m < 0.5$) and modulation zones numbering for odd vectors CCMV-SV.



(c) Linearity region ($m < 0.5$) and modulation zones numbering for even vectors CCMV-SV.



(d) The region where NS-SV is used ($0.5 \leq m < \sqrt{3}/2$).

Figure 13. Space Vector diagrams in the $\alpha - \beta$ plane. Odd vectors are red colored, even vectors are green colored.

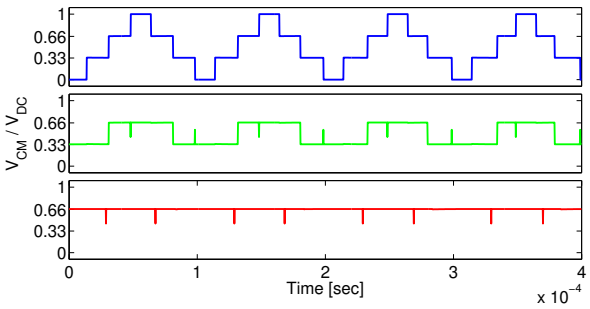


Figure 14. CMV evolution over four PWM periods in case of the inverter performing H6 with NS-SV (upper), H8 with NS-SV (central) and H8 with even-CCMV-SV (bottom).

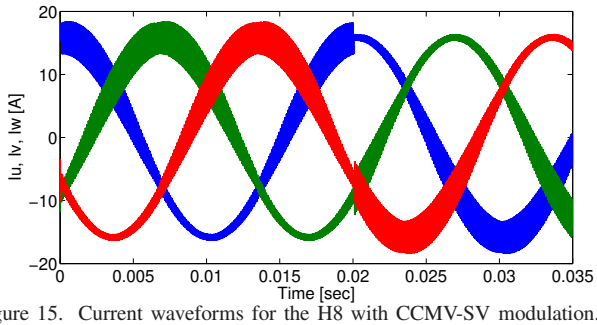


Figure 15. Current waveforms for the H8 with CCMV-SV modulation.

introduced a RL load in wye connection, with floating neutral point. The main parameters used for the simulations are given in Tab. III.

In Fig. 14, V_{CM} is shown for three cases of comparison: H6 with NS-SV, H8 with NS-SV and H8 with CCMV-SV. The H6 exhibits a V_{CM} varying from 0 to V_{DC} at the PWM frequency, the H8 inverter with NS-SV halves the number of V_{CM} transitions and limits its excursion to $\frac{1}{3}V_{DC} - \frac{2}{3}V_{DC}$, whereas the H8 inverter with CCMV-SV performs an almost constant V_{CM}. For the last two cases, adopting H8 architecture, CMV exhibits spikes at $\frac{4}{9}V_{DC}$ or $\frac{5}{9}V_{DC}$, depending on the odd or even vectors usage. These spikes occur in the transitions from active to inactive states, as discussed in Sec. III. For this comparison, a modulation index $m = 0.5$ was adopted for all the cases.

In Fig. 15 the output currents for the H8 architecture with CCMV-SV modulation and a modulation index $m = 0.4$ are depicted. It is worth to be noted that before $0.02s$ the modulation makes use of odd vectors, causing the current ripple to be greater in the upper part of the sinusoid, whereas after $0.02s$ the modulation changes to the usage of even vectors, causing an opposite behavior of the ripple.

Table III
SIMULATION PARAMETERS

Parameter	Value
V_{DC}	$600V$
f_{SW}	$10kHz$
f_e	$50Hz$
Wye load	$3 \times (10\Omega + 2mH)$

The spectrum of the output voltage was also investigated and the harmonic content of the common and differential voltages are depicted in Fig. 16 and Fig. 17, where the amplitudes of harmonics are normalized respectively to V_{DC} and to the amplitude of the fundamental. It is possible to see how the harmonic content of the CMV is reduced for CCMV-SV over NS-SV modulation of about four decades, while the spectrum of the differential voltage is substantially the same for all the three examined cases. For this comparison, all simulations were conducted with $m = 0.4$ and for a simulation time $t = 0.5s$, hence lasting 25 fundamental cycles.

A drawback of the proposed modulation consists in the increased distortion of the output voltage. This was investigated evaluating the weighted total harmonic distortion (WTHD), which is expressed as [20]:

$$WTHD = \frac{\sqrt{\sum_{n=2}^{\infty}\left(\frac{V_n}{n}\right)^2}}{V_1} \tag{6}$$

Figure 18 reports the WTHD for the two proposed modulations against the modulation index. As expected, CCMV-SV

Table IV
COMPARISON OF H8 WITH DIFFERENT MODULATIONS AND H6

Topology	H6	H8	H8
Modulation	NS-SV	NS-SV	CCMV-SV
DC clamping	No	Yes	Yes
Maximum mod. index	1	0.866	0.5
CMV	High	Medium	Low
WTHD %	$0.5 - 1.25$	$0.5 - 1.25$	$0.75 - 2.25$
Efficiency	Medium	Low	High

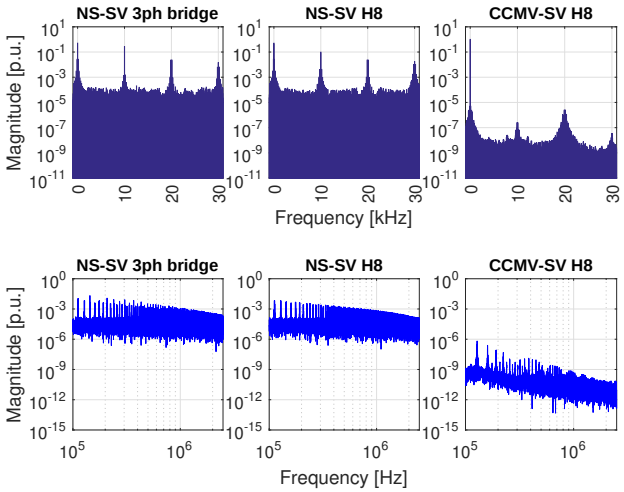


Figure 16. FFT of the CMV normalized to the supply voltage.

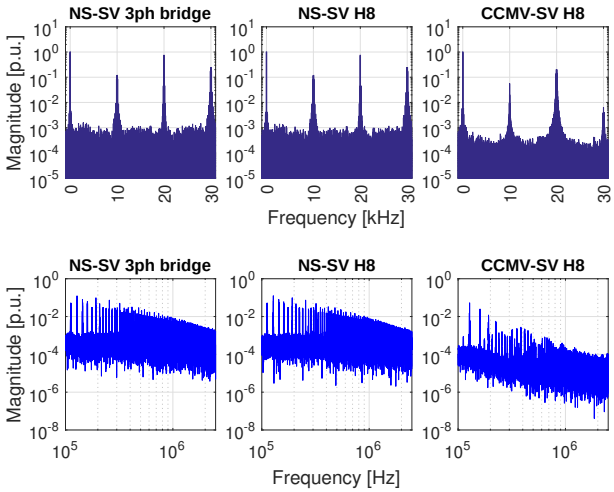


Figure 17. FFT of the line-to-line voltage normalized to the fundamental.

modulation exhibits a bigger output distortion than the NS-SV, resulting in a WTHD from 30% to 80% higher, depending on the modulation index. On the other hand, NS-SV modulation exhibit the same WTHD both in the case of the H6 and the H8 inverter.

As already mentioned in Section III, the proposed H8 has two additional devices for the decoupling of the DC side, which are responsible for additional losses. The efficiency of the proposed system was investigated and compared to a traditional one. Electrothermal simulations were conducted featuring the switching and conduction losses of a commercial power IGBT (Infineon IKW50N65H5). Figure 19 illustrates the performance for different combinations of the system in terms of topology and modulation (H8 or H6 and CCMV-SV or NS-SV). In particular, comparing the cases relative to the NS-SV modulation with H8 and H6 allows to evaluate the losses arising from the additional devices on the DC side of the H8 topology: the efficiency detriment results about 0.45%. Furthermore, comparing the cases with the same H8 configuration and the two proposed modulations, it is possible to observe that CCMV-SV performs better than NS-SV, with an efficiency improvement from 0.3% to 1.75% depending on the modulation index.

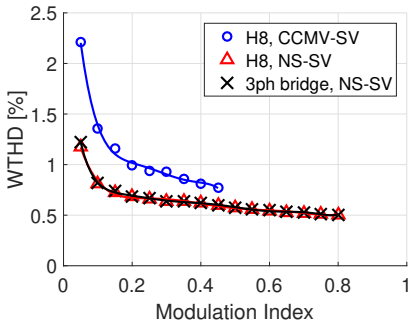


Figure 18. WTHD evolution against the modulation index for different configurations of the system.

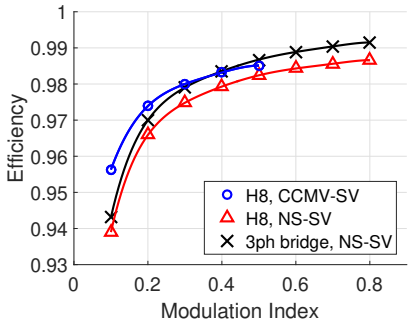


Figure 19. Efficiency performance for different combinations of the system.

Table V
EXPERIMENTAL TEST CASES

Test case	1	2	3
Topology	H6	H8	H8
DC clamping	No	Yes	Yes
Modulation	NS-SV	NS-SV	CCMV-SV
Mod. index m	0.6	0.6	0.25
V_{DC}	250V	250V	500V
f_{SW}		$10kHz$	
f_e		$50Hz$	
Load		$3 \times (10\Omega + 2mH)$, wye connected	

V. EXPERIMENTAL RESULTS

In order to prove the effectiveness of the H8 architecture and the proposed modulation strategies, a preliminary inverter prototype was built. A logic board, featuring a Freescale MCU MPC5643L, performs the proposed modulation and the current control. Test bed included a wye connected RL load in accordance to the simulations.

In order to compare the proposed solution with a traditional one, the following three operational configurations of the system, also summarized in Tab. V, were tested.

1) Operating as a H6 (maintaining the two DC side devices always on, therefore bypassing the DC-decoupling

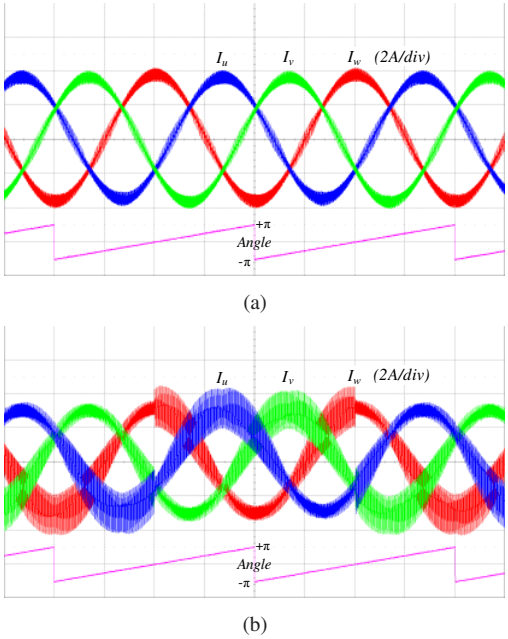


Figure 20. Current waveforms for the H8 prototype (blue, green and red) and evolution of the rotational angle (magenta) for two test cases: (a) NS-SV, $V_{DC} = 250V$, $m = 0.6$; (b) CCMV-SV, $V_{DC} = 500V$, $m = 0.25$. Time scale is 5 ms/div.

feature of the H8 architecture) and performing NS-SV modulation.

2) Enabling the DC decoupling during the inactive states execution and adopting the NS-SV modulation.
3) Enabling the DC decoupling during the inactive states execution and adopting the CCMV-SV modulation.

Tests present results in agreement with simulations. Fig. 20 presents current waveforms both in case of H8 performing NS-SV modulation, with a fixed modulation index of 0.6, and in case of H8 with CCMV-SV modulation with a fixed modulation index of 0.25. In the latter, the change in the current ripple behavior at every zero-crossing of the rotational angle is caused by the CCMV-SV modulation changing from odd to even vectors and vice versa. Moreover, in the CCMV-SV case the current ripple results to be higher than the NS-SV case. This is caused by two factors: CCMV-SV performs worse than NS-SV regarding this aspect, DC source voltage in the second testbed was the double than that in the first one.

Fig. 21 shows the reduction in V_{CM} for H8 over H6 and for CCMV-SV over NS-SV modulation. For the H6 V_{CM} varies in the range from $0V$ to V_{DC} at the PWM frequency (Fig. 21(a)); for H8 with NS-SV modulation the excursion of V_{CM} is reduced to $\frac{1}{3}V_{DC} - \frac{2}{3}V_{DC}$ (Fig. 21(b)); finally H8 with CCMV-SV modulation performs V_{CM} varying between $\frac{1}{3}V_{DC}$ and $\frac{2}{3}V_{DC}$ only once every rotational period, when the system changes between odd and even vectors (Fig. 21(c)), and exhibiting only small spikes around those main levels.

VI. Conclusions

In this work a modified two-level inverter was developed to reduce the common mode voltage. It makes use of a novel architecture called H8, which adds at the DC side of

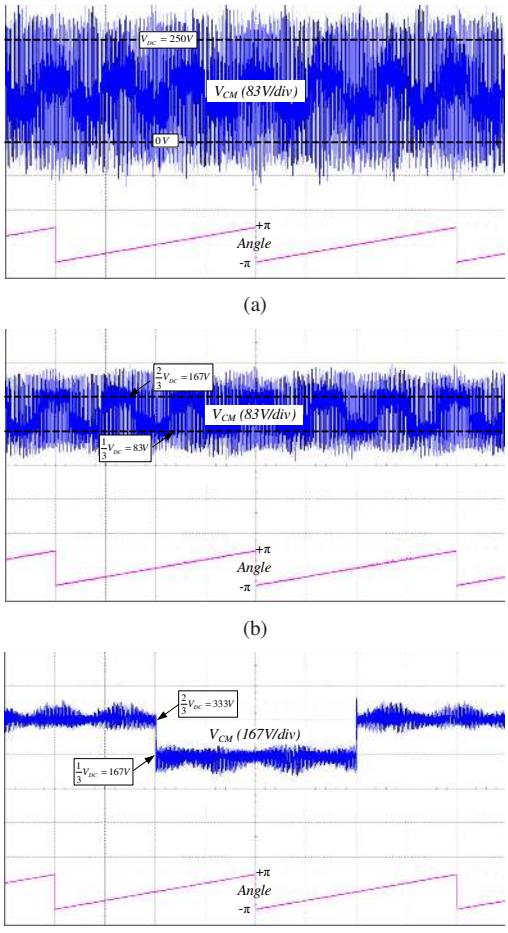


Figure 21. Common-mode voltage and rotational angle evolution for (a) the H6 performing NS-SV, $V_{DC} = 250V$; (b) H8 performing NS-SV, $V_{DC} = 250V$; (c) H8 performing CCMV-SV $V_{DC} = 500V$. Time scale is 5 ms/div.

a conventional H6 two active devices for decoupling the DC source and a passive circuit able to fix the voltage of the bridge at a reference value during the freewheeling phases. Moreover, two PWM modulation strategies have been developed as customized Space Vector modulations. One, denoted as CCMV-SV, is able to maintain the V_{CM} constant for an entire rotational period in case of modulation index smaller than 0.5. For higher modulation index, the control function exploits a different modulation strategy (NS-SV) that ensures a wider modulation range for the system at price of increased V_{CM}. Simulations have been conducted on Matlab/Simulink environment with good results. A preliminary prototype has been built and experimental results obtained, showing good performance of the system, in accordance with computer simulations. The proposed solutions allows reducing common-mode voltage both in amplitude and frequency respect to the two-level inverter.

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