Half adder capabilities of a coupled quantum dot device

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ABSTRACT

In this paper we demonstrate two realizations of a half adder based on a voltage-rectifying mechanism involving two Coulomb-coupled quantum dots. First, we examine the ranges of operation of the half adder's individual elements, the AND and XOR gates, for a single rectifying device. It allows a switching between the two gates by a control voltage and thus enables a clocked half adder operation. The logic gates are shown to be reliably operative in a broad noise amplitude range with negligible error probabilities. Subsequently, we study the implementation of the half adder in a combined double-device consisting of two individually tunable rectifiers. We show that this double device allows a simultaneous operation of both relevant gates at once. The presented devices draw their power solely from electronic fluctuations and are therefore an advancement in the field of energy efficient and autonomous electronics.

1. INTRODUCTION

Making use of surplus noise and heat has become a major focus of research situated at the intersection between physics and engineering[1–3]. While the related basic research concentrates on the discovery and exploration of new beneficial concepts and mechanisms such as brownian motors, phonon rectifiers, SQUID ratchets or piezoelectric nanogenerators[4–14] more application-near engineering turns its attention to the elaboration of self-powered and sustainable electronic devices[15–19]. Recently, we demonstrated voltage rectification and logical stochastic resonance in a semiconductor system based on Coulomb-coupled quantum cavities[20,21]. Here, we explore this system's capability to be configured and utilized as a half adder.

A half adder is an electronic circuit which is able to add up two binary digits x and y. It provides the two outputs sum (s) and carry (c). The half adder is one of the most elementary building blocks of electronic circuits which finds its use in more complex logic elements like full adders, multibit adders or arithmetic logic units[22]. The half adder can be realized by various interconnections of logic gates, for instance by a combination of several AND, OR, NAND and NOR gates or alternatively of five NAND gates or of five NOR gates. The most compact form, however, is a design which uses only one AND and one XOR gate. In this case, each gate is fed with the two inputs x and y. The XOR gate produces the output s, the AND gate the output c[22].

In this research, we examined two different devices named "single device" and "double device". Both devices are made up of modulation-doped GaAs/(Al,Ga)As heterostructures including a two-dimensional electron gas situated 80 nm below the surface. The devices were fabricated via molecular beam epitaxy and structured employing electron beam lithography and dry chemical etching methods. Whereas the single device has smaller dimensions compared with the double device, it requires a working in two sequential steps. The double device, on the other hand, allows a time independent, simultaneous output of both the sum and the carry bits. Both devices operate using electronic noise as power source and gate voltages as logic inputs.

V_l (V)	0	0	0.6	0.6
V_r (V)	0	0.6	0	0.6
Input	0	1	1	2
AND	0	0	0	1
XOR	0	1	1	0

TABLE I. Definition of the variable *Input* and logic truth table including AND and XOR (low: 0, high: 1) with respect to the logic input voltages which either take the high level 0.6 V or the low level 0 V.

2. DEVICE OPERATION

Figure 1(a) shows an electron microscopy image of the single device which features two Coulomb-coupled quantum dots QD_t and QD_b which are coupled via quantum point contacts (QPCs) to two leads (blue shaded region) and a single reservoir (red shaded region), respectively. Two side gates (green regions) can be used to influence the conductances of the upper QPCs. Tuning these QPCs to an asymmetric configuration and applying a noise voltage $V_{noise}(t)$ to the lower reservoir causes a current flow through the upper leads. To provide the noise voltage, a source with Gaussian-distributed, spectrally flat noise output with a cut-off frequency f=20 MHz and a root mean square noise amplitude σ_{noise} was employed. For an extended description of the basic operational details and theoretical backgrounds see references [20] and [21] as well as [10] and [11].

In order to realize logic gates, the voltages applied to the sidegates, V_l and V_r, are considered as logical inputs and the output current I as logical output. Throughout this work, the values for high and low input voltages are defined to be 0.6 V and 0 V, respectively. To simplify the notation, we introduce the parameter $Input$ which represents the side gate voltage configurations according to Table 1. Table 1 also includes the truth table for the relevant AND and XOR gates.

On a similar sample, we were in a recent publication able to demonstrate OR, NOR, AND and NAND gate functionalities which can be switched between, varying the root mean square noise amplitude σ_{noise} and the static voltage V_{gb}[21]. Varying V_{gb}, it is possible to dynamically change the device's logic functionality and to obtain the other above

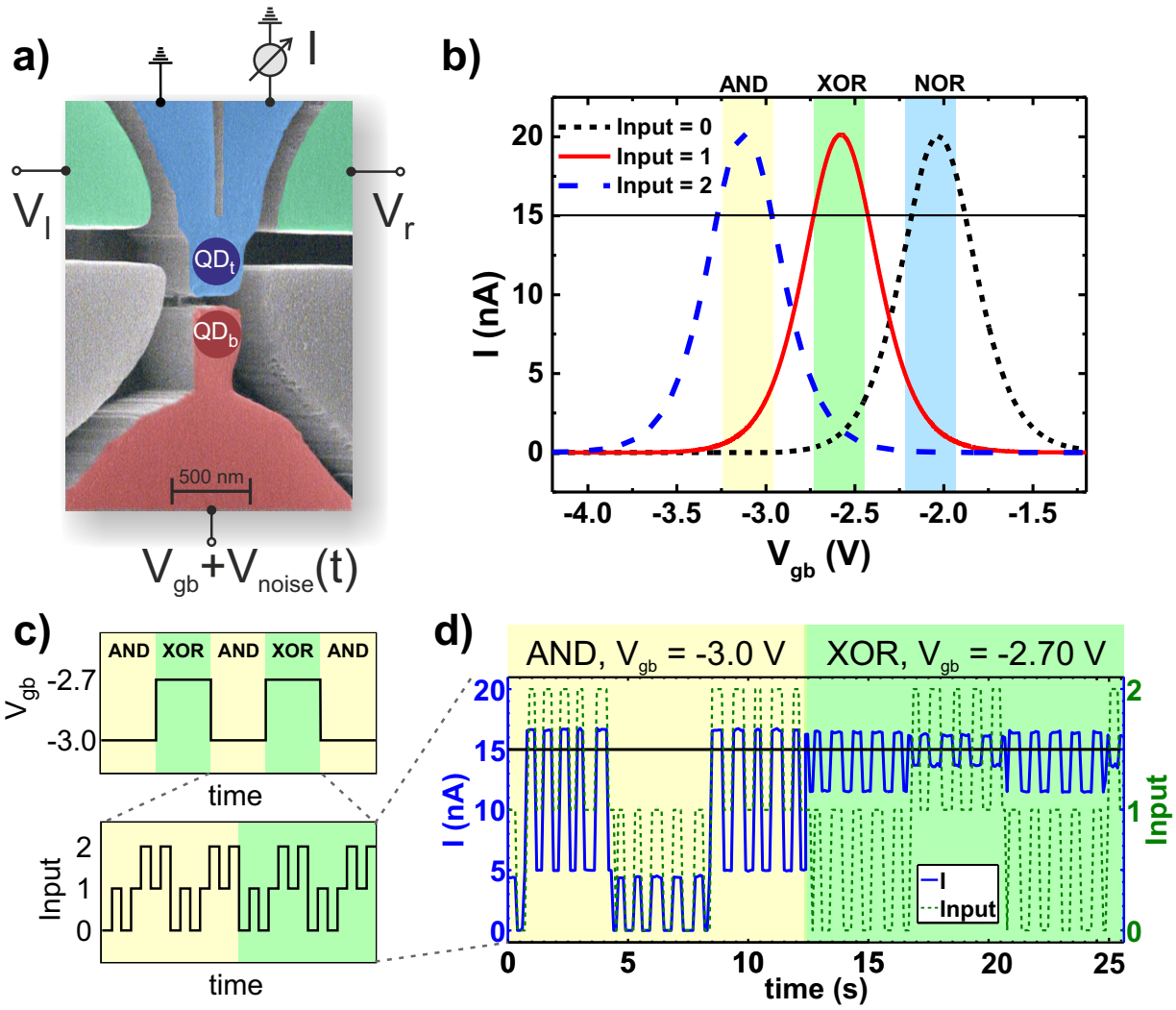

FIG. 1. (a) Electron microscopy image of the single device with attached circuit diagram. A current I flows through the upper part of the device (blue) when electronic fluctuations ($V_{noise}(t)$) are applied to the lower part (red). Logic input voltages V_l and V_r can be applied to the upper side gates (green) and enable a logic functioning of the device. (b) Simulation of the output current depending on V_{gb}. The yellow shaded region shows the range where an AND gate is to be expected, the green region the XOR gate range, and the blue region the NOR gate range. Details can be found in the main text. (c) Graphical explanation of the measurement scheme used in (d). V_{gb} is switched between -2.7 and -3.0 V in order to alternate the system's logical characteristic between AND and XOR. While an AND or XOR functionality is established, the *Input* parameter is switched between 0, 1 and 2. (d) Time-dependent measurements of the output currents for switching input levels and sσ_{noise} = 35.25 mV. The black lines designate the threshold I_{th} between high and low output values which is set to 15 nA.

mentioned gate functionalities, particularly the AND functionality, and moreover the XOR functionality, which are necessary for the compact half adder. All experiments reported here were performed in the dark at 4.2 K by immersing the samples in liquid helium.

3. RESULTS AND DISCUSSION - SINGLE DEVICE

We simulated the system's dependence on V_{gb} and on the input parameters according to the modelling in reference [21]. The following model parameters were used: $c = 0.014, \eta_{\mathrm{l,l}} = 3.78 \times 10^{-3}, \eta_{\mathrm{l,r}} = 2.44 \times 10^{-3}, \eta_{\mathrm{r,r}} = 2.84 \times 10^{-3}, \eta_{\mathrm{r,l}} = 2.40 \times 10^{-3}, \eta' = 2.4 \times 10^{-4}, E_{0,\mathrm{l}} = 7.0 \times 10^{-3}$ eV, $E_{0,\mathrm{r}} = 5.3 \times 10^{-3}$ eV and $\sigma_{noise} = 35.25$ mV. The results are displayed in Figure 1(b). Going from lower to higher V_{gb}, the current traces for the individual input configurations successively cross the current threshold, so that AND, XOR and NOR gate functionalities can be obtained. According to the simulation, the AND gate can be found in the V_{gb} voltage range from -3.27 to -2.97 V, the XOR gate between -2.73 and -2.43 V and the NOR gate between -2.18 and -1.88 V.

Time-dependent current traces during a switching of the input voltages can be seen in Figure 1(d), the switching scheme is graphically explained in Figure 1(c). We set the threshold I_{th} between high and low output currents to a value of 15 nA. For $\sigma_{noise} = 35.25$ mV $V_{gb} = -3.00$ V leads to an AND gate and $V_{gb} = -2.70$ V to an XOR gate. Consequently, changing of V_{gb} between these two values switches the device's output between the carry and sum bits. The possibility to switch between the gates allows the implementation of a sequential half adder, working in a two-step cycle and requiring a clocking of V_{gb}. Moreover, programmable, multi-function logic gates offer the possibility to realize software based computing architectures which entail the chance to improve computing efficiency and speed, for instance by adapting the logic network ideally to specific problems and upcoming calculations or by facilitating approximate computing schemes[23–25]. Furthermore, reconfigurable architectures allow functional upgrades, ameliorations and rearrangements during their lifecycle[26].

In order to determine the range of σ_{noise} in which an operation of the AND and XOR gates are possible, we measured the particular output currents for different σ_{noise}. The results are presented in Figure 2(a) and (b), respectively. The current rises with increasing σ_{noise} and the AND gate is available when only the $Input = 2$ output values are above

threshold. Correspondingly, the XOR gate is available when only the $Input = 1$ output values are above threshold. The green regions indicate the σ_{noise} range where an operation of both gates and thus of the half adder is possible. Figure 2(c) shows the probabilities of erroneous switchings for the individual gates with $I_{th} = 15$ nA. The probabilities were calculated from approx. 2000 switchings for each noise value. The σ_{noise} ranges for low error probabilities coincide largely with the operational ranges from Figure 2(a) and(b). In a narrower interval, the system reaches error probabilities close to zero. The optimal scope for the implementation of a sequential half adder is hence for $I_{th} = 15$ nA between approx. 33.8 and 35.3 mV.

In principle, if I_{th} is set to lower values, smaller σ_{noise} can be used as well. Tests of the device at lower noise amplitudes revealed error probabilities of about 0.4 % for $\sigma_{noise} = 9$ and 15 mV using XOR and AND gate configurations. Only if σ_{noise} is further lowered, the error probabilities increase significantly. For those evaluations, the threshold current was chosen to yield best results. The low noise error probabilities are presented in Figure 2(d).

Using the same parameters as for the simulation in Figure 1(b), we can model the output current's dependence on σ_{noise}. As Figure 3 shows, the output currents as well as the difference between the individual curves increase with increasing noise amplitude. Consequently, higher output powers and higher signal to noise ratios are expected for higher σ_{noise}. Figure 3(a) presents the AND gate simulation, Figure 3(b) the XOR gate simulation. For the AND gate, it is desired, that the $Input = 2$ curve features significantly higher currents than the other curves. For the XOR gate, the $Input = 1$ currents need to be higher than the other ones.

Since the device converts the noise into useful energy, we can calculate the highest input switching frequency at which the converted energy still exceeds the energy needed to switch the logic functionality. The maximal switching frequency at which the converted energy just equals the energy dissipated on a single side gate ($E = 1/2\ CV^2,\ V = 0.6$ V) depends on the output power's magnitude and thus on the noise amplitude. In order to evaluate the maximal gate switching frequency for the measurements done at $\sigma_{noise} = 35.25$ mV (Figure 1(d)), we estimate the side gate - channel capacitance C from Coulomb-diamond measurements and from geometrical considerations. For the latter, we assume the model of a plate capacitor which gives $C = \epsilon_0 \epsilon_r A/d$, with the vacuum permittivity ϵ_0, the permittivity of liquid helium $\epsilon_r \approx 1$, the distance between a side gate and the channel $d \approx 300$ nm and the

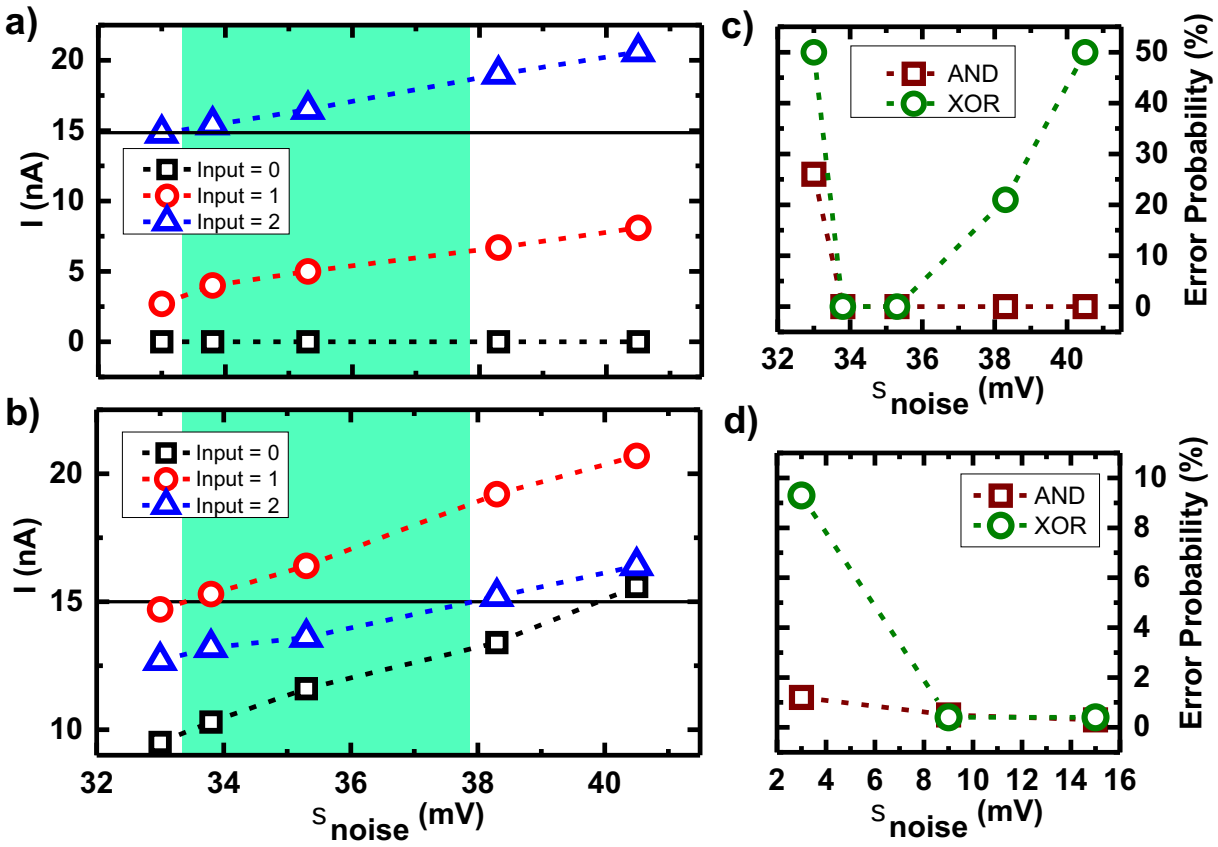

FIG. 2. (a), (b) Output currents for the different *Input* values in dependence on σ_{noise}. The green areas show the region, where an AND gate (a) and an XOR gate (b) is established, the black line designates the output threshold. (a) $V_{gb} = -3.00$ V. (b) $V_{gb} = -2.70$ V. (c) Error probabilities versus σ_{noise} for $V_{gb} = -3.00$ V (AND) and $V_{gb} = -2.70$ V (XOR). $I_{th} = 15$ nA. (d) Error probabilities for lower noise amplitudes. I_{th} is set to the values yielding the lowest error probability for each σ_{noise} individually. The dotted lines are guides for the eye.

side-area of the gate next to the channel $A \approx 6 \times 10^{-14}$ m^2 (about 30 nm width and 2 μm length). The estimations yield 0.27 aF and 23 aF for the Coulomb-diamond and geometrical considerations, respectively. Assuming that the system spends equal amounts of time in the different output states defined by the input configurations, we calculate a mean output current of $I_{mean} = 10$ nA. According to reference [20] the device provides an output power of approx. 3 pW at this output current. From this, we calculate the maximal switching frequency to be between 0.72 MHz and 62 MHz for the Coulomb-diamond and geometrical considerations, respectively. Below this frequency, the energy dissipation during a charging

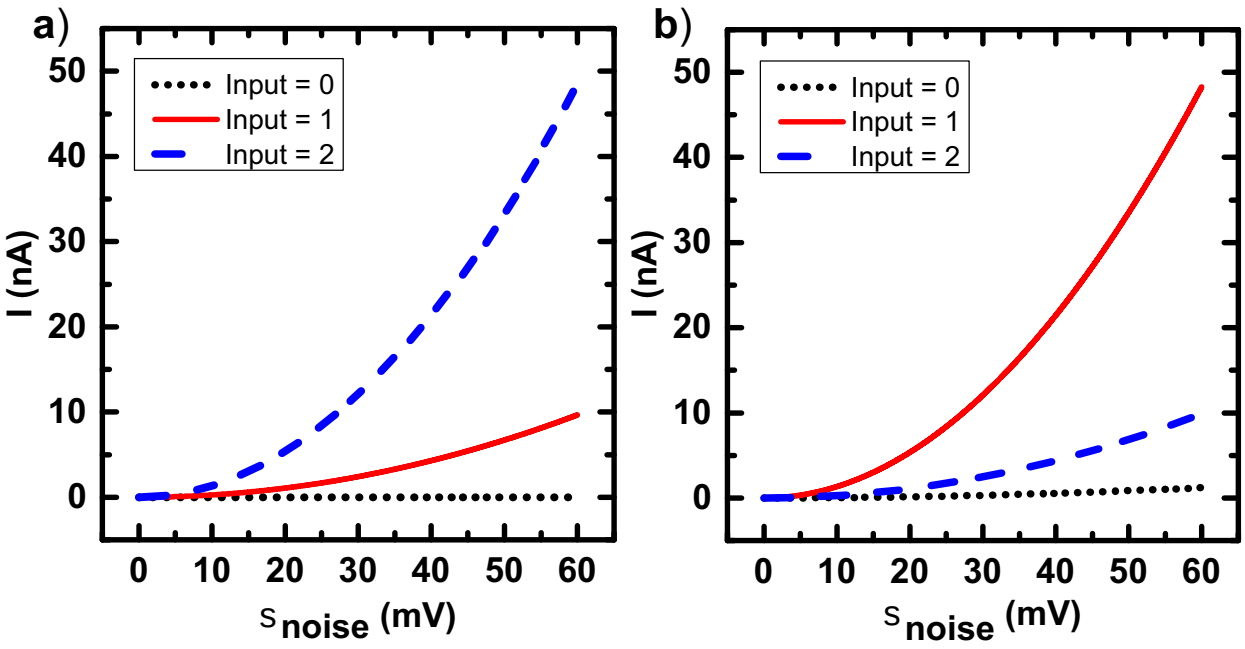

FIG. 3. Simulation of the output current depending on σ_{noise} for $Input = 0$, 1 and 2. a) AND gate, $V_{\mathrm{gb}} = -3.0$ V, b) XOR gate, $V_{\mathrm{gb}} = -2.7$ V. The simulations in (a) and (b) correspond to the experiments shown in Fig. 2 (a) and (b) respectively.

of the side gate - channel capacitance is smaller than the energy generated by the device which theoretically allows an operation which solely relies on the noise floor as power source. In contrast to a conventional logic gate, output currents which are larger than zero for the low output states are advantageous in our device, since higher output currents mean a higher output power which theoretically allows higher switching frequencies.

4. RESULTS AND DISCUSSION - DOUBLE DEVICE

Aiming for a simultaneous operation of the half adder in a single device, we fabricated the double device which is shown in Figure 4(a). The upper part of the figure displays an electron microscopy image of the main structured area whereas the lower part zooms into the sample's two functional regions. These two parts are connected by a common noise source contact (red) where the voltage $V_{com} = V_{gb} + V_{noise}(t)$ can be applied. Beyond that, the two parts each resemble the single device in their functional design. They consist of

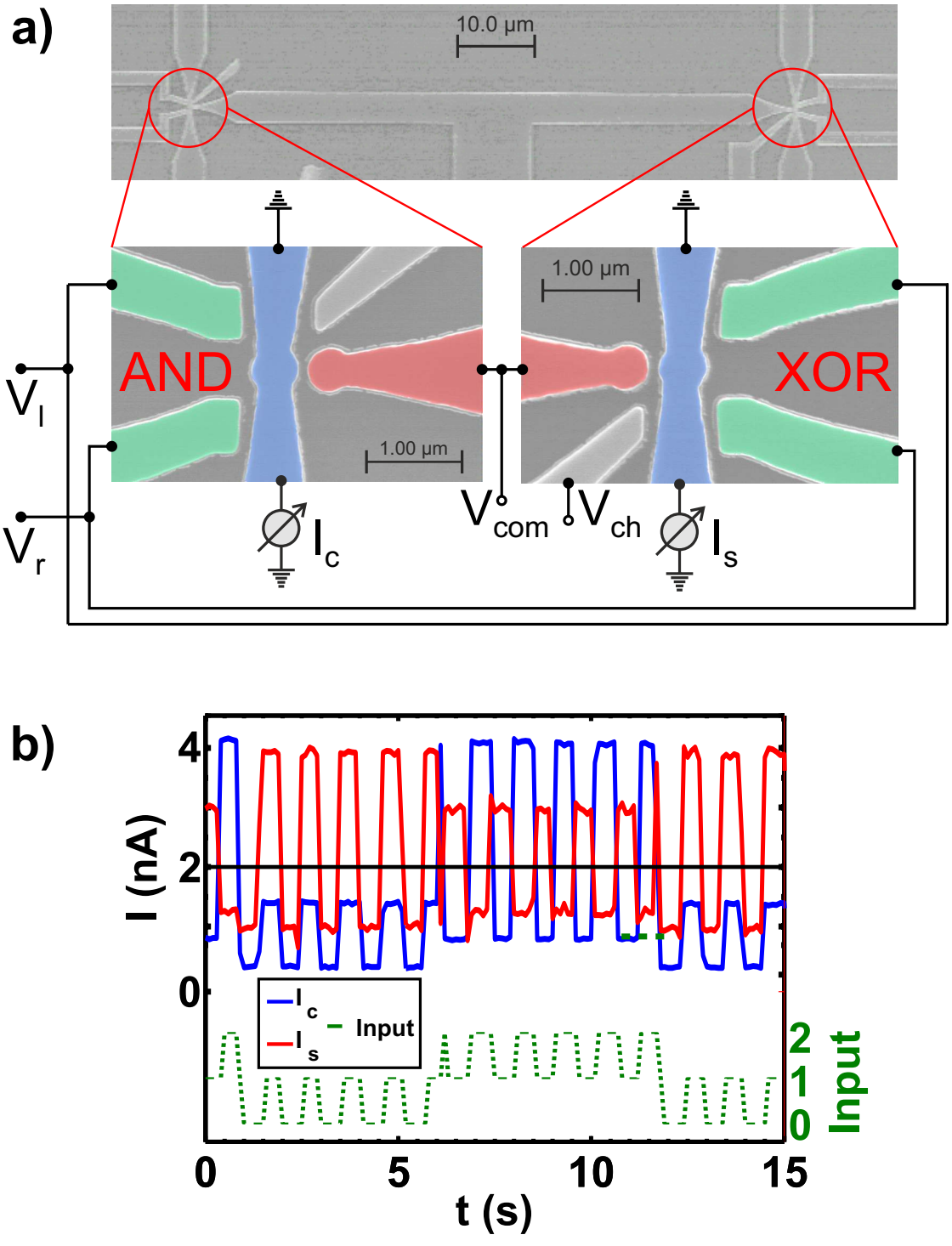

FIG. 4. (a) Electron microscopy image of the double device with attached circuit diagram. The double device consists of two individual rectifiers which have a common contact with the applied voltage $V_{com} = V_{gb} + V_{noise}(t)$. Additionally, V_{ch} can influence the conductance of solely the right channel. (b) Time-dependent measurement of the output currents I_c and I_s for switching input levels. I_c shows the logical characteristics of an AND, I_s of an XOR gate. $\sigma_{noise} = 37.5$ mV, $V_{gb} = -1.8$ V, $V_{ch} = -0.7$ V, $I_{th} = 2$ nA.

a single reservoir (where V_{com} is applied and which is connected to a quantum dot, red), of a second quantum dot (which is capacitively coupled to the first one and connected to two leads, blue), and of two side gates (which influence the second quantum dots QPCs, green). Since V_{gb} now affects both functional regions at the same time, the right region is furthermore equipped with a supplementary gate where the voltage V_{ch} has an additional effect on the right channel's conductance. Figure 4(a) moreover displays the equivalent circuit of the half adder where V_l and V_r are both applied to the left and right side gates simultaneously. I_c represents the half adder's carry signal and I_s the half adder's sum signal.

Similar to the single device, the logical functionalities of the double device can be manipulated to obtain several different gates varying V_{com}, i.e. V_{gb} and σ_{noise}. In order to change both subdevices' functionalities independently, V_{ch} needs to be employed as well. However, a purposeful unequal fabrication of the double device's two parts could be used to intrinsically tune one part to the AND and the other part to the XOR functionality. In this case, V_{gb} and V_{ch} would no longer be necessary for a half adder operation. For the measurement with the present sample in Figure 4(b), where the output currents are plotted versus time for switching input voltages, the control voltages were tuned to $V_{gb} = -1.8$ V and $V_{ch} = -0.7$ V, so that I_c produces the logical characteristics of an AND, I_s of an XOR gate. Consequently, the device is a realization of a half adder which adds up the binary values represented by V_l and V_r and produces the output signals sum I_s and carry I_c.
Analogous to the single device, we estimate the capacitance between a side gate and the current carrying channel from geometrical considerations and thereby assess a maximal switching frequency at which the energy conversion just outweighs the energy dissipated during a side gate charging. The calculations yield a capacitance of 0.44 aF (d=120 nm, A=10 nm $\times$ 600 nm = 6×10^{-15} m^2), a mean output current of $I_{mean} = 2$ nA, a mean output power of $P_{mean} = 0.2$ pW and a switching frequency of approx. 0.25 MHz which is smaller than the values estimated with the single device. This is due to the lower output currents and output powers which result from a lower capacitive coupling between the two quantum dots.

5. CONCLUSION

In summary, we introduced a nanoscale half adder powered by electronic fluctuations. We examined the characteristics and working ranges of our voltage rectifier tuned with a control voltage to provide AND and XOR gate functionalities. A reliable functioning of both gates is shown to be possible starting from noise magnitudes as low as 9 mV. The controllable switching between the gates allows a sequential, clocked operation, having as advantage the small size of the logic element. Moreover, we demonstrated the integration of two individually rectifying structures into a single device, making possible the realization of a time-independent, combinational logic half adder working solely by means of voltage rectification and noise exploitation. Lastly, we assessed the maximal switching frequency at which the generated energy just equals the energy needed for a switching operation. This frequency was found to be between 0.72 and 62 MHz for the single device and to be around 0.25 MHz for the double device.

This work presents a proof of concept. Next steps towards a fully employable device would involve research tackling the efficiency of the device and aiming for an increase of the output/input voltage ratio. Furthermore, it is conceivable to customize the design of the rectifying elements so as to avoid the application of the control voltages V_{gb} and V_{ch} and to allow a direct operation of the desired logic gate. Our findings are advances on the way leading to autonomous and energy-efficient electronics which could rely solely on excess electronic fluctuations, waste heat or thermal gradients.

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