Handheld electrocardiogram measurement instrument using a new peak quantification method algorithm built on a system-on-chip embedded system

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This article reports on the new design and development of an electrocardiogram (ECG) measurement instrument built on a system-on-chip (SOC) embedded system. A new approach using the peak quantification method (PQM) for measuring the human heart rate is described. A computer, some medical equipment, and other facilities are often required for conducting the traditional ECG measurements. However, the monitors of such instruments have some disadvantages, e.g., bulky, not very easy to transport, expensive, and so forth. Hence, we propose a new design for ECG measurement which is built on an embedded system. Our system adopts a SOC and ECG detection circuits to carry out a real-time, low-cost, and compact ECG measurement system. Regarding heart rate computation, the experimental results show that the new PQM algorithm, when applied to heart rate measurements, yields error smaller than 1 bpm. In addition, the correlation coefficient between the measured and actual heartbeats can reach 0.94 when the heart rate is less than 153 bpm. It shows that the use of the PQM algorithm gives an extremely high degree of accuracy. © *2006 American Institute of Physics.* [DOI: 10.1063/1.2349295]

I. INTRODUCTION

The electrocardiogram (ECG) is a highly valuable diagnostic aid and clinical tool in modern medicine. This is primarily because a visual inspection of the recorded ECG wave form is critical to the correct diagnosis and treatment of cardiovascular diseases.[1] Measured from the surface of body, the ECG wave form conveys vital physiological information of the condition of the patient's heart and cardiovascular system. At present, measuring ECG wave form would primarily require the use of electrocardiograph.[2]

The traditional electrocardiographs have some disadvantages, such as bulky, not very easy to transport, and expensive. Consequently, only hospitals have such medical equipment. In order for people to use electrocardiographs in home care situations, they need to be smaller and more portable. Hence, in the past few years, personal digital assistant (PDA) has started to be developed and employed to measure ECG wave form.[3]

However, at present, the original designed function of PDA is primarily for simple secretarial management and personal organizer. It is not used for measuring physiological signals in general. Hence, if one wants to measure ECG, an ECG signal detection circuit must be externally added to the PDA. In addition, the signal obtained must be transmitted via a low-speed universal asynchronous receiver transmitter (RS-232) interface so that it may be sent to the PDA.[4] Results show low performance, and it is not easy to show wave forms on the PDA screen in real time.[5]

In this article, we propose a new design for the ECG measurement instrument that is built on a system-on-chip (SOC) embedded system. We incorporate a 32 bit ARM7 SOC microprocessor in order to develop a real-time and smaller sized embedded-type ECG measurement system. To further reduce the size of the system, we used a complex programmable logic device (CPLD) to implement the digital logic control circuit. The CPLD can replace many digital logic parts (gates, decoders, and multiplexers); as a result, the system is lighter and more portable.

The heart rate computation and heartbeat inspection can be estimated from an electrocardiogram, a phonocardiogram (PCG), or a blood pressure wave form. At present, the heart rate is mainly calculated by analyzing the time and feature differences on the RR interval,[6,7] which is detected for every input heartbeat signal. Various algorithms or methods were used to identify the heartbeats and the subsequent heart rate

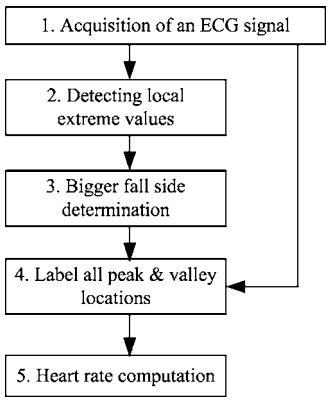

FIG. 1. The PQM algorithm.

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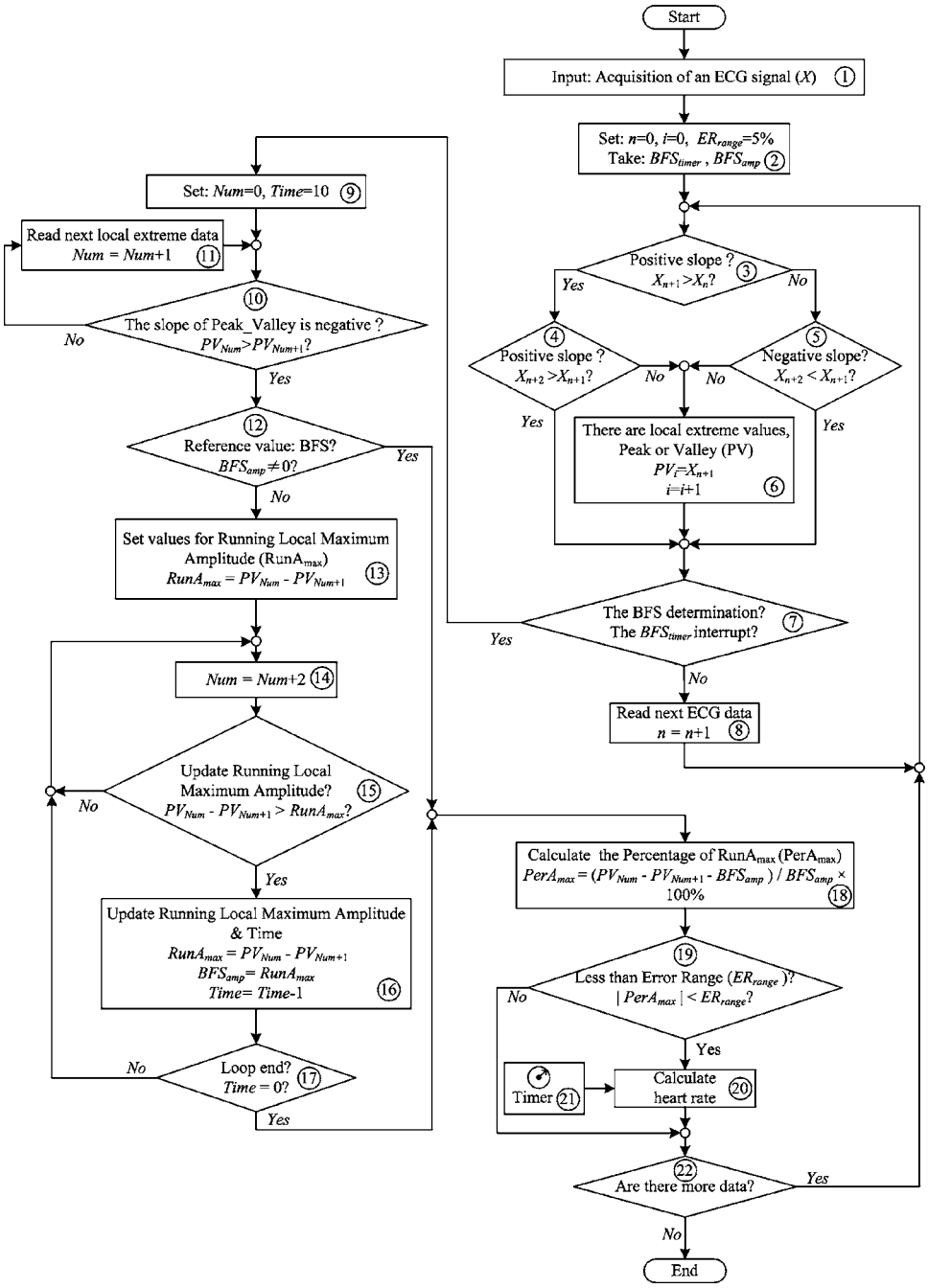

FIG. 2. Flow diagram of the PV detection in the ECG signal.

computation. For example, the simplest method for estimating the heart rate is to calculate the inverse of the RR interval (the period between the two R waves), for example, if the RR interval is 800 ms, the heart rate is 75 bpm [Heart rate =60 000/(RR interval)].

However, most computational methods set a threshold for the signal amplitude in order to compute the heart rate from the peak values. It is often hampered by too small or too large signal amplitudes or noises and the like, thus causing the measured heart rate to be substantially inaccurate. In this article, we present a new peak quantification method (PQM) algorithm for detecting the peak of the signal amplitude. The algorithm requires no user intervention and thus adjusts automatically the detection parameters to match the ECG signal profile.

This article is organized as follows. The PQM algorithm is introduced in Sec. II. The system implementation is presented in Sec. III. The software programming and system calibration are described in Sec. IV. In Sec. V, we discuss the clinical testing results and concludes and discusses the new design concepts proposed in this study that can help diversify the applications of the embedded system to the field of medical instrumentation.

II. THE PQM ALGORITHM

We propose a PQM algorithm that is used to obtain the peak-valley (PV) values from the ECG signal wave forms and then to compute the heart rate. The concept of the PQM is illustrated in Fig. 1. First, it searches and records all the possible magnitudes of the maximum and minimum and their locations, including the line-section-wise turning points

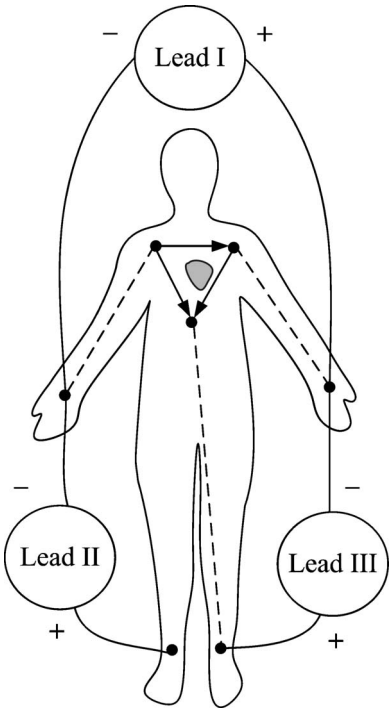

FIG. 3. The Einthoven triangle, showing leads I, II, and III.

from a whole chunk of an ECG signal. Second, it deletes the turning points between the maximum and the minimum. After obtaining the PV values, we can convert them into the heart rate.

Figure 2 shows the flowchart of the PV detection procedure. In steps 1 and 2, the acquisition of an ECG signal (X), where X_n represents the nth ECG data and $\mathrm{BFS}_{\mathrm{timer}}$ stands for the timer of the computer or microprocessor, is automatically disrupted in fixed intervals wherein the $\mathrm{BFS}_{\mathrm{amp}}$ is the amplitude of the bigger fall side (BFS), and the $\mathrm{ER}_{\mathrm{range}}$ is the acceptable error range.

In steps 3–5, if the slope of the curve changes from positive to negative, it is possible that a local maximum exists. On the other hand, it may have a local minimum if the reverse condition occurs, as depicted in Eq. (1). If $\mathrm{BFS}_{\mathrm{timer}}$ interruption occurs, then the process of BFS detection (BFSD) will start (step 7). The BFSD is obtained by comparing all extreme values (local maximums and local minimums) in the unit circle (an ECG wave form). Each BFSD on the circle corresponds to one RR interval or heartbeat.

$$\text{Local minimum} = (X_{n+1} < X_n) \text{ and } (X_{n+2} > X_{n+1}),$$

$$\text{Local maximum} = (X_{n+1} > X_n) \text{ and } (X_{n+2} < X_{n+1}). \quad (1)$$

In the first place, the PV values read from memory are compared with each other in order to find a group with the running local maximum amplitude ($\mathrm{RunA}_{\mathrm{max}}$) (steps 12–16), e.g., comparing X_{n+1} with X_n, and X_{n+2} with X_{n+1}, and so on. If $X_{n+1} > X_n$ and $X_{n+2} < X_{n+1}$, then there is a local minimum. On the other hand, if $X_{n+1} < X_n$ and $X_{n+2} > X_{n+1}$, there exists a local maximum. Either the local minimum or local maximum can be a PV value, as shown in Eq. (2).

$$\mathrm{PV} = \begin{bmatrix} (X_{n+1} > X_n) \text{ and } (X_{n+2} < X_{n+1}) \\ (X_{n+1} < X_n) \text{ and } (X_{n+2} > X_{n+1}) \end{bmatrix}. \quad (2)$$

The negative slope detection method is proposed in this work (Fig. 2) in order to detect the group with negative slope

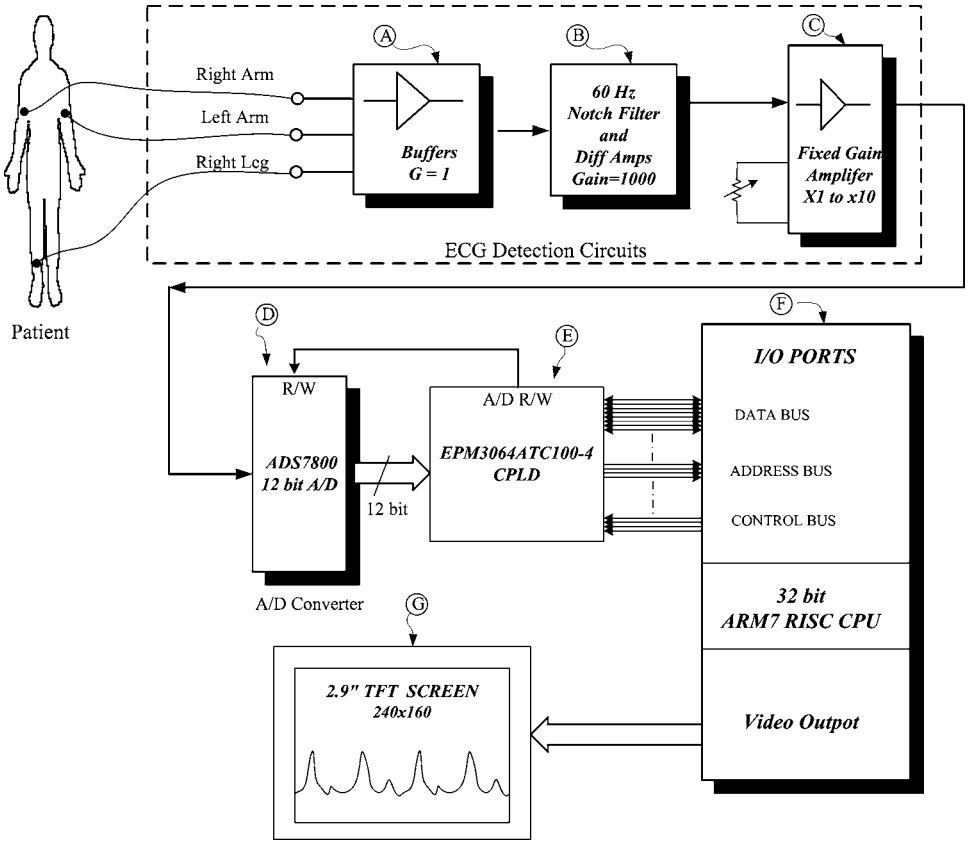

FIG. 4. The system block diagram.

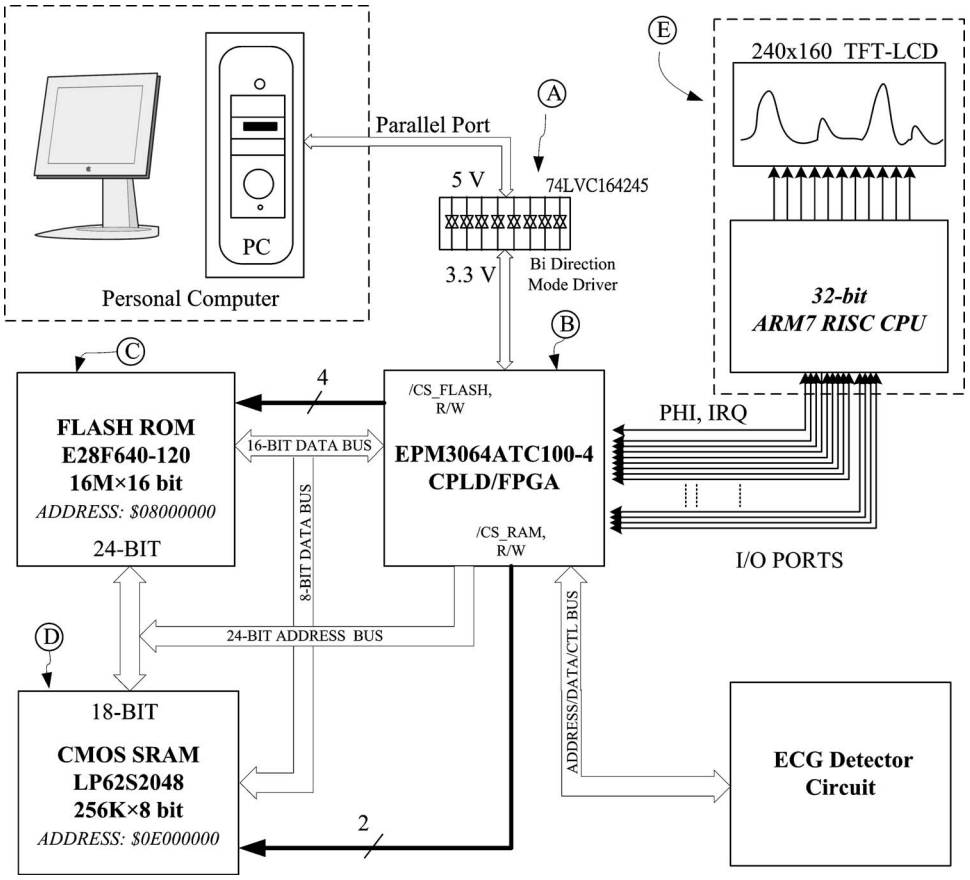

FIG. 5. The interconnection among the computer, the memory, and the ARM7 and will execute functions in compliance with the computer commands.

only. For instance, the line from PV_{num+1} to PV_{2num} can form a positive slope while the line from PV_{2num} to PV_{2num+1} can form a negative slope. One positive slope and one negative slope can generate a peak or valley value. The negative slope group (for example, $PV_{knum} \rightarrow PV_{knum+1}$, $k=1,2,3,\ldots$) was only used for detection purposes and for getting rid of the positive group.

The BFS_{amp} is the absolute maximum amplitude. It runs only once during the detection process. The BFS_{amp} is used as the reference value and may represent the maximal amplitude of the amplified ECG signals of subjects, while the acceptable error range is added to increase the accuracy when measuring the heart rate.

Finally, if the error between $RunA_{max}$ and BFS_{amp} is less than ER_{range}, it means that one heart beat is detected (steps 18–20). In step 21, the timer is employed to calculate the heart rate.

III. SYSTEM IMPLEMENTATION

An ECG wave form is obtained by measuring the potential difference between two electrodes placed on the surface of the skin, as shown in Fig. 3. Leads I, II, and III are measured over the limbs. Lead I is measured from the right to the left arm, lead II is measured from the right arm to the right leg, and lead III is measured from the left arm to the left leg.[8] The other nine leads are derived from the potential between this point and the three limb leads (aVR, aVL, and aVF) and the six precordial (chest) leads (V1–V6). There are therefore 12 leads in total. In this study, the patient's ECG wave forms were obtained from lead I loop with the right leg as the common electrode for the reference signal.

A block diagram of the ECG electrocardiogram measurement system is shown in Fig. 4. The hardware is composed of an ARM7 SOC microprocessor, a CPLD component, a 12 bit analog-to-digital (A/D) converter, an eight-button keypad, a thin film transistor liquid crystal display (LCD) module, and ECG measurement circuits. The operating frequency of the ARM7 SOC microprocessor is 16 MHz, and the input-output (I/O) interfaces via a CPLD chip for the port expansion. The TFT-LCD supports up to 16 bit, 240 $\times$ 160 real color displays.

Initially, three ECG electrode plates are stuck to the right arm, left arm, and right leg of the subject receiving the test. Then, a 1:1 buffer amplifier is added to the input end to prevent a poststage signal interference with the prestage ECG signals (shown as A in Fig. 4). The amplitude of the ECG signals is approximately 1 mV p.-p. (peak-to-peak voltage). The signals must be amplified with the 60 Hz noise interferences (B) filtered out, and then quantized as digital data (D). This study adopts the Burr-Brown's ADS7800 IC, which is a 12 bit A/D converter with a sampling capability of 333 kHz. The digitized ECG data (E) are transmitted to ARM7 (F) via a CPLD component and displayed on the TFT-LCD screen (G).

Modern digital designs are increasingly being built on complex programmable logic devices. A single high-density device, such as the EPM3064ATC100 from ALTERA Semiconductors, is employed to perform the data transmission

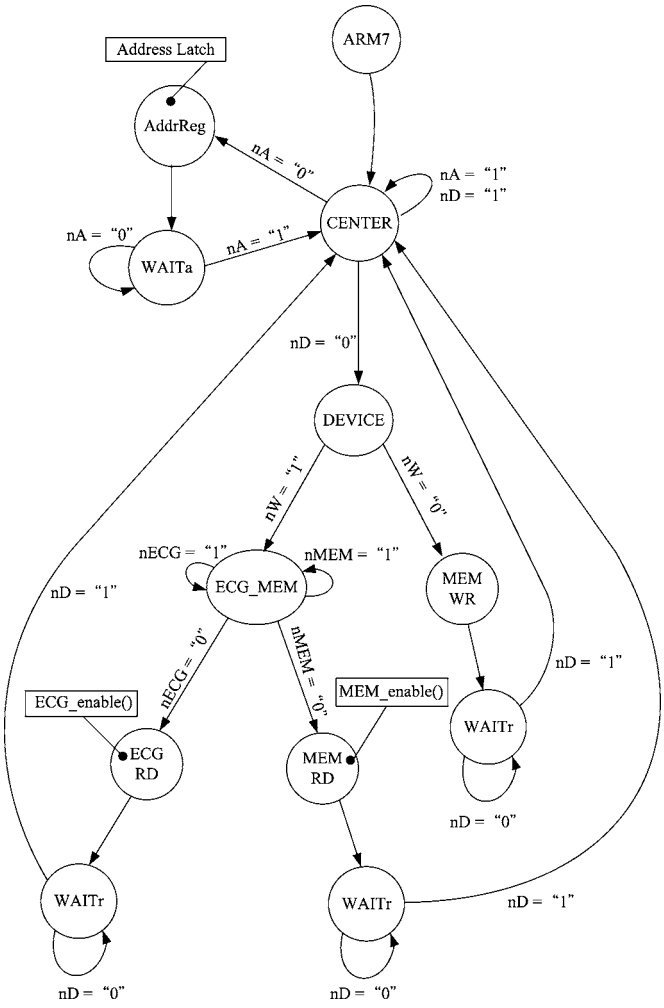

FIG. 6. The CPLD chipset state machine diagram.

between the ARM CPU and the A/D converter. The logic functions in the CPLD are implemented by very high-speed integrated circuit hardware description language (VHDL) and are synthesized and simulated using the ALTERA MAX +PLUS II V.10.2 development software.[9,10]

The CPLD component (shown as B in Fig. 5) is employed to coordinate the data transmission between the computer, the memory, and the ARM7 and will execute functions in compliance with the computer commands (C, D, E). After compiling the program, the compiled code is transmitted to the CPLD via the computer parallel port and then burned into the flash ROM. Finally, the code in the flash ROM is executed by the ARM7 to control the ECG measurement circuits (A/D converter, decoders, and multiplexers).

Since the parallel port uses a standard 5-V TTL level, while the standard level of the CPLD and ARM7 components is 3.3 V, we need to insert a level conversion component between the two to avoid the CPLD from getting easily get damaged. We use the 74LVC164245 component (A) to accomplish the design.

The state machine of the CPLD is shown in Fig. 6. The CPLD will analyze all the states of the input signals to control the peripheral circuits.

(1) Under the CENTER state, the machine will keep waiting for an address trigger (nA) signal or a Data Trigger (nD) signal.
(2) If nA is detected as zero, the machine will start an address write cycle and the address will be latched to an address register.
(3) If nD is detected as zero, the machine will start a data read/write cycle and the chipset will enter a DEVICE state.
(4) The DEVICE state designates that the ARM7 needs to retrieve the memory data if nW is 1 and nMEM is 0. At this moment, the chipset enters a MEM_RD state to get ready to retrieve data from memory.
(5) The ARM7 needs to retrieve the ECG data if nW is 1 and nECG is 0. The chipset will enable the A/D converter and enter an ECG_RD state to get ready to retrieve the ECG data.
(6) The system intends to write data into the memory if nW is 0.
(7) If nD changes from 0 to 1, data read/write is complete and the chipset returns to the CENTER state.

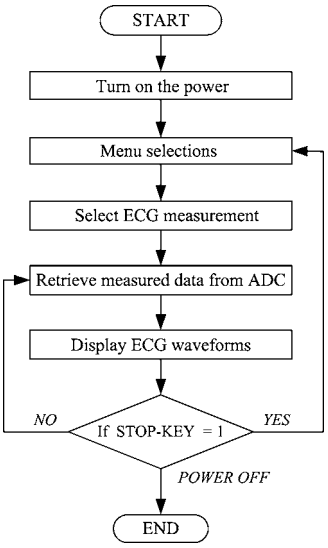

FIG. 7. Software flowchart of the system.

The above process is vital to the measurement system, which

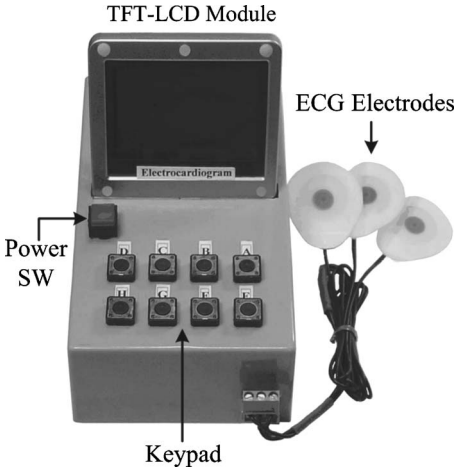

FIG. 8. The ECG measurement system.

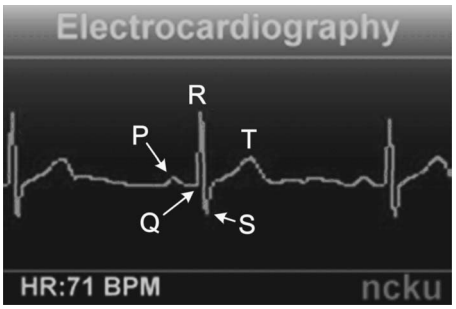

FIG. 9. The ECG measurement screen.

might not function normally if one of the states incurs an error. If an error occurs, it represents that there are some bugs in the states, and it is necessary to redesign or check each state.

IV. SOFTWARE IMPLEMENTATION AND SYSTEM CALIBRATION

The system program is developed on a personal computer using *C* language and the ARM Developer Suite (ADS v1.2) software for compiling. The flowchart is shown in Fig. 7. Once the system is turned on, its screen will display the selection menu. If ECG function is selected, ECG data will be retrieved and displayed on the TFT-LCD. The system will continuously retrieve and display the data until the STOP button is pushed.

The system must be calibrated by utilizing a known ECG signal. The calibration signal is generated from a KL700 ECG simulator (K&H Mfg. Co., Ltd.), which can output an ECG signal in the range from 2 to 100 bpm.

The accomplished ECG measurement system is shown in Fig. 8. The complete system is composed of a power switch, three electrode plates, a keypad, a TFT-LCD module, and the ECG detection circuits.

V. RESULTS AND DISCUSSION

In Fig. 9, the screen clearly displays an ECG cycle (P, Q, R, S, and T waves). The P wave is followed by a QRS complex. The QRS complex represents the depolarization of the ventricular myocardium. The lower left side on the screen displays a message "HR: 71 bpm," which indicates a heart rate of 71 bpm. The normal human heart rate (HR) is 60–100 bpm with a variation of less than 10%. The diagrams in Fig. 9 describe the normal ECG wave form that can be proven by referring to the database provided by the MIT-BIH.[11]

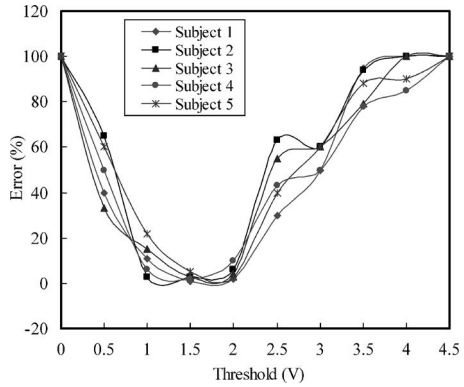

FIG. 10. The heart rate of five subjects using traditional measurement methods.

In the heart rate computation, we noticed from the experiments that the P and T waves will be distorted when the electrode plates are shifted due to the motion of the subject or placed in an incorrect position and cause a measurement error in the heart rate. The most generally used traditional method for computing the heart rate is according to a preset threshold value, e.g., if the R wave exceeds the threshold value once, it means one heartbeat. Although this method can rapidly compute the heart rate, serious judgment discrepancies can occur when the threshold value is not appropriately set as illustrated in Fig. 10.

Figure 10 shows the heart rate of five subjects using traditional measurement methods. The ERROR (%) designates the percentage error between the measured and the actual heartbeat values. For example, if the actual heartbeat is 100 bpm and the measured result is 99 or 101, the ERROR is equal to 1%. From Fig. 10, we can apparently observe that a threshold of 1–2 V is the most appropriate value for the cases we studied. The experimental results show that although it is feasible to compute for the heart rate with the threshold value method, this method is, however, not precise in practical applications and the resulted discrepancies can be quite large too. In view of this fact, this study proposes the PQM algorithm to compute the heart rate. This new method has nothing to do with the magnitude of the threshold value and hence will not affect the heart rate reading due to the different locations the electrode plates are placed.

Table I illustrates the heart rate measurements of five

TABLE I. The heart rate measurement using the PQM algorithm.

Subjects		1	2	3	4	5
Correct heart rate	Total (5 min)	345 beats	367 beats	339 beats	381 beats	412 beats
	Average (bmp)	69.0	73.4	67.8	76.2	82.4
Using PQM to detect heart rate	Total (5 min)	343 beats	365 beats	339 beats	380 beats	414 beats
	Average (bpm)	68.6	73.0	67.8	76.0	82.0
Testing errors of PQM (%)		−0.58	−0.54	0.0	−0.26	0.49
BFS [average amplitude (V)]		1.1	2.8	1.9	4.0	3.6

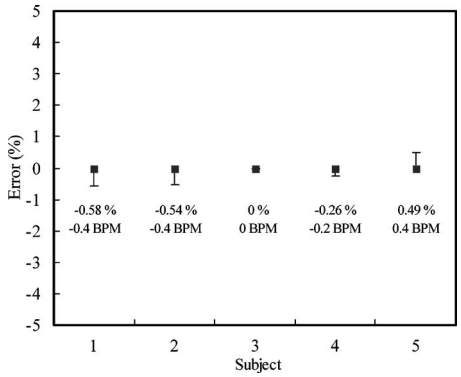

FIG. 11. The error margins when using the PQM algorithm to measure the heart rate.

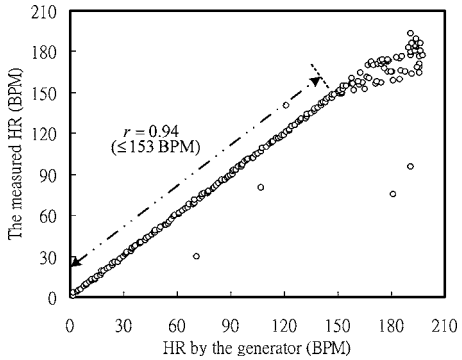

FIG. 12. The maximum effective range of the proposed system on the heart rate measurement. The results show that this system can accurately measure the heart rate (r=0.94) up to 153 bpm.

patients using the PQM algorithm. The correct heart rates of these subjects are 69.0, 73.4, 67.8, 76.2, and 82.4 bpm, respectively. The measured heart rates when using the PQM algorithm are 68.6, 73.0, 67.8, 76.0, and 82.0 bpm, respectively. The errors are all within 1 bpm range (Fig. 11). In addition, on the fourth item (average amplitude) in Table I, even if the ECG amplitude of each participant is not consistent and shows a big difference (from 1.1 to3.6 V), the algorithm can still accurately predict the ECG peak and calculate the heart rate correctly. The experimental results verify that the PQM algorithm can rapidly compute the heart rate with fine accuracy.

A programmable ECG generator[12] was employed to produce the ECG signals with different speeds for testing the system. The heart rate can be adjusted in increments of 1 bpm, from 20 to 200 bpm, while the amplitude of the ECG signal can be set from 0.1 to 400 mV with a 0.1 mV resolution. Figure 12 shows the maximum effective range of this system on the heart rate measurement. X axis is the heart rate produced by the ECG generator, while Y axis is the measured heart rate derived from this system. The correlation coefficient (r) between the simulated and the measured heart rates is employed to judge the correction. The results show that up to 153 bpm, this system can accurately measure the heart rate (r=0.94). Hence, this system is sufficient enough to be used under the normal range of heart rate.

This study takes a new approach to employ an ARM7 SOC embedded system to develop a handheld ECG measurement system. Our experimental results show that such an approach is feasible. We also showed that the new PQM algorithm is applicable to a range of other cardiovascular signals that display oscillations around a mean level (e.g., pulse oximetry). The new design concepts proposed in this study can help diversify the applications of the embedded system to the field of medical instrumentation and thus enable the medical equipment to be more accessible to the general public and foster a healthier society.

ACKNOWLEDGMENT

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