Hardware Simulation of BPSK Modem

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ABSTRACT

This paper presents the hardware simulation of a BPSK Modulator and Demodulator using Matlab/Simulink environment and System Generator, a tool from Xilinx used for FPGA design of the Modulator and Demodulator. VHDL programming code is used to generate BPSK digital signal. The modulator and demodulator VHDL algorithm has been simulated in MATLAB R2009a and system generators Xilinx ISE 12.1. This paper also focuses on error performance parameter of BPSK modulation and demodulation schemes in AWGN channel.

General Terms

Hardware, Simulation, Digital, Logic, Modulation, Demodulation, Algorithm.

Keywords-

BPSK (Binary Phase Shift Keying), FPGA (Field Programmable Array Logic), AWGN (Additive White Gaussian Noise), BER (Bit Error Rate), System Generator, Xilinx, Wavescope, Resource Estimator, RRC (Root Raised cosine).

1. INTRODUCTION

The Programmable logic device (PLD) based modulator design introduces the importance of digital communication in today's wired & wireless networks. Modulation is the process in which a property of one signal (the carrier) is varied in proportion to the second signal (the message or information signal). Modulation is performed at the transmitter side and the reverse operation, demodulation, is performed at the receiving end.

Modulation can be

a) Baseband modulation used for transmitting the signal over short distances, also called line coding.
b) Bandpass modulation used for transmitting the signal over long distances, also called carrier modulation.

Therefore, the successful implementation of wireless communication system depends on the use of modulator & demodulator models. Digital modulation is a process by which digital symbols are transmitted into waveforms that are compatible with the characteristics of the channel.The modulation process converts a baseband signal into a band pass signal compatible with available transmission facilities. There are various digital modulation /demodulation techniques in communication system such as ASK, FSK, PSK etc [1].

The objective of the work is to demonstrate BPSK modulation/demodulation which is a popular modulation technique used in communication industry, because of its better performance in the presence of noise. The experimentation is carried out using simulation of a BPSK Modulator and Demodulator using MATLAB/Simulink environment and Xilinx System Generator.

1.1 BPSK Modulation

In paper [2], BPSK (Binary Phase Shift Keying) signal is used to demonstrate different applications with feasible tool for system generator. BPSK is one of the basic digital modulation techniques. In BPSK modulation, carrier phase is changed in accordance with the information signal in digital form keeping amplitude and frequency of carrier constant thus the modulated signal has two different phases. One phase represents a logical '1' and the other one a logical '0'. It has as a result only two phases of the carrier, at the same frequency, but separated by 180º phase shift. The block diagram of modulator is shown in figure 1.

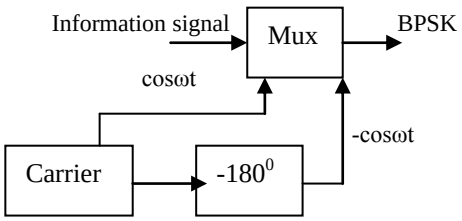


Figure 1. BPSK Modulator [2]

During transmission of '1' the modulated signal remains same as the carrier, with 0 º initial phases, but if '0' is transmitted; the modulated signal changes with 1800. The general form for the BPSK signal as given in equation (1),

$$Si(t) = \{S1(t) = -A\cos(2\pi fct)\}$$ if binary '0'

$$\{S2(t) = +A\cos(2\pi fct)\}$$ if binary '1'

Where,

A = peak amplitude

f_c = carrier frequency (1)

1.2 BPSK Demodulation

As shown in Figure 2. BPSK receiver block contains, noise contaminated BPSK input signal, regenerated carrier signal, balanced modulator and low pass filter. Balanced modulator multiplies BPSK signal and recovery signal and Low pass FIR filer. Since the only possible outputs at balance modulator are the signals cos(ωt) and –cos(ωt), so the product detector's output will be [2].

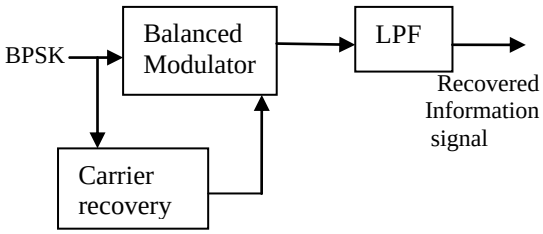


Figure 2. BPSK Demodulator[2]

$$\cos 2(\omega t) = 1/2 + 1/2\cos(2\omega t)$$
$$\cos 2(\omega t) = -1/2 - 1/2\cos(2\omega t) \quad (2)$$

The paper is organised into 7 sections. Section I, describes the basic information about the BPSK modulation and demodulation. Section II, Introduces the channel model. Section III, provides the design flow of BPSK modulator. Section IV & V, describes the XILINX block description & experimentation of the BPSK modulator and demodulator in Simulink by using switch & using system generator. The final two sections, VI & VII, represents the result & conclusions in various mode.

2. AWGN CHANNEL MODEL

The term noise means unwanted electrical signals that are always present in electric systems [3] and the term additive Means added to the signals. AWGN is a channel model in which the only impairment to communication is a linear addition of white noise with a constant spectral density and a Gaussian distribution of amplitude. According to [3] the AWGN channel is a good model for many real time applications like satellite and deep space telemetry. With Binary Phase Shift Keying (BPSK), the binary digits 1 and 0 may be represented by the analog levels $\sqrt{Eb}$ and $-\sqrt{Eb}$ respectively. The system model is as shown in the Figure 3.

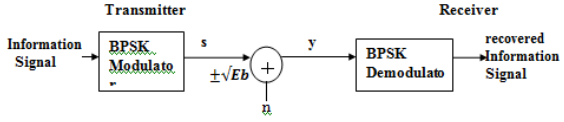


Figure 3. Simplified diagram with BPSK Transmitter Receiver [3]

The transmitted waveform gets corrupted by noise typically referred to as Additive White Gaussian Noise (AWGN).

- **Additive** : As the noise gets 'added' (and not multiplied) to the received signal
- **White** : The spectrum of the noise is flat for all frequencies.
- **Gaussian** : The values of the noise n follows the Gaussian probability distribution function,

The values of the noise 'n' follow the Gaussian probability distribution function p(x) is [3]

$$P(x) = \frac{1}{\sqrt{2\pi\sigma^2}} * e^{-\frac{(x-u)^2}{2\sigma^2}}$$

with $\mu = 0$ and $\sigma^2 = \frac{N_0}{2}$. (3)

In digital modulation the number of bit errors are the number of received bits over a AWGN channel. The BER is the ratio of number of bit in error to the total number of transferred bits.BER is a unit less performance parameter. Therefore the BER for BPSK is given by the following equation.

$$Pb = \frac{1}{2} erfc\left(\sqrt{\frac{Eb}{No}}\right)$$

Where,
Eb/No = signal to noise ratio (4)

The general formula for probability of error or BER of MPSK for AWGN channel is given as,

$$Pb = \frac{1}{m} erfc\sqrt{\left(\frac{mEb}{N0}\right)} \sin\frac{\pi}{M}$$

Where,

$M=2^m$, m = 2,3,4……

For, BPSK m=2 (5)

3. DESIGN FLOW

Figure 4. Shows the design flow of Xilinx ISE [4]. The first step of design flow consists of MATLAB based model using simulink environment. The system generator tool provides VHDL code simulink based model which in turn can be synthesized, simulated, and placed and routed into FPGA. While generating code it automatically creates net list file. This netlist file is used for layout place and route to configuring data on FPGA .

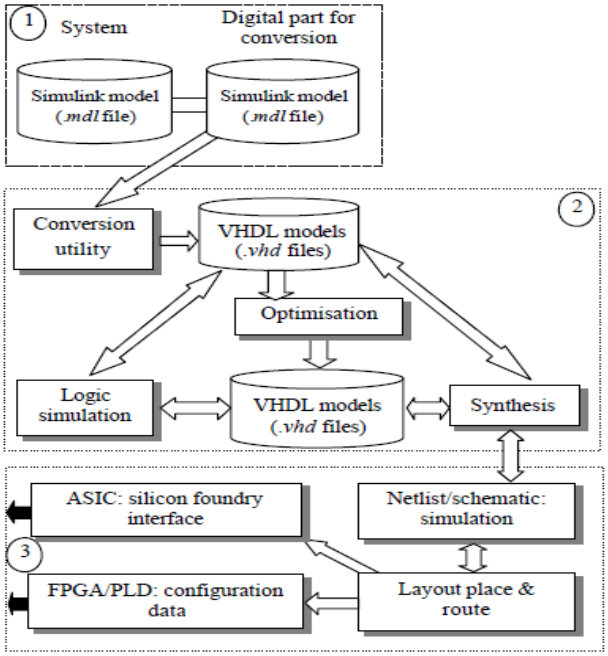


Figure 4. Design flow of Xilinx ISE [4]

4. XILINX BLOCK DESCRIPTION

The Xilinx System Generator, a high-performance design tool, is a part of Simulink. The System Generator elements are grouped as the Xilinx Blockset and available in the Simulink library browser. The simulation was done using Simulink and the components of System Generator. The following tools were necessary for the simulation and implementation:-

4.1 Simulink Blockset

Subsystem: - Subsystem used to create another model within model
Scope: -Scope used to visualize the results
Sine Wave: - It generates sine functions

4.2 System Generator Blockset

Mcode: - It calls a Matlab .m file and executes it inside the simulation.
Gateway In: - It makes an approach to the behaviour of a signal in hardware.
Gateway Out: - It returns an approach of the behaviour of a signal in hardware to the simulation mode
FIR: - It simulates a digital FIR filter, making a call to the MATLAB FDA Tool
System Generator: - It provides control of the system and simulation parameters. It is used to invoke the generated VHDL code
Resource Estimator: - It presents the resources of the device used in the simulation of the circuit like LUT's, IOB's etc.
FDATool: - Filter Design and Analysis tool
Work scope: - Similar type as that of Simulink Scope which shows analog/digital waveform within hardware system.

5. EXPERIMENTATION

5.1 Simulation of BPSK modulator :

Figure 5 shows the simple design of a BPSK modulator in the MATLAB Simulink environment using binary data generator [5].

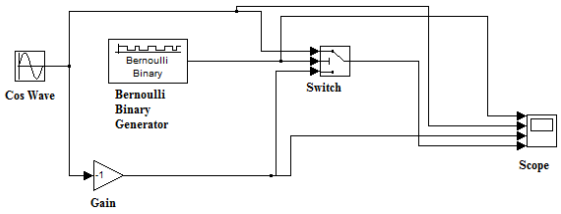


Figure 5. BPSK Modulator using MATLAB Simulink [5]

The Simulink blockset contains the cos wave block which generates a cosine waveform which is used as a carrier. The binary data generator block generates the information signal m(t) i.e modulating signal. The Switch block be a output of information signal, where the first input or the third input depending on the value of the second input. The first and third inputs are data inputs & the second input is the control input and it is specified on the Function Block Parameters for the Switch block. If the second input is '1', the output value will be 00 phase shift or sine waveform, but if the second input is '0' the output will be 1800 phase shift or cosine waveform.

5.2. Simulation of BPSK Demodulator

Figure 6 shows simulation of a BPSK demodulator in the Simulink environment. The Simulink blockset contains:-
The carrier cos wave block generates a cosine waveform and the distorted BPSK transmitted signal generated from AWGN block are multiplied (Mult). The low pass filter FIR separates the continuous signal of + ½ amplitude recovered from the demodulated complex signal and allows selecting the zero frequency signals. Comparators block compares that will provide levels of voltage of ones and zero.

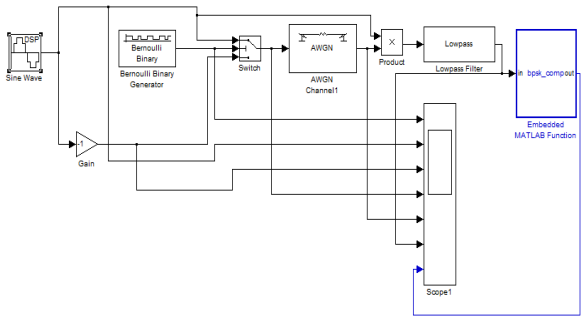


Figure 6 .Simulation of BPSK modulator using embedded MATLAB function

```
Function out = sys_comp_mcode (in)
If
    in > 0
    out = 1;
```

```
else
    out = 0;
end
```

This code, allows us to obtain at the output a voltage level 1, when the input (in) is higher than certain reference voltage in this case 0V and a level voltage 0 when the input (in) is lower than such reference voltage.

5.3 Simulation of BPSK modulator using System Generator :

Implementation of BPSK modulator using System generator is illustrated in figure 7 [5], which contains similar blocks that of Simulink blocks. Additional blocks such as Gateway In and Gateway Out are for an approach of the behaviour of a signal in hardware to the simulation mode. The system generator block set contains following types of token:-

System Generator: - It is used to invoke the generated VHDL code

Resource Estimator: - It gives device utilization summary of simulated model for the hardware, like LUT's, IOB's etc.

FDA Tool: - Filter Design and Analysis tool

Work scope: - which shows analog/digital waveform within hardware system

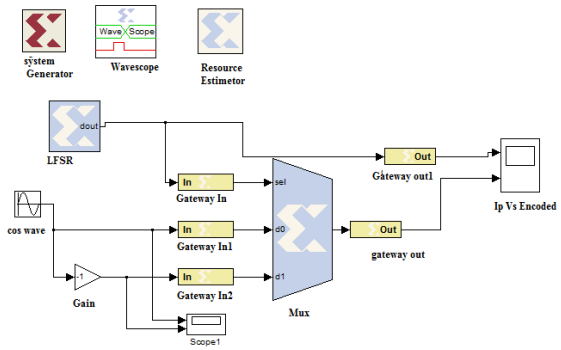


Figure 7. BPSK Modulator in System Generator [5]

5.4 Simulation of BPSK Demodulator using System Generator:

Figure 8 shows simulation of BPSK demodulation using Simulink filter design tool. The Simulink based filter block is implemented by means of system generator block with help of FDA tool..in this diagram the matched filter is used to eliminate the intersymbol interference. The main data path includes a matched filter is root raised cosine filter (RRC).

The RRC filter is used to maximize the dynamic range of the signal magnitude & maintain an optimal output sample level for symbol decision [7].

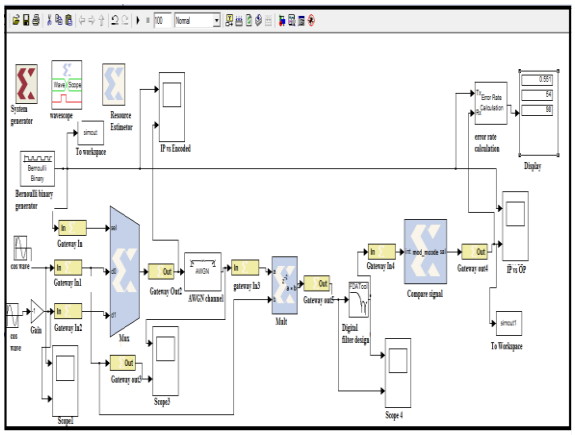


Figure 8. BPSK Demodulator in system Generator

6. RESULTS

The figure 9 illustrate the waveform generated by the corresponding blocks by using a carrier signal or modulating signal from simulation model by figure 2.

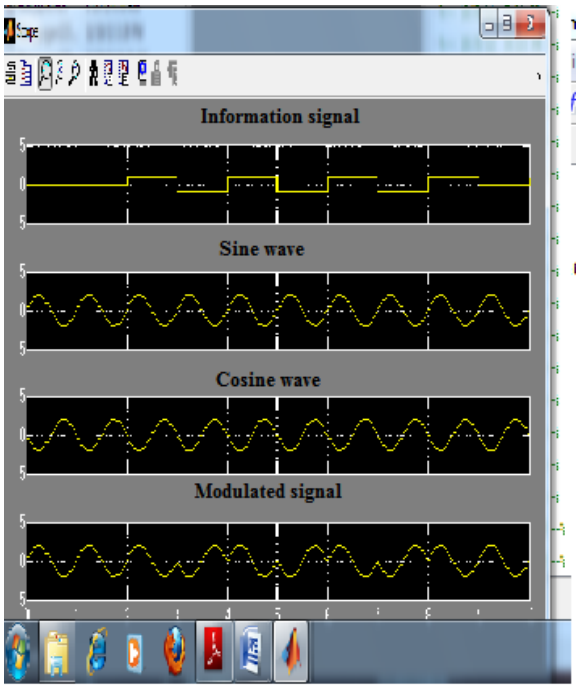


Figure 9. The waveforms on the scope (a)Sine (b) Cosine (c) Modulating signal (d) Demodulated signal [5].

Figure 10 shows the waveform generated by the BPSK demodulator using filter. Fig.10(a) & (b) shows the carrier wave having frequency 1kHz & recovered phase shift with '0' & '180' degree, to the BPSK modulator. Fig.10(c),(d),(e) & (f) shows the AWGN output with SNR, multiplied output , & binary data which are generated by using filter.

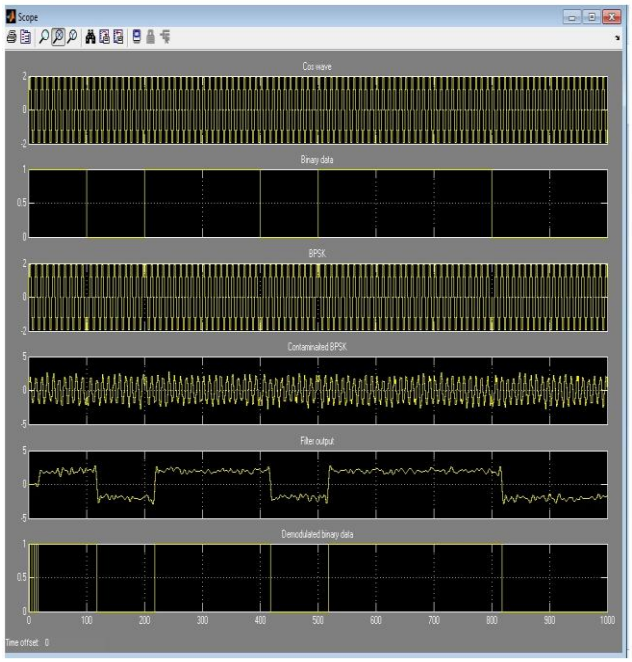


Figure 10. BPSK modulator waveform on the scope

The figure 11 shows the BPSK modulation in scope with binary data generator, and modulated data output. These simulation results are obtained from model shown in figure 4.

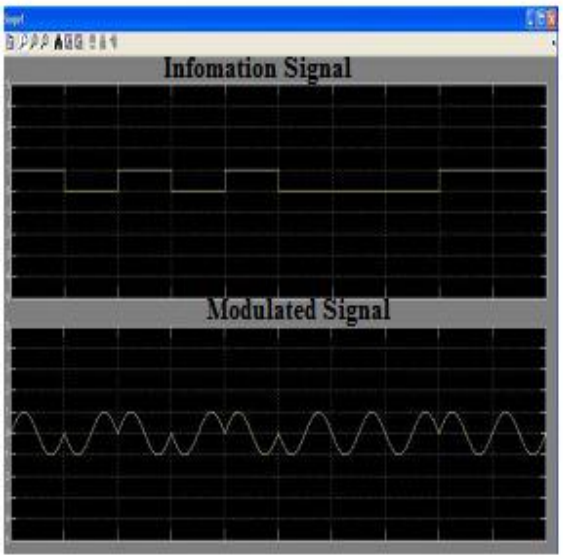


Figure 11. BPSK modulator waveform on the scope using system generator

The waveform of BPSK demodulator on wave-scope which generates the recovered binary data at 31.250 KHz carrier frequency and RRC filter to eliminate the intersymbol interference using filter design tool(FDA), and AWGN channel having 10 db of SNR is shown in Figure 12 .

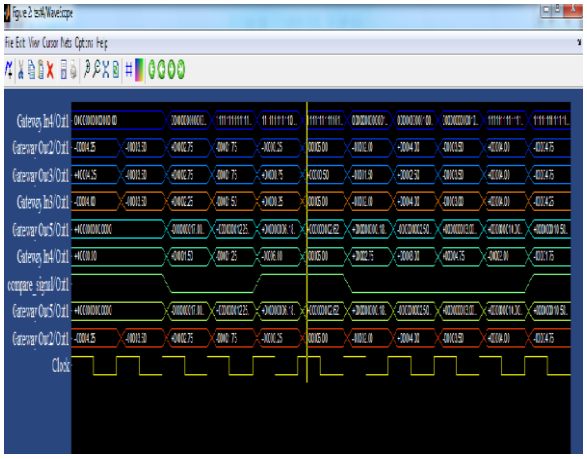


Figure 12. BPSK demodulator waveform on wavescope

Figure 13 & table.1 shows the RTL schematic and resource estimator generation of BPSK demodulator using System generator.

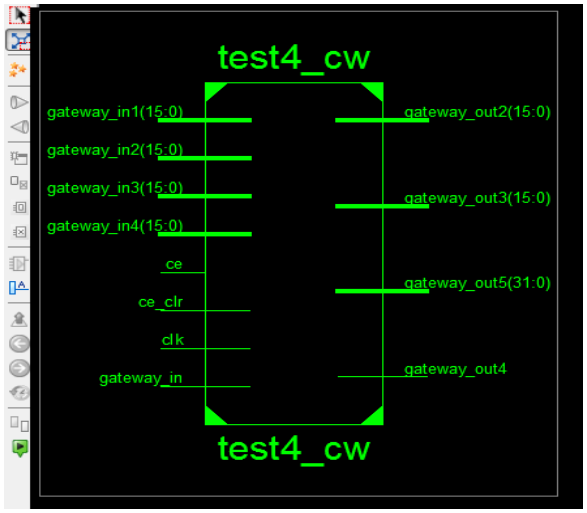
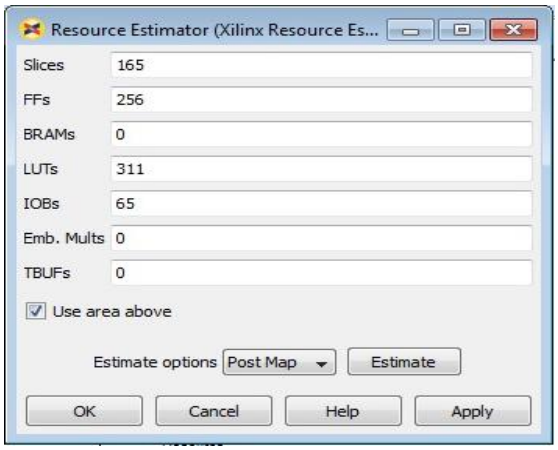


Figure 13. RTL Schematic of BPSK Demodulator

Table 1. Resource Estimation of BPSK Demodulator



The device utilization summery of BPSK modulator and demodulator using ISE 12.1 simulator is discussed in table 2. Target device selected for reference is SPARTAN III with clock period of 20ns.

Table 2. Device utilization summery of BPSK Demodulator
(Target Device- Spartan 3 xc3s400, Xilinx ISE design Suite-12.1)

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	32	7,168	1%
Number of 4 input LUTs	21	7,168	1%
Number of occupied Slices	41	3,584	1%
Number of Slices containing only related logic	41	41	100%
Number of Slices containing unrelated logic	0	41	0%
Total Number of 4 input LUTs	22	7,168	1%
Number used as logic	21		
Number used as a route-thru	1		
Number of bonded IOBs	131	141	92%
Number of MULT18X18s	1	16	6%
Number of BUFGMUXs	1	8	12%
Average Fanout of Non-Clock Nets	1.34		

Figure 14. shows the BER Vs SNR graph for BPSK modem is evaluated the performance parameter using AWGN channel. Simulation graph shows that, when SNR increases BER decreases.

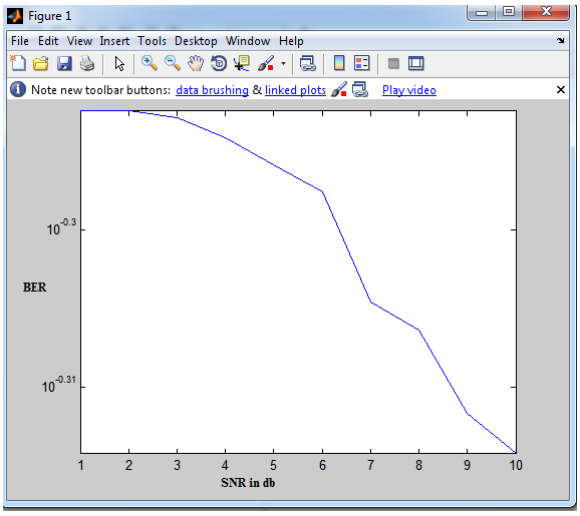


Figure 14. BER Performance for BPSK modem

7. CONCLUSION AND FUTER SCOPE

7.1 Conclusion

The work demonstrates the concept of hardware accelerator for communication application. Performance of BPSK modulator and demodulator has been simulated using switch & system generator is a tool of Xilinx ISE 12.1. Simulink tools offer a simplified environment for the simulation of communication systems. If "1" would be transmitted, the modulated signal remained same as the carrier, but if "0" would be transmitted, the modulated signal is changing with a 180º phase. BPSK modulation is a popular modulation technique because of its better error performance. It is widely used in Deep Space Telemetry, Zig-Bee & low rate personal area network (LR-PAN) i.e in wireless communication. Simulated results from both the environments as well as FPGA device utilization summary and corresponding schematic are shown in the results section. Finally the the paper is concerned with the performance evaluation of the BPSK modulated system using AWGN channel and it is found that the bit error rate of BPSK is quiet low as compared to other modulation techniques such as DPSK, ASK, FSK [4].

7.2 Future Scope

The next goal of this work is to implement the BPSK modulator using FPGA device and to use it for applications.

8. REFERENCES

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