Hardware Timestamping for Image Acquisition System Based on FlexRIO and IEEE 1588 v2 Standard

S. Esquembri, D. Sanz, E. Barrera, M. Ruiz, A. Bustos, J. Vega, R. Castro

Extended Abstract– Current fusion devices consist of multiple diagnostics and hundreds or even thousands of signals. This situation forces on multiple occasions to use distributed data acquisition systems as the best approach. In this type of distributed systems, one of the most important issues is the synchronization between signals, so that it is possible to have a temporal correlation as accurate as possible between the acquired samples of all channels. In last decades, many fusion devices use different types of video cameras to provide inside views of the vessel during operations and to monitor plasma behavior. The synchronization between each video frame and the rest of the different signals acquired from any other diagnostics is essential in order to know correctly the plasma evolution, since it is possible to analyze jointly all the information having accurate knowledge of their temporal correlation. The developed system described in this paper allows timestamping image frames in a real-time acquisition and processing system using 1588 clock distribution. The system has been implemented using FPGA based devices together with a 1588 synchronized timing card (see Fig.1).

The solution is based on a previous system [1] that allows image acquisition and real-time image processing based on PXIe technology. This architecture is fully compatible with the ITER Fast Controllers [2] and offers integration with EPICS to control and monitor the entire system. However, this set-up is not able to timestamp the frames acquired since the frame grabber module does not present any type of timing input (IRIG-B, GPS, PTP). To solve this lack, an IEEE1588 PXI timing device its used to provide an accurate way to synchronize distributed data acquisition systems using the Precision Time Protocol (PTP) IEEE 1588 2008 standard. This local timing device can be connected to a master clock device for global synchronization. The timing device has a buffer timestamp for each PXI trigger line and requires that a software application assigns each frame the corresponding timestamp. The previous action is critical and cannot be achieved if the frame rate is high. To solve this problem, it has been designed a solution that distributes the clock from the IEEE 1588 timing card to all FlexRIO devices [3]. This solution uses two PXI trigger lines that provide the capacity to assign timestamps to every frame acquired and register events by hardware in a deterministic way. The system provides a solution for timestamping frames to synchronize them with the rest of the different signals.
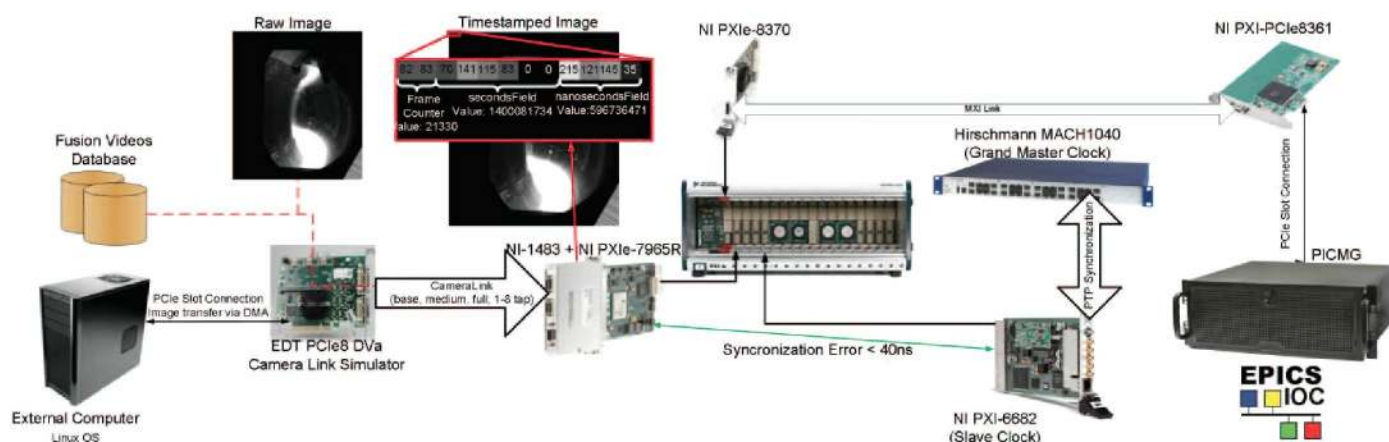
Figure 1. System architecture

[1] E. Barrera, M. Ruiz, D. Sanz, J. Vega, R. Castro, E. Juárez, R. Salvador. *Test bed for real-time image acquisition and processing systems based on FlexRIO, CameraLink, and EPICS*, Fusion Eng. Des. (2014), http://dx.doi.org/10.1016/j.fusengdes.2014.02.010

[2] M. Ruiz, J. Vega, R. Castro, D. Sanz, J. M. Lopez, G. de Arcas, E. Barrera, J. Nieto, B. Goncalves, J. Sousa, B. Carvalho, N. Utzel and P. Makijarvi, "ITER Fast Plant System Controller prototype based on PXIe platform," *Fusion Eng. Des.*, vol. 87, pp. 2030-2035, DEC, 2012.

[3] D. Sanz, M. Ruiz, J.M. Lopez, R. Castro, J. Vega, E. Barrera. *IEEE1588 Clock Distribution for FlexRIO Devices in PXIe Platforms*. Fusion Eng. Des. (2014), Article in press. http://dx.doi.org/ 10.1016/j.fusengdes. 2014.02.029