HARMONIC ANALYSIS OF A STATIC VAR COMPENSATED MIXED LOAD SYSTEM

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ABSTRACT

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COMPENSATED MIXED LOAD SYSTEM

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As power electronic based controllers and loads become more prevalent in power systems, there is a growing concern about how the harmonics generated by these controllers and loads affect the power quality of the system. One widely used power electronic based load is the Variable Frequency Drive (VFDs) used to vary the speed of an induction motor; whereas a common example of a power electronic based controller used in power systems is the Static VAR Compensator (SVC) for improving a system's power factor. In this thesis, the harmonic content and overall performance of a system including both a VFD and a SVC will be studied and analyzed. Specifically, the cases of no compensation, static capacitor compensation, and power electronic based static VAR compensation are examined.

A small-scale model of a system for study was constructed in lab. Several cases were then performed and tested to simulate a system which contained both fixed and power electronic based harmonic generating loads. The performance of each case was

determined by total harmonic current and voltage distortions, true power factor, and RMS current levels at different points in the system.

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Table of Contents

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1 – INTRODUCTION

1.1 Background

In any industrial application, the primary challenge is how to maximize the output production while minimizing the input costs. From a power perspective, this means accomplishing the required output task at the minimum input power and current requirements. In induction motor applications, the use of power factor correction and variable frequency drives (VFDs) are two methods to maximize the efficiency of the system. By providing power factor support to the system the input current is minimized for the same amount of real power. This can result in fewer line losses and smaller, and thereby cheaper, circuit breakers. With the advent of power electronics, flexible AC transmission systems (FACTS) now provide a means to dynamically adjust the power factor as the load requirements of the system change. Another product of power electronics, VFDs, allow for the speed of the motor to easily be changed to ensure the motor is running at the optimal level for the required task.

The downside is VFDs and FACTS are based on switching power electronics and thereby produce harmonics which can be dangerous in power systems. To protect against this the Institute of Electrical Engineers (IEEE) has created a standard, IEEE Std 519-1992, which outlines the recommended practices and requirements for harmonics in a power system. Specifically, the standard sets the acceptable distortion limits a consumer can reflect back to the utility.

1.2 Thesis Scope

This thesis examines the harmonics and overall system effects of applying static VAR compensation to a node which contains VFD controlled and fixed speed induction motor loads. In general, it is not practical to apply conventional capacitive power factor correction to a VFD load. Since a VFD draws current in phase with the voltage, any power factor correction applied to a VFD should be in the form of a line filter to mitigate its harmonics and reduce its distortion power factor [1]. However, this project attempts to look at the more universal situation of providing power factor support at a single node which supplies many different loads. In this case the specific loads connected to the node may be unknown, such as a utility, or the number of loads may be enough so that it is not practical to provide individual power factor correction.

The goal of the thesis will then be to see how the harmonics generated by the VFD interact with the system when the VFD is connected to a node injected with capacitive VAR support. Of specific interest will be the case when static VAR compensation (SVC) is used. Since the SVC contains thyristors, which turn on and off to chop the input signal, the SVC will also produce harmonics. By comparing the results of an uncompensated, capacitively compensated, and a static VAR compensated system the thesis will determine whether harmonic cancellation occurs between the SVC and VFD or if the two simply add to a point where it is not practical to use a SVC in a system containing a VFD. As a minimum requirement for all cases, the harmonics reflected to the source will be compared against the guidelines set forth in the IEEE Std 519-1992. The cost implications of the harmonics, which include energy loss, equipment aging and

misoperation, will also be discussed. Additional conclusions will be drawn about the effectiveness of the compensation methods and efficiency of the system.

1.3 Thesis Organization

Chapter 1 of the report introduces the background for why VFDs and FACTS are used. An overview of the scope of the thesis is then presented. Justification is made for why classical VAR power factor correction would be used at a node containing a VFD. Finally, the basis for comparison between the different cases is discussed.

Chapter 2 begins with a background of what harmonics are and how they are created. Their effect on power quality is then discussed with special consideration given to the consequences of harmonics on rotating machines, transformers and capacitors. Different methods of mitigating harmonics are also presented. True, displacement, and distortion power factors are also defined and discussed. Time is spent to outline the difference between distortion power, reactive power and their roles on power factor as a whole. Once the reader has been given a detailed explanation of power factor, methods for improving it are offered.

Chapter 3 focuses on power electronic equipment as related to the thesis. An overview of VFDs is given by discussing their purpose, how they work, and the type of harmonics they generate. Since thyristors play a significant indirect role in this thesis, their background and the principles behind their operation are discussed. Next FACTs are talked about in general. The difference between shunt and series compensation is outlined and mention is made of popular FACTS such as STATCOM and UPFC. The static VAR compensator is then discussed in detail. Equations and derivations are given

for the susceptance, current, and extinction angle of an SVC. Harmonics generated by the SVC are also discussed. Lastly, the Enerpro thyristor firing board used in this experiment is detailed.

Chapter 4 gives a complete overview of the lab setup and procedure. Each case is outlined specifically and justification is made for the loading points at which data was collected. For both the capacitive and SVC cases, reasoning for the size of the equipment used is given and supported. An equipment list is supplied listing all equipment used with their corresponding model number and ratings. The chapter concludes with pictures of the actual lab setup.

Chapter 5 is the analysis portion of the thesis. It begins with a dialogue on possible causes of error in the data collection but concludes that these inaccuracies are minor. The harmonic current data is then presented both in TDDi% and THDi% as taken at the source. TDDi% data is compared against the IEEE Std 519-1992 to see if harmonic levels meet the basic requirements. The 5^{th} and 7^{th} individual harmonics are compared at the source location to see if harmonic cancellation between the VFD and SVC occur. Intersystem harmonics are then analyzed by looking at the K-Factor for the secondary of the transformer and current distortion at the motor terminals. Voltage distortion at the source is also explored by comparing the THDv% against IEEE 519-1992 requirements. Once the harmonics have been analyzed, the true, displacement, and distortion power factors are looked at for each case. The analysis ends with a look at the difference in total RMS current for the source and its impact on power and cost savings.

Chapter 6 attempts to summarize the findings of Chapter 5 and draw conclusions about them. The differences significant differences for each case are discussed succinctly

and quantified in terms of their real world implications. A conclusion is reached about which case is best suited for the test system used. How these conclusions apply to larger power systems is discussed and scenarios are given for when each compensation method would be best utilized. Finally, ideas are given for potential follow ups to this study.

CHAPTER 2 – HARMONICS AND POWER FACTOR

2.1 Harmonics

Harmonics were first defined with respect to music, where it referred to the vibration of a string or column of air at a multiple of its base frequency [2]. Applied to electric power systems, harmonics describe the content of a voltage or current signal whose frequency is an integer multiple of the system frequency. In the United States the standard power system frequency is 60Hz, meaning that harmonics occur at 120Hz, 180Hz, 240Hz…etc. To illustrate this Figure 2.1 shows a fundamental sine wave of 60Hz and its 3rd, 5th, and 7th harmonics. The harmonics are shown with typical amplitudes that are 1/nth that of the fundamental, where n is the order of the harmonic [2].

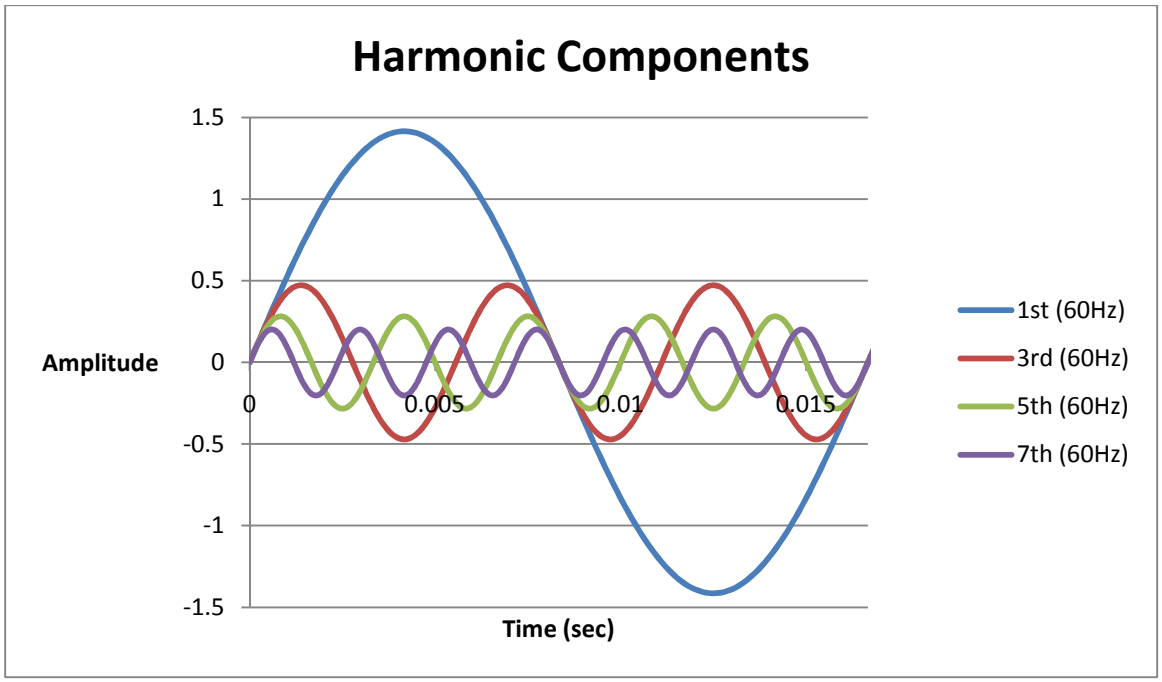

Figure 2.1 - Example of Individual Harmonic Components

When summed together the individual harmonics of Figure 2.1 form a new waveform which is no longer a pure sinusoid but the compilation of harmonics that are multiples of the original frequency. This can be seen in Figure 2.2, where the 3rd, 5th and 7th harmonics from Figure 2.1 were added to the fundamental wave.

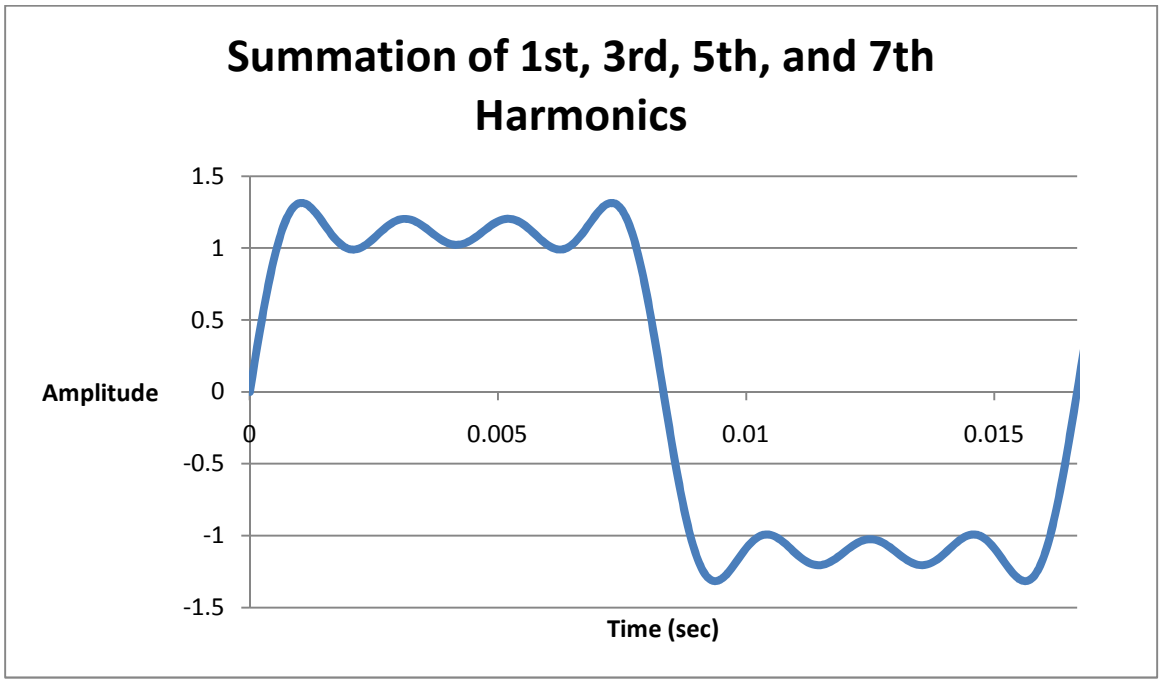

Figure 2.2 - Example of Harmonic Waveform Summation

Using the Fourier Transform, $(f) = \int_{-\infty}^{\infty} x(t)e^{-j2\pi ft}dt$, a continuous periodic signal from the time domain can be converted into discrete frequency components in the frequency domain [2]. The PowerSight analyzer has the ability to display both voltage and current waveforms in the time and frequency domains. As an example, Figure 2.3 shows the time domain of the current into the VFD at full load and no compensation, while Figure 2.4 shows the corresponding frequency domain representation.

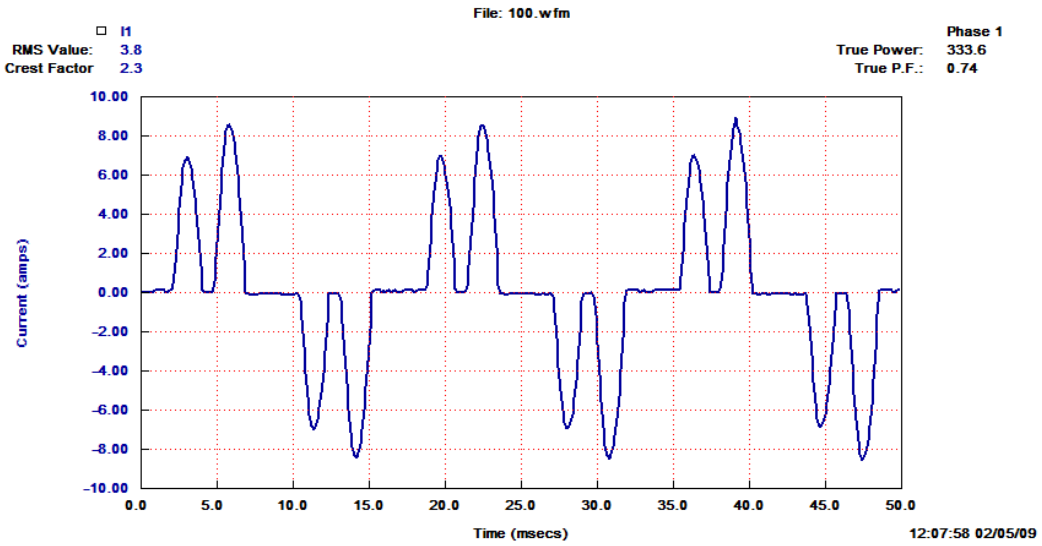

Figure 2.3 - PowerSight Full Load VFD Current vs. Time for No Compensation

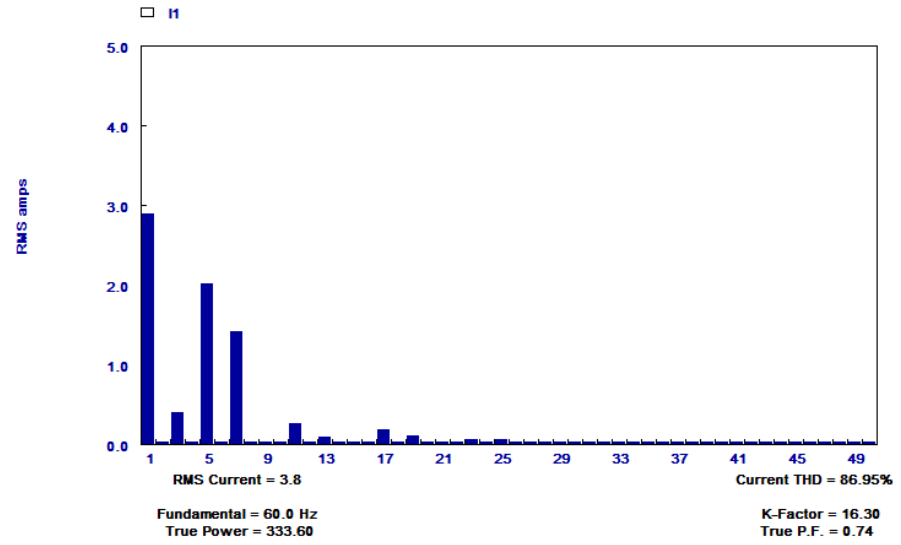

Figure 2.4 - PowerSight Full Load VFD Current Frequency Spectrum

In Figure 2.3, the double peaks are the result of the input current to the VFD being stopped by the commutation of the diodes at the input bridge rectifier. The inner workings of the VFD are explained in greater detail in Chapter 3. The frequency spectrum example of Figure 2.4 shows that the VFD distortion is concentrated at the 5^{th} and 7^{th} harmonics.

For a standard three phase power system, the phasors are said to follow the ABC positive sequence. If the rotation of the positive sequence is observed the A phase would appear first, followed by phase B, and finally phase C with 120° between each phase. Conversely, the phasors are said to follow the negative sequence if phase A appears first, followed by phase C and finally phase B. For the zero sequence, the three phases appear at the same time as there is zero phase displacement between them [3]. When harmonics are present in a balanced system, it can be shown that the phase sequence of a current or voltage is dependent on its harmonic order. For a positive sequence system to voltages as related to the harmonic order are shown in equations 2.1-2.3.

$$V_{ah(t)} = \sqrt{2}V_h \sin(h\omega_o t + \theta_h) \tag{2.1}$$

$$V_{bh(t)} = \sqrt{2}V_h \sin(h\omega_o t - 2h\frac{\pi}{3} + \theta_h) \tag{2.2}$$

$$V_{ch(t)} = \sqrt{2}V_h \sin(h\omega_o t + 2h\frac{\pi}{3} + \theta_h) \tag{2.3}$$

From the equations 2.1-2.3 it can be seen that positive sequence components are of the harmonic order (h=1,4,7,10…), while negative sequence components take the form (h=2,5,8,11…). The zero-sequence components then correspond to the triplen harmonics (h=3,6,9,12…) [4].

The harmonics in a system are usually quantified in terms of the Total Harmonic Distortion (THD) and the Total Demand Distortion (TDD). These harmonic indices are defined, for either voltage or current, by the IEEE as [5] [6]:

$$THD = \frac{\sqrt{\sum_{h=2}^{50} V_h^2}}{V_1} * 100\% \quad (2.4)$$

$$TDD = \frac{\sqrt{\sum_{h=2}^{50} I^2 h}}{I_{rated}} * 100\% \quad (2.5)$$

The two indices are identical except THD compares the harmonic content to the fundamental, where as TDD compares it to the rated value.

2.2 Power Quality

In the ideal balanced power network, voltage and current are supplied at a single frequency which is constant throughout the system and the three phases follow the positive sequence. However, in reality these conditions are never perfectly realized even in the best conditions. While achieving this ideal has been a concern of power engineers since the conception of alternating current, the rapid increase in non-linear loads over the last 30 years has drawn increased attention to the field of power quality.

One type of non-linear load is a device which interrupts the flow of current from the source, often by some switching mechanism, thereby distorting the original current waveform. Before the advent of the semiconductor, non-linear loads typically took the form of large arc furnaces and converters common only in industrial and utility applications [2]. However, with the introduction of power electronics the number of harmonic sources has grown dramatically to include common household items like

switch-mode power supplies and compact fluorescent lamps, as well as new industrial devices like FACTS and VFDs. The result is that harmonics now need to be considered in any major electrical design.

Consequences of harmonics vary depending on the type of equipment and load they are subjected to. The effects of harmonics on rotating machines, transformers and power factor correction capacitors will be explained further since this equipment is predominantly featured in this thesis.

Rotating Machines: In rotating machinery, harmonics can cause increased heating, power losses, audible noise, and pulsating or reduced torque. Both the rotor and stator experience additional iron and copper losses due to each harmonic component. These losses are often greater than those associated with the fundamental frequency because of eddy currents and the skin effect which are proportional to the square of the frequency [2]. An eddy current occurs when a conductor is exposed to a changing magnetic field and results in circulating eddies of current within the conductor that induce magnetic fields opposing the original field. The skin effect states that electrons increasingly gather near the surface of a conductor as the frequency of the current grows, thereby increasing the resistance of the conductor. Besides lowering the overall efficiency of the motor these loses produce extra heat which can shorten the overall life span of the motor. Even normally encountered acceptable harmonic content causes harmonic heating which can reduce typical performance to 90-95% of what's expected when a pure sinusoidal voltage is applied [5]. Of significant concern is the flow of harmonic current in the rotor. As mentioned in section 2.1, harmonics can have a positive, negative, or zero sequence orientation. When these harmonics appear in the

stator they produce a magnetomotive force in the air gap and a corresponding rotor current. Depending on the harmonic order, the mmf force generated in the air gap will have either a forward or backward rotation with respect to the rotor. Positive sequence harmonics will rotate forward while the negative sequence will rotate backwards. The result of this is that pairs of harmonics in the stator combine to produce a single harmonic occurring at multiples of 6 of the fundamental frequency [7]. Besides contributing to heating, these currents can result in torque pulsations leading to shaft fatigue and increased aging of associated mechanical parts [5].

Transformers: As with rotating machines, one of the main concerns of harmonics in transformers is increased heating. Current harmonics cause increased copper and stray flux loss while voltage harmonics contribute to increased iron losses [5]. Since these losses increase with frequency the expected amount of harmonic content sent through the transformer must be accounted for in the design process. A common design practice is to size the transformer based on a measurement called K-Factor, which places additional weight on the frequency of the current. Where K-factor is defined with per-unit values as:

$$\text{K-Factor} = \sum I_h^2 h^2 \tag{2.6}$$

Once the K-Factor is found a specifically designed K-Factor transformer may be used to handle the harmonic content. A K-Factor transformer has been built to account for additional heating from harmonics by including an oversized neutral and multiple conductors for the coil. Transformers are made for K sizes ranging from 1-50, with 1, 4, 9, 13, 20, 40, and 50 being the most common. A K-Factor transformer off 1 is used for linear loads. For most harmonic applications a K-Factor transformer of 13 is sufficient.

Using the K-Factor, a typical derating curve for oversizing a normal transformer is given in Figure 2.5 [8]. In addition to heating of the transformer core and windings the transformer neutral must also account for the harmonics. In a wye connected transformer harmonics sum in the neutral. As a result systems containing significant harmonic content must oversize their neutral cable to handle the additional current.

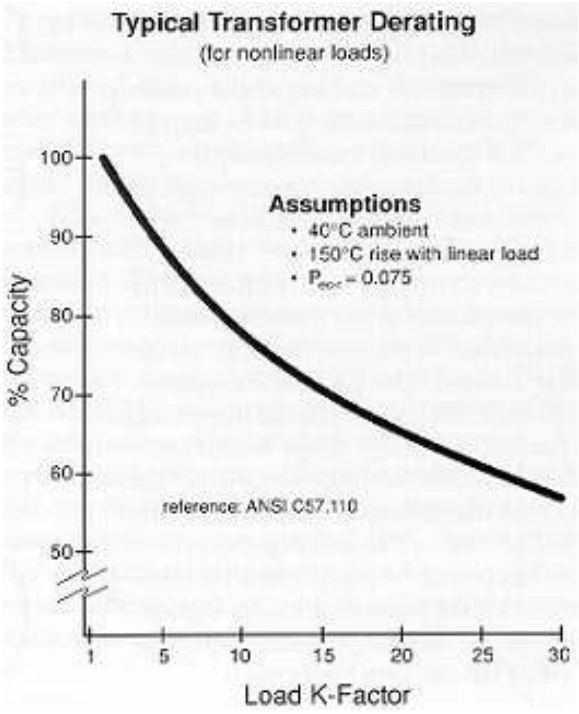

Figure 2.5 - Typical Transformer Derating Graph

Capacitors: Capacitors placed in networks containing high harmonics are susceptible to system resonance and current overload. Since the impedance of a capacitor is inversely related to frequency, a capacitor is a current sink for increasing harmonic frequencies. Therefore, care must be taken to ensure that all system capacitors are rated

high enough to withstand the increased current due to harmonics. Capacitors placed in parallel with harmonic sources should be designed to avoid parallel resonance. The parallel resonant frequency is created by the combination of all parallel capacitance and the system's short-circuit reactance. It is defined to be [4]:

$$f_r = \frac{1}{2\pi\sqrt{LC}} = f_1\sqrt{\frac{1000*S_{sc}}{Q_{cap}}} \quad (2.7)$$

Where f_r and f_1 are the resonant and fundamental frequencies respectively. S_{sc} and Q_{cap} are the short-circuit apparent power in MVA and the reactive power rating of the capacitors in kVAR. If the resonant frequency corresponds to a frequency generated by a harmonic source, resonance will occur causing excessive voltages and currents that are likely to damage the capacitors and other equipment. In general a small current flowing into the system from the bus while high harmonic voltages are present indicates resonance within the system [2].

2.3 Solutions

Harmonics can be mitigated through a combination of shunt and series filters. Selected components may be protected from harmonics by series inductance and capacitance tuned to appear as a high impedance path to a specific harmonic order. In the case of VFD's, series line reactors are often specified by the manufacturer to reduce the harmonics created by the drive [9]. However, since non-linear loads require certain harmonic components, series filtering is usually not the preferred method of reducing source harmonics. Instead the source is usually protected by a combination of shunt filters and isolation transformers. A shunt filter attempts to provide a low impedance

path to ground for the harmonics to redirect them away from the source [2]. Parallel resonant L-C branches are often tuned to appear as a short to specific frequencies, thereby giving them a path to ground and filtering that harmonic out of the system. Delta-wye isolation transformers are an effective method to prevent triplen harmonics from appearing at the source, since in a balanced system zero sequence components circulate in a delta connection but cannot enter the line side. Alternatively, when multiple harmonic sources are in parallel, some may be connected to the common bus through phase changing transformers to increase the likelihood of harmonic cancellation [4].

2.4 True, Displacement, and Distortion Power Factors

True power factor, often simply referred to as power factor, is the ratio of usable, real average power to apparent power. Mathematically this relationship is expressed as:

$$pf = \frac{P}{S} = \frac{P}{EI} \tag{2.8}$$

Where P is the average power in watts, S is the apparent power in voltamperes, and E and I are rms voltages and currents respectively. The power factor is an important ratio because it expresses how much of the voltage and current go toward usable power which produces a tangible result. For example, for the same amount of output power and input voltage a 0.5 power factor will require twice the RMS current as a unity power factor would. This difference in RMS current will result in higher power losses and larger

more expensive cabling and equipment. Due to the costs of larger equipment utilities often charge industrial and commercial customers a fee or higher rate [4].

A non-unity power factor occurs as the result of the voltage and current being out of phase with each other or when the voltage and current are distorted so they no longer have the same waveform [10]. The displacement power factor is a measure of the difference between the voltage and current phase angles and defined as:

$$pf_{disp} = \cos(\theta_v - \theta_i) \tag{2.9}$$

The displacement power factor is a result of the energy stored in inductive and capacitive components. Unlike a resistor, which simply dissipates energy, inductors and capacitors transfer energy between the source and their magnetic fields. For ideal inductors and capacitors, the energy transferred has a time averaged value of zero so that no real power is consumed by the components. While no power is used, these magnetic components reduce the amount of available real power by displacing the current by 90° with respect to the voltage. As a result, reactive power is defined as the component of the apparent power which is due to 90° out of phase current components. In equation form reactive power, Q, is given in voltamperes reactive (VARs) as:

$$Q = V_{rms}\, I_{1rms} \sin(\theta_v - \theta_I) \tag{2.10}$$

Capacitors result in the current leading the voltage by 90°, while inductors cause it to lag by 90°. Therefore, the power factor is said to be lagging for inductive loads and leading

for capacitive loads. It is easily seen in equation 2.10 that when the current lags the voltage Q will be negative and for a leading current Q will be positive. As a result, inductors are often thought of as absorbing reactive power, while capacitors are considered to supply it.

The other component of power factor, is the distortion factor, which is a result of current distortion caused by non-linear loads, such as VFDs and FACTS. The distortion power factor, is shown in equation 2.11, as the ratio of fundamental current to total RMS current.

$$pf_{dist} = \frac{I_{1\,rms}}{I_{total\,rms}} \tag{2.11}$$

In a circuit free of harmonics, all of the RMS current will occur at the fundamental frequency, making the distortion factor equal one. Like displacement factor, distortion reduces the available real power from a given apparent power. This reduction is quantified by distortion power and shown in equation 2.12 [11]. While both distortion and reactive power are measured in VARs, to avoid confusion it is useful to refer to them as distortion voltamperes and reactive voltamperes respectively.

$$Distortion\ Power = D = V_{rms}\sqrt{\sum_{n=2}^{\infty} I_{rms}^2} = V_{rms}\sqrt{I_{total}^2 - I_1^2} \tag{2.12}$$

Distortion power is the result of cross frequency voltages and currents. Like reactive power, it has a time average of zero and therefore increases the apparent power while making no contribution to the real power. The relationship between the different types of

power is often represented by the triangle shown in Figure 2.6, where the assumption is made that the voltage is undistorted.

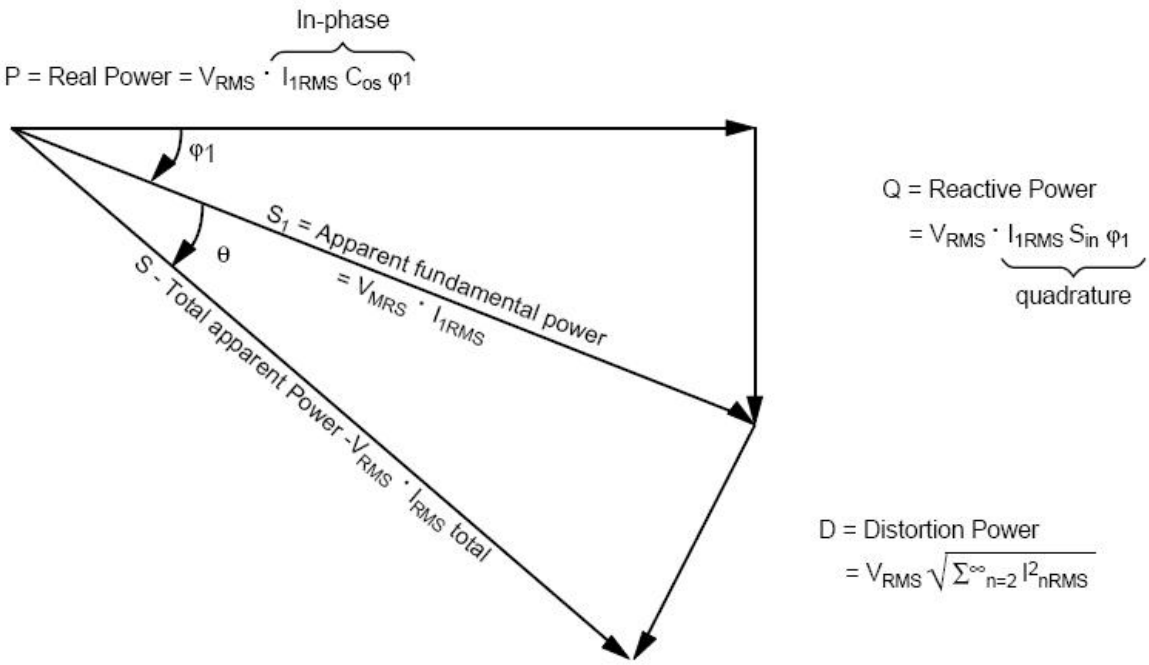

Figure 2.6 - Power Factor Triangle [12]

In the power factor triangle, φ_1 is the displacement angle between the fundamental voltage and current. The distortion angle is shown in the triangle as θ and found as the inverse cosine of the distortion power factor. From the relationships of the power triangle we see that the true power factor, defined in equation 2.8 as $pf = \frac{p}{s}$ can also be found as:

$$pf = pf_{disp} * pf_{dist} \tag{2.13}$$

Since neither the distortion or displacement power factor can be greater than one, the true power factor must also be at most one. Therefore, to achieve a unity true power factor, where the apparent power equals the real power, the displacement and distortion power factors must both be equal to one. In such a case all the RMS current is contained in the fundamental frequency and there is no phase difference between the voltage and current.

2.5 Power Factor Correction

A completely resistive linear system, one which naturally has a unity power factor, is not common in real world applications. As a result, nearly every power system needs some form of power factor correction to run most efficiently. To increase the true power factor, equation 2.13 showed that the displacement or the distortion power factor must be improved. Since the methods of correcting displacement and distortion are different, and sometimes conflicting, it is important to identify which type of correction will provide the greatest benefit to the system.

The most common method of displacement power factor correction is to place a parallel compensation branch at the point of the source. Since the large majority of loads are inductive, motors and transformers for example, most power systems will operate at a lagging power factor. To correct for a lagging power factor, capacitors are sized to provide VARs equal to the amount drawn by the system. The reactive power provided by a capacitor is shown in equation 2.14.

$$Q = \frac{V_{rms}^2}{X} = V_{rms}^2 * j\omega C \tag{2.14}$$

When parallel compensation is used in a non-linear system containing harmonics only the VARs resulting from phase lag may be compensated for by the parallel capacitance. It is important to remember that most power meters display the total VARs as the sum of both the reactive and distortion voltamperes. Despite this, only the reactive voltamperes can be compensated for by capacitance. This means that in the presence of harmonics, even if the system has been compensated so that the current and voltage are perfectly in phase, the source will still provide VARs to the system. The number of VARs which can't be corrected for by parallel compensation is equal to the distortion power given in equation 2.12.

Distortion power factor is improved by increasing the amount of fundamental current with respect to the total RMS current. This can be done by any method used to mitigate harmonics as discussed in section 2.4. Common solutions include line filters, resonant circuits, harmonic injection, and transformer cancellation.

CHAPTER 3 - POWER ELECTRONIC DEVICES

3.1 Overview of VFDs

Studies have shown that induction motors constitute half of the total electrical loads for most power systems [13]. Induction motors, specifically the squirrel cage rotor, are widely used thanks to their low maintenance, low cost and high power to weight ratios. However, these benefits come at the expense of speed flexibility. For an induction motor the speed is determined by the number of poles and the frequency of the voltage applied, as shown in equation 3.1.

$$\text{synchronous speed (rpm)} = 120 * \frac{f\ (hz)}{p} \tag{3.1}$$

Since the poles are a fixed physical parameter of the motor the most feasible way to adjust a motor's speed is to change the frequency of the applied voltage.

The variable frequency drive (VFD), is a power electronic device which is able to provide motor speed control by quickly and efficiently adjusting the frequency of the line voltage at the motors terminals. To change the frequency of the input voltage a VFD consists of three different stages, shown in Figure 3.1.

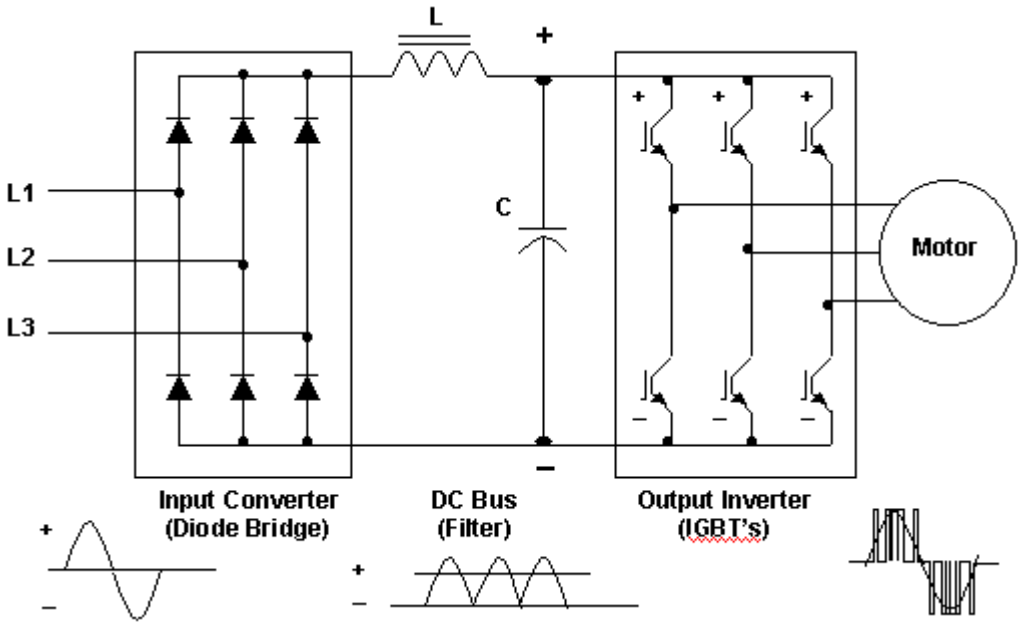

Figure 3.1 - VFD Block Diagram [14]

In a three phase VFD, the first stage typically uses a six diode full bridge rectifier to convert the AC input voltage to a DC voltage. The DC voltage is then sent to the second stage, the DC bus, which uses a combination of inductors and capacitors to filter the rectified voltage into a smooth DC voltage. In the final stage, Insulated Gate Bi-Polar Transistors (IGBTs) are switched on and off to produce a pulse width modulated (PWM) AC output voltage. By regulating how long the IGBTs are allowed to conduct the frequency and voltage of the output can be adjusted [14].

As shown in Figure 2.3, the input current to a VFD is not continuous due to the commutation of diodes during the rectification of AC line voltage to DC voltage. The resulting AC line current is therefore non-sinusoidal and can be described as the summation of currents of differing frequencies. Since the input current now contains multiple harmonics, the VFD is said to be a harmonic generator or source. The

harmonics created on the line side of the VFD are of the order k=np±1, with p being the pulse number of the converter and n being an integer [15]. The pulse number is defined as the number of diodes or thyristors that conduct during one full cycle of the system voltage. The Baldor 15J VFD used in this thesis is a 6 pulse converter. As a result it should produce harmonics of the order k=6n±1. Three phase VFDs can be pulse converters of any multiple of 6, although it is rare to see anything larger than 24 pulse VFDs. Higher pulse VFDs are more expensive but have fewer lower order harmonics. In addition the harmonics produced by high pulse VFDs have smaller magnitudes since theoretically the amplitude of the nth harmonic current is given in terms of the fundamental current, I_1, to be I_1/n [15]. For the majority of applications it is most cost effective to purchase a low pulse VFD and use line reactors to filter the harmonics as necessary.

Depending on the type of load driven by the motor, the VFD can provide different benefits and cost savings. Most loads can be classified as either a constant torque or a variable torque load. An example of a constant torque load is a conveyor, which must be able to provide its full load torque over a range of different speeds. To maintain a constant torque at changing speeds the air gap flux must also stay constant [15]. A VFD is able to achieve this by adjusting both the output frequency and voltage to keep a constant volts to hertz ratio as the speed changes. A variable torque load is one whose torque requirements change with the speed of the motor. Common variable torque loads are centrifugal pumps, fans and compressors. These loads follow a profile where their torque increases proportionally to the square of their speed. Fluid flow in centrifugal equipment is governed by the Affinity laws which state that flow is proportional to speed,

pressure is proportional to the square of the speed and power is proportional to the cube of the speed [16]. Traditionally, the output of pumps has been controlled with a discharge valve which limits the flow and pressure output. When a valve is used to regulate flow the motor driving the pump is operated at full power regardless of the output requirements. This inefficient method is analogous to placing a brick on the accelerator of a car and then controlling its speed solely with the brake [17]. A VFD offers the ability to directly control the speed to match the desired output. The cost savings is substantial since power is proportional to the cube of the speed or flow. Thus a 50% reduction in flow would translate to a 50% reduction in speed and require only 12.5% of the full load power. Since 60-65% of induction motor loads are centrifugal equipment [18] the VFD in this thesis was operated under a load profile where the torque is proportional to the speed squared.

In addition to energy savings, VFDs provide several other benefits. Since the motor is isolated from the source power by the DC bus, the VFD draws the current and voltage nearly in phase with each other so the displacement power factor into the VFD is nearly unity. Induction motors also require large inrush currents, typically 6-7 times their rated value, at start up. However, a high inrush current is avoided when a VFD is used because the motor can be started at a low frequency and voltage while still applying its rated torque.

3.2 Thyristors

Although no longer used in VFDs, the thyristor is one of the most important and widely used power electronic semiconductors. Also known as a silicon controlled

rectifier (SCR), the thyristor has remained popular since its conception in 1957 due to its high power ratings [6].

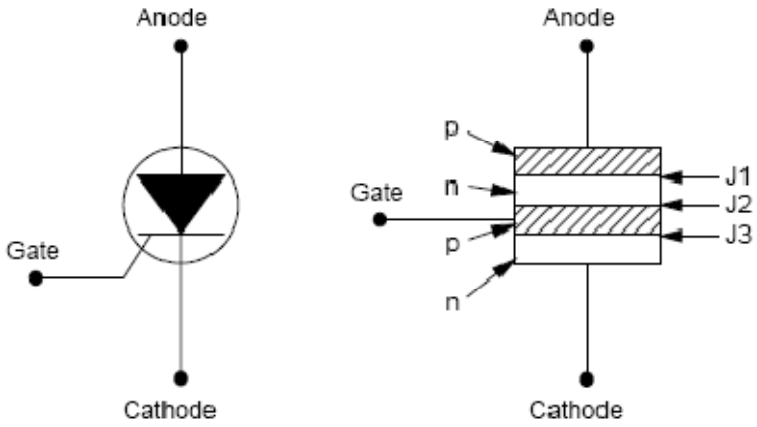

Figure 3.2 - Thyristor Symbol and Basic Structure [12]

As seen in Figure 3.2, the classical triode thyristor is a p-n-p-n sandwich with external connections applied to both p sections and the last n section. When the cathode voltage is more positive than the anode, junctions 1 and 3 are reversed biased and the device is blocked. If the anode is more positive than the cathode, junctions 1 and 3 are forward biased but junction 2 is reversed biased so the device still does not conduct. However, if a current greater than junction 2's breakdown level is applied to the gate, junction 2 will forward bias and the device will conduct so long as the anode is more positive than the cathode [12]. This gating scheme makes the thyristor a semi-controllable device in that its turn on is directly controlled but its turn off isn't.

When two thyristors are placed back-to-back, so that the cathode of one is tied to the anode of the other, they are said to be anti-parallel and form a semi-controllable bidirectional switch. If a sinusoidal voltage is applied across them, one thyristor will conduct during the positive half cycle and the other during the negative half cycle. When

the voltage sinusoid crosses zero the polarity of the cathode and anode will flip, turning off whichever thyristor was conducting. With this method the thyristors are said to be naturally commutated. The thyristors are turned on by signals sent to their respective gates 180° apart. This ensures that they will each be on for the same amount of time and not overlap conduction periods. A delay angle alpha can then be introduced so that the thyristors conduct for only a portion of the full sine wave. When used in series or parallel, with an impedance, this becomes an effective method of controlling the current or voltage seen by a device.

3.3 FACTS

In addition to the VFD, power electronics have taken a key role in controlling power flow in large scale electric networks. Flexible AC Transmission Systems (FACTS) is the general name given to the group of emerging technologies which use power electronic switches to control power flow in a transmission network. In the past traditional series and shunt impedances have been used to maintain steady state voltages and improve power transmission capacity. While these methods are effective they leave all dynamic control of the system to changes made at the generators or transformers. FACTS, however, are controller based allowing the series and shunt compensation to adjust to the real time demands of the system.

In series compensation, a series voltage is introduced in the transmission line in the form of a series inductive or capacitive impedance to regulate the flow of real power. Controlling this impedance lets the power transmitted from the sending end to the receiving end be adjusted. Adding a series capacitance decreases the overall series

transmission impedance allowing for an increase in line current and transmittable power. In contrast placing a series reactance on a transmission line increases its impedance and serves to limit the amount of power on the line. Two common series compensators are the Thyristor-Switched Series Capacitor (TSSC) and the Thyristor-Controlled Series Capacitor (TCSC). The TSSC consists of a number of capacitors in series with the transmission line that are shunted by parallel back-to-back thyristors allowing them to be individually switched into or out of the line. Similar to the TSSC, the TCSC is a series capacitor controlled by anti-parallel thyristors in series with a reactance. The thyristors are fired at a delay angle α with respect to the crest of the capacitor voltage. This allows the current through the reactor and therefore the effective impedance of the LC circuit to be controlled [6].

In shunt compensation, a current is injected into the system as a means of supplying or consuming reactive power. The Thyristor-controlled Reactor (TCR) is a shunt reactor that is controlled by series back-to-back thyristors. Similarly, the Thyristor-Switched Capacitor (TSC) is a fixed shunt capacitance controlled by series thyristors. When TCRs and TSCs are placed in parallel with each other and have the firing angles of their thyristors adjusted by a controller, the device is referred to as a Static VAR Compensator (SVC). If properly designed the SVC can adjust its effective impedance to either absorb or supply reactive power.

Aside from the SVC, which will be the focus of this paper, the STATCOM and Unified Power Flow Controller (UPFC) are also popular and powerful FACTS. The STATCOM is a shunt compensator which uses a voltage-sourced converter to produce a voltage which is coupled through a reactance to the transmission line. By controlling the

angle of the voltage produced, the STATCOM can cause current to flow to or from the system through a reactance, thereby providing or absorbing reactive power. The UPFC is the most complete controller. With two voltage-sourced converters the UPFC can control both reactive and real power through series and shunt compensation [6].

3.4 The Static VAR Compensator

A Static VAR Compensator can refer to any of several different combinations of controlled shunt capacitors and reactors. This paper will focus on the configuration used in this thesis, the fixed capacitor thyristor-controlled reactor shown in Figure 3.3.

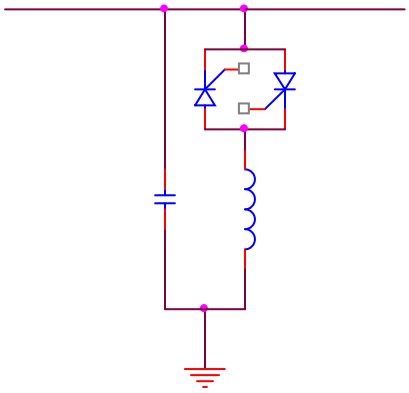

Figure 3.3 - Fixed Capacitor Thyristor-controlled Reactor

With this particular SVC configuration the shunt impedance seen by the system is a combination of a parallel fixed capacitor and a TCR. By changing the thyristor's firing angle, α, the current to the inductor can be varied anywhere from zero, when the switches are open, to the maximum, which occurs when the switches are open. For the TCR, α is measured with respect to the crest of the supply voltage, V_m, meaning that when $\alpha = 0^{\circ}$

the switches are open and when α = 90° the switches are fully closed. With α defined in this manner the current through the inductor can be derived as follows [6]:

Supply voltage is given as:

$$v(t) = V_m \cos \omega t \tag{3.1}$$

Instantaneous current through an inductor is defined as:

$$i_L(t) = \frac{1}{L}\int_{\alpha}^{\omega t} v(t)dt \tag{3.2}$$

Substituting 3.1 into 3.2 gives:

$$i_L(t) = \frac{V_m}{\omega L}(\sin \omega t - \sin \alpha) \tag{3.3}$$

Finding the RMS of 3.3 gives:

$$I_L(\alpha) = \frac{V}{\omega L}(1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}sin(2\alpha) \tag{3.4}$$

The inductor susceptance as a function of α is:

$$B_L(\alpha) = \frac{I_L}{\omega L} = \frac{1}{j\omega L}[1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin(2\alpha)] \tag{3.5}$$

When combined with the fixed capacitor the SVC susceptance is:

$$B_{svc}(\alpha) = B_L(\alpha) + B_c = \frac{1}{j\omega L}\left[1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin(2\alpha)\right] + j\omega C \tag{3.6}$$

Equation 3.5 shows the effective susceptance of the inductor for a given firing angle α, while the total SVC susceptance is shown in equation 3.6. The firing angle is limited to be between 0° and 90° with respect to the crest of the supply voltage to ensure that both thyristors are never gated at the same time. Since current can't change instantaneously through an inductor, a thyristor in series with a current carrying inductor will continue to conduct current even after the thyristor's voltage polarity has switched.

If thyristor one is still conducting when thyristor two is sent its gate signal, thyristor two won't be able to turn on. As a result only one thyristor will conduct for that period causing asymmetric output currents and voltages. The angle at which the current falls to zero and the thyristor is turned off is known as β, the extinction angle [6].

The extinction angle is given by the transcendental equation:

$$\sin(\beta - \theta) = \sin(\alpha - \theta)e^{\frac{\left(\frac{R}{L}\right)(\alpha-\beta)}{\omega}} \tag{3.7}$$

In equation 3.7, θ is the load angle and R and L are the series resistance and inductance. By limiting the firing angle to between 0° and 90° after the voltage crest, there is a 90° buffer after the voltage crosses zero for the thyristor to stop conducting before the next gate signal is sent.

Since the impedance of an SVC is regulated by switching thyristors the input current is distorted and harmonics are generated. However, because the thyristors are fired symmetrically during both positive and negative cycles, only odd harmonics are generated. Typical current harmonics for a theoretical TCR as a percentage of the fundamental are shown in Figure 3.4 with respect to the firing angle. While the TCR also generates triplen harmonics, these aren't shown in Figure 3.4 since the delta connected primary of our transformer should prevent them from appearing at the source.

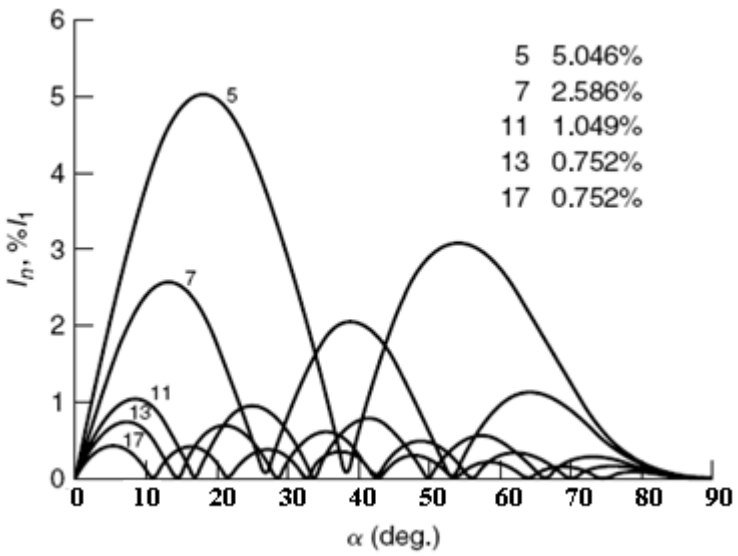

Figure 3.4 - Typical Current Harmonics in a TCR [19]

From Figure 3.4 it is seen that the SVC generates significant harmonics but they vary greatly depending on the firing angle.

3.5 The Enerpro Firing Board

In a true SVC, a programmed controller reads in transmission line parameters and determines the necessary firing angle to provide the thryistors in order to meet a predefined objective. This however, is very expensive and not practical for lab use. As a result, the thyristors used in this thesis will receive their gate signals from the Enerpro FCOG6100 Rev. K firing board where the firing angles can be manually adjusted. The FCOG6100 is a 3 phase multipurpose firing board that produces six 60° spaced sets of SCR gate signals. The board has the ability to power itself from 3 phase line voltages of 240V or 480V or single phase 120VAC. For this experiment, the board was powered by

single phase 120VAC for simplicity. The FCOG6100 is capable of producing gate signals spaced by 120°, 30°, or 60° that are made to be either in reference to the main phase voltage or lagging it by 30°. Since in our application the thyristors needed to operate as an in-line AC voltage controller, the board was configured for 120° gate signals and the reference signals were in phase with the main voltage. The firing angle is controlled by the voltage that appears on the board at position 10 of plug J3. This dc voltage can range between 0V and 5V. To supply the board the control voltage, a voltage divider was created using a potentiometer and the 5V dc output from the board. A switch was also connected to the voltage divider. Depending on how the switch was positioned the voltage divider provided a control signal between 0V-3.3V or 3.6V-5V to the Enerpro board. To maintain a firing angle below 90° the switch was positioned to provide a maximum of 3.3V. Beyond this voltage the system became unstable because the thyristor conduction periods overlapped due to their inability to stop the flow of current in the inductors.

The Enerpro firing board used is displayed in Figure 3.5. The output thyristor gate controls are labeled POS and NEG in the bottom right of the picture. The knob in the bottom left of the picture is a potentiometer which controls the firing angle output by the board. To the left of the knob is the switch which determined the range of voltage sent to the board. Additionally, the 120VAC board power input can be seen in the upper left of the picture.

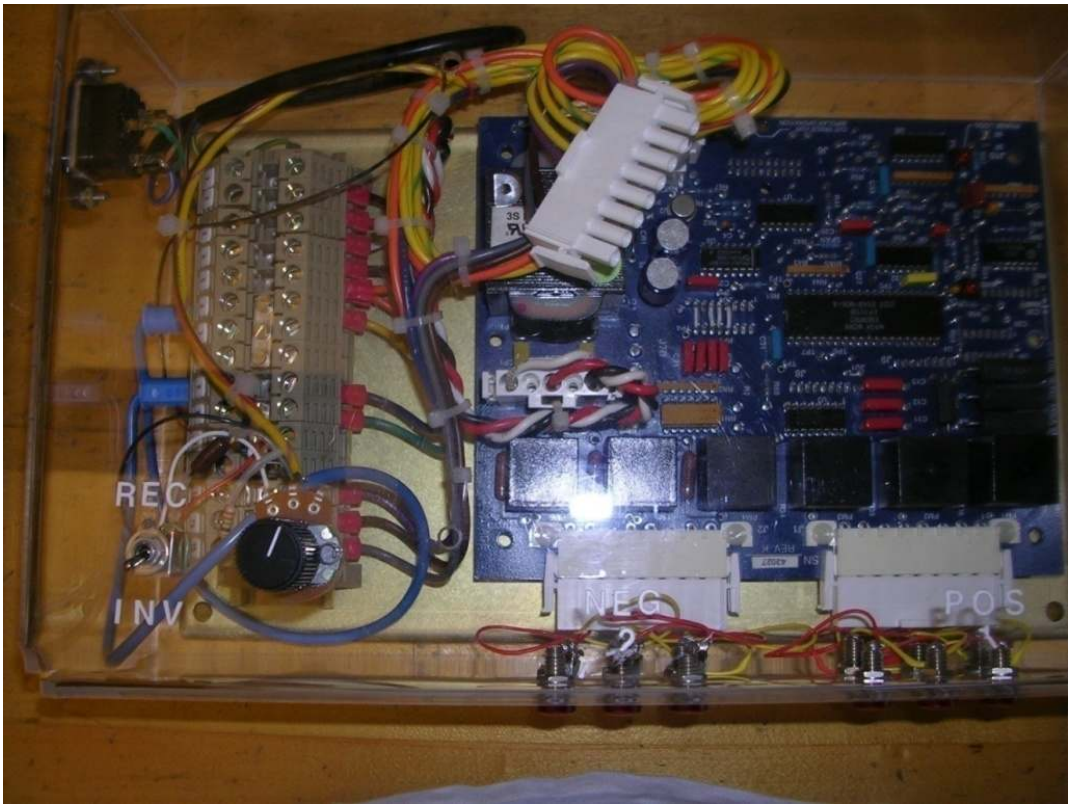

Figure 3.5 - Enerpro Firing Board Picture

The schematic of Figure 3.6 shows how the Enerpro firing board connected to the system. Not shown in the figure are the capacitors that were in parallel with the thyristor inductor series combinations. The delay command represents the voltage divider signal which controlled the firing angle. Instantaneous inhibit shown on pins 4 and 6 is a safety feature which serves to stop the gate signals if the board losses main power. Since our setup didn't require this provision, the inhibit was given a direct connection to 12V dc to insure it remained closed. The soft inhibit feature was not utilized in our system but it allows the firing board to ramp up or down the firing angle on start up and shut down. The J5 connection taps directly to the line voltages of each phase to provide the correct phase delay reference angles.

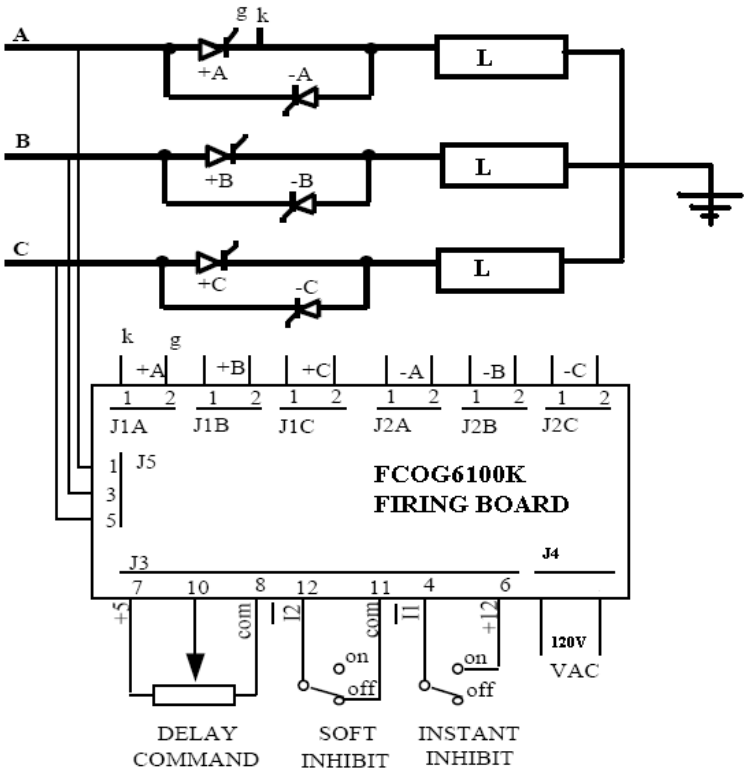

Figure 3.6 - Enerpro Firing Board Block Schematic [20]

CHAPTER 4 – LABORATORY SETUP AND DESIGN

4.1 Lab Procedure and Setup

For the purpose of this thesis, two Baldor 1HP induction motors were fed by a 240 V_{L-L} 3Φ 60Hz source through a 2:1 Delta-Wye grounded transformer. The Δ-Y connection was used based on the recommended grounding system by the VFD maker Baldor [9]. Additionally, the configuration is popular in distribution and commercial systems. The Δ-Y connection offers the benefits of a grounded secondary, a 30° phase shift to help keep voltages balanced, and a delta primary to protect the source against harmonics [21] [4]. After accounting for the connection and turns ratio, the transformer supplied the motors with their rated 208 V_{L-L} voltage. In this system the delta or source side represented the utility infinite bus. One of the motors was controlled by a Baldor Series 15J VFD, while the other's speed was left unchanged. This type of configuration was used to model a scenario where different types of loads are connected to the same bus. In this setup both a distortion and a displacement power factor less than unity will be present when no compensation is applied. If only VFD controlled motors were used the displacement power factor would be unity regardless of the loading conditions making capacitive or static var compensation completely unnecessary. Both motors were coupled to separate dynamometers so that their loads could be varied. Dynamometers are machines which can apply an adjustable torque to a motor shaft while displaying the motor's speed and torque. The base system schematic without any compensation is displayed in Figure 4.1.

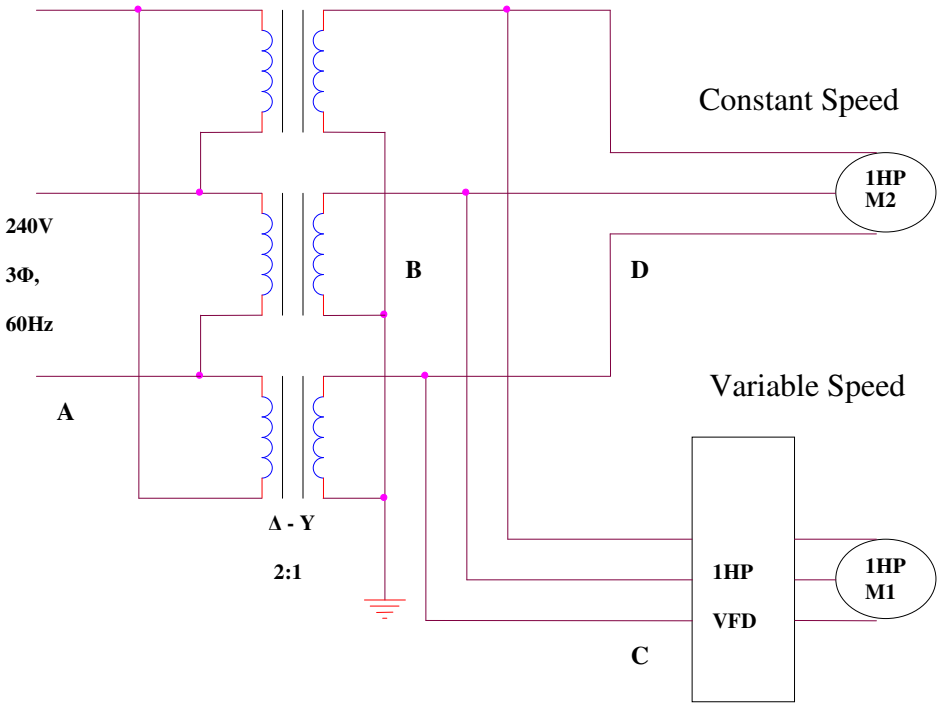

Figure 4.1 - Case 1 Base System Schematic

To best match the experiment to the real world, the VFD motor had its load and speed stepped to match a variable torque load. A variable torque load is one whose torque demand increases with its speed, usually proportionally to the speed squared [1]. This load characteristic is common to variable flow applications which can include fans, centrifugal pumps or blowers, propeller pumps, turbine pumps, agitators, and axial compressors. Since the torque increases proportional to the square of the speed, VFDs provide the greatest cost savings for this type of load [16]. This made the variable torque load profile the best choice for the experiment.

To determine the load points of the VFD motor, M1, the motor's rated torque was set equal to its rated speed squared and the proportionality constant K was solved for. This is shown in equation 4.1.

$$K = \frac{T_{rated}}{n_{rated}^2} = \frac{36.54\ lb*in}{1725\ ^2 rpm} = 1.23 \text{ e } -05\ \frac{lb*in}{rpm} \quad (4.1)$$

Finding this K value allowed the desired motor speed to be calculated for torque values between 0% and 100% of rated torque. These values along with the experimental frequency that came closest to providing the desired speed are summarized in the Table 4.1.

Table 4.1 - Motor 1 Torque Speed Values

% Full Load	Torque (lb*in)	Speed (rpm)	Frequency (Hz)
100	36.54	1725	60
90	32.88	1636	56
80	29.23	1543	53
70	25.57	1443	49
60	21.92	1336	45
50	18.27	1220	41
40	14.61	1091	37
30	10.96	945	32
20	7.31	771	26
10	3.65	546	18
0	0	0	0

Using the values in Table 4.1 Motor 1 was stepped from 0%-100% of full load torque in 10% increments. Meanwhile, Motor 2 was held constant at rated speed for cases of 25%, 50%, 75% or 100% of its full load torque. This loading scenario was repeated for three different situations. The first case was the base case shown in Figure 4.1 where no compensation was applied. For the second case a capacitor was placed between each of the secondary transformer phases and ground. This configuration was done to simulate the traditional method of power factor correction. For the final case, a static VAR compensator was placed between each secondary phase and ground. In both

cases, compensation was placed on the secondary of the transformer so that triplen harmonics introduced by the compensation would not reach the source. Schematics of cases 2 and 3 are shown in Figures 4.2 and 4.3 respectively.

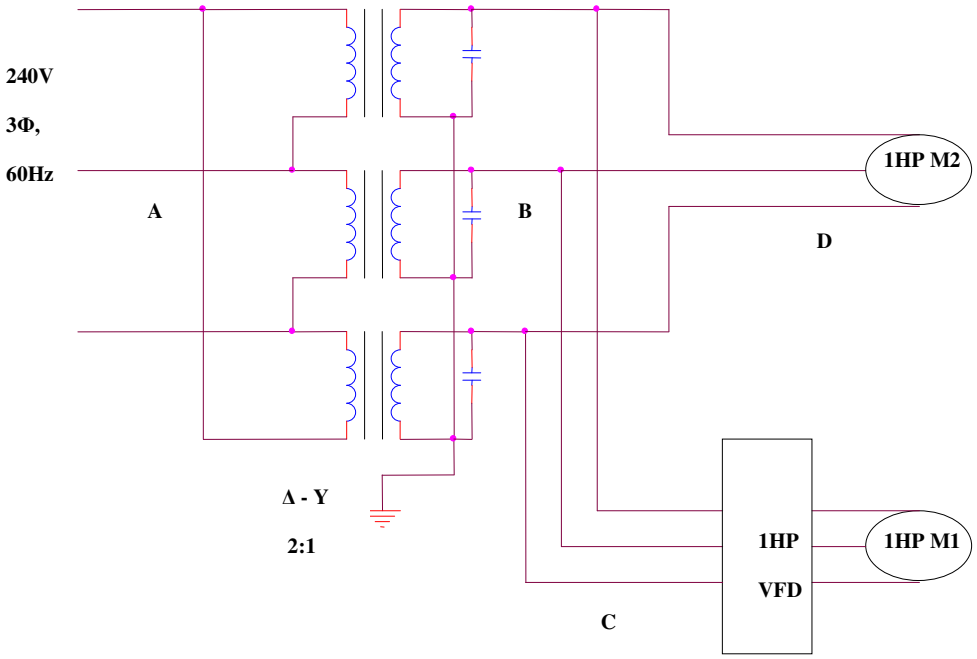

Figure 4.2 - Case 2 Capacitive Compensation Schematic

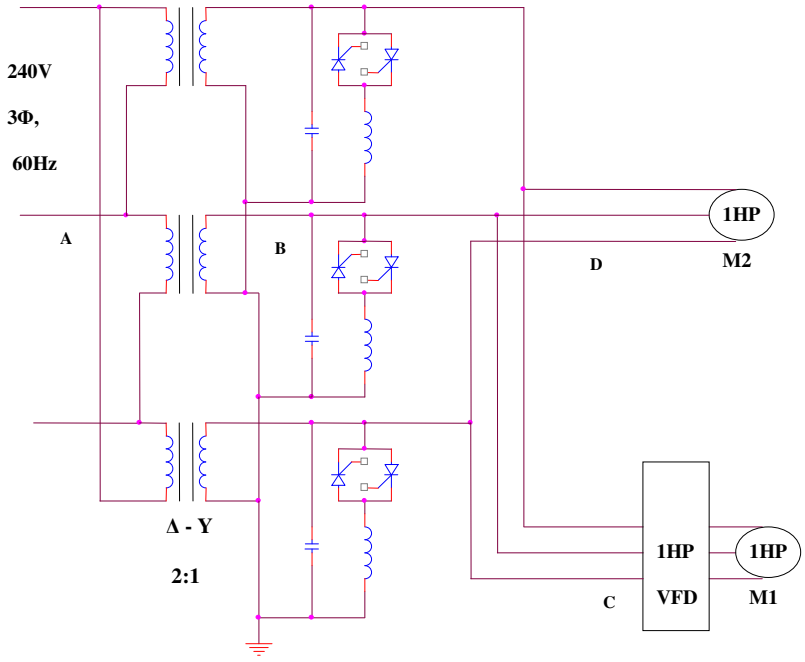

Figure 4.3 - Case 3 Static VAR Compensation Schematic

For each of the loading scenarios and cases described, data were taken on the delta and wye sides of the transformer, as well as on each of the motor branches. These points are labeled A, B, C and D in Figure 4.1. Data at each point was collected using two PowerSight PS3000 power quality analyzers. When measuring at points B, C, and D, the analyzers' current probes were moved between the respective branches while the voltage probes remained fixed at the secondary side of the transformer, since this node was common to all three points. Additionally, a 3Φ Yokogawa WT130 Wattmeter was connected between the source and the primary of the transformer. This provided a convenient method to monitor the input conditions. When the SVC was used in case 3, its firing angle was adjusted until the Yokogawa displayed the minimum achievable value of VARs being sent from the source. While the Yokogawa was used as a reference, all data presented in this report was obtained from one of the two PowerSight analyzers.

Unless mentioned otherwise all measurements will assume a balanced system so that the measurements of phases a, b and c are of the same magnitude. All harmonic data is from phase A unless otherwise stated.

4.2 Capacitor Sizing

For case 2 the capacitors were chosen to deliver a 0.95 power factor under the worse case VAR usage. A 0.95 power factor was selected instead of unity so that the capacitors wouldn't be over compensating when the motors were consuming less VAR. From the base case the most VARs sourced was 1332 VAR, which occurred when both motors were running at full load and corresponded to 2062.4W of real power. Listed below are the step-by-step design equations for determining the correct capacitance.

Maximum Apparent Power @ 0.95 PF:

$$\boldsymbol{S = \frac{P}{pf} = \frac{2062.4\,W}{0.95} = 2170.9}\ \text{VA} \tag{4.2}$$

Reactive Power @ 0.95 PF

$$Q_{desired} = \sqrt{2170.9\,VA^2 - 2062.4\,W^2} = 677.7\,VAR \tag{4.3}$$

Hence, the required Reactive Power from the Capacitors:

$$Q_{Cap} = Q_{actual} - Q_{desired} = 1332\,VAR - 677.7\ \text{VAR} = 654.3\ \text{VAR} \tag{4.4}$$

This yields the total system capacitance need:

$$C = \frac{Q_{cap}}{2*\pi*f*V_{L-N}^2} = \frac{654.3\,Var}{2*\pi*60hz*118V^2} = 124\mu F \tag{4.5}$$

$$C_{per\emptyset} = \frac{C}{3} = 41\mu F \tag{4.6}$$

Since the capacitors were Y connected the total capacitance need was found in equation 4.5 and then divided by 3 to give the capacitance per phase in equation 4.6. Due to availability constraints, 50μF capacitors were used instead. This difference results in the capacitors supplying 787 VAR as opposed to the calculated 654 VAR. The increase in reactive power from the capacitors means that under the worst case scenario the system should be corrected to a 0.97 pf as opposed to a 0.95 pf. Since 890VARs is the lowest amount of reactive power supplied by the source the extra capacitance will not cause the system to become overcompensated.

4.3 SVC Design

For the design of the static var compensator in case 3, it was important to ensure that the SVC could achieve a unity displacement power factor at every data point. Since the high point of a SVC's capacitance range occurs when there is no current through the inductor, the capacitor can be sized just like it was for case 2 with the exception that it is now for a power factor of 1 instead of 0.95.

Maximum Reactive Power to be supplied by capacitor:

$$Q_{Cap} = Q_{max} = 1332\,VAR \tag{4.7}$$

This yields a total capacitance of:

$$C_{tot} = \frac{Q_{cap}}{2*\pi*f*V_{L-N}^2} = \frac{1332\,Var}{2*\pi*60hz*118^2} = 254\mu F \tag{4.8}$$

$$C_{per\emptyset} = \frac{C}{3} = 85\mu F \tag{4.9}$$

The per phase capacitance value found in equation 4.9 is the minimum capacitance required by the SVC to compensate the system to a unity displacement factor. Since the SVC can lower the effective capacitance seen by the circuit, any value above 85μF can be used so long as the SVC can still meet the minimum VAR requirements. For simplicity a 100uF capacitor was selected and formed by placing two 50uF capacitors in parallel.

To size the inductor, it was necessary to determine the inductance which, when placed in parallel with the capacitor, will cancel enough capacitance to provide the minimum VARs for the system. If the inductance was too small the system would be over compensated at this point and draw a leading power factor. From the data collected the minimum VARs from the source was 890VAR and occurred when M2 was run at 25% and M1 was not running.

Minimum VARs to be supplied by the SVC:

$$Q_{SVC} = Q_{min} = 890\ VAR \tag{4.10}$$

This yields a total effective capacitance of:

$$C = \frac{Q_{cap}}{2*\pi*f*V_{L-N}^2} = \frac{890\ Var}{2*\pi*60hz*118^2} = 170\mu F \tag{4.11}$$

$$C_{min\ per\emptyset} = \frac{C}{3} = 57\mu F \tag{4.12}$$

The inductance could have been sized so that the SVC's inductive maximum, or capacitive minimum, was 57uF. This would have allowed the capacitance to be finely tuned over a range of 57uF to 100uF. However, it would have required a disproportionally large inductor and limited the overall flexibility of the system. Since

the main draw of the SVC is its ability to quickly compensate a system over a large range of positive and negative VAR requirements, a more practical way to size the inductance is so that the minimum system VARs occurs at a firing angle greater than 0 degrees. To replicate a more real world scenario, were the SVC might also be asked to compensate for a leading power factor, we chose 45 degrees as the angle to provide our system's minimum VAR requirements. As outlined in Chapter 3, the susceptance of the inductor as a function of the firing angle α is given in equation 4.13 [6].

Susceptance of the SVC inductor as a function of the firing angle:

$$B_L(\alpha) = B_L\left(45° = \frac{\pi}{4}\right) = \frac{1}{j\omega L}\left[1 - \frac{2}{\pi}\alpha - \frac{1}{\pi}\sin(2\alpha)\right] = 0.182\frac{1}{j\omega L} \tag{4.13}$$

Susceptance of the SVC Capacitor:

$$B_c = j\omega C = 2 * \pi * 60Hz * 100\mu F = 0.038\,S \tag{4.14}$$

$B_{svc}(45^{\circ})$ is found from the desired effective capacitance in eq. 4.12:

$$B_{SVC}(45°) = j\omega * C_{\min perΦ} = j * 2 * \pi * 60Hz * 57\mu F = 0.021S \tag{4.15}$$

Total Desired Susceptance of the SVC @ $\alpha = 45^{\circ}$:

$$B_{SVC}(45°) = B_L(45°) + B_c \tag{4.16}$$

Substituting equations 4.12, 4.13 and 4.14 into 4.15 yields the inductance:

$$L = \frac{B_{pu}(45°)}{(C - C_{\min perΦ}) * \omega^2} = \frac{0.182S}{(100\mu F - 57\mu F)(2*\pi*60Hz)^2} = 30\text{mH} \tag{4.17}$$

From equation 4.17, a per phase inductance of 30mH, with a firing angle of 45°, in parallel with a 100μF per phase capacitor will provide the minimum VARs our system requires. Since a 30mH inductor was not readily available, 40mH inductors were used instead. The slightly larger inductance means that our capacitive minimum will be

achieved at a smaller firing angle of roughly 40° as opposed to 45°. This change is minor and for our purposes has no tangible effect on the system. Using a 40mH inductor and 100µF capacitor, Figures 4.4 and 4.5 show how the SVC susceptance and its effective capacitance vary as a function of firing angle. It can be seen in Figure 4.4, that when the firing angle is less than 20° the SVC appears as an inductive load to the system, where as it is capacitive for firing angles above 20°. To achieve the minimum and maximum VAR requirements of the system, 890VAR at 57µF and 1332Var at 85µF, Figure 4.5 shows that the firing angle will need to be varied between 40-60 degrees.

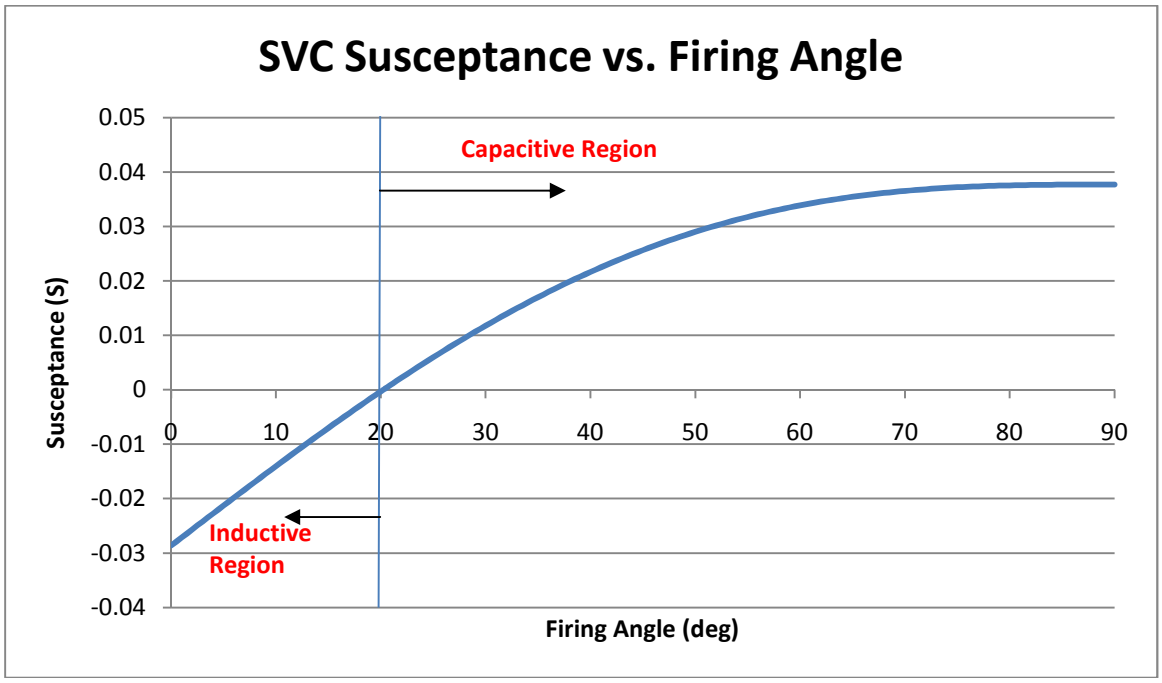

Figure 4.4 - SVC Per Phase Susceptance vs. Firing Angle

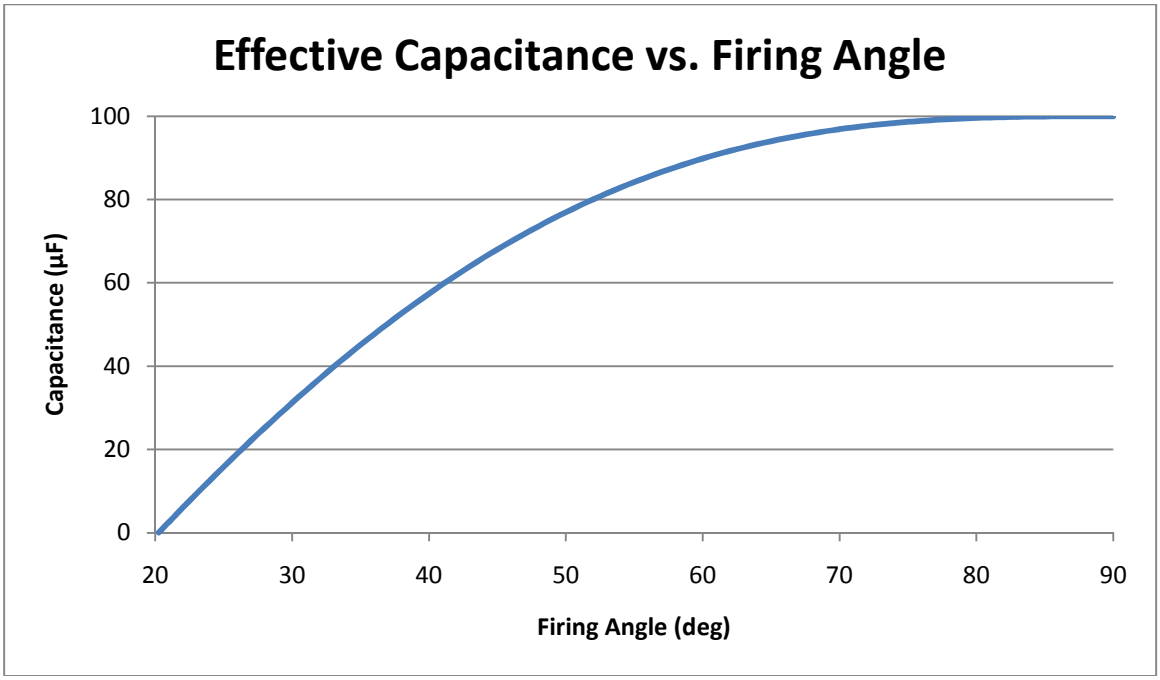

Figure 4.5 - Effective Capacitance Per Phase vs Firing Angle

4.4 Equipment List and Specifications

The following is a list of the equipment used for this lab setup, with the quantity in parenthesis.

- (1) Baldor Series 15J Inverter Control – AC Variable Frequency Drive

Model No.	IN0676C00
Motor Rating	1hp/750W
Input	3Φ, 60Hz/50Hz, 180-264VAC
Output	3C, 0-150Hz, 0-230VAC Continuous Amps 4.2A 60 Sec Ovld Amps 6.3A

- (2) Baldor – Induction Motors

Model No.	M3116T
Motor Ratings	1hp, 3Φ, 60Hz 208-230V FLA: 3.38A-3.12A RPM 1725 PF =0.73 Efficiency 82.5%

- (2) Magtrol – Dynamomter

Model No.	HD-705-6
Max Torque	50 lb-in

- (1) Enerpro – 6-SCR Firing Board

Model No.	FCOG6100-K
Input	3Φ, 60Hz/50Hz, 120-480VAC
Output	0° Phase Reference 120° bursts of 128 pulses 6° - 176° delay angle range Peak Gate OCV = 15V Peak Gate SCC = 2A

- (6) International Rectifier – Thyristors

Model No.	IRK -26
Ratings	I_t = 27A V_{rrm} = 400 -1600 V I_{rrm} =15A

- (6) Electrolytic Capacitors - 50µF
- (3) Power Inductors – 40mH
- (2) PowerSight – PS3000 Power Analyzers
- (1) Yokogawa – WT130 3Φ Wattmeter

4.5 Lab Setup and Equipment Pictures

The actual lab setup is shown in Figure 4.6. The inductors, firing board, and thyristors are in the front of the picture but are not connected. Directly behind them are the 50µF capacitors. The PowerSight Analyzer can be seen in the bottom left and the Yokogawa WT130 is in the upper left. The red letters on the picture correspond to the measurement points outlined in Figure 4.1.

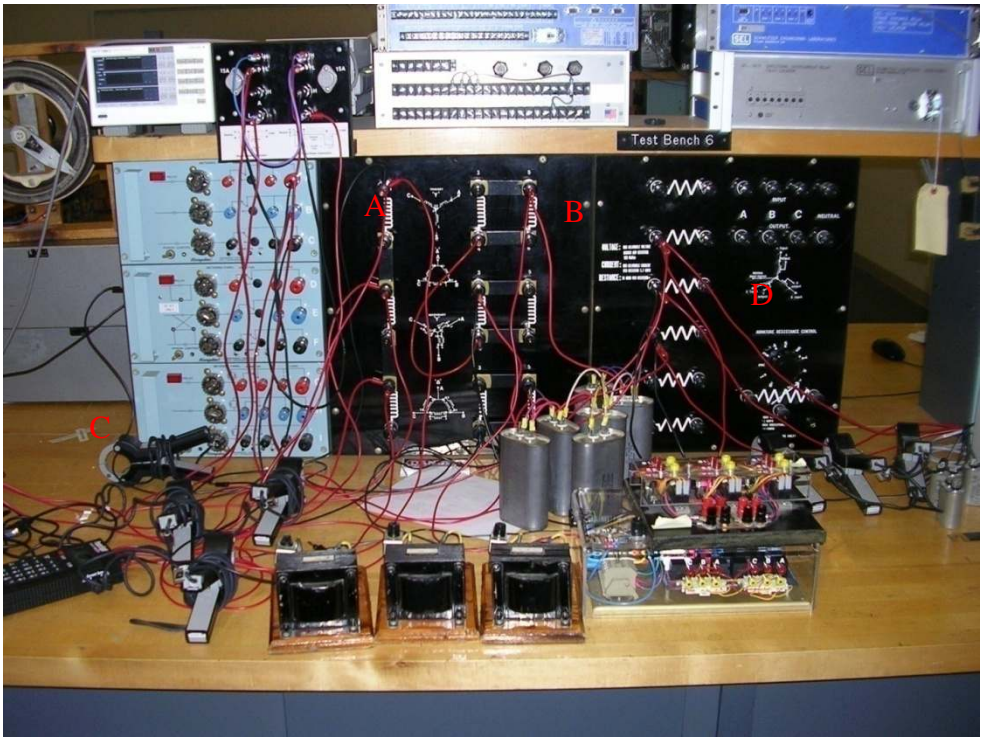

Figure 4.6 - Lab Bench Picture

Motor 1 can be seen in Figure 4.7 connected to the Magtrol dynamometer on the left. The torque of the motor is adjust be the small dial on the box next to the display. The VFD is shown to the right of the motor. Current probes attached can be seen measuring the input to the VFD. From the PowerSight analyzer the current and voltage data can be recorded to the laptop.

Figure 4.7 - Motor 1 and VFD Picture

The thyristors used for the SVC are shown in Figure 4.8. The connectors labeled A, B, and C at the top are directly connected to the respective phases on the secondary side of the transformer. The red and yellow connectors labeled G1 and G2 synch with the Enerpro firing board to provide the gate controls to the thyristors. The bottom connectors were jumped red to black for each phase, to configure the thyristors anti-parallel, and then connected in series to the inductor.

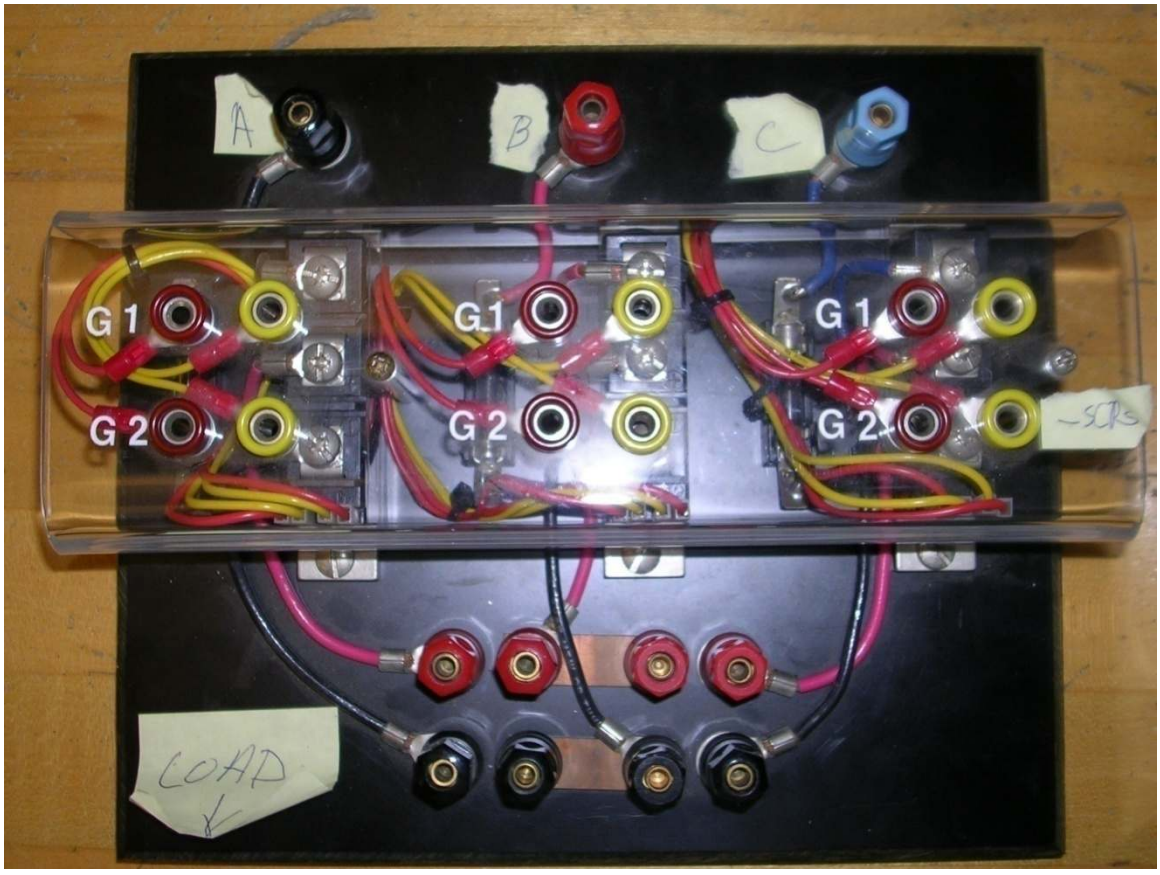

Figure 4.8 - Thyristor Board Picture

CHAPTER 5 –MEASUREMENTS AND ANALYSIS

5.1 Potential Sources of Error

Before the data collected are presented and analyzed, the possible causes for inconsistency and error will be discussed.

The most likely source for error in the data comes from the way in which they were collected. There were four different points of data collection, three from the secondary voltage node and one from the primary, but only two PowerSight Analyzers. Hence, all the data for one loading scenario could not be collected at the same time. In practice, Motor 2 would be held constant while Motor 1 was stepped from 0-100% and data was collected at points C and D. The system would then be de-energized, the probes repositioned, and the previous scenario would be repeated for points A and B. While every effort was made to make the settings identical in both steps, the reality is that the loading of the system could not be exactly the same as when the previous data were collected.

An additional complication came from the dynamometer's inability to keep a completely constant torque over a period of time. As a result, the motors had to be carefully monitored as any major delay in data collection would result in a drop of torque by as much a 1-2 lb*in. This became significant because the PowerSight Monitor (PSM) software, which saved the data to the computer, was buggy and would often require multiple attempts before it would save correctly. The dynamometers also required greater attention when the SVC was used, as the change in power factor and the time

required to manually adjust the SVC, would result in a different torque than was originally applied. Overall, though, it is safe to assume that all data were recorded within 0.25lb*in of the desired value.

As a reference, the voltage waveforms from the secondary side of the transformer for Motor 1 at full load with no VFD or other system loading are shown in Figure 5.1. Although not shown on the graph, PowerSight calculates the voltage and current imbalance as 1.968% and 3.3% respectively. The THDv% and THDi% are given in PowerSight as 2.02% and 3.78%.

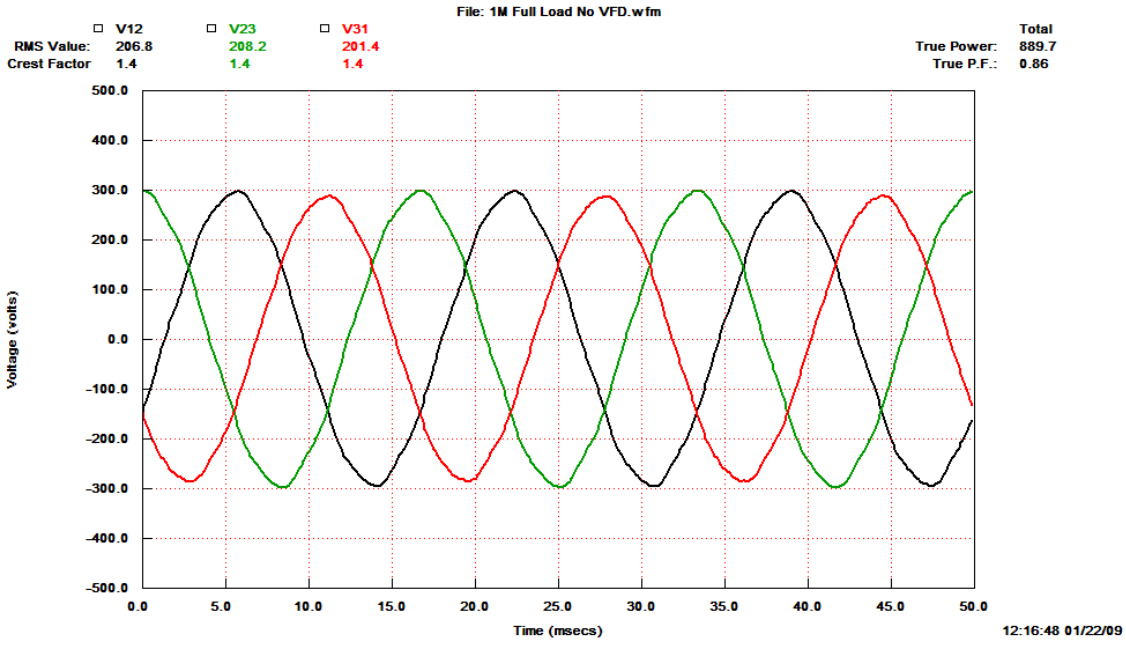

Figure 5.1 - System Reference Waveform

Assuming the motor to be a linear, balanced load we can see that the quality of the power source is good but not perfect. The system is not completely balanced with a maximum RMS line voltage of 208.2V and a minimum of 201.4V. The THD levels also show a very low level of harmonic distortion. Overall, these readings suggest that we should

expect under best case scenarios a slight imbalance and very small harmonics in the system.

Aside from the means of data collection and the power quality of the source, it should be noted that induction motors exhibit slightly different operating characteristics as their temperature increases. Therefore, data collected when the motors were first started and cold may vary slightly from data collected after the motors have warmed up. It is also important to remember that the impedance of capacitors and inductors are dependent on the frequency of the current through or voltage across them. As a result the effective impedance seen from these elements by the system will change as the harmonics in the system change. Additionally, while the inductors and capacitors where selected to be the same values for each phase, they likely had a slight variation between each other. This could contribute to voltage and current imbalance in the system. Finally, the design equations used to size the capacitors and inductors used the reactive power from the base case as their reference. Since the harmonics, and therefore the reactive power, will be different in the system for the other cases the design power factors will vary with the measured.

Overall, the possible causes of error are minor and do not invalidate the data as a whole. However, they are real and should be considered as whole when viewing the data. As a result, this analysis will focus on trends that can be seen across that data set as a whole as opposed to single instances which might be best explained by one of the above discrepancies.

5.2 Organization of Analysis Section

The analysis presented in this chapter will focus on three broad topics; harmonics, power factor and efficiency. Within each of these topics results of the three different methods of compensation will be compared. In each case, the analysis will attempt to translate the numerical findings in terms of their impact on equipment lifetime, performance and overall costs. The harmonics section will consume the bulk of the chapter and focus predominantly on current and voltage distortion. Additionally, individual harmonic components and the K-Factor at the transformer will be examined. True power factor will also be looked at in terms of its displacement and distortion components, as well as its impact on overall RMS current. Finally, the effects of the results on the overall efficiency of a power system will be discussed.

To avoid redundancy it will be assumed that the reader has familiarized themselves with the basic definitions and principles outlined in chapters 2 and 3.

5.3 Analysis of Harmonic Current Distortion

Before comparing the effects of the harmonics generated by each compensation method it is necessary to see if the methods tested fall beneath the maximum allowable levels of distortion. Generally, the most accepted way to measure the overall amount of harmonic content in a system is by the Total Harmonic Distortion (THD) index [4]. This method, described in chapter 2, provides an easy way to quickly compare the harmonic content of two waves. However, a waveform may have a very high THD level but be very small in terms of the overall load current of the system, thus having little impact on

the current injected to the utility at the point of common coupling (PCC). As a result the IEEE has set the maximum current distortion level, found in IEEE STD 519-1992, in terms of the Total Demand Distortion as seen in Table 5.1 [5].

Table 5.1 - IEEE 519-1992 Std Current Distortion Guidelines

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	<11	11≤*h*<17	17≤*h*<23	23≤*h*<35	35≤*h*	TDD
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed.						
* All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L.						
where I_{sc} = maximum short-circuit current at PCC. I_L = maximum demand load current (fundamental frequency component) at PCC.						

To properly use the IEEE guidelines, the system's short circuit current to load current ratio must be calculated. For the experimental system the ratio is calculated below [22] [23].

The transformer's rated current is found as:

$$\mathrm{I_{rated}} = \frac{kVA_{transformer}}{\sqrt{3}*V_{L-L\ Secondary}} = \frac{9kVA}{\sqrt{3}*208V} = 25\mathrm{A} \tag{5.1}$$

The transformer's short circuit current is:

$$\mathrm{I_{sc}} = I_{rated} \times \frac{100}{transformer\ impedance\ (\%)} = 25A \times \frac{100}{2.5} = 1000\mathrm{A} \tag{5.2}$$

The maximum experimental RMS load current @ PCC:

$$\boldsymbol{I_L} = 5.9\ \mathrm{A} \tag{5.3}$$

Short circuit to load current ratio:

$$\frac{I_{sc}}{I_L} = \frac{1000A}{5.9\,A} = 170 \tag{5.4}$$

From the result of equation 5.4 and Table 5.1, it is seen that to comply with IEEE STD 519-1992 the $TDD_i\%$ at the source must be less than 15%. Since the PowerSight analyzers provide THDi% but not TDDi%, TDDi% was calculated as:

$$TDD_i\% = \frac{THD_i\%}{I_L} \times I^{(1)} \tag{5.5}$$

Where $I^{(1)}$ in equation 5.5 is the magnitude of the fundamental current and I_L is the maximum load current. The IEEE Std 519-1992 defines I_L to be "the average current of the maximum demand for the preceding 12 months" [5]. For our purposes I_L will be the RMS current when both motors are running at full load. For the base case the current is 5.9A as used in equation 5.4. However, for the capacitive and SVC cases I_L is 5.3A. This difference is noticeable in the TDD_i calculations but since the I_{sc}/I_L ratio is still between 100 and 1000, the maximum allowable $TDD_i\%$ is still 15%.

Table 5.2 - TDDi% Values at the Source (Point A)

	TDD_i for M2 100%			TDD_i for M2 75%			TDD_i for M2 50%			TDD_i for M2 25%		
M1 % FLT	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100	34.91	37.98	39.40	34.52	37.51	39.41	32.86	38.73	39.55	32.54	38.30	38.90
90	29.56	32.91	34.48	29.80	33.06	34.04	29.31	32.99	34.16	28.96	34.08	33.63
80	26.47	29.60	29.85	26.24	29.32	29.75	25.63	28.24	29.78	25.09	30.14	29.28
70	23.20	25.57	25.56	22.38	24.80	25.71	22.34	25.44	25.51	21.75	26.11	25.45
60	19.02	21.48	21.50	19.12	21.60	21.93	19.27	21.18	22.14	18.41	22.13	21.49
50	16.64	18.14	18.74	15.75	17.96	18.33	16.24	17.65	18.06	15.33	18.06	17.77
40	13.61	14.99	16.34	12.97	14.37	16.08	12.96	13.90	15.38	12.48	14.56	15.15
30	10.10	11.53	13.44	10.41	11.38	13.25	10.39	11.23	13.44	9.94	11.86	12.83
20	8.59	8.55	11.69	8.24	8.81	11.78	8.16	8.53	11.94	7.89	9.00	11.73
10	7.19	7.29	11.37	6.64	7.16	10.68	6.89	7.36	11.21	6.68	7.25	10.52
0	2.46	4.34	10.77	2.59	4.01	10.23	2.73	4.08	10.62	2.80	4.44	10.75

From Table 5.2 it is clear that at full load all three cases are well above the 15% limits defined by the IEEE at the point of common coupling. All three cases begin to drop under the maximum allowable limits when the VFD motor M1 is loaded less than 40%. While the base case has smaller TDDi% for most instances, the differences between all three are small enough that no significant conclusions can be made about which compensation is best to use. However, if the size of our maximum load current were to increase, or the rating of our system decrease, these numbers would have to be reevaluated. In such a case it is possible that the small variations might be enough to be the difference in whether the IEEE guidelines are exceeded or not, making TDDi% pose a larger factor in choosing which compensation to use. It shouldn't be a surprise, however, that the TDD_i% exceeds the IEEE guidelines since there are only two loads in the system and one of them is a harmonic generator. Since the transformer is rated for 25A the average demand current could be significantly increased from 5.9A if more loads were added. If these loads were linear and harmonic free the TDD_i% levels would likely fall to acceptable levels, as the harmonic content would be a smaller portion of the demand current. However, if the load profile of the transformer remains the same it would be advised to add line reactors to the VFD to reduce the harmonic content seen at the PCC.

TDDi% is a measure of the harmonics with respect to the total maximum load current of the system, it is therefore useful to instead use THDi% for a more complete picture of how large the harmonics are with respect to the actual RMS current. The THDi% measured at the source point A, for the different loading scenarios, are shown in Figures 5.2-5.5.

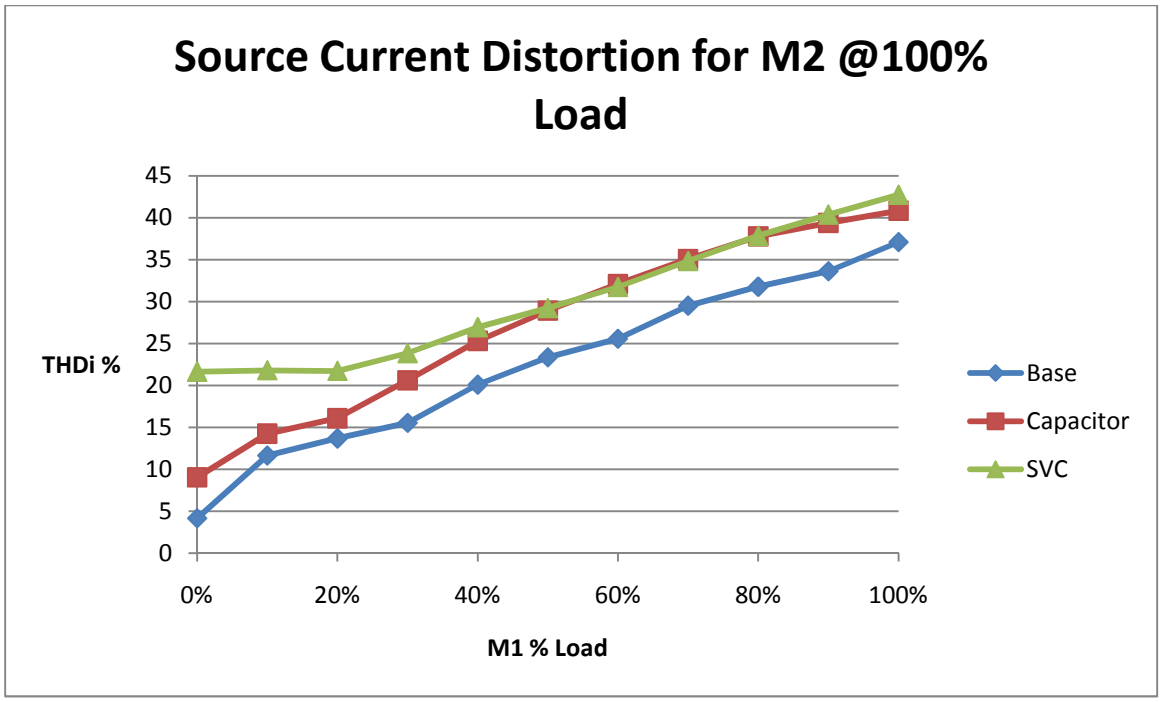

Figure 5.2 - Source THDi% vs. M1% Load for M2 @ 100% Load

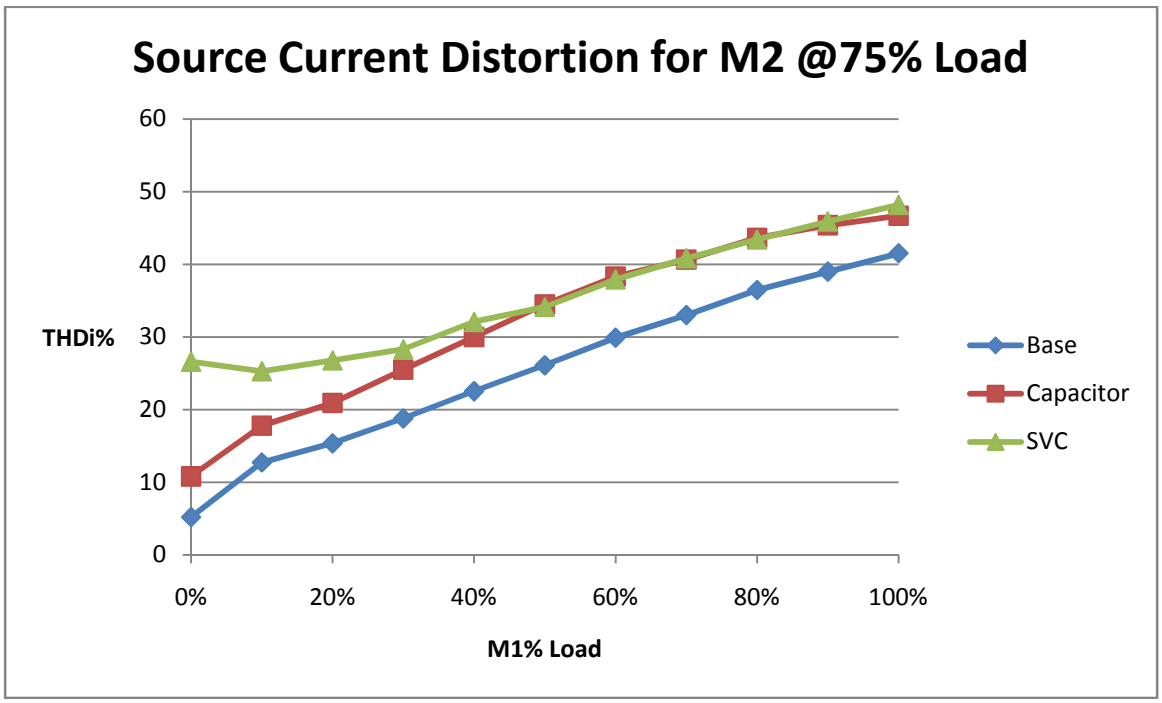

Figure 5.3 - Source THDi% vs. M1% Load for M2 @ 75% Load

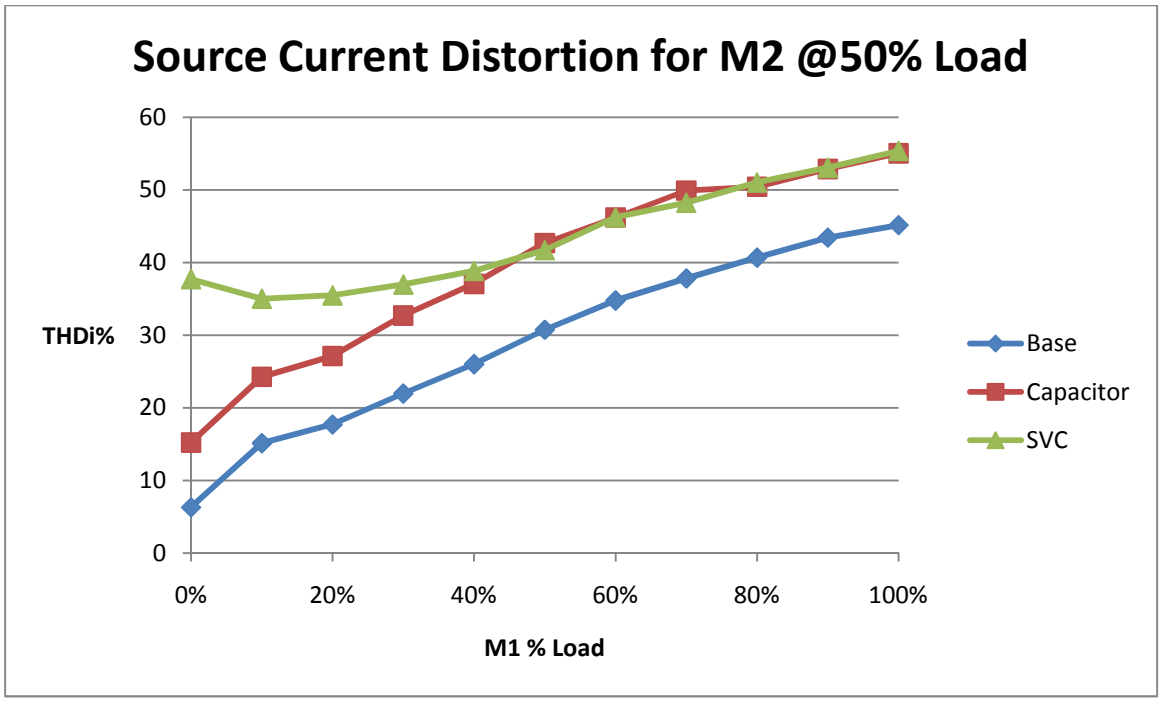

Figure 5.4 - Source THDi% vs. M1% Load for M2 @ 50% Load

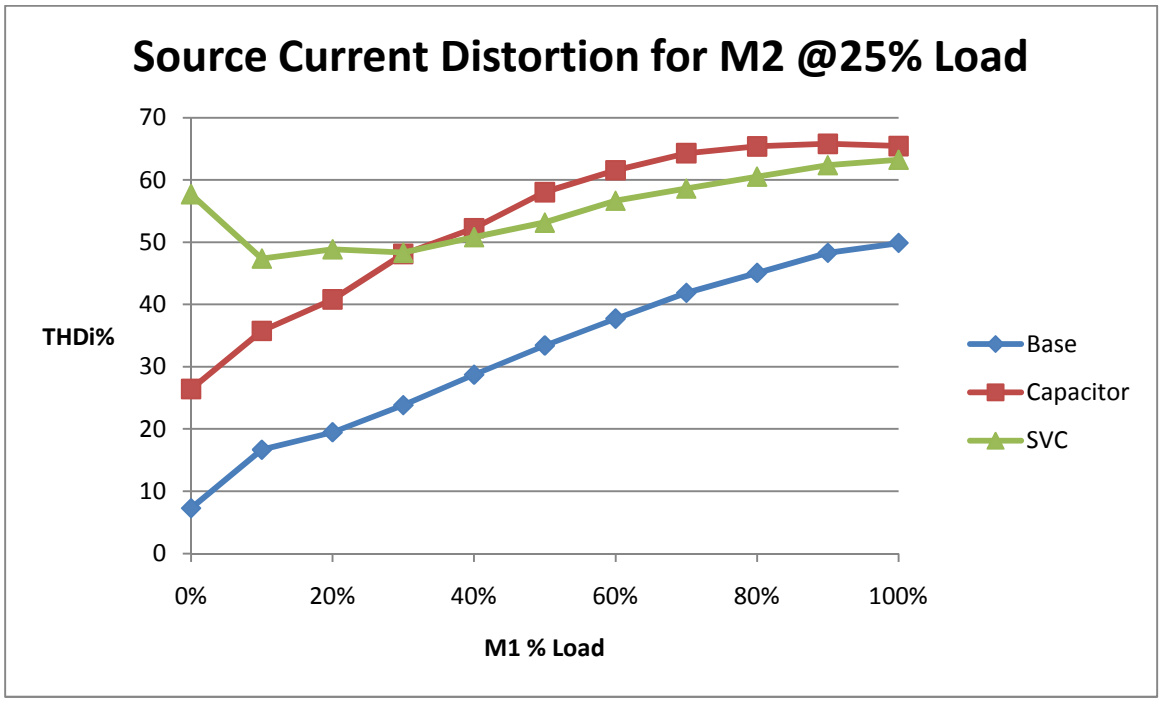

Figure 5.5 - Source THDi% vs. M1% Load for M2 @ 25% Load

From Figures 5.2-5.5 the most obvious trend is that as the VFD loading increases the THDi% for all cases also increases linearly. Assuming the input to the VFD is a standard full bridge diode rectifier the harmonics it generates will be the same, just proportionally larger, as the drives load increases [15]. Since THD_i% is a measure of the harmonics with respect to the RMS current the THDi% should linearly increase as the current through it increases. This is clearly seen in the base and capacitor cases. All cases also show greater harmonic levels for lower loading of the non VFD motor, M2. This too is intuitive, since for higher M2 loading the source current increases making the harmonics generated by the VFD a smaller percentage of the overall current. Compared to the other cases, the SVC shows significantly higher THDi% levels when the VFD is operating at low loads. Since the VFD draws less current at low loads, the SVC's harmonic content is a much larger percentage of the overall harmonic content at low loads. As the VFD loading increases, the THDi% for the SVC case remains almost constant up to 30% M1 loading. For M1 loading above 30% the SVC grows at a similar yet slightly slower rate compared to the other two cases. With respect to the capacitive case the SVC exhibits higher harmonics at VFD loading less than 50% but above 50% the SVC has equal or lesser harmonics than the capacitive case.

The most surprising aspect of Figures 5.2-5.5 is the great increase in THDi% between the base case and capacitive compensation. Since the SVC introduces a new source of harmonics through its switching thyristors, it was expected that its THDi% levels would be greater than the base case. However, the capacitive scenario features no new switching elements which would produce harmonics in addition to the VFD. Closer

inspection reveals that capacitors can behave as a source of harmonics themselves [4]. One measure gives the order of a capacitors harmonic current to be of:

$$h = \sqrt{\frac{X_c}{X_{sc}}} \tag{5.6}$$

In equation 5.6, X_c is the capacitor impedance, X_{sc} is the system short circuit impedance, and h is the order of the harmonic current. Further analysis shows that a harmonic voltage applied across a capacitor results in a disproportionally larger harmonic current [10].

The impedance of a capacitor at frequency nω is given as:

$$Z_c = \frac{1}{n\omega C} \tag{5.7}$$

Then the instantaneous capacitor voltage and current is :

$$e_{c(t)} = \sqrt{2}\sum_1^n E_n \sin(n\omega t + \alpha_n) \tag{5.8}$$

$$i_c(t) = \sqrt{2}\sum_1^n E_n \mathrm{n\omega C} * \sin(n\omega t + \alpha_n + \frac{\pi}{2}) \tag{5.9}$$

From 5.8 and 5.9 the RMS current and voltages are found to be:

$$E^2 = \sum_1^n E_n^2 = E_1^2 + E_2^2 + \cdots + E_n^2 \tag{5.10}$$

$$I_C^2 = \sum_1^n (E_n n\omega C)^2 = (E_1\omega C)^2 + (E_2 2\omega C)^2 + \cdots + (E_n n\omega C)^2 \tag{5.11}$$

Then the ratio of total RMS to fundamental RMS voltage and current are:

$$(\frac{E}{E_1})^{\mathbf{2}} = 1 + \sum_2^k (\frac{E_k}{E_1})^2 \tag{5.12}$$

$$(\frac{I_C}{I_{C1}})^{\mathbf{2}} = 1 + \sum_2^k (\frac{kE_k}{E_1})^{\mathbf{2}} \tag{5.13}$$

From Equations 5.12 and 5.13 we see that an increase in the harmonic voltage across a capacitor, where k represents the harmonic order, causes a significant increase in the harmonic current through it. For example, if the 5^{th} harmonic voltage was increased from 0% to 25% of the fundamental voltage it would cause the total current to fundamental current ratio to increase by 60%, while the total voltage to fundamental voltage ratio would only increase by 3%. Of course this is an extreme example, as this setup never measured the 5^{th} harmonic voltage across the capacitors to be more than 2% of the fundamental voltage. Nonetheless, it illustrates that capacitors can make significant contributions to the harmonic current distortion of a system if the voltage across them is non-sinusoidal.

Recapping, Figures 5.2-5.5 give the THDi% at the source, for both the capacitive and SVC cases, to have significantly more harmonics than the uncompensated base case. If selecting between the two compensation methods strictly by THDi%, the capacitive method is a better choice if the VFD loads are anticipated to operate at less than 50% for significant periods of time. The SVC is a good choice if the VFD loads are expected to be operating above 50% of rated load most of the time.

In addition to the harmonics at the source which effect the utility, a potentially more important aspect to the owner are the harmonic levels within the system. Harmonics, as detailed in chapter 2, led to increased power losses and temperatures in the stator and rotor of the induction motor. Temperatures above the rated value of the motor will cause it to have a decreased life span. The THDi% for each compensation case at the non VFD motor, M2, are shown in Figures 5.6-5.8.

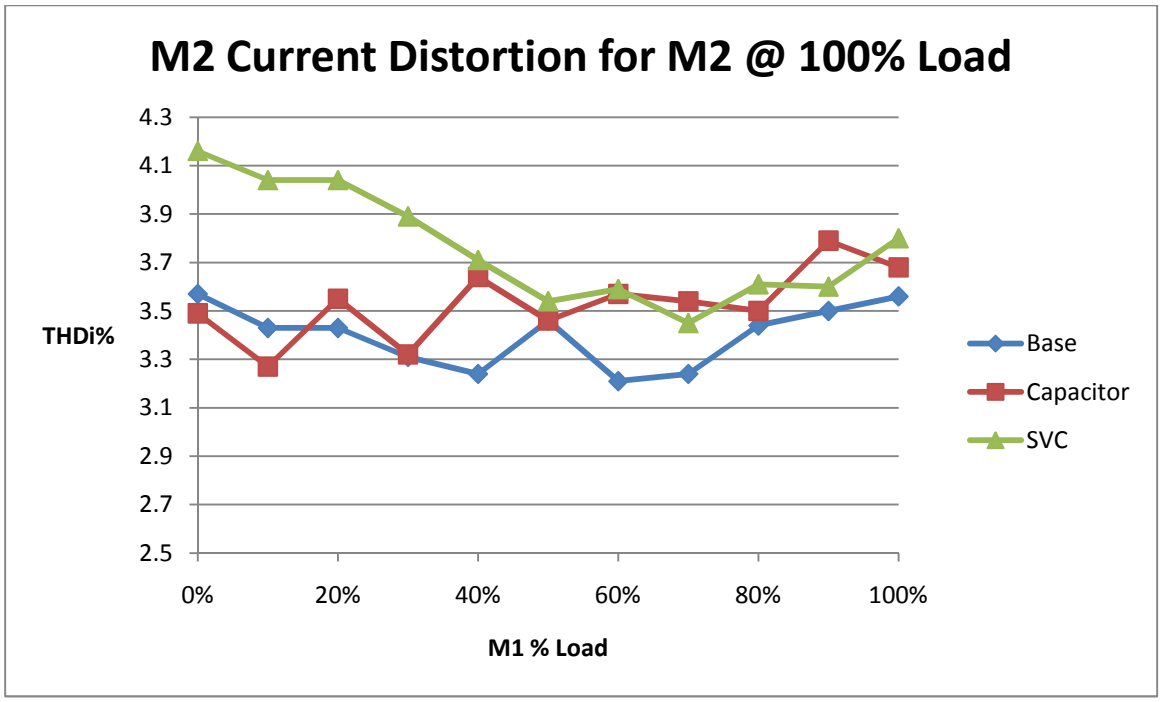

Figure 5.6 - M2 THDi% vs. M1 % Load for M2 @ 100% Load

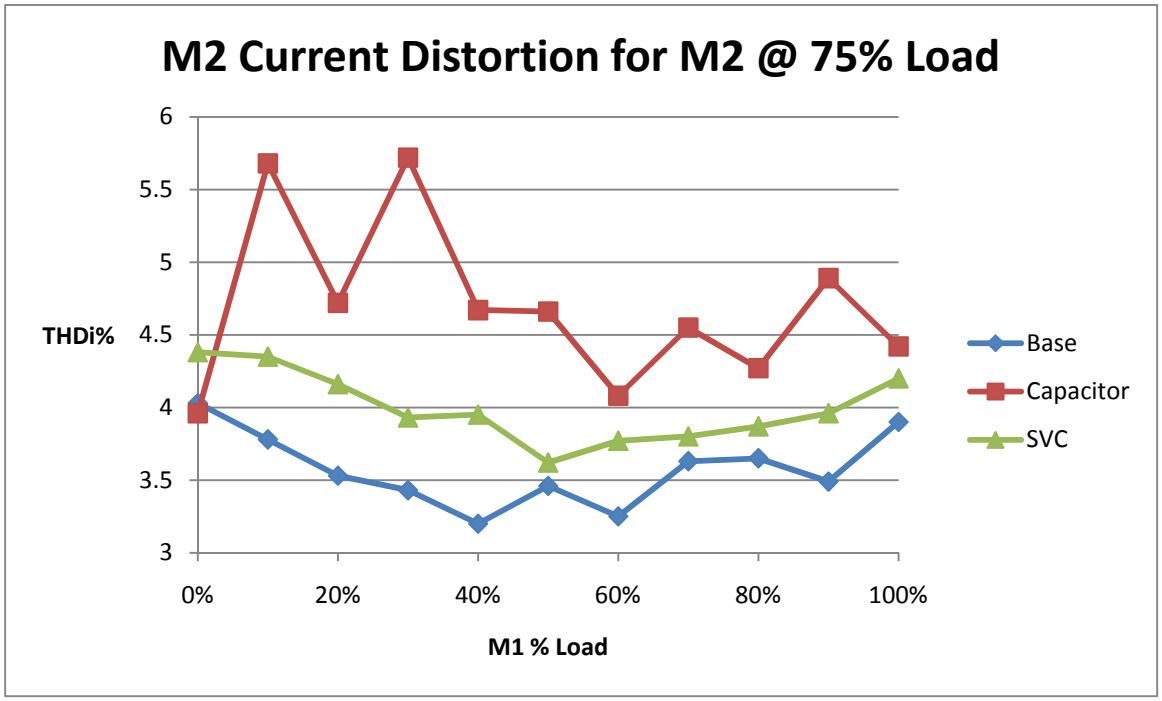

Figure 5.7 - M2 THDi% vs. M1 % Load for M2 @ 75% Load

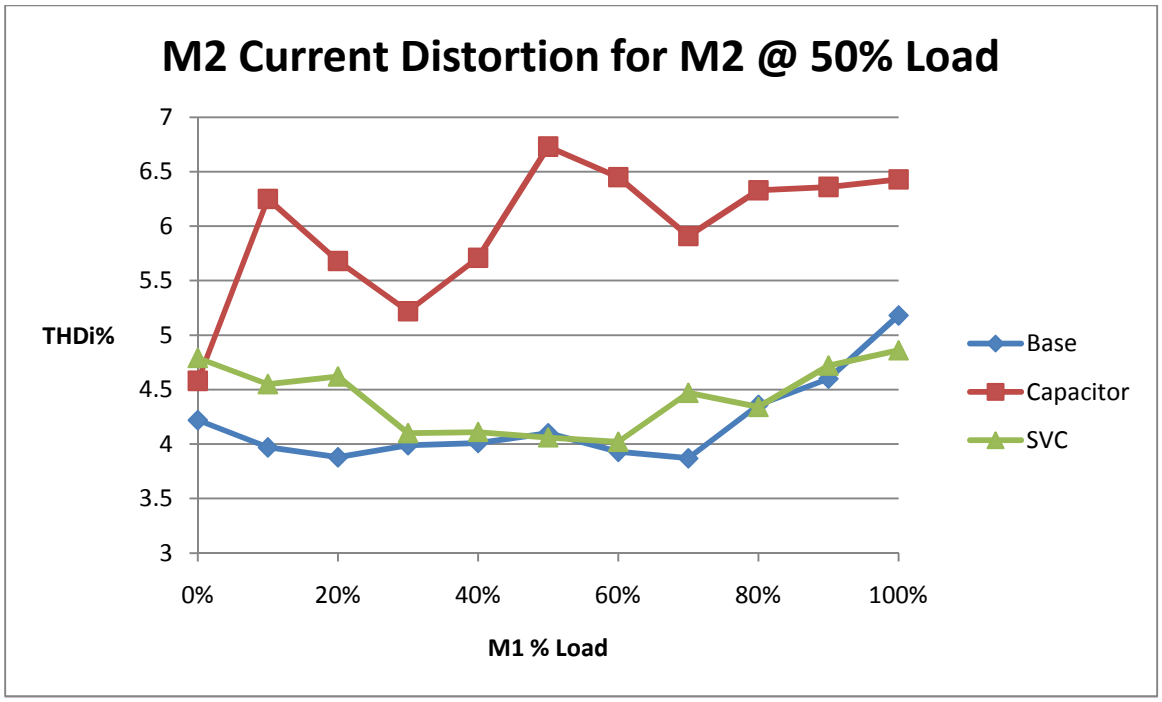

Figure 5.8 - M2 THDi% vs. M1 % Load for M2 @ 50% Load

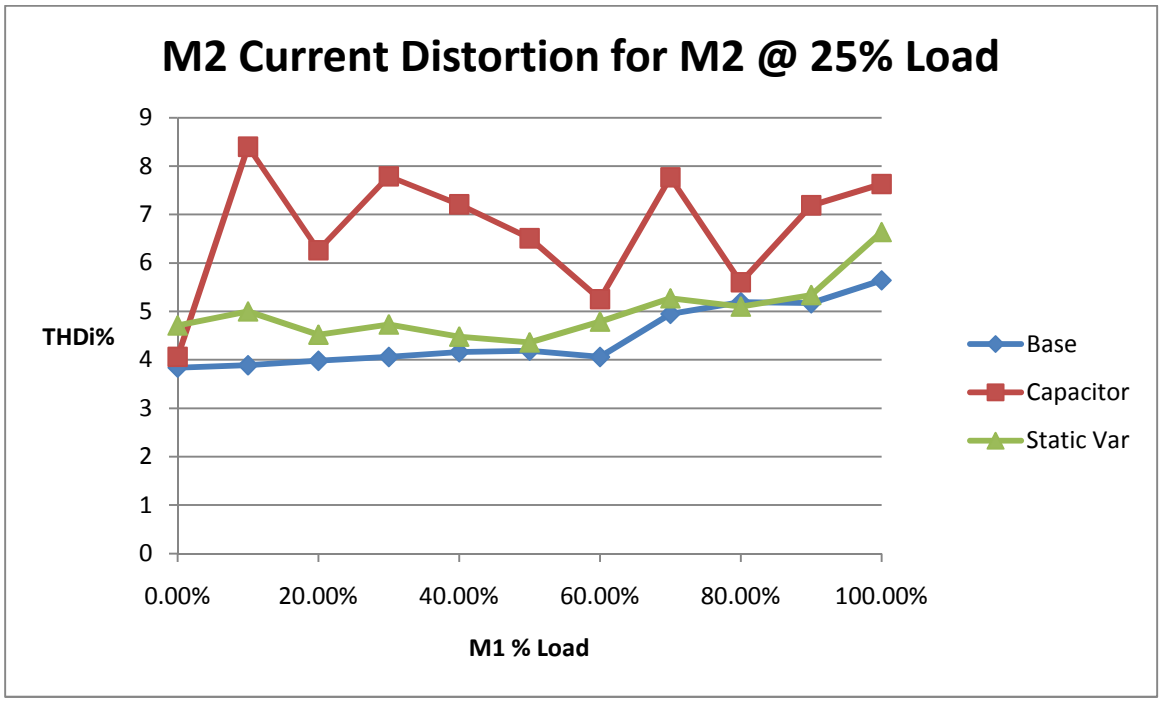

Figure 5.9 - M2 THDi% vs. M1 % Load for M2 @ 25% Load

The current drawn by M2 has the least harmonics during the base case. While the SVC has greater harmonics than the base case in most of the load scenarios, the two scenarios remain within roughly 0.5% throughout. This difference is small enough that the two methods can be said to result in roughly equal harmonic distortion at the motor input. Capacitive compensation compares well with the other two cases when M2 is at full load but becomes significantly worse as the load of M2 drops. When M2 is running at 75% or less, the capacitive case results in an increase of between 2 and 4 THDi% over the other two cases. In some loading situations this is double the amount of harmonic current distortion seen by the motor compared to the other cases.

Aside from the general trends, the graphs of Figures 5.6-5.9 increase and decrease sporadically as the M1 load is changed, this is especially evident in the capacitive case. These point to point oscillations in the data are difficult to explain. Since the measurements were all taken from phase A of the motor, it is possible that this is the result of a slight imbalance in the system. The slight perturbations in the data may also be the due to changing resonant conditions in the system or the load of M2 drifting over time. Since the variations are not consistent amongst the figures they are likely not significant. However, the overall trends of the data should not be discredited as they can be seen throughout the Figures.

5.4 Individual Harmonic Cancellation

At the onset of this thesis, one of the primary questions was how the harmonics generated by the SVC would interact with those created by the VFD. In section 5.3 we established that the addition of the SVC resulted in a significant increase in harmonic

current content at the source point. Now we will look at which specific harmonics are responsible for the differences in THDi%. Both the VFD and SCR are six pulse systems which produce odd harmonics of decreasing magnitude [15]. However, the triplen harmonics, or harmonics that are odd multiples of the 3rd harmonic, should not appear on the line side of a delta transformer. Triplen harmonics are zero sequence components which, according due to Kirchhoff's current law, can circulate within a delta configuration but can't leave the delta to appear as line currents [3]. Therefore the only harmonic currents of significance that should appear at the source are of the order 6p ± 1, where p is any integer number starting at 1. Since the harmonics decrease in magnitude as the order of the harmonic increases, we will only look at the 5th and 7th harmonics, as they should be most consequential. For six pulse rectification the ac current is given from Fourier analysis to be [2]:

$$i_a = \frac{2\sqrt{3}}{\pi} I_{dc}[\cos(\omega t) - \frac{1}{5}\cos(5\omega t) + \frac{1}{7}\cos(7\omega t) \ldots \pm \frac{1}{h}\cos(h\omega t)] \qquad (5.14)$$

In equation 5.14 it can be seen that the magnitude of the harmonic decreases proportionately to the size of the harmonic order. The RMS magnitude of the 5th harmonic at the source can be seen in Figures 5.10-5.13.

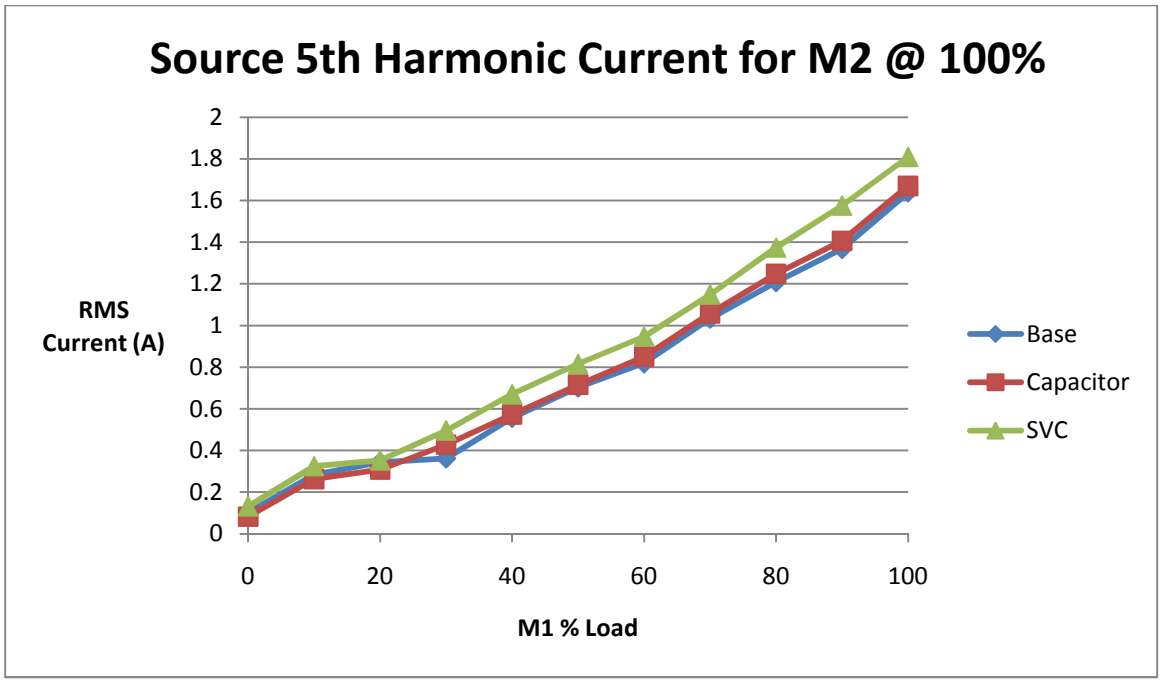

Figure 5.10 - 5th Harmonic Current vs. M1 % Load for M2 @ 100% Load

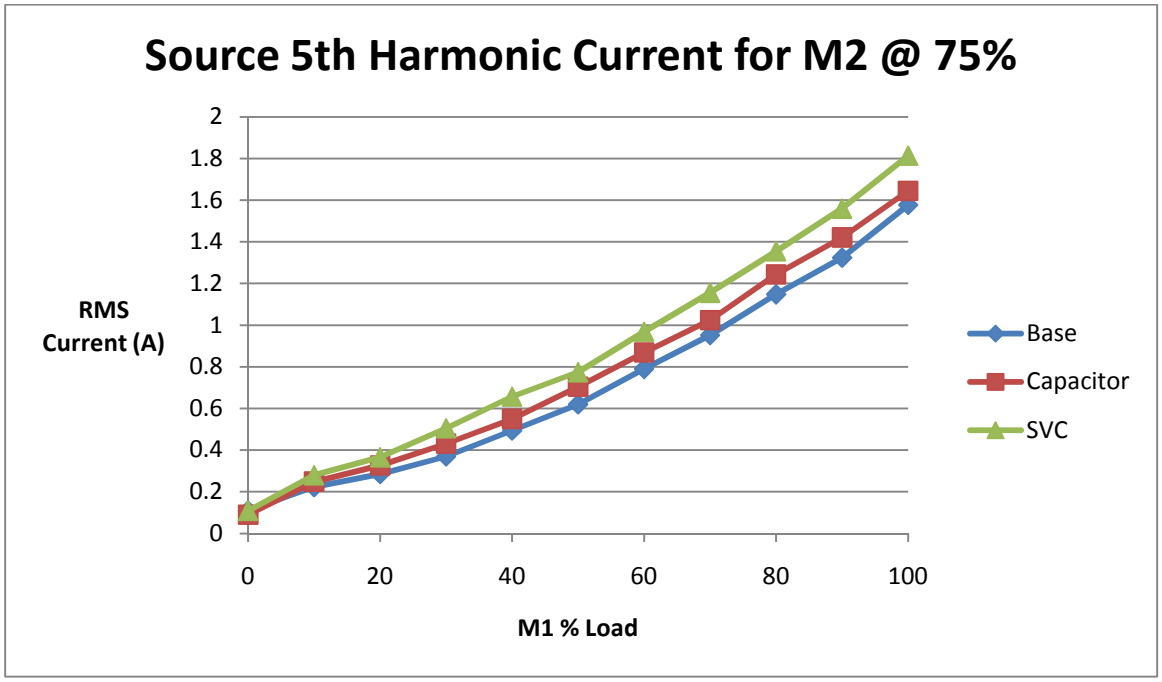

Figure 5.11 - 5th Harmonic Current vs. M1 % Load for M2 @ 75% Load

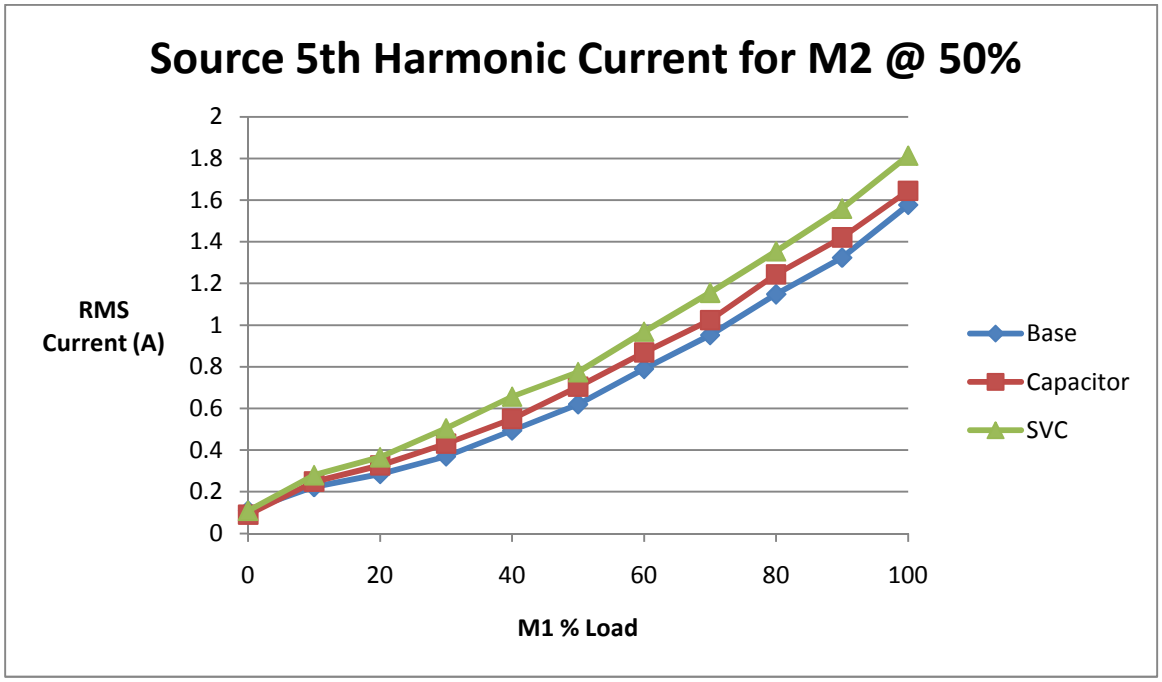

Figure 5.12 - 5th Harmonic Current vs. M1 % Load for M2 @ 50% Load

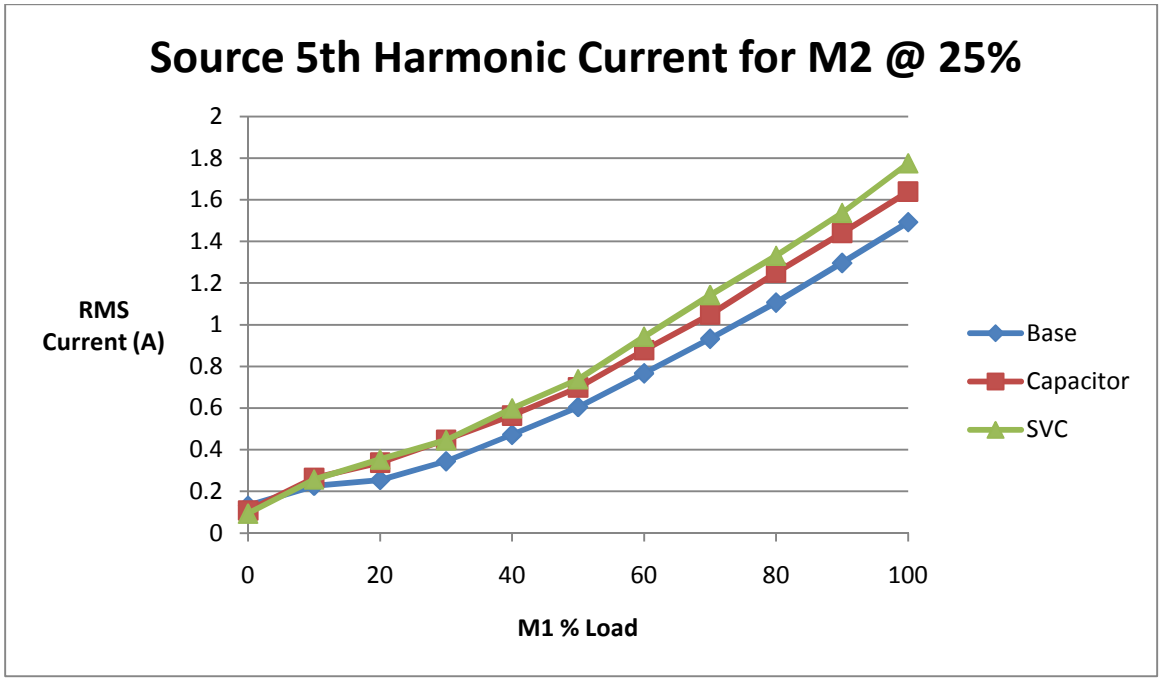

Figure 5.13 - 5th Harmonic Current vs. M1 % Load for M2 @ 25% Load

From the preceding figures it is seen that the SVC clearly has the largest 5th harmonic component. Even so all three cases have similar magnitudes at this harmonic order. The difference between the 5th harmonic for the base and SVC cases is at most 0.3A. The 0.3A increase for the SVC is a 20% increase over the base case's 1.5A magnitude. While this is significant, it also suggests that the majority of the content is coming from the VFD and not the SVC. This could imply that there is some small amount of cancellation between the SVC and the VFD or that the SVC just doesn't create as much 5th harmonic current as the VFD. The 7th harmonic RMS current at the source is shown in Figures 5.14-5.17.

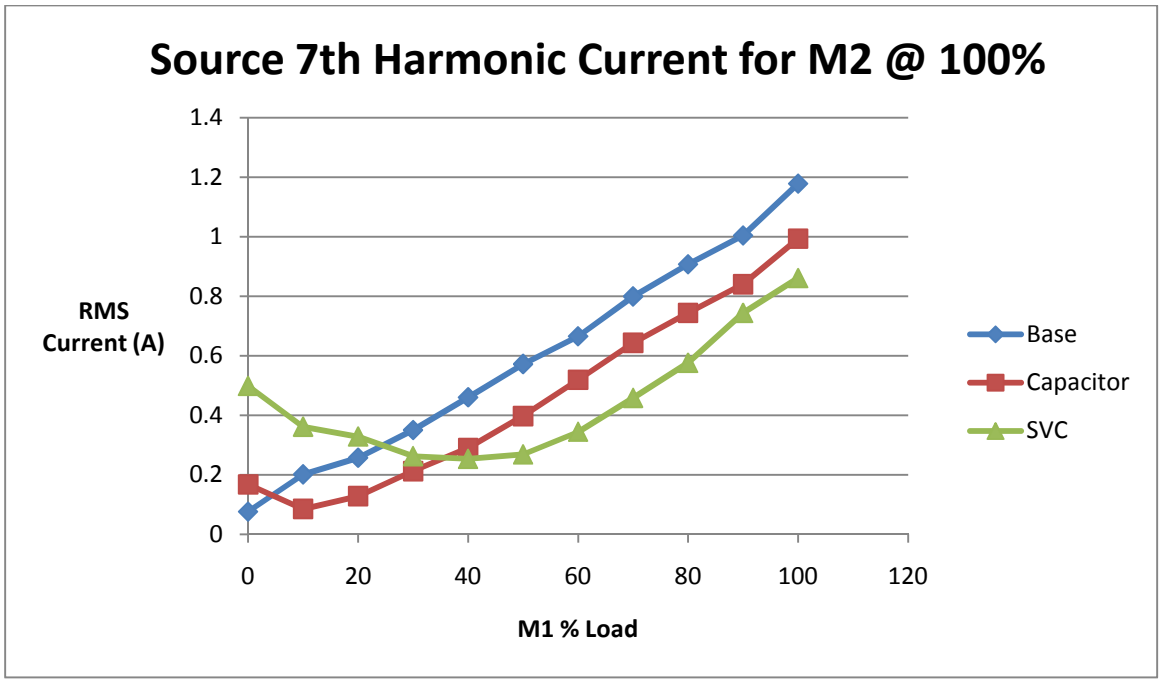

Figure 5.14 - 7th Harmonic Current vs. M1 % Load for M2 @ 100% Load

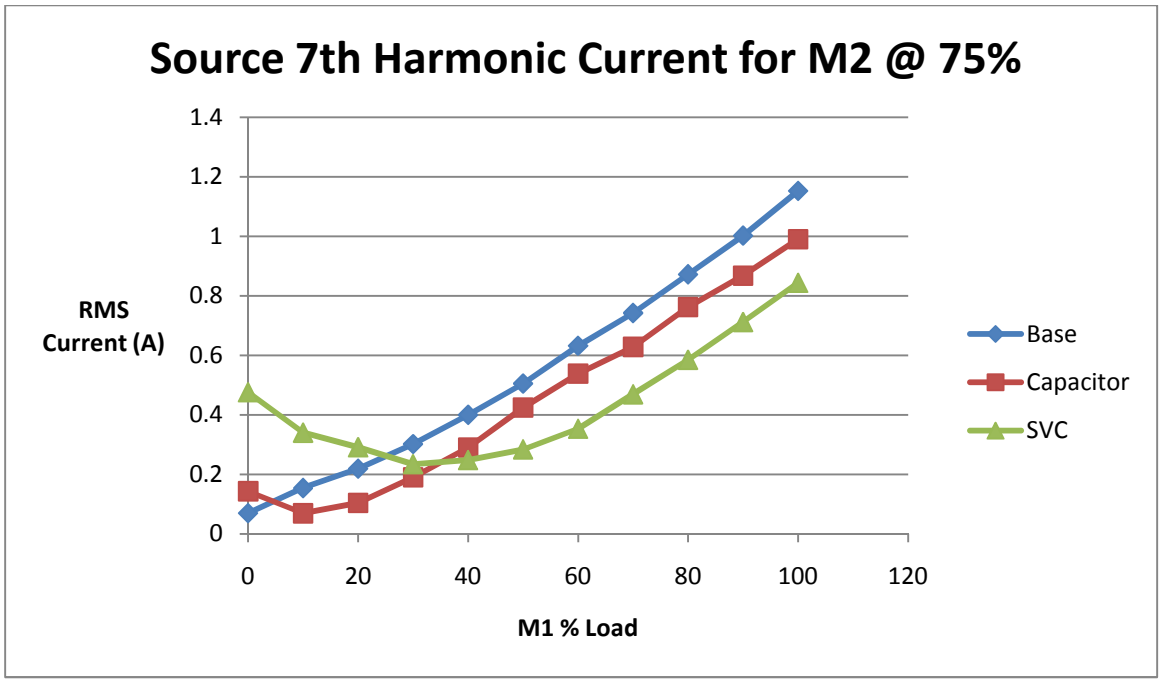

Figure 5.15 - 7th Harmonic Current vs. M1 % Load for M2 @ 75% Load

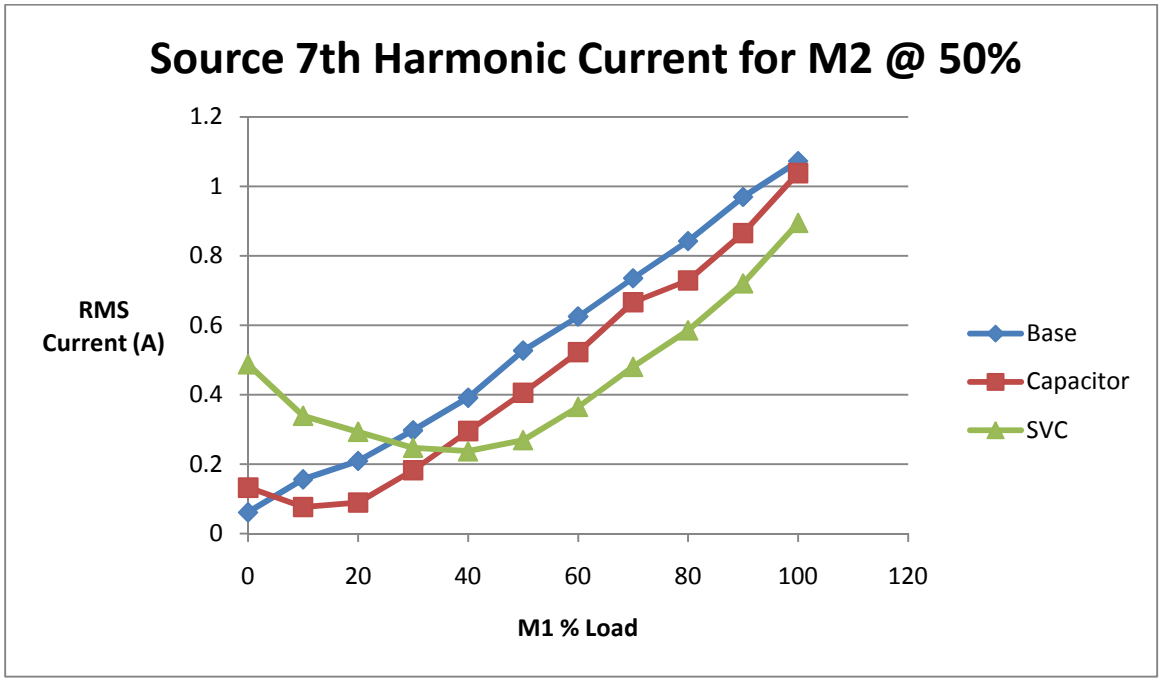

Figure 5.16 - 7th Harmonic Current vs. M1 % Load for M2 @ 50% Load

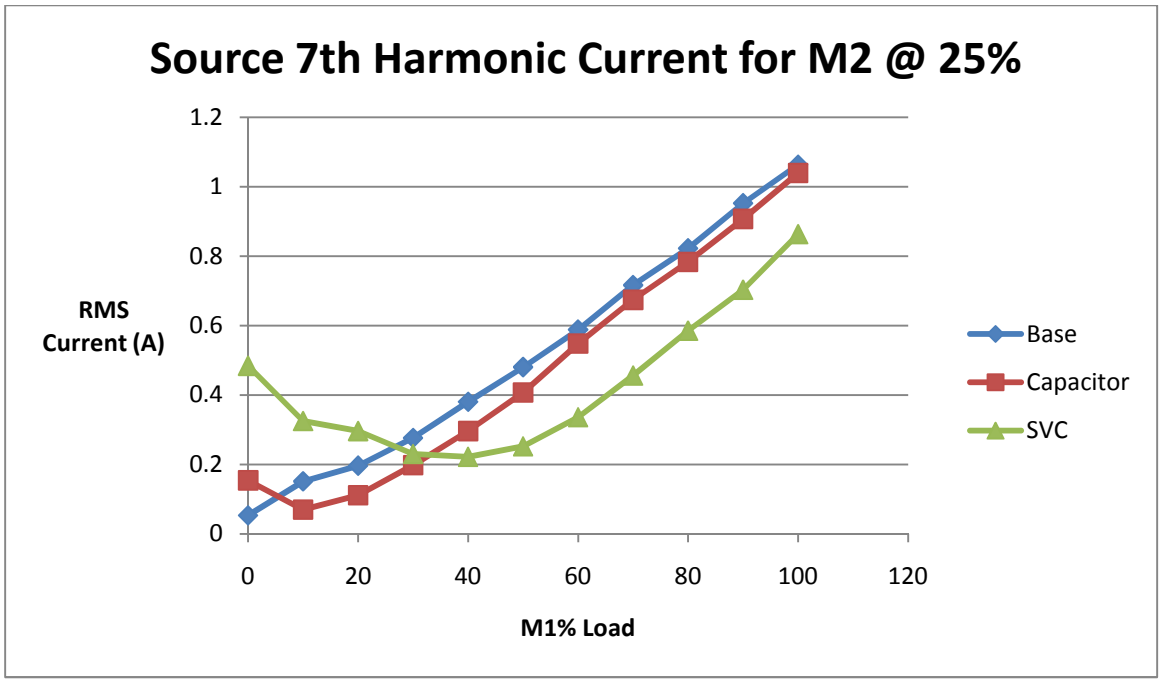

Figure 5.17 - 7th Harmonic Current vs. M1 % Load for M2 @ 25% Load

Unlike the 5th harmonic, the 7th harmonic shows the opposite results with the SVC having the lowest content and the base case the highest. For the 5th harmonic all three cases had the same magnitude when M1 was at 0% load. However, with the 7th harmonic the SVC begins at 0.5A while the other two cases start at close to 0A. Since the impact of the VFD on the system is very small when M1 is at 0%, all of the harmonic content at this point is likely a result of the SVC. Once the VFD begins drawing current, the magnitude of the 7th harmonic decreases for the SVC until M1 reaches 40%. Given that the harmonic was greater before the VFD began operating, it is likely that there is some cancellation occurring between the SVC and the VFD. Once M1's load increases beyond 40%, the harmonic magnitude starts to increase at the same rate as the base case, while continuing to be less than it. In addition to any cancellation that occurs between the SVC and VFD, the 7th harmonic is also less for the capacitive case. This suggests that at the

7^{th} harmonic the frequency is high enough that the capacitor begins to sink a more noticeable amount of the harmonic current. While this could also be occurring for the SVC, the fact that the SVC still has a significantly smaller magnitude than the capacitive case suggests that some cancellation is occurring with the VFD's 7^{th} harmonic.

It is also interesting to look back to Figure 3.4, which showed the expected harmonics of a TCR for different firing angles. In section 4 we showed that the SVC, which is composed of a TCR, should operate with a firing angle between 40° and 60°, with the angle increasing as the load increased. From Figure 3.4 we see that the 5^{th} harmonic is at its lowest point at a firing angle of 40° and then increases to a relative maximum at 60°. Meanwhile, the 7^{th} harmonic is at a relative maximum at 40° before decreasing to a minimum at 50° and then increasing through 60°. Both these trends are shown in the data collected and displayed in Figures 5.10-5.17 if we remember that the firing angle will increase with M1 loading. These figures illustrate, as predicted by Figure 3.4, that the 5^{th} harmonic increases when alpha goes from 40° to 60°, while the 7^{th} initially decreases before increasing. Additionally, Figure 3.4 showed that the 7^{th} harmonic actually has a higher magnitude than the 5^{th} harmonic at a firing angle of 40°. This is also confirmed in our data, where the 5^{th} harmonic has an initial magnitude of 0.1A compared to the 7^{th} harmonics magnitude of 0.5A. Also, supported by both our data and Figure 3.4 is that the 5^{th} harmonic has a higher amplitude than the 7^{th} harmonic when α is 60°, 1.8A compared to 0.9A.

Looking solely at the 5^{th} and 7^{th} harmonics one would expect all three cases to have similar THDi% levels. The difference must than come from the summation of many small magnitudes at higher harmonic levels. It would, however, be too exhaustive

to explore the minute variations in current for multiple harmonic orders, nor would it be beneficial as the largest harmonic magnitudes still occur at the 5th and 7th levels.

5.5 K-Factor

The primary concern for transformers supplying non-linear loads is the additional heat generated by the harmonic currents. Harmonic currents increase the copper losses in a transformer through additional eddy current and skin effect losses. These losses are proportional to the frequency squared and therefore higher level harmonics pose a greater threat to transformers [4] [24] [7]. K-Factor is a commonly used index which gives weight to the frequency as well as the magnitude of the harmonic currents. Special K rated transformers are made which have been designed to handle harmonics up to their corresponding K-Factor. When a transformer is exposed to a number of harmonic loads, it is often more cost effective to purchase a K-Rated transformer as opposed to over sizing a regular transformer.

The PowerSight analyzer records K-Factor values, defining it to be [25]:

$$KFactor = \sum_{h=1}^{50} \frac{(I_h h)^2}{I_{rms}} = \frac{1}{I_{RMS}}[(I_1)^2 + (2I_2)^2 + (3I_3)^2 + \cdots + (hI_h)^2] \quad (5.15)$$

Figures 5.18 -5.21 show the K-Factor as recorded on the secondary side of the transformer. When looking at the K-Factor it is important to look at the load side of the transformer before any harmonics are cancelled by the Δ-Y phase shift.

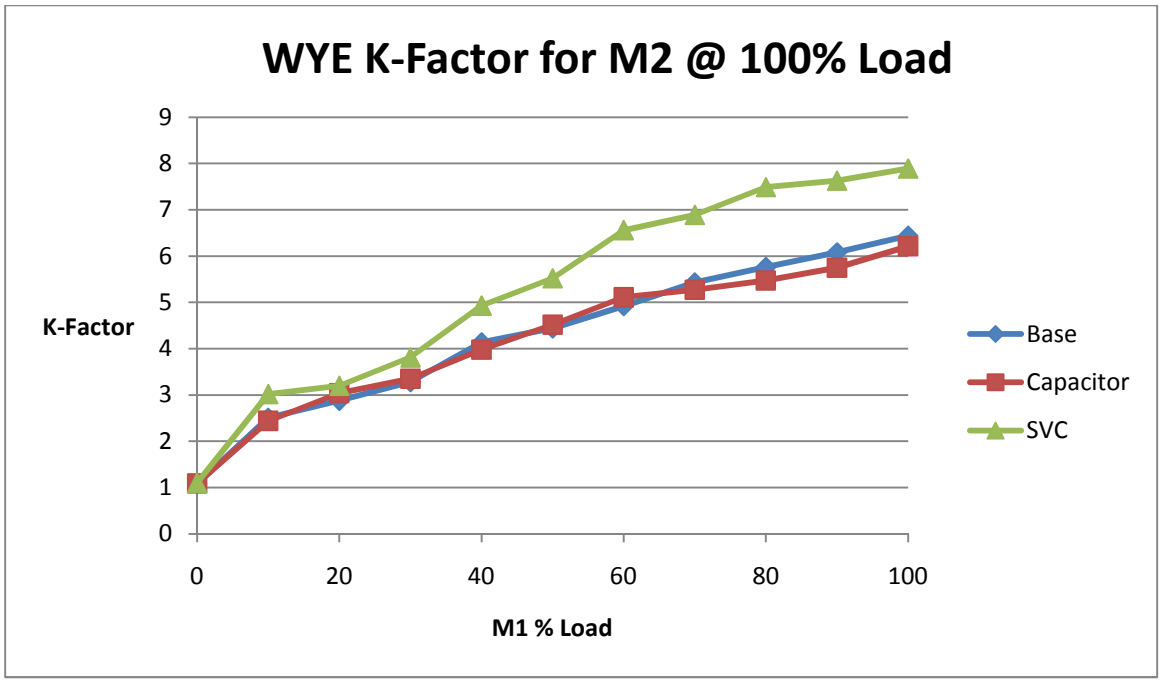

Figure 5.18 - K-Factor at Secondary Side for M2 @ 100% Load

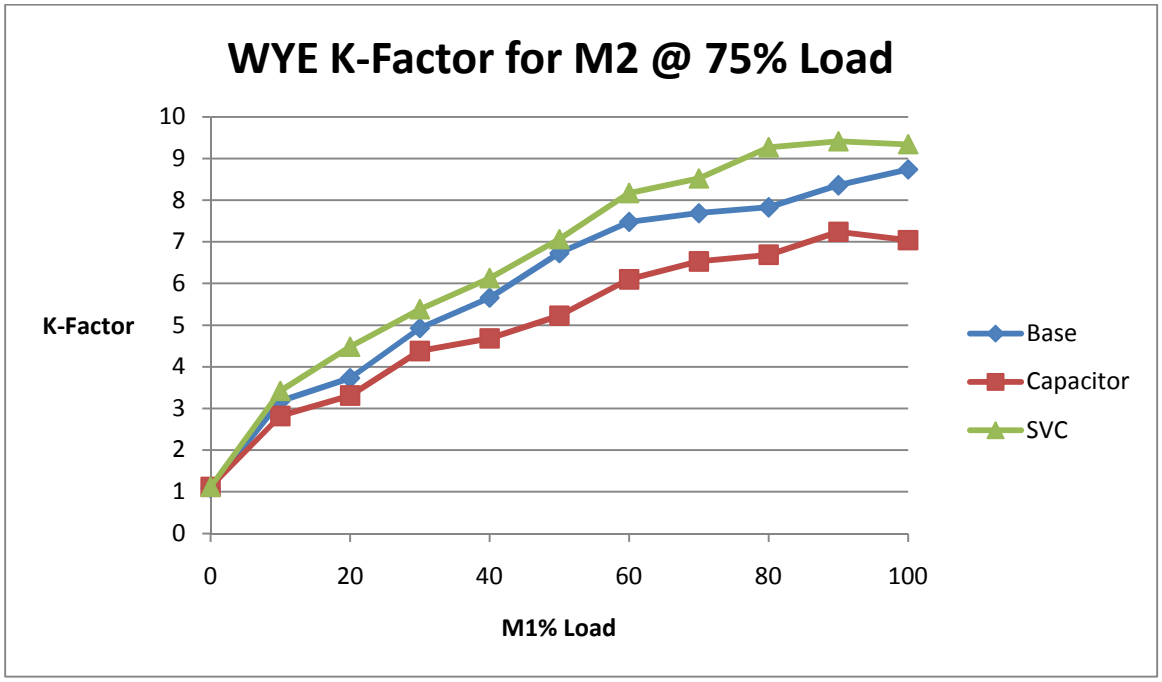

Figure 5.19 - K-Factor at Secondary Side for M2 @ 75% Load

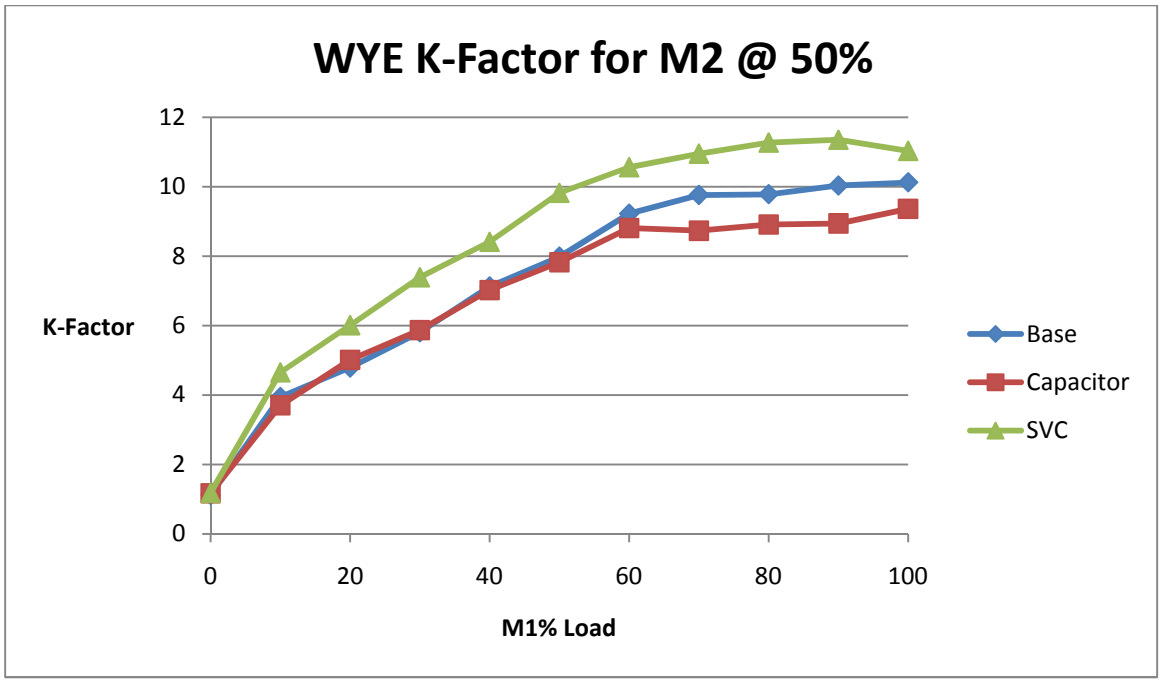

Figure 5.20 - K-Factor at Secondary Side for M2 @ 50% Load

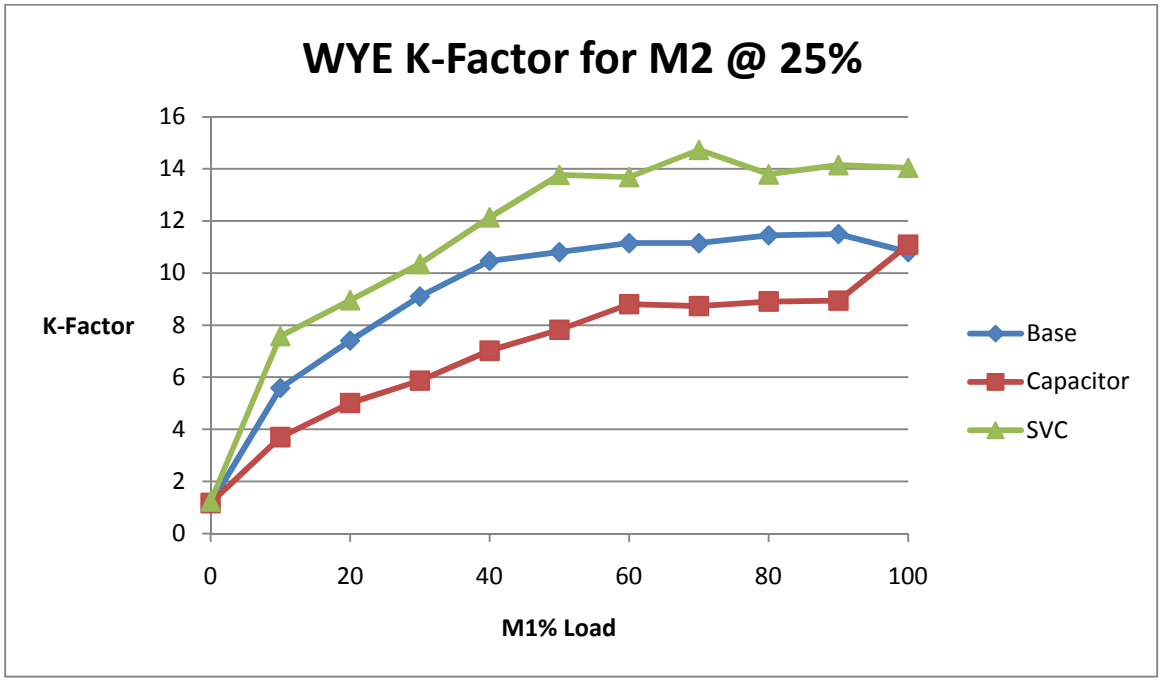

Figure 5.21 - K-Factor at Secondary Side for M2 @ 25% Load

The general trend from Figures 5.18-5.21 is that the SVC has the highest K-Factor rating while the capacitor compensation case has the lowest, with the discrepancy increasing as M2's load decreases. When examined closer it is logical that the capacitive case would generally have the smallest K-factor of the three cases. Since capacitors have low impedance for high frequencies much of the higher harmonic current will be trapped by the capacitors and not reflected back to the transformer [5]. While the SVC also contains capacitors, the additional harmonics current it generates is greater than whatever is trapped by its capacitors. As concluded in section 5.4, the SVC must generate small but noticeable currents at high harmonic frequencies in order to have a THDi% significantly greater than the base case. Given the additional weighting placed by the K-Factor calculation on frequency it follows that the SVC would have a higher K-Factor. The base case benefits from having only one harmonic source, the VFD, but since there is no additional capacitance its K-factor is better than the SVC but worse than the capacitive case. As we have seen with THDi%, the K-factor becomes worse for all cases when M2 decreases since the total RMS current is less while the harmonics from M1 remain unchanged.

Since K-Factor transformers are only manufactured for standard K values of 4, 9, 13, and 20, differences between the three cases only become significant when they require a higher rated transformer. For example, if M2 was planned to be continually operated at full load, Figure 5.10 shows that even though the SVC has the highest K-Factor, all three cases would require a transformer with a K rating of 9. However, if M2 was known to operate at loads as low as 25% then the SVC would require a K rated transformer of 20, while the other two methods would require one of 13. If the

transformer was chosen to be oversized, as opposed to K-rated, the derating chart shown in Figure 2.1, shows that the SVC method would likely result in a transformer 10% larger than the other methods. Under either scenario the SVC increases the K-Factor enough to warrant a larger, and thus more expensive, transformer.

It is also worth noting that while the capacitors help protect the transformer against higher harmonics, this is not an entirely good thing. As discussed in chapter two, by sinking higher frequency currents a capacitor's heating and dielectric stresses increase shortening its life span [5]. This combined with the possibility of resonance, means that capacitors used in conjunction with non-linear loads should be sized carefully and in accordance with IEEE Std 18-1992.

5.6 Analysis of Voltage Distortion

In addition to limits on the current distortion that a customer can reflect back to the utility, IEEE Std 519-1992 also defines the acceptable voltage distortion levels at the PCC.

Table 5.3 - IEEE 519-1992 Voltage Distortion Limits

Bus Voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD (%)
69 kV and below	3.0	5.0
69.001 kV through 161 kV	1.5	2.5
161.001 kV and above	1.0	1.5

For low and medium voltage systems under 69kV, such as this experimental setup, the maximum THDv% that can appear at the PCC is 5%. This guideline assumes the THDv% is present for at least an hour and not just the result of a transient or start-up condition in which case the limit may be exceeded by 50% [5]. Figures 5.22-5.25 display the THDv% levels at the PCC of our system, the source point A.

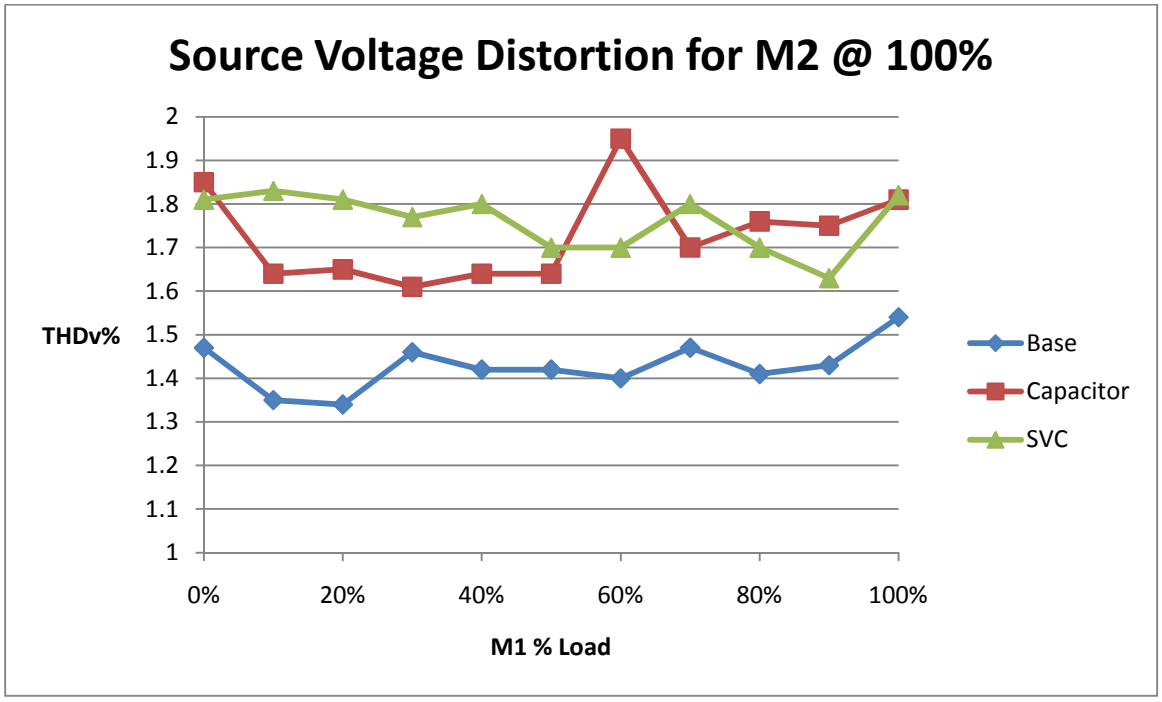

Figure 5.22 - Source THDv% vs. M1 % Load for M2 @ 100% Load

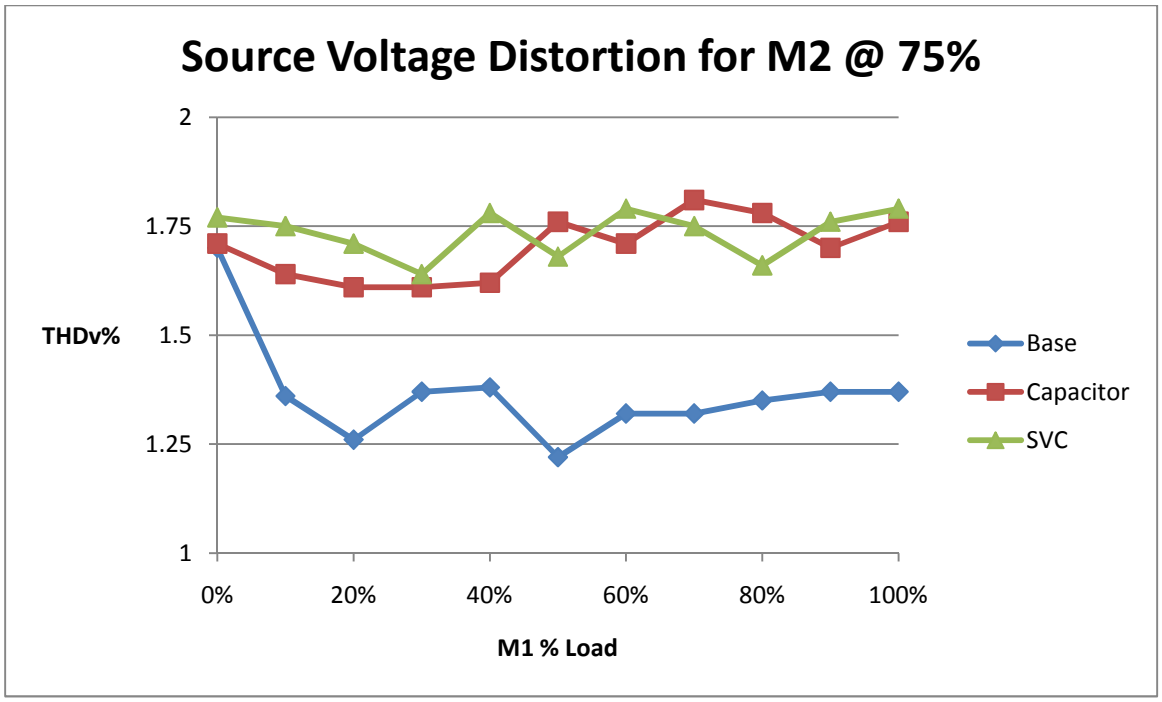

Figure 5.23 - Source THDv% vs. M1 % Load for M2 @ 75% Load

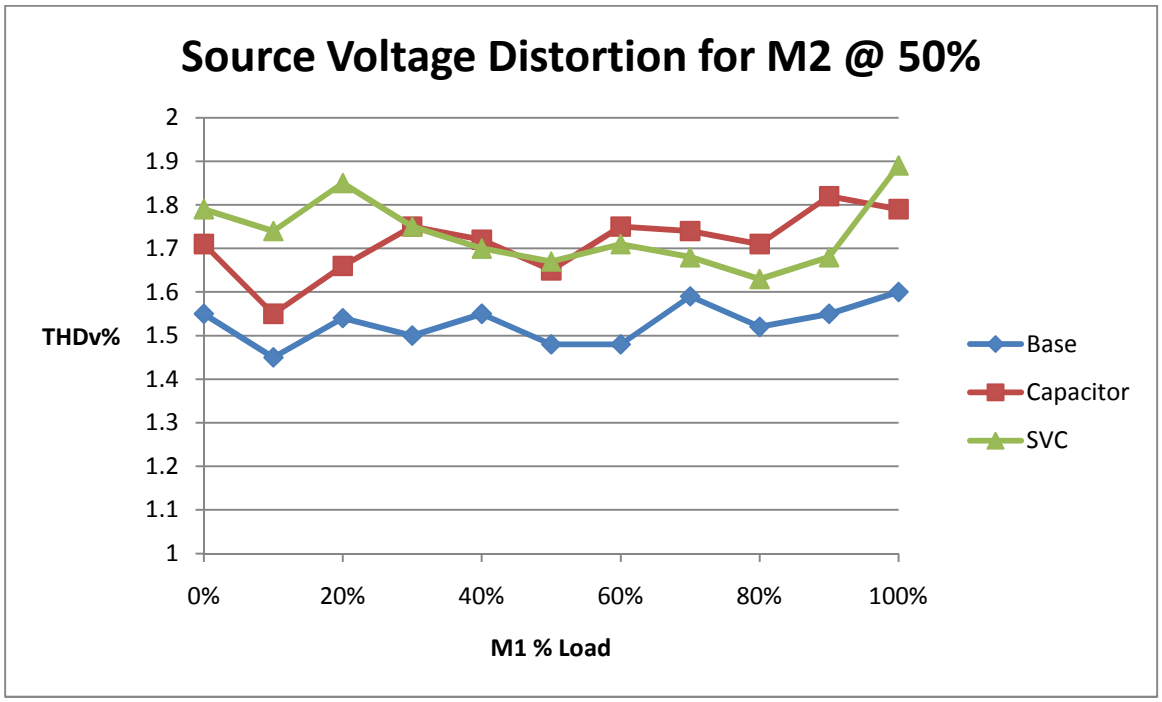

Figure 5.24 - Source THDv% vs. M1 % Load for M2 @ 50% Load

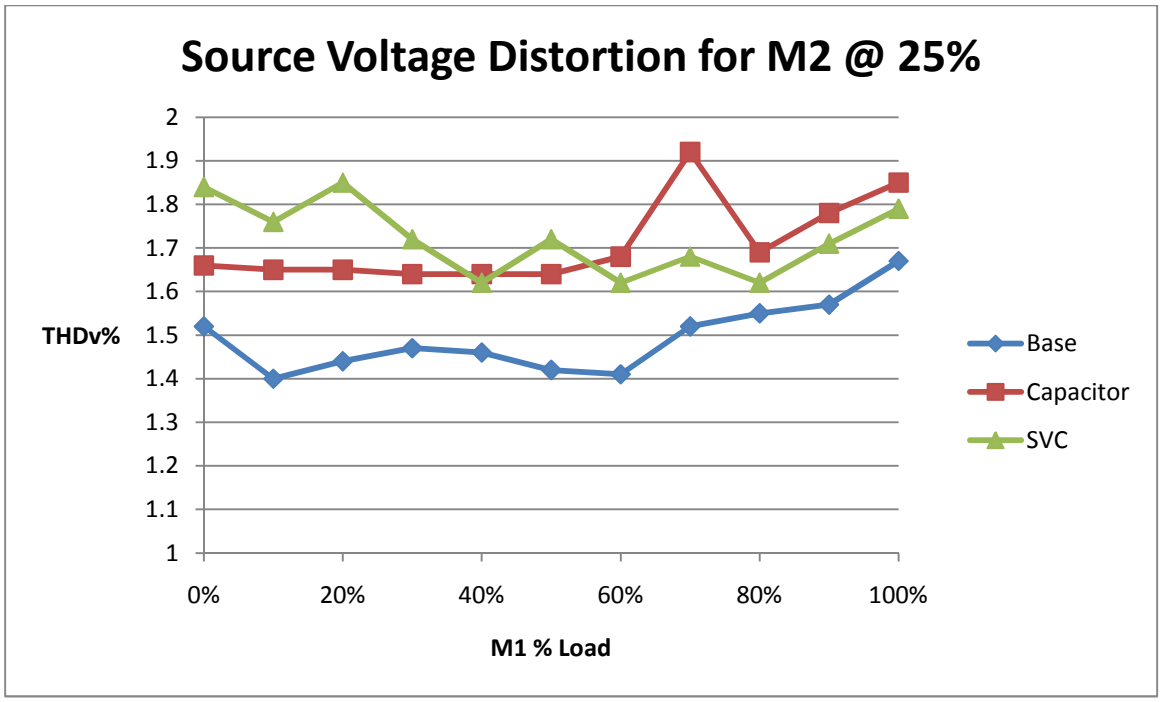

Figure 5.25 - Source THDv% vs. M1 % Load for M2 @ 25% Load

For all cases the THDv% was kept well below the 5% IEEE guidelents. Generally speaking the THDv% stays constant regardless of the changes in loading to M1 or M2. When the load increases the voltage ideally stays unchanged while the current increases. Since a change in load shouldn't significantly change the voltage, it is reasonable to see little variation in the THDv% levels. The main trend to in the preceding figures is that the base case THDv% is typically 0.1% to 0.4% lower than either the capacitive or SVC methods. While this number is small, its appearance in all of the data suggests that capacitive and static var compensation both increase the source THDv% by a small amount. Since our system is well beneath the IEEE guidelines this small increase in THDv% is not too important. However, for a system which is already close to its

THDv% limits the addition of one of these compensation methods could push it past the recommended guidelines.

5.7 Power Factor

The main purpose of the static var compensator is to supply or absorb VARs to meet the demands of the system and thereby improve the displacement power factor of a system. Its switch based design gives it the flexibility to compensate over a wide range of leading and lagging power factors, as opposed to traditional power factor correction which provides the same amount of reactive power regardless of the systems needs. As the previous sections have shown this comes at the cost of increased harmonic levels in the system. This section will look at how the SVC is able to affect the power factor of the system in comparison to the other two cases.

When viewing the power factor results there are a couple of items that should be remembered. First, the main advantage of the SVC is its ability to compensate a system through a large range of VAR requirements, both for a lagging and leading power factor. Since the system under test could only produce a lagging power factor, the SVC's ability to correct for a leading power factor goes unnoticed in this analysis. Were the system to feature a leading power factor, capacitive compensation would worsen the overall power factor while the SVC would improve it. Additionally, the range of VAR requirements for this setup is small, 890-1332VAR, meaning that classical capacitive power factor correction will be able to compensate the system very well. From the capacitor sizing discussion of chapter 4, it was shown that under the maximum VAR requirements the capacitors would be able to bring the system to a displacement power factor of 0.97 and

under the minimum requirements the system would have almost unity displacement power factor. If the system VAR requirements were for a wider range, such as 200-2000VAR, the SVC would be able to compensate for all cases equally, while capacitive compensation would either drastically over compensate the low end of the spectrum or be unable to supply enough VARs to compensate at the high end of the range. Finally, both capacitive compensation and SVC can only correct the displacement power factor. Due to harmonics from the VFD and SVC, neither compensation method will be able to achieve a unity true power factor. Any additional power factor correction would have to account for the distortion power factor through line reactors and filters.

With this in mind, any differences between the displacement power factor for the capacitive and SVC cases will be relatively small. These differences can be seen in Figure 5.18.

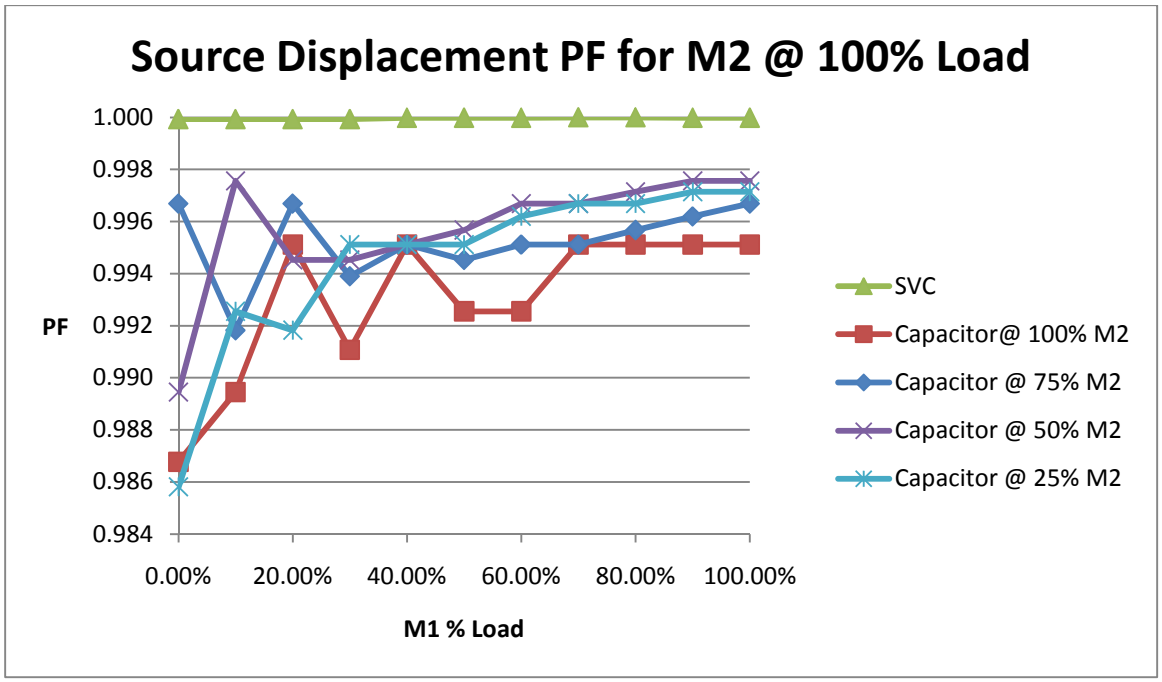

Figure 5.26 - Source Displacement PF for SVC vs. Capacitive Compensation

Here the SVC has a unity displacement power factor at the source for all loading conditions and the capacitive case has a displacement power factor between 0.986 and 0.998. This range corresponds to the current lagging the voltage by 4 to 10 degrees under capacitive compensation, while the currents and voltages are completely in phase for the SVC case.

When comparing the two methods of compensation, the small advantage of the SVC in displacement power factor is negated by the equally small advantage of the capacitors in distortion power factor. The distortion power factors for the three cases are shown in Figures 5.27-5.30.

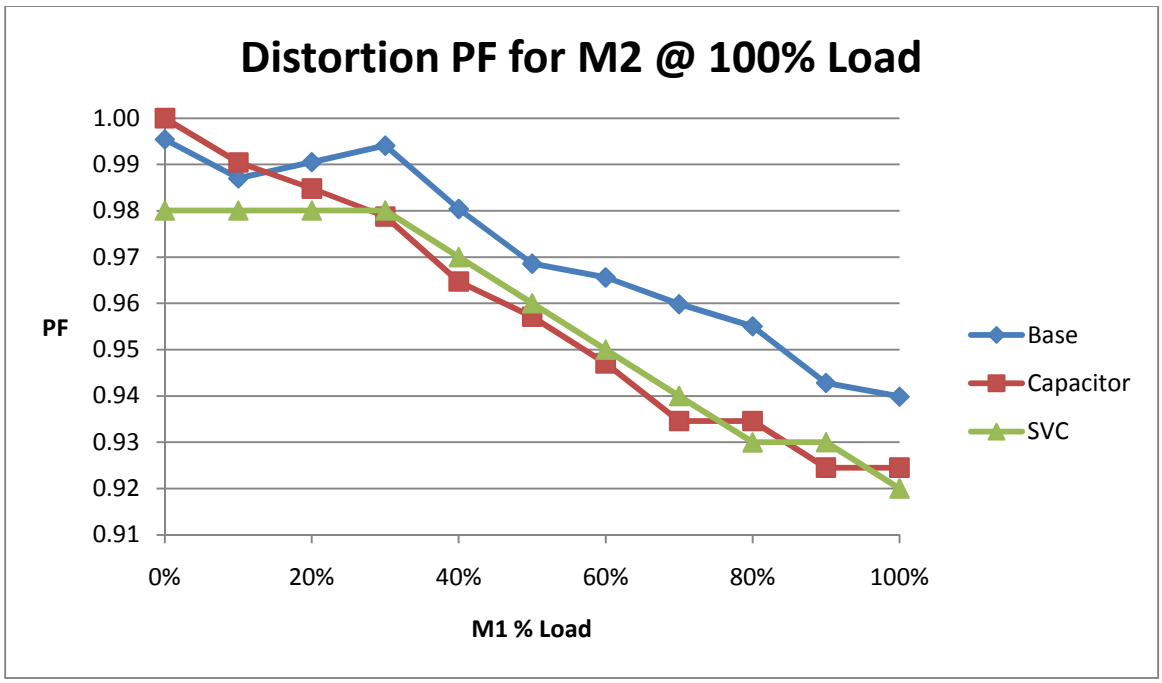

Figure 5.27 - Distortion PF vs. M1 % Load for M2 @ 100% Load

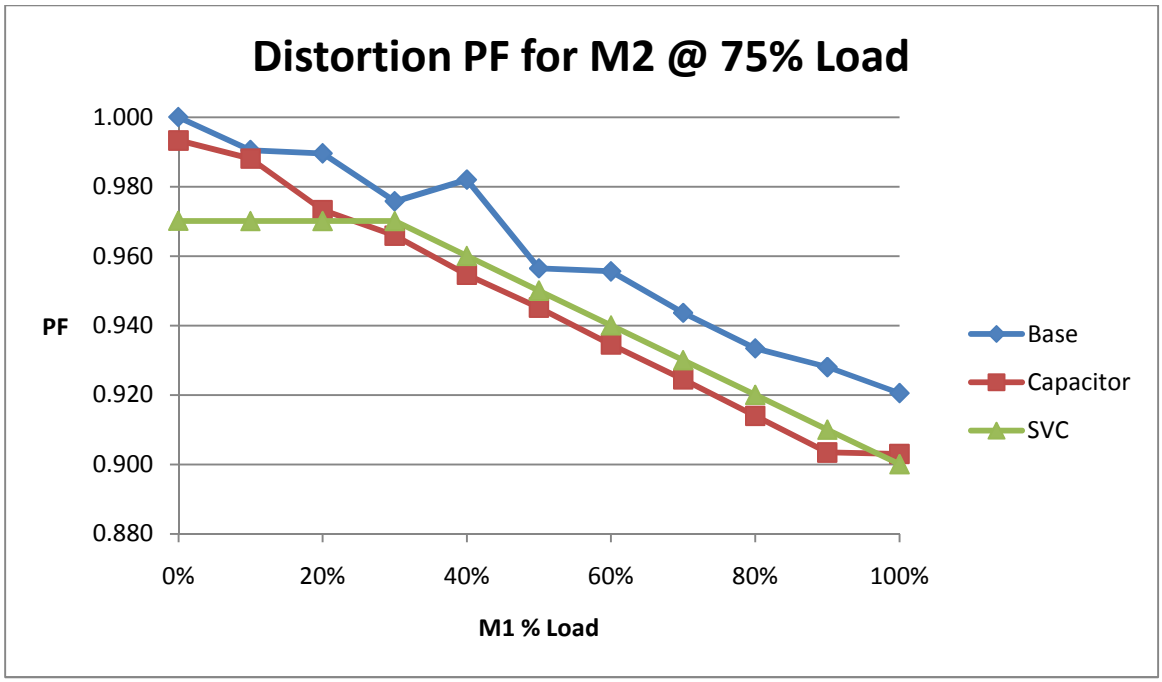

Figure 5.28 - Distortion PF vs. M1 % Load for M2 @ 75% Load

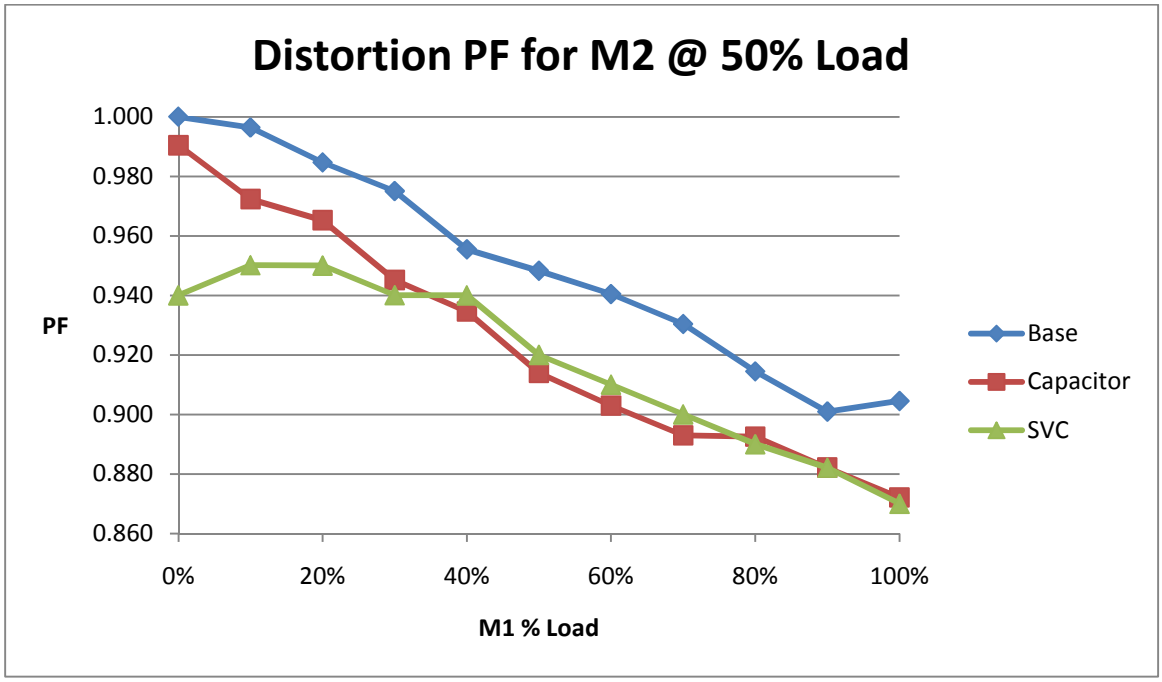

Figure 5.29 - Distortion PF vs. M1 % Load for M2 @ 50% Load

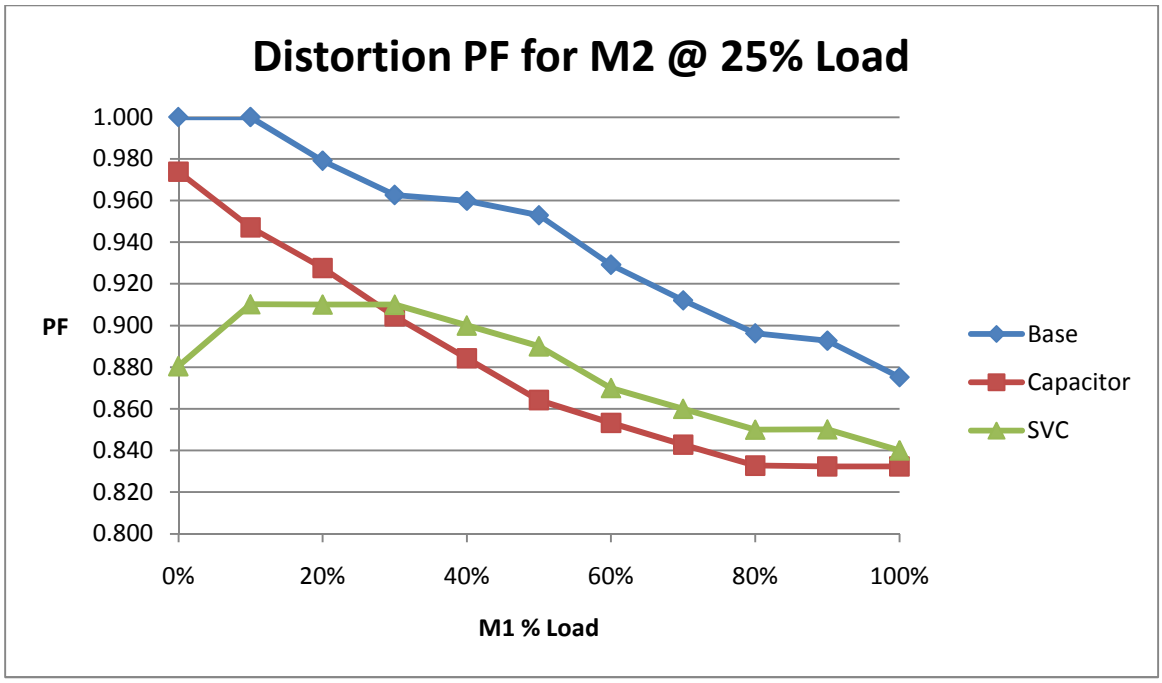

Figure 5.30 - Distortion PF vs. M1 % Load for M2 @ 25% Load

Since distortion power factor is a result of harmonics, the graphs in Figures 5.27-5.30 are a reflection of the THDi% graphs from Figures 5.2-5.5. As with THDi%, the distortion power factor is noticeably better for the base case since only one true harmonic source is present. The capacitive case is better than the SVC when M1 has a light load, since the SVC current and harmonics make up a larger percentage of the overall system current and harmonics. This difference is made up when M1 is loaded above 50%. For most of these data points the SVC actually has a higher distortion PF than the capacitive case. However, as the graphs show the difference between the two in distortion PF is much greater at low M1 loading than at high M1 loading. As a result the true power factor will be several points higher for the capacitive case at low M1 loading and the SVC will be just slightly higher for higher M1 loading. The true power factor for all

loading scenarios is listed in Table 5.4. The general trend of the true power factor for the three cases, as M1 loading increases, can be seen in Figure 5.23 for M2 at 100% load.

Table 5.4 - True Power Factor at the Source (Point A)

	Motor 2 @ 100%			Motor 2 @ 75%			Motor 2 @ 50%			Motor 2 @ 25%		
M1 % FLT	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100	0.84	0.92	0.92	0.8	0.9	0.9	0.77	0.87	0.87	0.76	0.83	0.84
90	0.83	0.92	0.93	0.79	0.9	0.91	0.75	0.88	0.88	0.74	0.83	0.85
80	0.83	0.93	0.93	0.78	0.91	0.92	0.74	0.89	0.89	0.72	0.83	0.85
70	0.82	0.93	0.94	0.77	0.92	0.93	0.73	0.89	0.9	0.69	0.84	0.86
60	0.81	0.94	0.95	0.76	0.93	0.94	0.71	0.9	0.91	0.66	0.85	0.87
50	0.8	0.95	0.96	0.74	0.94	0.95	0.69	0.91	0.92	0.62	0.86	0.89
40	0.79	0.96	0.97	0.73	0.95	0.96	0.66	0.93	0.94	0.58	0.88	0.9
30	0.78	0.97	0.98	0.71	0.96	0.97	0.64	0.94	0.94	0.54	0.9	0.91
20	0.77	0.98	0.98	0.7	0.97	0.97	0.62	0.96	0.95	0.5	0.92	0.91
10	0.76	0.98	0.98	0.68	0.98	0.97	0.6	0.97	0.95	0.48	0.94	0.91
0	0.74	0.99	0.98	0.66	0.99	0.97	0.56	0.98	0.94	0.4	0.96	0.88

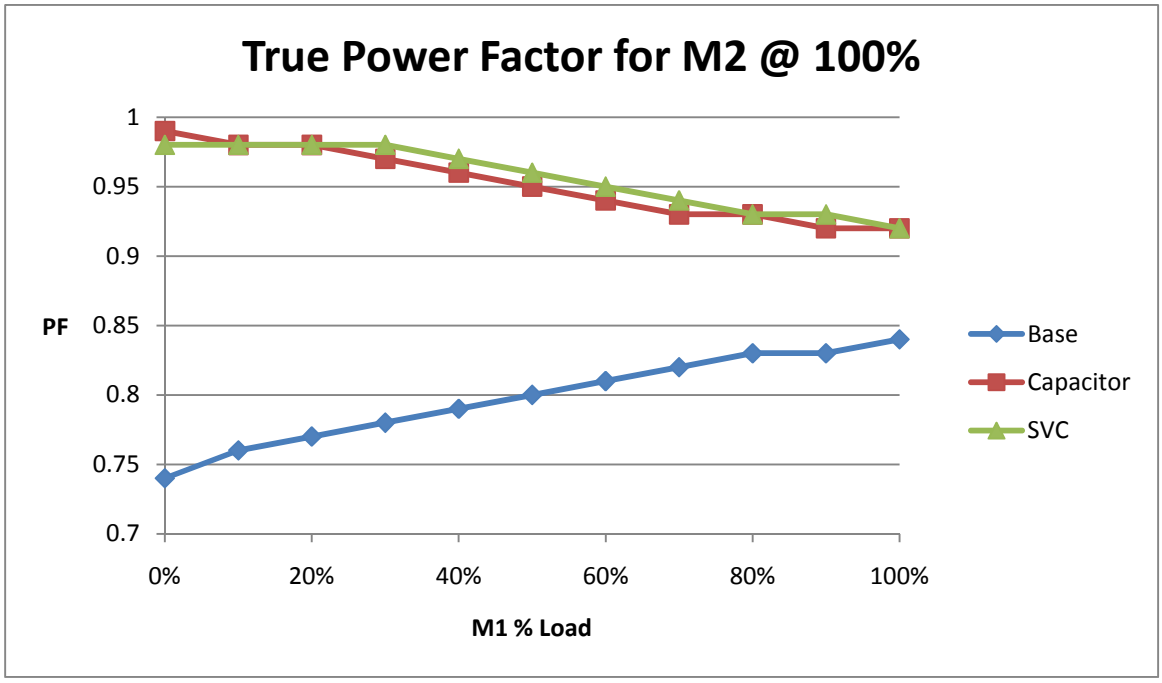

Figure 5.31 - True Power Factor vs. M1 % Load for M2 @ 100% Load

As expected Figure 5.31 shows that the capacitive and SVC compensation methods perform very similarly, with the SVC working better for higher M1 loading and the capacitive case has the edge at low M1 loading. The base case increases its power factor as M1 loading increases. Since the VFD draws current in phase with the voltage the source displacement power factor improves as M1 draws more current. While a higher M1 load will increase the harmonics and lower the distortion power factor, the increase in harmonics is smaller in comparison to raised levels of zero displacement current drawn from the source for the base case. However, the other two cases exhibit the opposite characteristic where there true power factor decreases as M1 increases. Since both cases provide enough compensation that the current and voltage are nearly in phase, the increase in M1 in phase current has no real effect on the true power factor. Instead the true power factor declines as M1 loading increases since the harmonics increase while the displacement power factor is left unchanged. To best see the small differences in the cases, consult Table 5.4 for the true power factor for different M2 loadings.

5.8 Efficiency

Often the primary reason for a facility to implement power factor correction is to reduce power factor surcharges from the utility. While this is often provides the largest cost savings, power factor correction also reduces power systems losses and increases the load carrying capability of existing transmission lines [4]. Both of these benefits arise from a reduction in RMS current that results from power factor correction. Copper losses in transmission lines, motors, and transformers are proportional to the square of the RMS current meaning that substantial savings occur when the RMS current is reduced. Figure

5.32-5.35 shows how the RMS current is reduced at the source as a result of power factor correction.

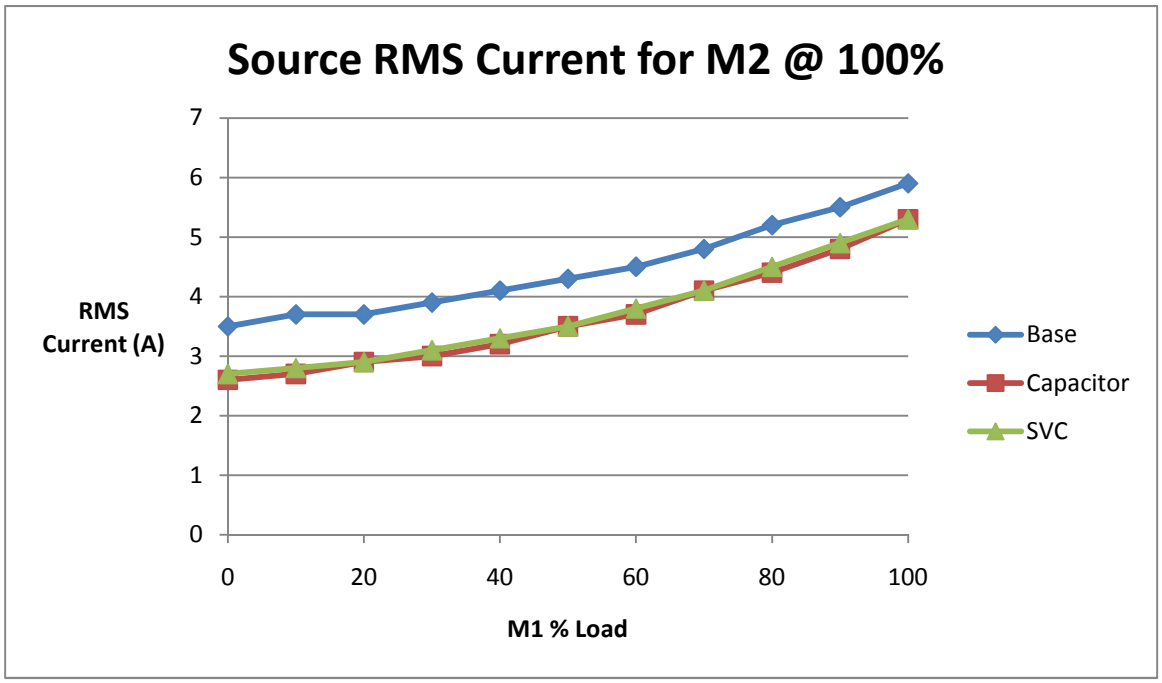

Figure 5.32 - Source RMS Current vs. M1% Load for M2 @ 100% Load

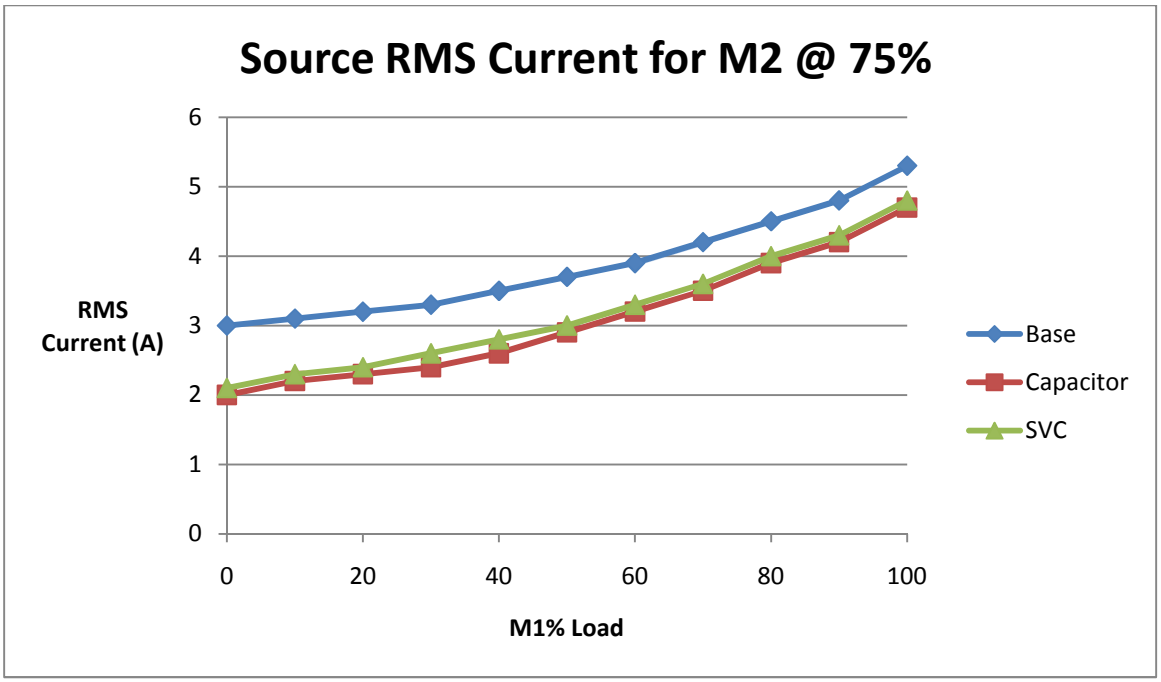

Figure 5.33 - Source RMS Current vs. M1 % Load for M2 @ 75% Load

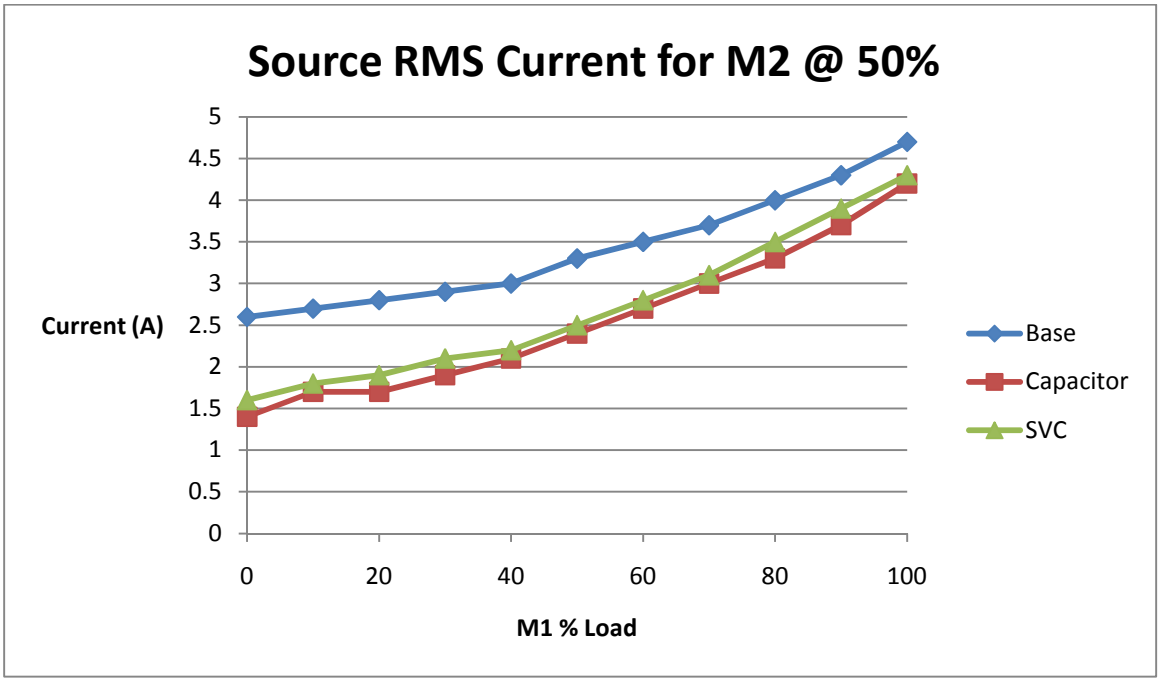

Figure 5.34 - Source RMS Current vs. M1 % Load for M2 @ 50% Load

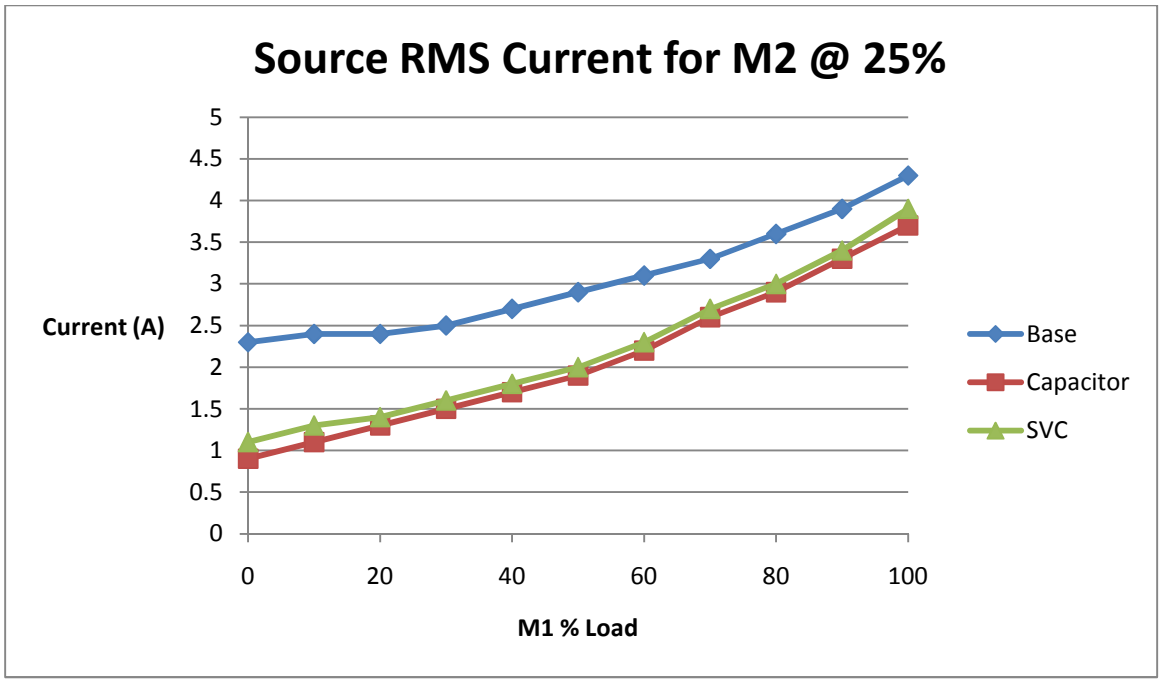

Figure 5.35 - Source RMS Current vs. M1 % Load for M2 @ 25% Load

The RMS current graphs shown in Figures 5.32-5.35 follow the same trends that the true power factor graph showed. Overall, the capacitive and SVC result in about the same reduction in RMS current, which is expected since both methods produced similar true power factors at the source. The two compensation methods result in a RMS source current that is 0.5-1.5A smaller than the base case. This is an impressive 10%-60% drop in current from the base case depending on the load. To illustrate the potential cost savings of RMS current reduction, let's assume that the test system is a low voltage distribution point within an industrial plant. If we assume that a typical 10AWG copper wire, with an ampacity of 15A, has an AC resistance of 1.2 ohms per 1000ft, as given in Table 9 of the NEC 2008 Code, and the transformer is 1000ft from its source the total copper loss in the distribution line can be calculated as [26]:

$$P_{Loss} = I_{rms}^2 * \frac{\Omega}{ft} * ft * \Phi \tag{5.16}$$

Using equation 5.16, where Φ is the number of phases , Figure 5.36 shows the expected power savings in a 1000ft distribution line, for the SVC verse the base case.

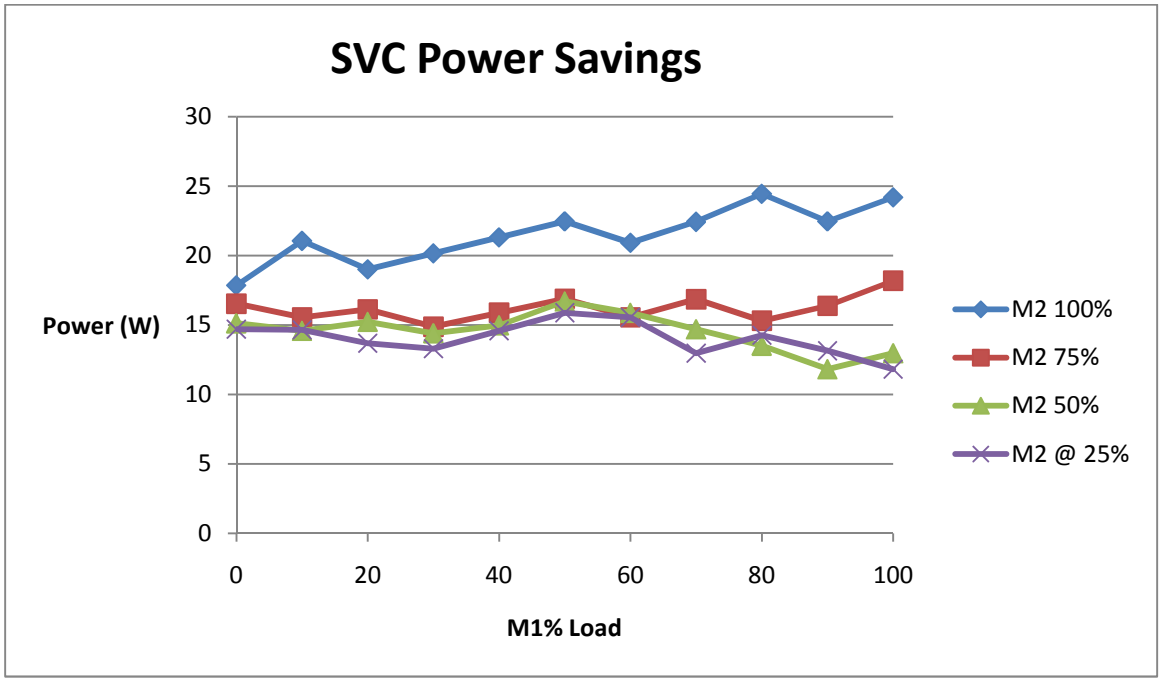

Figure 5.36 - SVC Power Saved Compared to Base Case vs. M1% Load

Since the SVC and capacitive compensation methods provided nearly the same RMS current, the reduction in losses shown in Figure 5.36 would roughly be the same for the capacitive case. The results of Figure 5.36 show that the reduction in RMS current could result in a 10-25W savings per phase. This savings represents close to 2% of the load demand power. Considering the load of our system is small, about 1.5kW, the actual cost savings over a year at $0.13/kWhr would be small, about $29 [27]. However,

it is easy to see that the 2% savings as a result of power factor correction could save significant money if applied to large industrial systems that have yearly electric costs exceeding $100,000. These savings also do not account for reduced utility surcharges due to poor power factor or from the increased power carrying capacity of the distribution lines.

CHAPTER 6 – RECOMMENDATIONS AND CONCLUSIONS

6.1 Conclusions

Based on the analysis of the data presented in this thesis, several conclusions may be drawn about the overall effectiveness of the different cases and the harmonics generated by the power electronic devices used in the system.

In section 5.3 we showed that all three compensation cases exceeded the IEEE limits for total current harmonic distortion at the source, when M1 was loaded above 40%. As a result, it was suggested that to meet IEEE guidelines the transformer should either supply additional linear loads or line reactors should be used to filter the VFD harmonics. Later in section 5.6 it was seen that the total voltage harmonic distortion at the PCC was beneath IEEE guidelines for each case. Since all three cases performed similar compared to IEEE Std 519-1992, the selection of which compensation method best fits our system can be decided solely by intersystem harmonics, power factor improvement, and overall costs.

When examining intersystem harmonics the SVC had a higher K-Factor at full load than either of the other cases. However, since K-Factor transformers come in standard sizes all three cases would still require the same K-9 transformer. The affects of the higher K-rating would still be seen though in the form of increased losses in the transformer. When the harmonics at Motor 2 were discussed it was seen that capacitive compensation produced more current distortion than either the SVC or base cases. This

increased harmonic current will result in lower efficiency and could shorten the life span of the motor.

For power factor improvement both the capacitive and SVC cases significantly outperformed the base case. The differences between the capacitive and SVC cases were minor as they both typically resulted in high power factors. If the system were to be run for significant periods of time with low VFD loading the additional harmonics generated by the SVC would become more apparent. In that case capacitive compensation would be more practical than static var compensation.

Since both SVC and capacitive compensation improved power factor comparably, they also both resulted in a similar reduction in RMS current compared with the base case. By reducing the RMS current the power losses throughout the system would be reduced. Equipment such as circuit breakers and cables could also be sized smaller [6]. These benefits could result in significant cost reduction.

6.2 Recommendations

For the case studied in this thesis, capacitive compensation would have been the best solution. Capacitive compensation provided the same benefits as the SVC but with slightly less overall harmonic content. Additionally, the capacitive case required only 3 capacitors, while the SVC need 6 capacitors, 3 inductors, 6 thyristors and an externally powered firing board. This additional equipment and costs make the SVC a less practical choice for our given setup.

However, our data showed that the differences between harmonic content is small enough that a SVC could be used instead of typical power factor correction. Given a

system with a wider range of VAR requirements, or one whose power factor varied between leading and lagging, the SVC would be the best option.

In some instances, where displacement factor is high and distortion factor is low, line reactors can provide the most effective means of correcting power factor while mitigating harmonics. Since our base case typically had distortion power factors above 0.95 while the displacement power factor was between 0.7-0.8 line reactors would not have significantly changed the power factor. However because the system did not met the IEEE guidelines for TDD current generated at the source line reactors would be recommended.

In the end it is difficult to draw general conclusions from a two motor, 2KVA system which remain applicable to large systems operating at multiple MVAs. Each system must be analyzed individually to determine what type of power factor correction or harmonic mitigation techniques will give it the best combination of performance, cost and safety. What this experiment did show was that all methods of compensation should be considered equally. Just because the SVC generates harmonics doesn't prohibit it from being used in a system already containing harmonics. In fact our study showed that while the SVC does increase most harmonic measurements this increase is not significantly greater than the effect of adding shunt capacitors. Similarly, the SVC should not be selected simply because it can adjust its compensation to always maintain a unity displacement power factor. For small ranges of VAR requirements properly designed static capacitors banks will compensate a system just as well as an SVC and for a fraction of the cost.

Like many things, designing power systems involves choosing between various tradeoffs. Once we accept that our system will be imperfect and contain some voltages and currents that are unbalanced, out of phase, and distorted we can seek a solution that minimizes costs while maximizing safety and reliability.

6.3 Additional Suggested Research

The findings of this thesis provide a good initial look at the harmonics of a static var compensated mixed load system. However, there are several aspects of the thesis which could be improved or studied further.

First, no attempt was made in this thesis to filter or mitigate harmonics. An additional study should be performed following the same setup but adding VFD line reactors. Besides the VFD filtering, shunt filters could also be tuned to help eliminate harmonics from the SVC. With these filters, it would be interesting to see whether the system meets IEEE limits for TDD current at the source. Furthermore, tuning shunt filters to the SVC could help establish how much harmonic cancellation really occurs between the VFD and the SVC.

Aside from filtering, conducting this study for a load which could provide a leading and lagging power factor would show the true benefits of a SVC. With this setup, classical capacitive compensation would worsen the leading power factor case but likely have fewer harmonics than the SVC case. The pros and cons of this could be compared against the SVC's ability to compensate the leading case but at the expense of additional harmonics. Besides providing leading and lagging power factor, the system load could require a larger range of VAR requirements to better show the benefits of a

SVC. An increased disparity in VAR demand would also require the SVC to operate over a greater firing angle range. This would allow the differences in SVC harmonics to be compared for different firing angles.

Finally, a study similar to this could be done for different types of SVCs. The case studied in this thesis was a fixed capacitance thyristor controlled reactor SVC. However, fixed reactor thyristor switched capacitor and thyristor switched capacitor thyristor controlled reactor SVC configurations also exist. A comparison of the harmonics for these three different SVCs would be interesting. Outside the SVC family, a comparison of harmonics for different FACTS such as STATCOM and UPFC, would be useful.

BIBLIOGRAPHY

[1] Turkel, Solomon S. "Understanding Variable Speed Drives." *Engineering, Construction and Maintenance*, April 1997.

[2] Arrillaga, J., D.A. Bradley, and P.S. Bodger. *Power System Harmonics.* New York: John Wiley & Sons, 1985.

[3] Grainger, John J, and JR., William D. Stevenson. *Power System Analysis.* McGraw-Hill, Inc., 1994.

[4] Fuchs, Ewald F., and Mohammad A.S Masoum. *Power Quality in Power Systems and Electrical Machines.* San Diego: Elsevier Academic Press, 2008.

[5] "IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems." no. IEEE Std 519-1992.

[6] Rashid, Muhammed H. *Power Electronics: Circuits, Devices, and Applications.* 3rd. Upper Saddle River, New Jersey: Prentice-Hall, Inc., 2004.

[7] Arrillaga, Jos., and Neville R. Watson. *Power System Harmonics.* 2nd. John Wiley & Sons, 2003.

[8] "K-Factor Transformers and Nonlinear Loads." *Emerson Network Power India.* 2000. http://www.emersonnetworkpower.co.in/KnowledgeCenter/Whitepapers/K-FactorTransformer.pdf (accessed May 2009).

[9] Baldor Motors and Drives. *Series 15J Inverter Control Installation and Operating Manual.* 1999.

[10] Shepherd, W., and P. Zand. *Energy Flow and Power Factor in Nonsinusoidal Circuits.* London: Cambridge University Press, 1979.

[11] Wuidart, L. *Application Note: Understanding Power Factor.* STMicroelectronics, 2003.

[12] Philips Semiconductor. "Power Semiconductor Applications."

[13] Martins, Nelson, Jr., Sergio Gomez, Ricardo Henriques, Camilo Gomez, Adriano Barbosa, and Antonio Martin. "Impact of Induction Motor Loads in System Loadability Margins and Damping of Inter-Area Modes." (Power Engineering Society General Meeting 2003) 3 (2003).

[14] Polka, Dave. "ABB Traning Notes: What is a VFD?" (ABB) 2001.

[15] Murphy, JMD, and FG Turnbull. *Power Electronic Control of AC Motors.* Elmsford: Pergamon Press, 1988.

[16] Carrow, Robert S. *Electronic Drives.* New York: McGraw-Hill, 1996.

[17] Irvine, Geoff, and Ian H Gibson. "VF Drives as Final Control Elements in the Petroleum Industry." (IEEE Industry Applications Magazine) 2002.

[18] Bhaduri, A. "The Use of Variable Frequency Drives in Existing HVAC Installations." (Air Conditioning and Refrigeration Journal) 2001.

[19] Mathur, R. Mohan, and Rajiv K. Varma. *Thyristor-Based FACTS Controllers for Electrical Transmission Systems.* New York: Wiley-Interscience, 2002.

[20] Enerpro. *Operating Manual For a 6-SCR General Purpose Firing Board.* Goleta, CA, August 31, 1995.

[21] "IEEE Recommended Practice for Powering and Grounding Electronic Equipment."

[22] DeDad, John A. "Basic Short Circuit Current Calculation." *Electrical Construction and Maintenance*, December 1997.

[23] Matsumoto, Erin. *The Analysis of Harmonics in a Multiple Adjustable Speed Drive System.* Cal Poly San Luis Obispo, 2007.

[24] Kennedy, Barry W. *Energy Efficient Transformers.* McGraw Hill Professional, 1997.

[25] "User's Manual for PowerSight PS3000." Summit Technology, Inc., 2008.

[26] National Fire Protection Association. *National Electric Code.* NFPA, 2008.

[27] *Electricity Rate Comparison By State.* May 5th, 2009. http://www.neo.ne.gov/statshtml/115.htm (accessed May 17th, 2009).

[28] Frank, Paul. "The Basics of Voltage Imbalance." *Electrical Construction and Maintenance*, September 1999.

Appendix A - Data Tables

Table A.1 - THD Data for Base Case M2 @ 100%

	THDv for M2 @ 100%				THDi for M2 @ 100%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.54	2.33	2.35	2.41	37.09	42	86.95	3.56
90%	1.43	2.11	2.14	2.14	33.62	40.11	92.46	3.5
80%	1.41	2.16	2.02	2.17	31.77	37.87	96.72	3.44
70%	1.47	2.05	2	1.99	29.51	35.55	102.59	3.24
60%	1.4	2.01	1.79	1.99	25.56	31.84	109.14	3.21
50%	1.42	1.85	1.84	1.73	23.36	28.78	115.1	3.46
40%	1.42	1.85	1.72	1.74	20.09	26.08	125.48	3.24
30%	1.46	1.68	1.67	1.67	15.53	20.87	133.36	3.31
20%	1.34	1.65	1.65	1.58	13.68	17.87	144.46	3.43
10%	1.35	1.79	1.64	1.63	11.64	14.87	167.15	3.43
0%	1.47	1.79	1.8	1.85	4.16	4.05	136.8	3.57

Table A.2 - THD Data for Base Case M2 @ 75%

	THDv for M2 @ 75%				THDi for M2 @ 75%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.37	2.37	2.24	2.55	41.5	52.11	93.92	3.9
90%	1.37	2.04	2.03	2.15	38.97	49.89	97.94	3.49
80%	1.35	2.07	2.17	2.02	36.44	47.36	101.88	3.65
70%	1.32	1.88	1.86	1.92	33	45.37	108.89	3.63
60%	1.32	1.88	1.7	1.66	29.88	42.32	113.02	3.25
50%	1.22	1.76	1.67	1.98	26.09	38.04	122.09	3.46
40%	1.38	1.53	1.72	1.57	22.52	33.17	130.84	3.2
30%	1.37	1.61	1.33	1.68	18.78	28.94	141.07	3.43
20%	1.26	1.48	1.45	1.59	15.35	22.92	153.55	3.53
10%	1.36	1.58	1.36	1.68	12.72	19.27	168.49	3.78
0%	1.7	1.47	1.34	1.86	5.2	4.14	112.32	4.03

Table A.3 - THD Data for Base Case M2 @ 50%

	THDv for M2 @ 50%				THDi for M2 @ 50%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.6	2.23	2.3	2.89	45.15	58.77	94.78	5.18
90%	1.55	2.27	2.11	2.31	43.43	56.94	97.42	4.6
80%	1.52	2.02	1.95	2.16	40.68	55.03	101.81	4.36
70%	1.59	2.01	1.71	1.93	37.81	52.8	107.9	3.87
60%	1.48	1.71	1.62	2.03	34.78	49.41	113.66	3.93
50%	1.48	1.83	1.89	2.06	30.75	43.95	118.74	4.1
40%	1.55	1.85	1.77	1.79	26.02	39.75	128.82	4.01
30%	1.5	1.87	1.69	1.8	21.97	34	139.12	3.99
20%	1.54	1.65	1.58	1.86	17.72	28.12	150.62	3.88
10%	1.45	1.67	1.84	1.75	15.14	23.19	170.1	3.97
0%	1.55	1.66	1.78	1.75	6.31	4.71	98.57	4.22

Table A.4 - THD Data for Base Case M2 @ 25%

	THDv for M2 @ 25%				THDi for M2 @ 25%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.67	2.44	2.39	2.55	49.86	63.85	90.07	5.64
90%	1.57	2.36	2.33	2.28	48.28	64.82	94.59	5.17
80%	1.55	2.27	2.15	2.26	45.05	62.91	98.72	5.19
70%	1.52	2.22	2	2.27	41.86	61.17	103.28	4.95
60%	1.41	1.98	1.94	1.93	37.72	58.55	110.84	4.06
50%	1.42	2.05	1.82	1.76	33.4	54.56	119.4	4.19
40%	1.46	1.76	1.83	1.88	28.7	49.79	128.64	4.16
30%	1.47	1.78	1.7	1.89	23.81	43.99	137.36	4.06
20%	1.44	1.81	1.77	1.78	19.46	36.66	152.64	3.98
10%	1.4	1.79	1.64	1.7	16.66	28.86	164.08	3.89
0%	1.52	1.73	1.61	1.64	7.28	4.82	112.53	3.84

Table A.5 - THD Data for Capacitive Compensation M2 @ 100%

	THDv for M2 @ 100%				THDi for M2 @ 100%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.81	2.78	2.65	2.63	40.82	41.26	83.91	3.68
90%	1.75	2.59	2.51	2.59	39.39	38.9	85.98	3.79
80%	1.76	2.41	2.35	2.32	37.77	37.22	91.5	3.5
70%	1.7	2.5	2.24	2.43	35.05	35.62	97.76	3.54
60%	1.95	2.31	2.1	2.38	32.1	33.47	104.87	3.57
50%	1.64	2.09	1.98	2.13	28.91	30.01	112.1	3.46
40%	1.64	2	2.06	2.57	25.31	26.14	119.59	3.64
30%	1.61	1.92	1.98	1.83	20.6	22.37	1272.8	3.32
20%	1.65	1.95	1.92	2.15	16.08	19.22	138.42	3.55
10%	1.64	1.89	2.1	1.86	14.24	15.67	156.04	3.27
0%	1.85	2.11	2.07	2.16	9.03	4.24	100.15	3.49

Table A.6 - THD Data for Capacitive Compensation M2 @ 75%

	THDv for M2 @ 75%				THDi for M2 @ 75%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.76	2.71	2.77	2.76	46.67	46.33	83.79	4.42
90%	1.7	2.65	2.47	2.57	45.38	45.3	86.78	4.89
80%	1.78	2.53	2.56	2.31	43.65	42.69	91.91	4.27
70%	1.81	2.3	2.28	2.33	40.65	40.7	96.53	4.55
60%	1.71	2.17	2.27	2.17	38.32	38.44	103.03	4.08
50%	1.76	2.51	1.99	2.47	34.48	33.26	110.51	4.66
40%	1.62	2.07	2.04	1.96	29.99	29.97	116.91	4.67
30%	1.61	1.9	2.01	1.94	25.48	26.96	124.84	5.72
20%	1.61	1.92	1.96	1.9	20.9	21.15	131.89	4.72
10%	1.64	1.92	1.92	2.32	17.79	18.37	141.41	5.68
0%	1.71	2.1	2.08	2	10.8	4.92	90.23	3.96

Table A.7 - THD Data for Capacitive Compensation M2 @ 50%

	THDv for M2 @ 50%				THDi for M2 @ 50%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.79	2.77	2.57	2.73	55.03	53.33	82.18	6.43
90%	1.82	2.43	2.42	2.49	52.87	52.27	85.84	6.36
80%	1.71	2.43	2.41	2.33	50.42	50.82	91.25	6.33
70%	1.74	2.4	2.3	2.31	49.89	49.59	98.68	5.91
60%	1.75	2.14	2.12	2.15	46.2	47.23	101.72	6.45
50%	1.65	2.14	2.06	2.1	42.67	42.82	111.02	6.73
40%	1.72	1.99	1.97	2.01	37.06	37.69	118.59	5.71
30%	1.75	2.43	2.1	1.96	32.7	32.63	122.32	5.22
20%	1.66	1.93	2	1.99	27.13	27.22	131.76	5.68
10%	1.55	1.87	2.04	2.02	24.27	21.49	150.8	6.25
0%	1.71	2.07	2.11	2.14	15.21	5.33	115.29	4.58

Table A.8 - THD Data for Capacitive Compensation M2 @ 25%

	THDv for M2 @ 25%				THDi for M2 @ 25%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.85	2.61	2.72	2.51	65.44	61.98	84.66	7.63
90%	1.78	2.47	2.44	2.41	65.8	60.25	86.04	7.19
80%	1.69	2.33	2.3	2.31	65.39	60.05	92.54	5.6
70%	1.92	2.18	2.37	2.34	64.3	58.61	97.25	7.77
60%	1.68	2.14	2.14	2.11	61.54	56.13	104.3	5.25
50%	1.64	2.06	2.14	2.05	58.04	52.22	111.08	6.51
40%	1.64	2.02	1.98	2.48	52.25	47.09	116.7	7.21
30%	1.64	1.93	2.03	1.9	48.11	41.29	125.02	7.79
20%	1.65	1.98	1.89	1.94	40.81	33.32	138.76	6.26
10%	1.65	2.02	1.91	1.93	35.76	27.12	141.38	8.4
0%	1.66	2.05	2.04	2.14	26.42	5.42	107.68	4.06

Table A.9 - THD Data for Static Var Compensation M2 @ 100%

	THDv for M2 @ 100%				THDi for M2 @ 100%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.82	2.75	N/A	2.68	42.74	46.37	N/A	3.8
90%	1.63	3.08	2.42	2.5	40.38	43.84	93.73	3.6
80%	1.7	2.44	2.33	2.42	37.84	41.9	98.58	3.61
70%	1.8	2.4	2.35	2.3	34.84	38.85	103	3.45
60%	1.7	2.37	2.49	2.25	31.73	36.31	109.54	3.59
50%	1.7	2.45	2.27	2.35	29.21	32.22	114.8	3.54
40%	1.8	2.41	2.3	2.17	26.93	30.01	121.9	3.71
30%	1.77	2.36	2.25	2.26	23.83	24.41	132.67	3.89
20%	1.81	2.29	2.29	2.19	21.72	20.72	139.74	4.04
10%	1.83	2.21	2.33	2.22	21.8	17.99	150.36	4.04
0%	1.81	2.43	2.42	2.42	21.62	4.5	125.31	4.16

Table A.10 - THD Data for Static Var Compensation M2 @ 75%

	THDv for M2 @ 75%				THDi for M2 @ 75%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.79	2.55	2.53	2.74	48.17	51.34	92.63	4.2
90%	1.76	2.5	2.44	2.54	45.9	49.06	96.21	3.96
80%	1.66	2.48	2.36	2.39	43.42	48.17	97.71	3.87
70%	1.75	2.36	2.33	2.3	40.84	44.87	102.63	3.8
60%	1.79	2.39	2.32	2.22	37.92	41.86	108.1	3.77
50%	1.68	2.35	2.29	2.17	34.12	38.16	111.51	3.62
40%	1.78	2.31	2.32	2.1	32.08	34.19	118.91	3.95
30%	1.64	2.32	2.44	2.19	28.29	30.43	127.9	3.93
20%	1.71	2.25	2.19	2.22	26.77	25.29	140.67	4.16
10%	1.75	2.28	2.25	2.23	25.29	21.19	149.55	4.35
0%	1.77	2.33	2.43	2.36	26.6	4.95	154.02	4.38

Table A.11 - THD Data for Static Var Compensation M2 @ 50%

	THDv for M2 @ 50%				THDi for M2 @ 50%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.89	2.74	2.6	2.72	55.37	58.28	90.52	4.86
90%	1.68	2.53	2.36	2.61	53.06	56.52	95.5	4.72
80%	1.63	2.41	2.42	2.41	51.02	55.25	99.54	4.34
70%	1.68	2.31	2.31	2.37	48.24	52.58	102.94	4.47
60%	1.71	2.4	2.34	2.22	46.22	50.05	109.62	4.02
50%	1.67	2.31	2.24	2.21	41.7	46.43	115.49	4.06
40%	1.7	2.27	2.31	2.3	38.85	41.33	123.78	4.11
30%	1.75	2.7	2.21	2.17	36.97	36.41	132.83	4.1
20%	1.85	2.34	2.33	2.17	35.47	31.23	142.6	4.62
10%	1.74	2.35	2.34	2.18	35.02	24.5	148.5	4.55
0%	1.79	2.52	2.43	2.46	37.71	5.92	164.03	4.79

Table A.12 - THD Data for Static Var Compensation M2 @ 25%

	THDv for M2 @ 25%				THDi for M2 @ 25%			
M1 % Load	A	B	C	D	A	B	C	D
100%	1.79	2.67	2.7	3.13	63.26	67.24	91.92	6.64
90%	1.71	2.61	2.39	2.54	62.38	66.37	94.52	5.34
80%	1.62	2.97	2.32	2.33	60.55	63.96	97.12	5.1
70%	1.68	2.32	2.36	2.68	58.63	64.23	102.34	5.27
60%	1.62	2.45	2.3	2.21	56.67	60.42	108.06	4.79
50%	1.72	2.37	2.28	2.16	53.16	57.37	113.25	4.36
40%	1.62	2.34	2.34	2.2	50.83	51.75	123.08	4.48
30%	1.72	2.37	2.26	2.23	48.34	45.75	133.32	4.73
20%	1.85	2.33	2.35	2.21	48.88	38.86	143.07	4.52
10%	1.76	2.79	2.3	2.26	47.39	32.39	154.17	5
0%	1.84	2.46	2.44	2.34	57.72	5.98	152.59	4.71

Table A.13 - Source Power Factors for the Base Case

	M2@100%			M2@75%			M2@50%			M2@25%		
M1 % Load	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF
100%	0.84	0.894	0.94	0.8	0.869	0.921	0.77	0.851	0.905	0.72	0.823	0.875
90%	0.83	0.880	0.94	0.79	0.851	0.928	0.75	0.832	0.901	0.71	0.795	0.893
80%	0.83	0.869	0.96	0.78	0.836	0.933	0.74	0.809	0.914	0.68	0.759	0.896
70%	0.82	0.854	0.96	0.77	0.816	0.944	0.73	0.785	0.930	0.66	0.724	0.912
60%	0.81	0.839	0.97	0.76	0.795	0.956	0.71	0.755	0.940	0.63	0.678	0.929
50%	0.8	0.826	0.97	0.74	0.774	0.956	0.69	0.728	0.948	0.6	0.630	0.953
40%	0.79	0.806	0.98	0.73	0.743	0.982	0.66	0.691	0.955	0.56	0.583	0.960
30%	0.78	0.785	0.99	0.71	0.728	0.976	0.64	0.656	0.975	0.52	0.540	0.963
20%	0.77	0.777	0.99	0.7	0.707	0.990	0.62	0.630	0.985	0.49	0.500	0.979
10%	0.76	0.770	0.99	0.68	0.687	0.990	0.6	0.602	0.996	0.47	0.470	1.000
0%	0.74	0.743	1.00	0.66	0.656	1.000	0.56	0.560	1.000	0.4	0.397	1.000

Table A.14 - Source Power Factors for Capacitive Compensation

	M2@100%			M2@75%			M2@50%			M2@25%		
M1 % Load	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF
100%	0.92	0.995	0.925	0.9	0.997	0.903	0.87	0.998	0.872	0.83	0.997	0.832
90%	0.92	0.995	0.925	0.9	0.996	0.903	0.88	0.998	0.882	0.83	0.997	0.832
80%	0.93	0.995	0.935	0.91	0.996	0.914	0.89	0.997	0.893	0.83	0.997	0.833
70%	0.93	0.995	0.935	0.92	0.995	0.925	0.89	0.997	0.893	0.84	0.997	0.843
60%	0.94	0.993	0.947	0.93	0.995	0.935	0.9	0.997	0.903	0.85	0.996	0.853
50%	0.95	0.993	0.957	0.94	0.995	0.945	0.91	0.996	0.914	0.86	0.995	0.864
40%	0.96	0.995	0.965	0.95	0.995	0.955	0.93	0.995	0.935	0.88	0.995	0.884
30%	0.97	0.991	0.979	0.96	0.994	0.966	0.94	0.995	0.945	0.9	0.995	0.904
20%	0.98	0.995	0.985	0.97	0.997	0.973	0.96	0.995	0.965	0.92	0.992	0.928
10%	0.98	0.989	0.990	0.98	0.992	0.988	0.97	0.998	0.972	0.94	0.993	0.947
0%	0.99	0.987	1.000	0.99	0.997	0.993	0.98	0.989	0.990	0.96	0.986	0.974

Table A.15 - Source Power Factors for Static Var Compensation

	M2@100%			M2@75%			M2@50%			M2@25%		
M1 % Load	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF	True P.F.	Disp PF	Dist PF
100%	0.92	1.000	0.920	0.9	1.000	0.900	0.87	1.000	0.870	0.84	1.000	0.840
90%	0.93	1.000	0.930	0.91	1.000	0.910	0.88	0.998	0.882	0.85	1.000	0.850
80%	0.93	1.000	0.930	0.92	1.000	0.920	0.89	1.000	0.890	0.85	1.000	0.850
70%	0.94	1.000	0.940	0.93	1.000	0.930	0.9	1.000	0.900	0.86	1.000	0.860
60%	0.95	1.000	0.950	0.94	1.000	0.940	0.91	1.000	0.910	0.87	1.000	0.870
50%	0.96	1.000	0.960	0.95	1.000	0.950	0.92	1.000	0.920	0.89	1.000	0.890
40%	0.97	1.000	0.970	0.96	1.000	0.960	0.94	1.000	0.940	0.9	1.000	0.900
30%	0.98	1.000	0.980	0.97	1.000	0.970	0.94	1.000	0.940	0.91	1.000	0.910
20%	0.98	1.000	0.980	0.97	1.000	0.970	0.95	1.000	0.950	0.91	1.000	0.910
10%	0.98	1.000	0.980	0.97	1.000	0.970	0.95	1.000	0.950	0.91	1.000	0.910
0%	0.98	1.000	0.980	0.97	1.000	0.970	0.94	1.000	0.940	0.88	0.999	0.881

Table A.16 - Source Total RMS Current for All Cases

	Irms for M2@100%			Irms for M2@75%			Irms for M2@50%			Irms for M2@25%		
M1 % Load	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100%	5.9	5.3	5.3	5.3	4.7	4.8	4.7	4.2	4.3	4.3	3.7	3.9
90%	5.5	4.8	4.9	4.8	4.2	4.3	4.3	3.7	3.9	3.9	3.3	3.4
80%	5.2	4.4	4.5	4.5	3.9	4.0	4.0	3.3	3.5	3.6	2.9	3.0
70%	4.8	4.1	4.1	4.2	3.5	3.6	3.7	3.0	3.1	3.3	2.6	2.7
60%	4.5	3.7	3.8	3.9	3.2	3.3	3.5	2.7	2.8	3.1	2.2	2.3
50%	4.3	3.5	3.5	3.7	2.9	3.0	3.3	2.4	2.5	2.9	1.9	2.0
40%	4.1	3.2	3.3	3.5	2.6	2.8	3.0	2.1	2.2	2.7	1.7	1.8
30%	3.9	3.0	3.1	3.3	2.4	2.6	2.9	1.9	2.1	2.5	1.5	1.6
20%	3.7	2.9	2.9	3.2	2.3	2.4	2.8	1.7	1.9	2.4	1.3	1.4
10%	3.7	2.7	2.8	3.1	2.2	2.3	2.7	1.7	1.8	2.4	1.1	1.3
0%	3.5	2.6	2.7	3.0	2.0	2.1	2.6	1.4	1.6	2.3	0.9	1.1

Table A.17 - Source Fundamental RMS Current for All Cases

	I Fundamental for M2 @ 100%			I Fundamental for M2 @ 75%			I Fundamental for M2 @ 50%			I Fundamental for M2 @ 25%		
M1 % Load	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100%	5.55	4.93	4.89	4.91	4.26	4.34	4.29	3.73	3.79	3.85	3.10	3.26
90%	5.19	4.43	4.53	4.51	3.86	3.93	3.98	3.31	3.41	3.54	2.75	2.86
80%	4.92	4.15	4.18	4.25	3.56	3.63	3.72	2.97	3.09	3.29	2.44	2.56
70%	4.64	3.87	3.89	4.00	3.23	3.34	3.49	2.70	2.80	3.07	2.15	2.30
60%	4.39	3.55	3.59	3.78	2.99	3.07	3.27	2.43	2.54	2.88	1.91	2.01
50%	4.20	3.33	3.40	3.56	2.76	2.85	3.12	2.19	2.30	2.71	1.65	1.77
40%	4.00	3.14	3.22	3.40	2.54	2.66	2.94	1.99	2.10	2.57	1.48	1.58
30%	3.84	2.97	2.99	3.27	2.37	2.48	2.79	1.82	1.93	2.46	1.31	1.41
20%	3.70	2.82	2.85	3.17	2.23	2.33	2.72	1.67	1.78	2.39	1.17	1.27
10%	3.65	2.71	2.76	3.08	2.13	2.24	2.69	1.61	1.70	2.37	1.08	1.18
0%	3.49	2.55	2.64	2.94	1.97	2.04	2.55	1.42	1.49	2.27	0.89	0.99

Table A.18 - Source 3rd Harmonic RMS Current for All Cases

	3rd Harmonic Current for M2@100%			3rd Harmonic Current for M2@75%			3rd Harmonic Current for M2@50%			3rd Harmonic Current for M2@25%		
M1 % Load	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100%	0.245	0.265	0.196	0.433	0.243	0.207	0.482	0.246	0.190	0.477	0.277	0.18
90%	0.261	0.374	0.192	0.426	0.271	0.190	0.457	0.254	0.173	0.469	0.287	0.17
80%	0.245	0.349	0.212	0.413	0.268	0.182	0.444	0.269	0.169	0.432	0.283	0.18
70%	0.255	0.293	0.221	0.382	0.286	0.184	0.403	0.234	0.137	0.397	0.262	0.15
60%	0.231	0.282	0.204	0.354	0.227	0.139	0.38	0.226	0.135	0.387	0.223	0.15
50%	0.208	0.265	0.172	0.334	0.238	0.132	0.315	0.235	0.139	0.36	0.221	0.14
40%	0.207	0.248	0.153	0.302	0.227	0.129	0.32	0.174	0.113	0.315	0.194	0.10
30%	0.193	0.189	0.134	0.281	0.184	0.105	0.294	0.178	0.108	0.3	0.147	0.10
20%	0.17	0.151	0.099	0.244	0.17	0.080	0.27	0.153	0.093	0.267	0.118	0.08
10%	0.169	0.146	0.086	0.225	0.155	0.080	0.228	0.104	0.071	0.228	0.105	0.06
0%	0.066	0.068	0.038	0.076	0.068	0.036	0.077	0.067	0.033	0.081	0.063	0.03

Table A.19 - Source 5th Harmonic RMS Current for All Cases

	5th Harmonic Current for M2 @ 100%			5th Harmonic Current for M2 @ 75%			5th Harmonic Current for M2 @ 50%			5th Harmonic Current for M2 @ 25%		
M1 % Load	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100%	1.639	1.67	1.809	1.577	1.645	1.814	1.511	1.686	1.799	1.493	1.639	1.78
90%	1.368	1.406	1.576	1.324	1.421	1.560	1.315	1.424	1.558	1.297	1.44	1.54
80%	1.208	1.248	1.374	1.148	1.244	1.355	1.127	1.198	1.354	1.107	1.25	1.33
70%	1.033	1.058	1.149	0.952	1.024	1.156	0.958	1.049	1.144	0.933	1.049	1.14
60%	0.819	0.85	0.947	0.79	0.869	0.969	0.801	0.862	0.974	0.767	0.878	0.94
50%	0.703	0.716	0.816	0.62	0.704	0.775	0.66	0.692	0.757	0.605	0.699	0.74
40%	0.557	0.573	0.670	0.494	0.55	0.657	0.492	0.548	0.601	0.472	0.564	0.60
30%	0.362	0.428	0.496	0.37	0.431	0.505	0.368	0.427	0.478	0.345	0.448	0.45
20%	0.343	0.308	0.353	0.285	0.327	0.366	0.271	0.318	0.373	0.255	0.338	0.35
10%	0.284	0.263	0.325	0.223	0.249	0.280	0.245	0.255	0.290	0.227	0.265	0.26
0%	0.101	0.082	0.132	0.11	0.09	0.109	0.126	0.099	0.095	0.132	0.108	0.09

Table A.20 - Source 7th Harmonic RMS Current for All Cases

	7th Harmonic Current for M2 @ 100%			7th Harmonic Current for M2 @ 75%			7th Harmonic Current for M2 @ 50%			7th Harmonic Current for M2 @ 25%		
M1 % Load	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC	Base	Cap	SVC
100%	1.178	0.993	0.861	1.152	0.99	0.844		1.038	0.894	1.063	1.039	0.86
90%	1.004	0.84	0.744	1.002	0.867	0.712	0.969	0.865	0.720	0.952	0.907	0.70
80%	0.907	0.744	0.576	0.872	0.762	0.585	0.842	0.729	0.585	0.822	0.783	0.59
70%	0.799	0.643	0.458	0.742	0.628	0.469	0.735	0.666	0.480	0.716	0.674	0.46
60%	0.665	0.519	0.344	0.632	0.538	0.353	0.625	0.522	0.365	0.588	0.548	0.34
50%	0.572	0.397	0.268	0.505	0.424	0.284	0.527	0.405	0.269	0.48	0.407	0.25
40%	0.46	0.29	0.253	0.4	0.29	0.248	0.391	0.295	0.237	0.38	0.296	0.22
30%	0.35	0.212	0.262	0.302	0.19	0.234	0.297	0.182	0.247	0.276	0.198	0.23
20%	0.257	0.128	0.328	0.219	0.104	0.291	0.209	0.089	0.293	0.196	0.111	0.30
10%	0.201	0.085	0.361	0.154	0.069	0.340	0.156	0.076	0.339	0.151	0.07	0.33
0%	0.076	0.167	0.498	0.07	0.143	0.476	0.061	0.132	0.487	0.053	0.154	0.48